Intel® IXF1104 Quad-Port Gigabit Ethernet Media Access Controller

Datasheet

The Intel® IXF1104 is a four-port Gigabit MAC that supports IEEE 802.3 10/100/1000 Mbps applications. The IXF1104 supports a System Packet Interface Phase 3 (SPI3) system interface to the network processor or ASIC, and concurrently supports copper and fiber physical layer devices (PHYs).

The copper PHY interface implements the Gigabit Media Independent Interface (GMII) and the Reduced Gigabit Media Independent Interface (RGMII) as defined in Version 1.2a of the Hewlett-Packard* specification. RGMII has the benefit of reducing the PHY interface pin count for high-port-count applications.

The fiber PHY interface implements an internal Serializer/Deserializer (SerDes) on each port to allow direct connection to optical modules. The integration of the SerDes functionality reduces PCB area requirements and system cost.

Product Features

- SPI3 interface
  - —Capable of data transfers at:
    3.3 Gbps with standard 104 MHz clock
    4.0 Gbps with 125-133 MHz overclocking
  - —Two modes for 4 Gbps transfer:
    32-bit Multi-PHY mode
    4 x 8 Single-PHY mode
- Supports four independent 10/100/1000 Mbps full-duplex PHYs:
  - —RGMII full-duplex-capable at 10/100/1000 Mbps
  - —RGMII half-duplex-capable at 10/100 Mbps
  - —GMII full-duplex-capable at 1000 Mbps
- Three different interfaces to PHY devices:
  - —SerDes with GBIC support
  - —GMII
  - —RGMII
- Operating Temperature Ranges:

	MIN	MAX
Copper Mode:	-40°C	+85°C
Fiber Mode:	0°C	+70°C

- IEEE 802.3 MII Management Interface (MDIO) capable for Copper PHY configuration
- 32/16/8-bit microprocessor interface
- RMON statistics
- JTAG- and boundary-scan-capable
- Automatic padding of transmitted packets less than 64 bytes
- Jumbo frame support for 10 kbyte packets
- Loss-less flow control for up to 9.6 kbyte packets and 5 km of fiber
- Internal 32 kbyte receive FIFO and 10-Kbyte transmit FIFOs per channel
- Broadcast, multicast, and unicast address filtering
- Loopback modes for testing and diagnostics
- Detection of length error, runt or overly large packets
- Error counters for dropped packets and error packets
- CRC calculation and error detection
- Programmable option to drop packets with errors
- Compliance with IEEE 802.3x Specification MAC Command Frames; the IXF1104 receives and executes PAUSE Command Frames
- 576-ball BGA package with 6 balls removed diagonally from each corner, for a total of 552 balls used
- 1.8 V, 2.5 V, and 3.3 V operation

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Applications

- Load Balancing Systems
- MultiService Switch
- Web Caching Appliances
- Intelligent Backplane Interfaces
- Edge Router
- Base Station Controller
- Redundant Line Cards
- Base Transceiver Station
- Serving GRPS Support Node (SGSN)
- General Packet Radio Services (GGSN)
- Packet Data Serving Note (PDSN)
- Digital Subscriber Line Access Multiplexer (DSLAM)
- Cable Modem Termination System (CMTS)

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19	Modified Table 1 “Intel® IXF1104 Signal Descriptions”
53	Modified Section 5.1.1.1, “Padding of Undersized Frames on Transmit”.
60	Modified text for etherStatsCollision in Table 9 “RMON Additional Statistics”.
87	Modified Table 17 “Intel® IXF1104-to-GBIC Connections”
65	Modified first paragraph under Section 5.3.1.2, “Clock Rates”.
87	Modified Section 5.8.2.1, “High-Speed Serial Interface”.
100	Modified Figure 27 “Microprocessor — External and Internal Connections”.
110	Changed PECL to LVDS under Section 6.1, “DC Specifications”.
113	Modified table note 4 in Table 32 “SPI3 Receive Interface Signal Parameters”.
119	Modified Table 37 “SerDes Timing Parameters”.
125	Modified Table 40 “Microprocessor Interface Write Cycle AC Signal Parameters”.
140	Modified Table 53 “IPG Receive and Transmit Time Register (Addr: Port_Index + 0x0A – + 0x0C)”.
143	Modified Table 60 “Short Runts Threshold Register (Addr: Port_Index + 0x14)”.
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143	Modified Table 62 “RX Config Word Register Bit Definition (Addr: Port_Index + 0x16)”.
145	Modified Table 64 “DiverseConfigWrite Register (Addr: Port_Index + 0x18)”.
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171	Added Table 98 “RX FIFO Jumbo Packet Size 0-3 Register (Addr: 0x5B8 – 0x5BB”.
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172	Added Table 102 “RX FIFO Jumbo Packet Size Port 3 Register Bit Definitions (Addr: 0x5BB)”.
178	Modified Table 110 “TX FIFO Number of Dropped Packets Register Ports 0-3 (Addr: 0x625 – 0x629)”.
177	Modified Table 108 “TX FIFO Port Reset Register (Addr: 0x620)”.
177	Modified Table 108 “TX FIFO Port Reset Register (Addr: 0x620)”.
177	Modified Table 107 “Loop RX Data to TX FIFO Register Ports 0 - 3 (Addr: 0x61F)”.
179	Added Table 111 “TX FIFO Occupancy Counter for Ports 0 - 3 Registers (Addr: 0x62D – 0x630)”.
180	Added Table 112 “TX FIFO Port Drop Enable Register (Addr: 0x63D)”.
181	Modified Table 114 “MDI Single Command Register (Addr: 0x680)”.
186	Added Table 122 “Tx and Rx Power-Down Register (Addr: 0x787)”.
194	Replaced Figure 53 “Intel® IXF1104 Example Package Marking”.

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	Internal releases.

1.0 Introduction

This document contains information on the Intel® IXF1104 4-Port 10/100/1000 Ethernet Media Access Controller.

1.1 What You Will Find in This Document

This document contains the following sections:

- Table 2.0 “Block Diagram” on page 16
  IXF1104 block diagram system architecture.
- Table 3.0 “Pin Assignments and Signal Descriptions” on page 18
  Signal naming methodology and signal descriptions.
- Section 4.0, “Ball Assignments and Ball List Tables” on page 39
  IXF1104 ball grid diagram with two ball list tables (by pin number and signal name)
- Section 5.0, “Functional Descriptions” on page 52
  Detailed information about the operation of the IXF1104 including general features, and interface types and descriptions.
- Section 6.0, “Electrical Specifications” on page 108
  Information on the product-operating parameters, electrical specifications, and timing parameters.
- Section 7.0, “Register Set” on page 130
  Memory map/detailed descriptions and default values for the register set.
- Section 8.0, “Mechanical Specifications” on page 191
  IXF1104 packaging information.

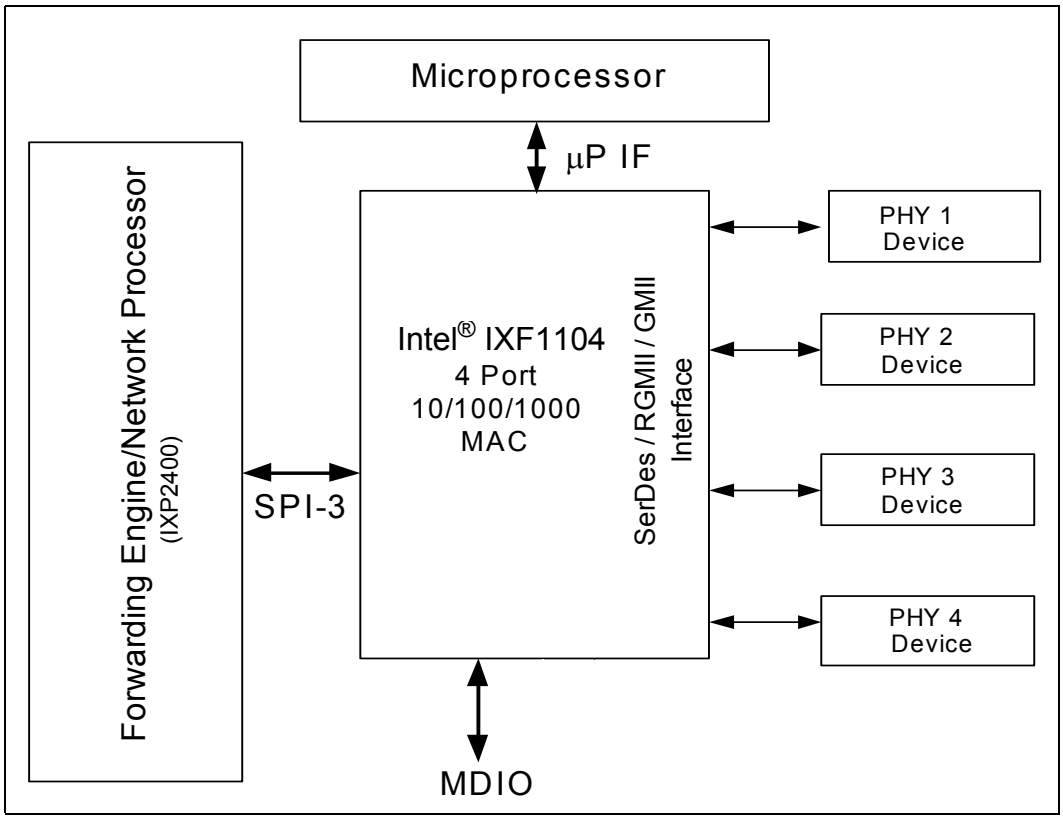
1.2 Related Documents

Document	Document Number
Intel® IXF1104 Design and Layout Guide	278696
Intel® IXF1104 Thermal Design Considerations	278751
Intel® IXF1104 Development Kit Manual	278785

2.0 Block Diagram

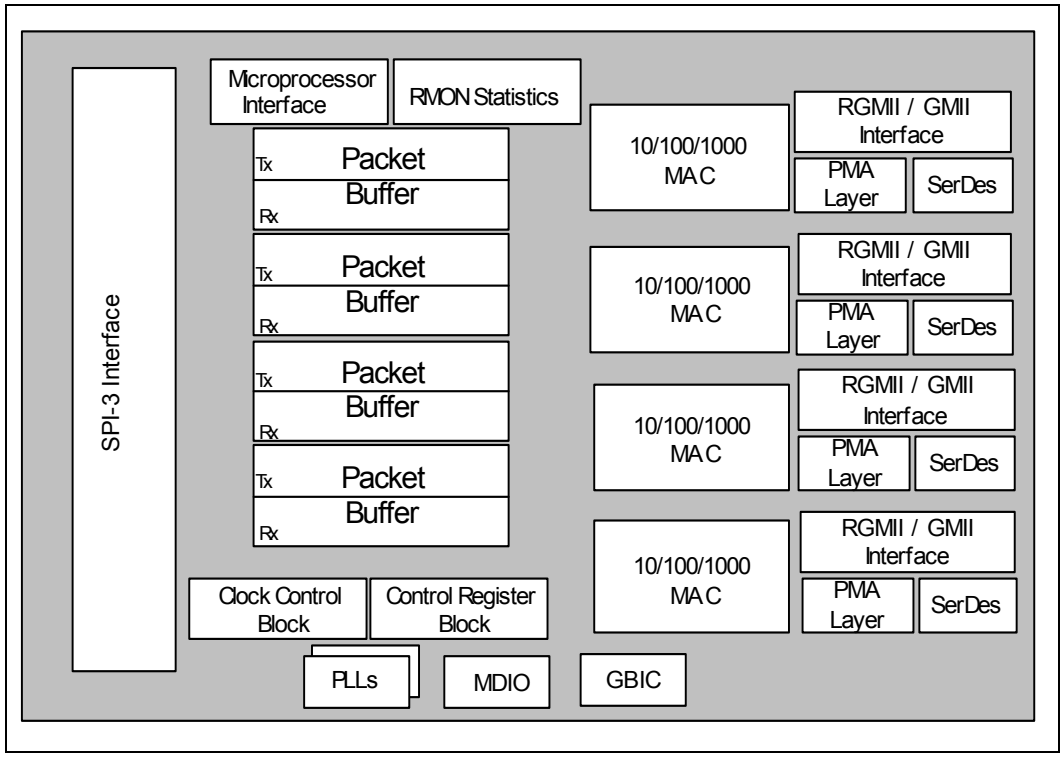
The Intel® IXF1104 is a 4 x 1 Gigabit Ethernet MAC device that provides a 2.4 to 4.0 Gbps network processor interface to four individual 10/100/1000 Mbps full-duplex and 10/100 half-duplex-capable Ethernet Media Access Controllers (MACs). The interface to the network processor is supported through a System Packet Interface Phase 3 (SPI3) media interface, and the PHY interfaces are Serializer/Deserializer (SerDes) with GBIC support, Gigabit Media Independent Interface, (GMII) or Reduced GMII (RGMII) selected on a per-port basis.

Figure 1. Intel® IXF1104 Block Diagram



The internal architecture of the IXF1104 is shown in Figure 2.

Figure 2. Intel® IXF1104 Internal Architecture

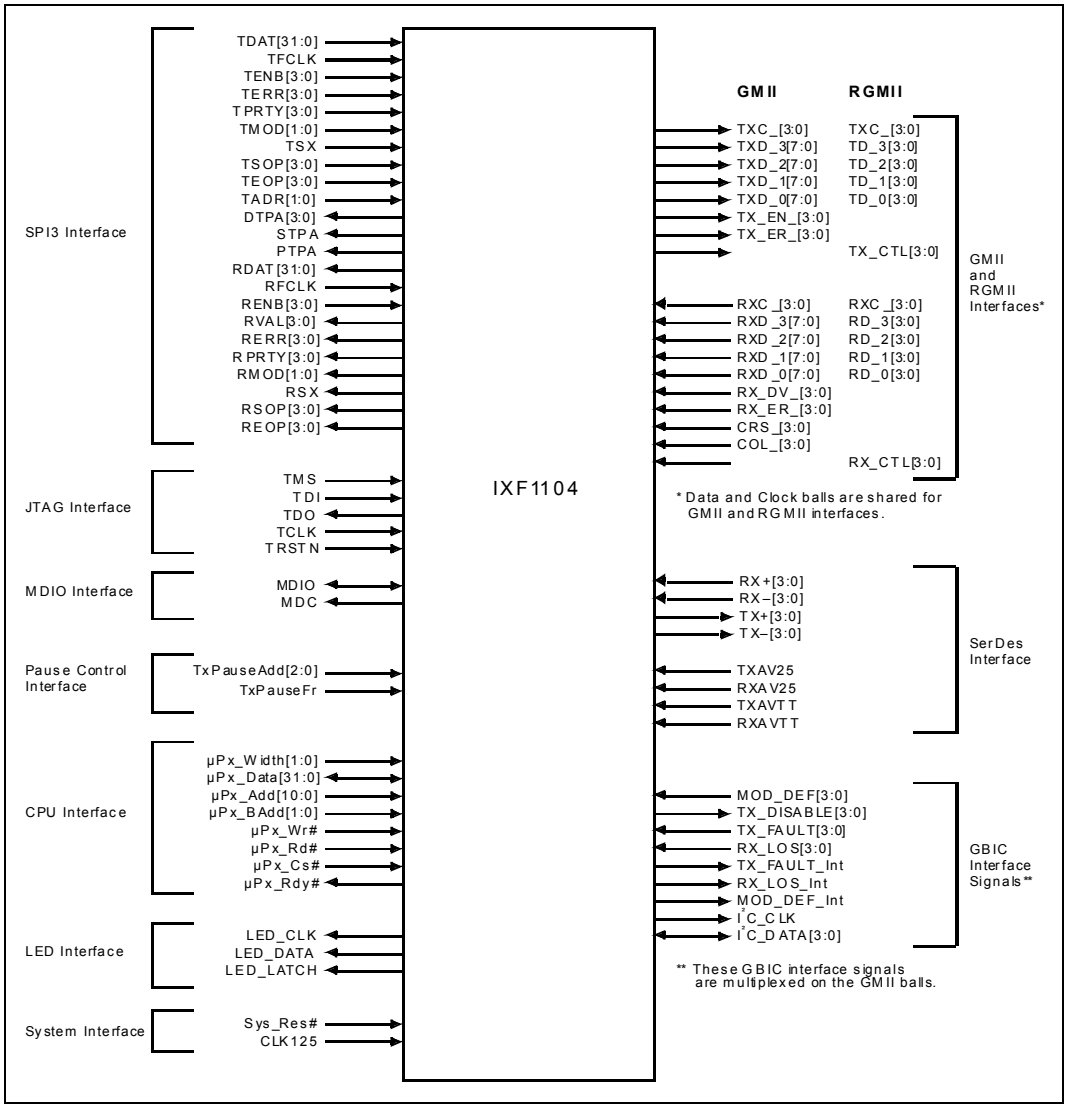


3.0 Pin Assignments and Signal Descriptions

Section 3.0 provides the IXF1104 pinout diagram and signal description information as follows:

- Figure 3 “Intel® IXF1104 Preliminary Pinout Diagram”
- Section 3.1, “Signal Name Conventions”
- Section 3.2, “Signal Descriptions”
- Section 3.3, “Ball Usage Summary”
- Section 3.4, “Ball State During Reset”
- Section 3.5, “Power Supply Sequencing”
- Section 3.6, “Pull-Up/Pull-Down and Unused Ball Guidelines”

Figure 3. Intel® IXF1104 Preliminary Pinout Diagram



3.1 Signal Name Conventions

Signal names may contain either a port designation (media interface) or a serial designation (system interface). Signal naming conventions are as follows:

Port Designation: Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, GBIC Serial Data signals would be identified as I^2C_DATA_0, I^2C_DATA_1, etc.

Serial Designation: A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by a bracketed serial designation. For example, SPI3 Transmit Data Bus signals would be identified as TDAT[31:0].

3.2 Signal Descriptions

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 1 of 15)

Ball Designator	Signal Name	Type	Standard	Description
SPI3 Interface				
F7, F5, G9, G8, G7, G6, G5, G4	TDAT[31], TDAT[30], TDAT[29], TDAT[28], TDAT[27], TDAT[26], TDAT[25], TDAT[24] TDAT_3[7:0]	Input	3.3 V LVTTL	**Transmit Data Bus.** Carries payload data to IXF1104 egress path. **Mode** **Bits** 32-bit Multi-PHY [31:24] 4 x 8 Single-PHY [7:0] for port 3
C8, F9, E10, E9, E8, E7, E6, E5	TDAT[23], TDAT[22], TDAT[21], TDAT[20], TDAT[19], TDAT[18], TDAT[17], TDAT[16] TDAT_2[7:0]	Input	3.3 V LVTTL	**Transmit Data Bus.** Carries payload data to IXF1104 egress path. **Mode** **Bits** 32-bit Multi-PHY [23:16] 4 x 8 Single-PHY [7:0] for port 2
H3, J3, J2, J1, H1, G2, G1, F1	TDAT[15], TDAT[14], TDAT[13], TDAT[12], TDAT[11], TDAT[10], TDAT[9], TDAT[8] TDAT_1[7:0]	Input	3.3 V LVTTL	**Transmit Data Bus.** Carries payload data to IXF1104 egress path. **Mode** **Bits** 32-bit Multi-PHY [15:8] 4 x 8 Single-PHY [7:0] for port 1
C6, B5, C5, C4, D1, C3, C2, B3	TDAT[7], TDAT[6], TDAT[5], TDAT[4], TDAT[3], TDAT[2], TDAT[1], TDAT[0] TDAT_0[7:0]	Input	3.3 V LVTTL	**Transmit Data Bus.** Carries payload data to IXF1104 egress path. **Mode** **Bits** 32-bit Multi-PHY 7:0] 4 x 8 Single-PHY [7:0] for port 0

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 2 of 15)

Ball Designator	Signal Name	Type	Standard	Description
D7	TFCLK	Input	3.3 V LVTTL	**Transmit Clock.** Clock associated with all transmit signals. Data and control lines are sampled on the rising edge of TFCLK.
J6, B9, G3, D5	TPRTY[3], TPRTY[2], TPRTY[1], TPRTY[0]	Input	3.3 V LVTTL	**Transmit Parity.** Odd parity for the TDAT bus. TPRTY is valid only when a channel has either TENB or TSX asserted. Odd parity is the default configuration; however, even parity can be selected (see Table 118 on page 183). **32-bit Multi-PHY mode:** TPRTY[0] is the parity bit covering all 32 bits. **4 x 8 Single-PHY mode:** PRTY[3:0] bits correspond to the respective TDAT_n[3:0] channels.
J4, C9, E2, B7	TENB[3], TENB[2], TENB[1], TENB[0]	Input	3.3 V LVTTL	**Transmit Write Enable.** TENB[n] asserted causes an attached PHY to process TDAT[n], TMOD, TSOP, TEOP and TERR signals. **32-bit Multi-PHY mode:** TENB[0] is the enable bit for all 32 bits. **4 x 8 Single-PHY mode:** ENB[3:0] bits correspond to the respective TDAT_n[3:0] channels and their associated control and status signals.
J8, E11, K1, A8	TERR[3], TERR[3], TERR[3], TERR[3]	Input	3.3 V LVTTL	**Transmit Error.** Indicates that there is an error in the current packet. TERR is valid when simultaneously asserted with TEOP and TENB. **32-bit Multi-PHY mode:** TERR[0] is the bit asserted for all 32 bits. **4 x 8 Single-PHY mode:** Each bit of TERR[3:0] corresponds to the respective TDAT_n[3:0] channel.
J5, C10, E3, C7	TSOP[3], TSOP[2], TSOP[1], TSOP[0]	Input	3.3 V LVTTL	**Transmit Start-of-Packet.** TSOP is valid, indicating the start of a packet, when asserted simultaneously with TENB. **32-bit Multi-PHY mode:** TSOP[0] is the bit asserted for all 32 bits. **4 x 8 Single-PHY mode:** Each bit of TSOP[3:0] corresponds to the respective TDAT_n[3:0] channel.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 3 of 15)

Ball Designator	Signal Name	Type	Standard	Description
H5, E4, F3, A7	TEOP[3], TEOP[2], TEOP[1], TEOP[0]	Input	3.3 V LVTTL	**Transmit End-of-Packet.** TEOP is valid, indicating the end of a packet, when asserted simultaneously with TENB. **32-bit Multi-PHY mode:** TEOP[0] is the bit asserted for all 32 bits. **4 x 8 Single-PHY mode:** Each bit of TEOP[3:0] corresponds to the respective TDAT_n[3:0] channel.
D9, A6	TMOD[1], TMOD[0]	Input	3.3 V LVTTL	**Transmit Word Modulo.** **32-bit Multi-PHY mode:** MOD[1:0] indicates the valid data bytes of TDAT[31:0]. During transmission, TMOD[1:0] should always be “00” until the last double word is transferred on TDAT[31:0]. When TEOP is asserted, TMOD[1:0] specifies the valid bytes of TDAT: TMOD[1:0] – Valid Bytes of TDAT 00 = 4 bytes [31:0] 01 = 3 bytes [31:8] 10 = 2 bytes [31:16] 11 = 1 byte [31:24] TENB must be simultaneously asserted for TMOD[1:0] to be valid. **4 x 8 Single-PHY mode:** MOD[1:0] is not required.
E1	TSX	Input	3.3 V LVTTL	**Transmit Start of Transfer.** **32-bit Multi-PHY mode:** TSX asserted with TENB = 1 indicates that the address of the PHY is present on TDAT[7:0]. Because the *IXF1104* has only four ports, the valid values on TDAT[7:0] are 3, 2, 1, and 0. When TENB = 0, TSX is not used by the PHY device. **Note:** Only TDAT[1:0] are relevant, all other bits are ‘Don’t Care’. **4 x 8 Single-PHY mode:** TSX is not used.
A12, A11	TADR[1], TADR[0]	Input	3.3 V LVTTL	**Transmit PHY Address.** The value on TADR[1:0] selects one of the *IXF1104* four PHY ports that drives the PTPA signal after the rising edge of TFCLK.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 4 of 15)

Ball Designator	Signal Name	Type	Standard	Description
J7, A9, L1, D3	DTPA[3], DTPA[2], DTPA[1], DTPA[0]	Output	3.3 V LVTTL	**Direct Transmit Packet Available.** A direct status indication for transmit FIFOs of ports[3:0] DTPA transitions High for a port when the programmed minimum number of bytes is available in its transmit FIFO. Once High, the DTPA signal indicates that its corresponding transmit FIFO is not full. When DTPA transitions Low, it indicates that its transmit FIFO is above the near-full threshold. **Note:** For more information, see Table 103 “TX FIFO High Watermark Register Ports 0 to 3 (Addr: 0x600 – 0x603)” on page 173 and Table 104 “TX FIFO Low Watermark Register Ports 0 to 3 (Addr: 0x60A – 0x60D)” on page 174. DTPA is required for byte-level transfer mode and is updated on the rising edge of TFCLK.
C11	STPA	Output	3.3 V LVTTL	**Selected-PHY Transmit Packet Available.** STPA is only meaningful in a 32-bit multi-PHY mode. A direct status indication for transmit FIFOs of ports[3:0]. STPA transitions High when the programmed minimum number of bytes is available in the transmit FIFO specified by the latest in-band address. Once High, STPA indicates that the transmit FIFO is not full. When STPA transitions Low, it indicates that the transmit FIFO is above the near-full threshold. **Note:** For more information, see Table 103 “TX FIFO High Watermark Register Ports 0 to 3 (Addr: 0x600 – 0x603)” on page 173 and Table 104 “TX FIFO Low Watermark Register Ports 0 to 3 (Addr: 0x60A – 0x60D)” on page 174. STPA always provides status indication for the selected port in order to avoid FIFO overflows while polling is performed. The port about which STPA reports is updated on the following rising edge of TFCLK after TSX is sampled as asserted. STPA is updated on the rising edge of TFCLK.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 5 of 15)

Ball Designator	Signal Name	Type	Standard	Description
B11	PTPA	Output	3.3 V LVTTL	**Polled-PHY Transmit Packet Available.** PTPA allows the polling of the port selected by the TADR address bus. PTPA transitions high when the programmed minimum number of bytes is available in the transmit FIFO. Once high, PTPA indicates that the transmit FIFO is not full. When PTPA transitions low, it indicates that the transmit FIFO is above the near-full threshold. **Note:** For more information, see Table 103 "TX FIFO High Watermark Register Ports 0 to 3 (Addr: 0x600 – 0x603)" on page 173 and Table 104 "TX FIFO Low Watermark Register Ports 0 to 3 (Addr: 0x60A – 0x60D)" on page 174. The port PTPA reports on is updated on the following rising edge of TFCLK after the port address on TADR is sampled by the PHY device. PTPA is updated on the rising edge of TFCLK.
F24, G24, G23, G22, G21, G20, G19, G18	RDAT[31], RDAT[30] RDAT[29], RDAT[28], RDAT[27], RDAT[26], RDAT[25], RDAT[24] RDAT_3[7:0]	Output	3.3 V LVTTL	**Receive Data Bus.** Carries payload data and in-band address from IXF1104. **Mode** / **Bits** 32-bit Multi-PHY / [31:24] 4 x 8 Single-PHY / [7:0] for port 3
E21, E22, D22, C22. C21, C20, B22, B20	RDAT[23], RDAT[22], RDAT21], RDAT[20], RDAT[19], RDAT[18], RDAT[17], RDAT[16] RDAT_2[7:0]	Output	3.3 V LVTTL	**Receive Data Bus.** Carries payload data and in-band address from IXF1104. **Mode** / **Bits** 32-bit Multi-PHY / [23:16] 4 x 8 Single-PHY / [7:0] for port 2
F18, E18, E17, F16, E16, D16, C17, A17	RDAT[15], RDAT[14], RDAT[13], RDAT[12] RDAT[11], RDAT[10] RDAT[9], RDAT[8] RDAT_1[7:0]	Output	3.3 V LVTTL	**Receive Data Bus.** Carries payload data and in-band address from IXF1104. **Mode** / **Bits** 32-bit Multi-PHY / [15:8] 4 x 8 Single-PHY / [7:0] for port 1
F14, E14, D14, C13, C14, B14, A14, A15	RDAT[7], RDAT[6], RDAT[5], RDAT[4], RDAT[3], RDAT[2], RDAT[1], RDAT[0] RDAT_0[7:0]	Output	3.3 V LVTTL	**Receive Data Bus.** Carries payload data and in-band address from IXF1104. **Mode** / **Bits** 32-bit Multi-PHY / [7:0] 4 x 8 Single-PHY / [7:0] for port 0

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 6 of 15)

Ball Designator	Signal Name	Type	Standard	Description
A19	RFCLK	Input	3.3 V LVTTL	**Receive Clock.** Clock associated with all receive signals. Data and controls are driven on the rising edge of RFCLK.
F20, E20, G16, E15	RPRTY[3], RPRTY[2], RPRTY[1], RPRTY[0]	Output	3.3 V LVTTL	**Receive Parity.** Odd parity for the RDAT bus. RPRTY is valid only when a channel has RENB or RSX asserted. Odd parity is the default configuration; however, even parity can be selected (see Table 119 on page 184). **32-bit Multi-PHY mode:** RPRTY[0] is the parity bit for all 32 bits. **4 x 8 Single-PHY mode:** Each bit of RPRTY[3:0] corresponds to the respective RDAT_n[3:0] channel. (where n = 0,1,2, or 3)
E24, C19, A18, A13	RENB[3], RENB[2], RENB[1], RENB[0]	Input	3.3 V LVTTL	**Receive Read Enable.** The RENB signal controls the flow of data from the receive FIFOs. During data transfer, RVAL must be monitored as it indicates if the RDAT[], RPRTY, RMOD[1:0], RSOP, REOP, RERR and RSX are valid. The system may deassert RENB at any time if it is unable to accept data from the *IXF1104*. When RENB is sampled Low, a read is performed from the receive FIFO and the RDAT[], RPRTY, RMOD[1:0], RSOP, REOP, RERR, RSX and RVAL signals are updated on the following rising edge of RFCLK. When RENB is sampled High by the PHY device, a read is not performed, and the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, RERR, RSX and RVAL signals remain unchanged on the following rising edge of RFCLK. **32-bit Multi-PHY Mode:** RENB[0] covers all receive bits. **4 x 8 Single-PHY Mode:** The RENB[3:0] bits correspond to the per-port data and control signals.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 7 of 15)

Ball Designator	Signal Name	Type	Standard	Description
H20, D20, G17, A16	RERR[3], RERR[2], RERR[1], RERR[0]	Output	3.3 V LVTTL	**Receive Error.** RERR is used to indicate that the current packet is in error. RERR will only be asserted when REOP is asserted. Conditions that can cause RERR to be set include FIFO overflow, CRC error, code error, and runt or giant packet. RERR is considered valid only when RVAL is asserted. **32-bit Multi-PHY mode:** RERR[0] covers all 32 bits. **4 x 8 Single-PHY mode:** The RERR[3:0] bits correspond to the RDAT_n[3:0] channels. (where n=0,1,2 or 3)
F22, E19, B18, C15	RVAL[3], RVAL[3], RVAL[3], RVAL[3]	Output	3.3 V LVTTL	**Receive Data Valid.** RVAL indicates the validity of the receive data signals. RVAL is low between transfers and when RSX is asserted. It is also low when the *IXF1104* pauses a transfer due to an empty receive FIFO. When a transfer is paused by holding RENB High, RVAL holds its value unchanged, although no new data is present on RDAT[] until the transfer resumes. When RVAL is High, the RDAT[], RMOD[1:0], RSOP, REOP, and RERR signals are valid. When RVAL is Low, the RDAT[31:0], RMOD[1:0], RSOP, REOP, and RERR signals are invalid and must be disregarded. The RSX signal is valid only when RVAL is Low. **32-bit Multi-PHY mode:** RVAL[0] covers all receive bits. **4 x 8 Single-PHY mode:** The RVAL[3:0] bits correspond to the per-port data and control signals.
J18, E23, C18, B16	RSOP[3], RSOP[2], RSOP[1], RSOP[0]	Output	3.3 V LVTTL	**Receive Start of Packet.** Indicates the start of a packet when asserted along with RVAL. **32-bit Multi-PHY mode:** RSOP[0] covers all 32 bits. **4 x 8 Single-PHY mode:** The RSOP[3:0] bits correspond to the RDAT_n[7:0] channels.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 8 of 15)

Ball Designator	Signal Name	Type	Standard	Description
J19, C23, D18, C16	REOP[3], REOP[2], REOP[1], REOP[0]	Output	3.3 V LVTTL	**Receive End of Packet.** Indicates the end of a packet when asserted with RVAL. **32-bit Multi-PHY mode:** REOP[0] covers all 32 bits. **4 x 8 Single-PHY mode:** The REOP[3:0] bits correspond to the RDAT_n[7:0] channels.
G13, G14	RMOD[1], RMOD[0]	Output	3.3 V LVTTL	**Receive Word Modulo:** **32-bit Multi-PHY mode:** RMOD[1:0] indicates the valid bytes of data in RDAT[31:0]. During transmission, RMOD should always be “00”, except when the last double-word is being transferred on RDAT[31:0]. When REOP is asserted, RMOD[1:0] specifies the valid packet data bytes on RDAT[31:0]. *RMOD[1:0]* *Valid Bytes of RDAT* 00 = 4 bytes [31:0] 01 = 3 bytes [31:8] 10 = 2 bytes [31:16] 11 = 1 byte [31:24] **4 x 8 Single-PHY mode:** RMOD[1:0] is not required. RMOD is considered valid only when RVAL is simultaneously asserted. RENB must be asserted for RMOD[1:0] to be valid.
E13	RSX	Output	3.3 V LVTTL	**Receive Start of Transfer.** **32-bit Multi-PHY mode:** RSX indicates when the in-band port address is present on the RDAT bus. When RSX is High and RVAL = “0”, the value of RDAT[7:0] is the address of the receive FIFO to be selected. Subsequent data transfers on RDAT[] will be from the FIFO specified by this in-band address. Values of {0, 1, 2, 3} select the corresponding port. RSX is ignored when RVAL is deasserted. **4 x 8 Single-PHY mode:** RSX is ignored.
Serializer/Deserializer (SerDes) Interface				
Y13, AD13, W16, AC18	TXP[0], TXP[1], TXP[2], TXP[3]	Output	LVDS	Transmit Differential Output, Positive.
Y14, AD14, Y16, AD18	TXN[0], TXN[1], TXN[2], TXN[3]	Output	LVDS	Transmit Differential Output, Negative.
P22, V22, T24, U24	RXP[0], RXP[1], RXP[2], RXP[3]	Input	LVDS	Receive Differential Input, Positive.
R22, U22, R24, V24	RXN[0], RXN[1], RXN[2], RXN[3]	Input	LVDS	Receive Differential Input, Negative.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 9 of 15)

Ball Designator	Signal Name	Type	Standard	Description
Gigabit Media Independent Interface (GMII) (Refer to the RGMII Interface for shared data and clock pins)				
Y4, AB4, AC3, AB3, AA3, Y3, Y2, Y1 AC9, AD8, AB8, AA7, AD9, AB9', AB7, AC7 AA18, AA20, AB19, AD16, AB23, AB22, AB21, AB20 W14, AA16, Y15, AA14, V17, V16, V15, V14	TXD_0 [7], TXD_0 [6], TXD_0 [5], TXD_0 [4], TXD_0 [3], TXD_0 [2], TXD_0 [1], TXD_0 [0] TXD_1 [7], TXD_1 [6], TXD_1 [5], TXD_1 [4], TXD_1 [3], TXD_1 [2], TXD_1 [1], TXD_1 [0] TXD_2 [7], TXD_2 [6], TXD_2 [5], TXD_2 [4], TXD_2 [3], TXD_2 [2], TXD_2 [1], TXD_2 [0] TXD_3 [7], TXD_3 [6], TXD_3 [5], TXD_3 [4], TXD_3 [3], TXD_3 [2] TXD_3 [1], TXD_3 [0]	Output	2.5 V CMOS	**Transmit Data.** Each bus carries eight data bits [7:0] of the transmitted data stream to the PHY device. **RGMII Mode:** When a port is configured in copper mode, and the RGMII interface is selected, only bits TXD_n[3:0] are used. The data is transmitted on both edges of TXC_*n*. **Fiber Mode:** The following pins have multiplexed functions when a port is configured in fiber mode: TXD_n[4]: TxDisable[3:0]
AB2, Y8, AC22, V12	TX_EN_0, TX_EN_1, TX_EN_2, TX_EN_3	Output	2.5 V CMOS	**Transmit Enable.** Indicates that valid data is being driven on the corresponding Transmit Data: TXD_0, TXD_1, TXD_2, and TXD_3.
AB2, Y8, AC22, V12	TX_ER_0, TX_ER_1, TX_ER_2, TX_ER_3	Output	2.5 V CMOS	**Transmit Error:** Indicates a transmit error in the corresponding Transmit Data: TXD_0, TXD_1, TXD_2, and TXD_3.
AC5, AB5, Y5, Y6, Y7, W7, V7, V8 Y10, AA11, AC11, AD10, W9, W11, Y11, Y9 W20,V19, V20, W22, Y23, Y22, Y21, Y20 T19, T18, T17, T16, W18, Y19, Y18, W17	RXD_0[7],RXD_0[6], RXD_0[5], RXD_0[4], RXD_0[3], RXD_0[2], RXD_0[1], RXD_0[0] RXD_1[7], RXD_1[6], RXD_1[5], RXD_1[4], RXD_1[3], RXD_1[2], RXD_1[1], RXD_1[0] RXD_2[7], RXD_2[6], RXD_2[5], RXD_2[4], RXD_2[3], RXD_2[2], RXD_2[1], RXD_2[0] RXD_3[7], RXD_3[6], RXD_3[5], RXD_3[4], RXD_3[3], RXD_3[2] RXD_3[1], RXD_3[0]	Input	2.5 V CMOS	**Receive Data:** Each bus carries eight data bits [7:0] of the received data stream. **RGMII Mode:** When a port ID is configured in copper mode and the RGMII interface is selected, only bits RXD_*n*[3:0] are used to receive data. **Fiber Mode**: The following pins have multiplexed functions when a port is configured in fiber mode: RXD_*n*[4]: Mod_Def[3:0] RXD_*n*[5]: TxFault[3:0] RXD_*n*[6]: RX_LOS[3:0]
AB11, Y24, V18, W5	RX_DV_0, RX_DV_1, RX_DV_2, RX_DV_3	Input	2.5 V CMOS	**Receive Data Valid.** Indicates that valid data is being driven on Receive Data: RXD_0, RXD_1, RXD_2, and RXD_3.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 10 of 15)

Ball Designator	Signal Name	Type	Standard	Description
U20, AA22, Y12, W5	RX_ER_0, RX_ER_1, RX_ER_2, RX_ER_3	Input	2.5 V CMOS	**Receive Error.** Indicates an error in Receive Data: RXD_0, RXD_1, RXD_2, and RXD_3.
AA5, AA9, AB15, AC16	CRS_0, CRS_1, CRS_2, CRS_3	Input	2.5 V CMOS	**Carrier Sense.** Indicates the PHY device has detected a carrier.
AB6, AB10, AD15, AB17	COL_0, COL_1. COL_2, COL_3	Input	2.5 V CMOS	**Collision (detection).** Indicates detection of a collision. Only meaningful in half-duplex mode at 10 Mbps or 100 Mbps.
Reduced Gigabit Media Independent Interface (RGMII)				
	TD_0 [3], TD_0 [2], TD_0 [1], TD_0 [0] TD_1 [3], TD_1 [2], TD_1 [1], TD_1 [0] TD_2 [3], TD_2 [2], TD_2 [1], TD_2 [0] TD_3 [3], TD_3 [2], TD_3 [1], TD_3 [0]	Output	2.5 V CMOS	**Transmit Data.** Bits [3:0] are clocked on the rising edge of TXC. Bits [7:4] are clocked on the falling edge of TXC.
	TX_CTL_0, TX_CTL_1, TX_CTL_2, TX_CTL_3	Output	2.5 V CMOS	**Transmit Control.** This signal is TXEN on the rising edge of TXC and a logical derivative of TXEN and TXERR on the falling edge of TXC.
V23, AA24, AD11, V4	RXC_3, RXC_2, RXC_1, RXC_0	Input	2.5 V CMOS	**Receiver Reference Clock.** Operates at: 125 MHz for 1 Gigabit 25 MHz for 100 Mbps
	RD_0 [3:0], RD_1 [3:0] RD_2 [3:0], RD_3 [3:0]	Input	2.5 V CMOS	**Receive Data.** Bits [3:0] are clocked on the rising edge of RXC. Bits [7:4] are clocked on the falling edge of RXC.
	RX_CTL_0, RX_CTL_1 RX_CTL_2, RX_CTL_3	Input	2.5 V CMOS	**Receive Control.** This signal is RXDV on the rising edge of RXC and a logical derivative of RXDV and RXERR on the falling edge of RXC.
AB14, AC20, AD7, AA1	TXC_3, TXC_2 TXC_1, TXC_0	Output	2.5 V CMOS	**Source Synchronous Transmit Clock.** This clock is supplied synchronous to the transmit data bus in either RGMII or GMII mode.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 11 of 15)

Ball Designator	Signal Name	Type	Standard	Description
Microprocessor Interface				
T3, U3, V3, V2, V1, U1, T1, R1, P1, N1, P3	uPx_Add[10], uPx_Add[9], uPx_Add[8], uPx_Add[7], uPx_Add[6], uPx_Add[5], uPx_Add[4], uPx_Add[3], uPx_Add[2], uPx_Add[1], uPx_Add[0]	Input	3.3 V LVTTL	Address bus from microprocessor
W3, T2	uPx_BAdd[1], uPx_BAdd[0]	Input	3.3 V LVTTL	**16-bit mode:** Data word select 16-bit mode uses uPx_BAdd[1]. **8-bit mode:** uPx_BAdd[1:0] selects the individual bytes.
L17, J17, H16, J16, M15, N15, K15, H14, K13, G12, K12, G11, H11, G10, K10, J10, N10, J9, H9, L8, N7, L7, L6, P5, K5, M5, N5, L4, M3, L3, K3, L2	uPx_Data[31], uPx_Data[30], uPx_Data[29], uPx_Data[28], uPx_Data[27], uPx_Data[26], uPx_Data[25], uPx_Data[24], uPx_Data[23], uPx_Data[22], uPx_Data[21], uPx_Data[20], uPx_Data[19], uPx_Data[18], uPx_Data[17], uPx_Data[16], uPx_Data[15], uPx_Data[14], uPx_Data[13], uPx_Data[12], uPx_Data[11], uPx_Data[10], uPx_Data[9], uPx_Data[8], uPx_Data[7], uPx_Data[6], uPx_Data[5], uPx_Data[4], uPx_Data[3], uPx_Data[2], uPx_Data[1], uPx_Data[0]	Bi-Directional	3.3 V LVTTL	**Data bus.** **32-bit mode:** Uses [31:0] **16-bit mode:** Uses [15:0] **8-bit mode:** Uses [7:0]
R3	uPx_Cs	Input	3.3 V LVTTL	**Chip Select.** Active Low.
T4	uPx_Wr	Input	3.3 V LVTTL	**Write Strobe.** Active Low.
V6	uPx_Rd	Input	3.3 V LVTTL	**Read Strobe.** Active Low.
M1	uPx_Rdy	Output	3.3 V LVTTL	**Cycle complete indicator.** Active Low.
T5, U16	uPx_Width[1], uPx_Width[0]	Input	3.3 V LVTTL	**Data bus width select.** Specifies microprocessor bus width. **uPx_Width[1:0]** **Mode** 00 8-bit 01 16-bit 1x 32-bit
Pause Frame Control Interface				
P21, P20. N20	TxPauseAdd(2), TxPauseAdd(1), TxPauseAdd(0)	Input	2.5 V CMOS	Port selection address for pause frame insertion.
T20	TxPauseFr	Input	2.5 V CMOS	Tx Pause Interface Strobe.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 12 of 15)

Ball Designator	Signal Name	Type	Standard	Description
GBIC Interface (All pins are shared with the GMII pins)				
	TX_DISABLE_0 TX_DISABLE_1 TX_DISABLE_2 TX_DISABLE_3	Output	2.5 V CMOS	Outputs used to disable the GBIC transmitter. **Note:** These signals are multiplexed with the TCD_*n*[4] bits of the GMII Interface
	MOD_DEF_0 MOD_DEF_1 MOD_DEF_2 MOD_DEF_3	Input	2.5 V CMOS	Inputs used to determine when a GBIC module is present **Note:** These signals are multiplexed with the RXD_*n*[4] bits of the GMII interface.
	RX_LOS_0 RX_LOS_1 RX_LOS_2 RX_LOS_3	Input	2.5 V CMOS	Inputs used to determine when the GBIC receiver has lost synchronization. **Note:** These signals are multiplexed with the RXD_*n*[6] bits of the GMII interface.
	TX_FAULT_0 TX_FAULT_1 TX_FAULT_2 TX_FAULT_3	Input	2.5 V CMOS	Inputs used to determine a GBIC transmitter fault **Note:** These signals are multiplexed with the RXD_*n*[5] bits of the GMII Interface.
P19	RX_LOS_Int	Output	2.5 V CMOS	Open drain interrupt output to signal an RX_LOS condition.
P23	TX_FAULT_Int	Output	2.5 V CMOS	Open drain interrupt output to signal a TX_FAULT condition.
N22	MOD_DEF_Int	Output	2.5 V CMOS	Open drain interrupt output to signal a MOD_DEF condition.
L23	I^2C_CLK	Output	2.5 V CMOS	Clock used for the I^2C bus interface.
P24, N24, M24, L24	I^2C DATA_3, I^2C DATA_2, I^2C DATA_1, I^2C DATA_0	Bi-Directional	2.5 V CMOS	Data I/O for the I^2C bus interface
MDIO Interface				
V21	MDIO	Bi-Directional	2.5 V CMOS	Management data input and output.
W24	MDC	Output	2.5 V CMOS	Management clock to external devices.
LED Interface				
K24	LED_CLK	Output	2.5 V CMOS	Clock output for the LED block
M22	LED_DATA	Output	2.5 V CMOS	Data output for the LED block
L22	LED_LATCH	Output	2.5 V CMOS	Latch enable for LED block

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 13 of 15)

Ball Designator	Signal Name	Type	Standard	Description
JTAG Interface				
J22	TCLK	Input	2.5 V CMOS	JTAG Test Clock
H22	TMS	Input	2.5 V CMOS	Test Mode Select
J24	TDI	Input	2.5 V CMOS	Test Data Input
H24	TDO	Output	2.5 V CMOS	Test Data Output
J23	TRSTN	Input	2.5 V CMOS	Test Reset; reset input for JTAG test
System Interface				
AD19	CLK125	Input	2.5 V CMOS	Input clock to PLL; 125 MHz +/- 50 ppm
AD12	Sys_Res	Input	2.5 V CMOS	System hard reset. Active low.

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 14 of 15)

Ball Designator	Signal Name	Type	Standard	Description
Power Supplies				
B6, B10, B15, B19, DR, D8, D12, D13, D17, D21, F2, F6, F10, F15, F19, F23, H4, H8, H12, H13, H17, H21, J10, J15, K2, K6, K9, K11, K14, K16, K19, K23, L5, L10, L12, L13, L15, L20, M4, M8, M11, M14, M17, M21, N4, N8, N11, N14, N17, N21, P10, P12, P13, P15, R2, R6, R7, R9, R11, R14, R16, R19, R23, T10, T15, U4, U8, U12, U13, U17, U21, W2, W6, W10, W15, W19, W23, AA4, AA8, AA12, AA13, AA17, AA21, AB12, AC6, AC10, AC14, AC15, AC19	GND	Input	–	Digital ground
A10, C12, D6, D10, D11, D15, D19, F4, F21, H10, H15, J11, J14, J20, K4, K8, K17, K21, L9, L11, L14, L16, P9, P11, P14, P16, R4, R8, R17, R21, T11, T14, U10, U15, W4, W21, AA6, AA10, AA15, AA19	VDD	Input	1.8 V	Digital 1.8 V supply

Table 1. Intel® IXF1104 Signal Descriptions (Sheet 15 of 15)

Ball Designator	Signal Name	Type	Standard	Description
B4, B8, B12, D2, F8, F12, H2, H6, J12, M2, M6, M9, M12	VDD2	Input	3.3 V	Digital 3.3 V supply
B13, B17, B21, D23, F13, F17, H19, H23, J13, M13, M16, M19, M23	VDD3	Input	3.3 V	Digital 3.3 V supply
N13, N16, N19, N23, T13, U19, U23, W13, W17, AA23, AC13, AC17, AC21	VDD4	Input	2.5 V	Digital 2.5 V supply
N2, N6, N9, N12, T12, U2, U6, W8, W12, AA2, AC4, AC8, AC12	VDD5	Input	2.5 V	Digital 2.5 V supply
A4	PLL1_GNDA	Input	0 V	PLL1 analog ground
A5	PLL1_VDDA	Input	1.8 V	PLL1 analog 1.8 V supply
A21	PLL2_GNDA	Input	0 V	PLL2 analog ground
A20	PLL2_VDDA	Input	1.8 V	PLL2 analog 1.8 V supply
AD21	PLL3_GNDA	Input	0 V	PLL3 analog ground
AD20	PLL3_VDDA	Input	2.5 V	PLL3 analog 2.5 V supply
AB16	TXAVTT	Input	1.8 V	SerDes transmitter analog 1.8 V supply
T23	RXAVTT	Input	1.8 V	SerDes receiver analog 1.8 V supply
U14	TXAV25	Input	2.5 V	SerDes transmitter analog 2.5 V supply
R18	RXAV25	Input	2.5 V	SerDes transmitter analog 2.5 V supply

3.3 Ball Usage Summary

Table 2. Ball Usage Summary

Type	Quantity
Inputs	158
Outputs	126
Bi-directional	37
Total Signals	321
Power	75
Ground	82
No Connects	74
Total	**552**

3.4 Ball State During Reset

Table 3. Definition of Output and Bi-directional Balls During Hardware Reset (Sheet 1 of 2)

Function	Ball Name	Ball Reset State	Comment
SPI3	DTPA[3:0]	0x0	–
SPI3	STPA	0x0	–
SPI3	PTPA	0x0	–
SPI3	RDAT[31:0]	0x00000000	–
SPI3	RVAL[3:0]	0x0	–
SPI3	RERR[3:0]	0x0	–
SPI3	RPRTY[3:0]	0x0	–
SPI3	RMOD[1:0]	0x0	–
SPI3	RSX	0x0	–
SPI3	RSOP[3:0]	0x0	–
SPI3	REOP[3:0]	0x0	–
JTAG	TDO	0x0	–
MDIO	MDIO	0xZ (High Impedance)	Bi-directional
MDIO	MDC	0x0	–
Microprocessor	UPX_DATA[31:0]	0xZZZZZZZZ (High Impedance)	Bi-directional
Microprocessor	UPX_RDYN	0X1	Open-drain output, requires an external pull-up
LED	LED_CLK	0x0	–
LED	LED_DATA	0x0	–
LED	LED_LATCH	0x0	–
GMII/RGMII	TXC[3:0]	0xZ (High Impedance)	Fiber mode is the default. Copper interfaces are disabled.
GMII/RGMII	TXD_3[7:0]	0xZZZ0ZZZ	Fiber mode is the default. Bit 4 driven by the GBIC module as MOD_DEF[3].
GMII/RGMII	TXD_2[7:0]	0xZZZ0ZZZ	Fiber mode is the default. Bit 4 driven by the GBIC module as MOD_DEF[2].
GMII/RGMII	TXD_1[7:0]	0xZZZ0ZZZ	Fiber mode is the default. Bit 4 driven by the GBIC module as MOD_DEF[1].
GMII/RGMII	TXD_0[7:0]	0xZZZ0ZZZ	Fiber mode is the default. Bit 4 driven by the GBIC module as MOD_DEF[0].
GMII/RGMII	TX_EN[3:0]	0xZ	Fiber mode is the default. Copper interfaces are disabled.
GMII/RGMII	TX_ER[3:0]	0xZ	Fiber mode is the default. Copper interfaces are disabled.
NOTE: Z = High impedance.			

Table 3. Definition of Output and Bi-directional Balls During Hardware Reset (Sheet 2 of 2)

Function	Ball Name	Ball Reset State	Comment
RGMII	TX_CTL[3:0]	0xZ	Fiber mode is the default. Copper interfaces are disabled.
SerDes	TXP[3:0]	0x0	–
SerDes	TXN[3:0]	0x0	–
GBIC	TXFAULT_INT	0xZ	–
GBIC	RX_LOS_INT	0xZ	–
GBIC	MOD_DEF_INT	0xZ	–
GBIC	I^2C_CLK	0x1	Open-drain output, requires external pull-up.
GBIC	I^2C_DATA[3:0]	0xF	Open-drain output, requires external pull-up.
NOTE: Z = High impedance.			

3.5 Power Supply Sequencing

The power-up and power-down sequences described in this section must be followed to ensure correct IXF1104 operation. The sequence described in Section 3.5 covers all digital and analog supplies for the IXF1104.

Note: Ensure that the 1.8 V supply is applied and stable prior to the application of the 2.5 V supply to the cores.

Caution: Failure to follow the sequence described in this section will damage the IXF1104.

Note: If the 2.5 V supply exceeds the 1.8 V supply by more than 2.0 V during power-up or power-down, damage can occur to the ESD structures within the analog IOs.

Since the power-down sequence is the reverse of the power-up sequence, remove the analog supply prior to the removal of the digital core supply.

Figure 4 and Table 4 provide the IXF1104 power supply sequencing.

Figure 4. Power Supply Sequencing

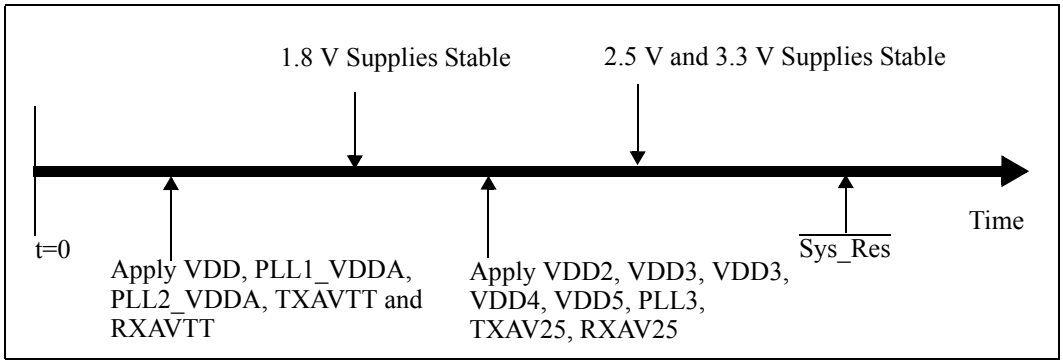


Table 4. Power Supply Sequencing

Power Supply	Power-Up Order	Time Delta to Next Supply[1]	Notes
VDD	First	0	Digital 1.8 V core supply
PLL1_VDDA	First	0	1.8 V analog supply to PLL1
PLL2_VDDA	First	0	1.8 V analog supply to PLL2
TXAVTT	First	0	1.8 V analog supply to SerDes
RXAVTT	First	0	1.8 V analog supply to SerDes
VDD2	Second	10 µs	Digital 3.3 V supply
VDD3	Second	10 µs	Digital 3.3 V supply
VDD4	Second	10 µs	Digital 2.5 V supply
VDD5	Second	10 µs	Digital 2.5 V supply
PLL3	Second	10 µs	2.5 V analog supply to PLL3
TXAV25	Second	10 µs	2.5 V analog supply to SerDes
RXAV25[a]	Second	10 µs	2.5 V analog supply to SerDes

1. The value of 10 µs given is a nominal value only. The exact time difference between the application of the 2.5 V analog supply is determined by a number of factors, depending on the power management method used. The key requirement that must be met to avoid damage to the IXF1104 is that the TXAV25 supply must not exceed the VDD supply by more than 2 V at any time during the power-up or power-down sequence.

3.6 Pull-Up/Pull-Down and Unused Ball Guidelines

The signals shown in Table 5 require a pull-up or pull-down resistor to be added to the board design for normal operation. Any balls marked as unused (N/C) should be unconnected.

Table 5. Pull-Up/Pull-Down and Unused Ball Guidelines

Pin Name	Pull-Up/Pull-Down	Comments
Tx_Fault_Int	Pull-up	4K7 to 2.5 V. GBIC Interface signal with open-drain IO.
Rx_LOS_Int	Pull-up	4K7 to 2.5 V. GBIC Interface signal with open-drain IO.
Mod_Def_Int	Pull-up	4K7 to 2.5 V. GBIC Interface signal with open-drain IO.
TDI	Pull-up	10 K to 3.3 V. JTAG test pin.
TDO	Pull-up	10 K to 3.3 V. JTAG test pin.
TMS	Pull-up	10 K to 3.3 V. JTAG test pin.
TCLK	Pull-up	10 K to 3.3 V. JTAG test pin.
TRSTN	Pull-up	10 K to 3.3 V. JTAG test pin.

4.0 Ball Assignments and Ball List Tables

4.1 Ball Assignments

See Figure 5, Table 6 "Ball List in Alphanumeric Order by Signal Name" on page 40, and Table 7 "Ball List in Alphanumeric Order by Ball Location" on page 46 for the IXF1104 ball assignments.

Figure 5. Intel® IXF1104 552-Ball CBGA Assignments (Top View)

	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	AD1	AC1	AB1	AA1	Y1	W1	V1	U1	T1	R1	P1	N1	M1	L1	K1	J1	H1	G1	F1	E1	D1	C1	B1	A1	1
2	AD2	AC2	AB2	AA2	Y2	W2	V2	U2	T2	R2	P2	N2	M2	L2	K2	J2	H2	G2	F2	E2	D2	C2	B2	A2	2
3	AD3	AC3	AB3	AA3	Y3	W3	V3	U3	T3	R3	P13	N3	M3	L3	K3	J3	H3	G3	F3	E3	D3	C3	B3	A3	3
4	AD4	AC4	AB4	AA4	Y4	W4	V4	U4	T4	R4	P4	N4	M4	L4	K4	J4	H4	G4	F4	E4	D4	C4	B4	A4	4
5	AD5	AC5	AB5	AA4	Y5	W5	V5	U5	T5	R5	P5	N5	M5	L5	K5	J5	H5	G5	F5	E5	D5	C5	B5	A5	5
6	AD6	AC6	AB6	AA6	Y6	W6	V6	U6	T6	R6	P6	N6	M6	L6	K6	J6	H6	G6	F6	F6	D6	C6	B6	A6	6
7	AD7	AC7	AB7	AA7	Y7	W7	V7	U7	T7	R7	P7	N7	M7	L7	K7	J7	H7	G7	F7	E7	D7	G7	B7	A7	7
8	AD8	AC8	AB8	AA8	Y8	W8	V8	U8	T8	R8	P8	N8	M8	L8	K8	J8	H8	G8	F8	E8	D8	C8	B28	A8	8
9	AD9	AC9	AB9	AA9	Y9	W9	V9	U9	T9	R9	P9	N9	M9	L9	K9	J9	H9	G9	F9	E9	D9	C9	B9	A9	9
10	AD10	AC10	AB10	AA10	Y10	W10	V10	U10	T10	R10	P10	N10	M10	L10	K10	J10	H10	G10	F10	E10	D10	C10	B10	A10	10
11	AD11	AC11	AB11	AA11	Y11	W11	V11	U11	T11	R11	P11	N11	M11	L11	K11	J11	H11	G11	F11	E11	D11	C11	B11	A11	11
12	AD12	AC12	AB12	AA12	Y12	W12	V12	U12	T12	R12	P12	N12	M12	L12	K12	J12	H12	G12	F12	E12	D12	C12	B12	A12	12
13	AD13	AC13	AB13	AA13	Y13	W13	V13	U13	T13	R13	P13	N13	M13	L13	K13	J13	H13	G13	F13	E13	D13	C13	B13	A13	13
14	AD14	AC14	AB14	AA14	Y14	W14	V14	U14	T14	R14	P14	N14	M14	L14	K14	J14	H14	G14	F14	E14	D14	C14	B14	A14	14
15	AD15	AC15	AB15	AA15	Y15	W15	V15	U15	T15	R15	P15	N15	M15	L15	K15	J15	H15	G15	F15	E15	D15	C15	B15	A15	15
16	AD16	AC16	AB16	AA16	Y16	W16	V16	U16	T16	R16	P16	N16	M16	L16	K16	J16	H16	G16	F16	E16	D16	C16	B16	A16	16
17	AD17	AC17	AB17	AA17	Y17	W17	V17	U17	T17	R17	P17	N17	M17	L17	K17	J17	H17	G17	F17	E17	D17	C17	B17	A17	17
18	AD18	AC18	AB18	AA18	Y18	W18	V18	U18	T18	R18	P18	N18	M18	L18	K18	J18	H18	G18	F18	E18	D18	C18	B18	A18	18
19	AD19	AC19	AB19	AA19	Y19	W19	V19	U19	T19	R19	P19	N19	M19	L19	K19	J19	H19	G19	F19	E19	D19	C19	B19	A19	19
20	AD20	AC20	AB20	AA20	Y20	W20	V20	U20	T20	R20	P20	N20	M20	L20	K20	J20	H20	G20	F20	E20	D20	C20	B20	A20	20
21	AD21	AC21	AB21	AA21	Y21	W21	V21	U21	T21	R21	P21	N121	M21	L21	K21	J21	H21	G21	F21	E21	D21	C21	B21	A21	21
22	AD22	AC22	AB22	AA22	Y22	W22	V22	U22	T22	R22	P22	N22	M22	L22	K22	J22	H22	G22	F22	E22	D22	C22	B22	A22	22
23	AD23	AC23	AB23	AA23	Y23	W23	V23	U23	T23	R23	P23	N23	M23	L23	K23	J23	H23	G23	F23	E23	D23	C23	B23	A23	23
24	AD24	AC24	AB24	AA24	Y24	W24	V24	U24	T24	R24	P24	N24	M24	L24	K24	J24	H24	G24	F24	E24	D24	C24	B24	A24	24
	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

= No Pad (A1)

= No Ball (A2, A3, A22, A23, A24, B1, B2, B23, B24, C1, C24, AB1, AB24, AC1, AC2, AC23, AC24, AD1, AD2, AD3, AD22, AD23, AD24)

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4.2 Ball List Tables

4.2.1 Balls Listed in Alphabetic Order by Signal Name

Table 6 shows the ball locations and signal names arranged in alphanumeric order by signal name.

Table 6. Ball List in Alphanumeric Order by Signal Name

Signal Name	Ball Location
CLK125	AD19
COL[0]	AB6
COL[1]	AB10
COL[2]	AD15
COL[3]	AB17
CRS[0]	AA5
CRS[1]	AA9
CRS[2]	AB15
CRS[3]	AC16
DTPA[0]	D3
DTPA[1]	L1
DTPA[2]	A9
DTPA[3]	J7
GND	B6
GND	B10
GND	B15
GND	B19
GND	D4
GND	D8
GND	D12
GND	D13
GND	D17
GND	D21
GND	F2
GND	F6
GND	F10
GND	F15
GND	F19
GND	F23
GND	H4
GND	H8
GND	H12
GND	H13
GND	H17
GND	H21
GND	J10
GND	J15
GND	K2
GND	K6
GND	K9
GND	K11
GND	K14
GND	K16
GND	K19
GND	K23
GND	L5
GND	L10
GND	L12
GND	L13
GND	L15
GND	L20
GND	M4
GND	M8
GND	M11
GND	M14
GND	M17
GND	M21
GND	N4
GND	N8
GND	N11
GND	N14
GND	N17
GND	N21
GND	P10
GND	P12
GND	P13
GND	P15
GND	R2
GND	R6
GND	R7
GND	R9
GND	R11
GND	R14
GND	R16
GND	R19
GND	R23
GND	T10
GND	T15
GND	U4
GND	U8
GND	U12
GND	U13
GND	U17
GND	U21
GND	W2
GND	W6
GND	W10
GND	W15
GND	W19
GND	W23
GND	AA4
GND	AA8
GND	AA12

Signal Name	Ball Location
GND	AA13
GND	AA17
GND	AA21
GND	AB12
GND	AC6
GND	AC10
GND	AC14
GND	AC15
GND	AC19
I2C_CLK	L23
I2C_DATA[0]	L24
I2C_DATA[1]	M24
I2C_DATA[2]	N24
I2C_DATA[3]	P24
LED_CLK	K24
LED_DATA	M22
LED_LATCH	L22
MDC	W24
MDIO	V21
MOD_DEF_INT	N22
N/C	A1
N/C	A2
N/C	A3
N/C	A22
N/C	A23
N/C	A24
N/C	B1
N/C	B2
N/C	B23
N/C	B24
N/C	C1
N/C	C24
N/C	D24
N/C	E12
N/C	F11
N/C	G15
N/C	H7
N/C	H18

Signal Name	Ball Location
N/C	J21
N/C	K7
N/C	K18
N/C	K20
N/C	K22
N/C	L18
N/C	L19
N/C	L21
N/C	M7
N/C	M18
N/C	M20
N/C	N3
N/C	N18
N/C	P2
N/C	P4
N/C	P6
N/C	P7
N/C	P8
N/C	P17
N/C	P18
N/C	R5
N/C	R10
N/C	R12
N/C	R13
N/C	R15
N/C	R20
N/C	T6
N/C	T7
N/C	T8
N/C	T9
N/C	T21
N/C	T22
N/C	U5
N/C	U7
N/C	U9
N/C	U11
N/C	U18
N/C	V9

Signal Name	Ball Location
N/C	V10
N/C	V11
N/C	V13
N/C	AB1
N/C	AB18
N/C	AB24
N/C	AC1
N/C	AC2
N/C	AC23
N/C	AC24
N/C	AD1
N/C	AD2
N/C	AD3
N/C	AD4
N/C	AD5
N/C	AD22
N/C	AD23
N/C	AD24
PLL1_GNDA	A4
PLL1_VDDA	A5
PLL2_GNDA	A21
PLL2_VDDA	A20
PLL3_GNDA	AD21
PLL3_VDDA	AD20
PTPA	B11
RDAT[0]	A15
RDAT[1]	A14
RDAT[2]	B14
RDAT[3]	C14
RDAT[4]	C13
RDAT[5]	D14
RDAT[6]	E14
RDAT[8]	A17
RDAT[9]	C17
RDAT[10]	D16
RDAT[11]	E16
RDAT[12]	F16
RDAT[13]	E17

Signal Name	Ball Location
RDAT[14]	E18
RDAT[15]	F18
RDAT[16]	B20
RDAT[17]	B22
RDAT[18]	C20
RDAT[19]	C21
RDAT[20]	C22
RDAT[21]	D22
RDAT[22]	E22
RDAT[23]	E21
RDAT[24]	G18
RDAT[25]	G19
RDAT[26]	G20
RDAT[27]	G21
RDAT[28]	G22
RDAT[29]	G23
RDAT[30]	G24
RDAT[31]	F24
RDAT[7]	F14
RENB[0]	A13
RENB[1]	A18
RENB[2]	C19
RENB[3]	E24
REOP[0]	C16
REOP[1]	D18
REOP[2]	C23
REOP[3]	J19
RERR[0]	A16
RERR[1]	G17
RERR[2]	D20
RERR[3]	H20
RFCLK	A19
RMOD[0]	G14
RMOD[1]	G13
RPRTY[0]	E15
RPRTY[1]	G16
RPRTY[2]	E20
RPRTY[3]	F20

Signal Name	Ball Location
RSOP[0]	B16
RSOP[1]	C18
RSOP[2]	E23
RSOP[3]	J18
RSX	E13
RVAL[0]	C15
RVAL[1]	B18
RVAL[2]	E19
RVAL[3]	F22
RX_LOS_INT	P19
RXAV25	R18
RXAVTT	T23
RXC[0]	V4
RXC[1]	AD11
RXC[2]	AA24
RXC[3]	V23
RXD_0[0]	V8
RXD_0[1]	V7
RXD_0[2]	W7
RXD_0[3]	Y7
RXD_0[4]	Y6
RXD_0[5]	Y5
RXD_0[6]	AB5
RXD_0[7]	AC5
RXD_1[0]	Y9
RXD_1[1]	Y11
RXD_1[2]	W11
RXD_1[3]	W9
RXD_1[4]	AD10
RXD_1[5]	AC11
RXD_1[6]	AA11
RXD_1[7]	Y10
RXD_2[0]	Y20
RXD_2[1]	Y21
RXD_2[2]	Y22
RXD_2[3]	Y23
RXD_2[4]	W22
RXD_2[5]	V20

Signal Name	Ball Location
RXD_2[6]	V19
RXD_2[7]	W20
RXD_3[0]	Y17
RXD_3[1]	Y18
RXD_3[2]	Y19
RXD_3[3]	W18
RXD_3[4]	T16
RXD_3[5]	T17
RXD_3[6]	T18
RXD_3[7]	T19
RXDV[0]	V5
RXDV[1]	AB11
RXDV[2]	Y24
RXDV[3]	V18
RXERR[0]	W5
RXERR[1]	Y12
RXERR[2]	AA22
RXERR[3]	U20
RXN[0]	R22
RXN[1]	U22
RXN[2]	R24
RXN[3]	V24
RXP[0]	P22
RXP[1]	V22
RXP[2]	T24
RXP[3]	U24
STPA	C11
SYS_RSTN	AD12
TADR[0]	A11
TADR[1]	A12
TCLK	J22
TDAT[0]	B3
TDAT[1]	C2
TDAT[2]	C3
TDAT[3]	D1
TDAT[4]	C4
TDAT[5]	C5
TDAT[6]	B5

Signal Name	Ball Location
TDAT[7]	C6
TDAT[10]	G2
TDAT[11]	H1
TDAT[12]	J1
TDAT[13]	J2
TDAT[14]	J3
TDAT[15]	H3
TDAT[16]	E5
TDAT[17]	E6
TDAT[18]	E7
TDAT[19]	E8
TDAT[20]	E9
TDAT[21]	E10
TDAT[22]	F9
TDAT[23]	C8
TDAT[24]	G4
TDAT[25]	G5
TDAT[26]	G6
TDAT[27]	G7
TDAT[28]	G8
TDAT[29]	G9
TDAT[30]	F5
TDAT[31]	F7
TDAT[8]	F1
TDAT[9]	G1
TDI	J24
TDO	H24
TENB[0]	B7
TENB[1]	E2
TENB[2]	C9
TENB[3]	J4
TEOP[0]	A7
TEOP[1]	F3
TEOP[2]	E4
TEOP[3]	H5
TERR[0]	A8
TERR[1]	K1
TERR[2]	E11

Signal Name	Ball Location
TERR[3]	J8
TFCLK	D7
TMOD[0]	A6
TMOD[1]	D9
TMS	H22
TPRTY[0]	D5
TPRTY[1]	G3
TPRTY[2]	B9
TPRTY[3]	J6
TRSTN	J23
TSOP[0]	C7
TSOP[1]	E3
TSOP[2]	C10
TSOP[3]	J5
TSX	E1
TX_FAULT_INT	P23
TXAV25	U14
TXAVTT	AB16
TXC[0]	AA1
TXC[1]	AD7
TXC[2]	AC20
TXC[3]	AB14
TXD_0[0]	Y1
TXD_0[1]	Y2
TXD_0[2]	Y3
TXD_0[3]	AA3
TXD_0[4]	AB3
TXD_0[5]	AC3
TXD_0[6]	AB4
TXD_0[7]	Y4
TXD_1[0]	AC7
TXD_1[1]	AB7
TXD_1[2]	AB09
TXD_1[3]	AD9
TXD_1[4]	AA7
TXD_1[5]	AB8
TXD_1[6]	AD8
TXD_1[7]	AC9

Signal Name	Ball Location
TXD_2[0]	AB20
TXD_2[1]	AB21
TXD_2[2]	AB22
TXD_2[3]	AB23
TXD_2[4]	AD16
TXD_2[5]	AB19
TXD_2[6]	AA20
TXD_2[7]	AA18
TXD_3[0]	V14
TXD_3[1]	V15
TXD_3[2]	V16
TXD_3[3]	V17
TXD_3[4]	AA14
TXD_3[5]	Y15
TXD_3[6]	AA16
TXD_3[7]	W14
TXEN[0]	AB2
TXEN[1]	Y8
TXEN[2]	AC22
TXEN[3]	V12
TxErr[0]	W1
TxErr[1]	AD6
TxErr[2]	AD17
TxErr[3]	AB13
TXN[0]	Y14
TXN[1]	AD14
TXN[2]	Y16
TXN[3]	AD18
TXP[0]	Y13
TXP[1]	AD13
TXP[2]	W16
TXP[3]	AC18
TxPause_Add[0]	N20
TxPause_Add[1]	P20
TxPause_Add[2]	P21
TxPauseFr	T20
uPx_Addr[0]	P3
uPx_Addr[3]	R1

Signal Name	Ball Location
uPx_Addr[5]	U1
uPx_Addr[9]	U3
uPx_Addr[1]	N1
uPx_Addr[10]	T3
uPx_Addr[2]	P1
uPx_Addr[4]	T1
uPx_Addr[6]	V1
uPx_Addr[7]	V2
uPx_Addr[8]	V3
uPx_BAddr[0]	T2
uPx_BAddr[1]	W3
uPx_CsN	R3
uPx_Data[0]	L2
uPx_Data[8]	P5
uPx_Data[1]	K3
uPx_Data[10]	L7
uPx_Data[11]	N7
uPx_Data[12]	L8
uPx_Data[13]	H9
uPx_Data[14]	J9
uPx_Data[15]	N10
uPx_Data[16]	M10
uPx_Data[17]	K10
uPx_Data[18]	G10
uPx_Data[19]	H11
uPx_Data[2]	L3
uPx_Data[20]	G11
uPx_Data[21]	K12
uPx_Data[22]	G12
uPx_Data[23]	K13
uPx_Data[24]	H14
uPx_Data[25]	K15
uPx_Data[26]	N15
uPx_Data[27]	M15
uPx_Data[28]	J16
uPx_Data[29]	H16
uPx_Data[3]	M3
uPx_Data[30]	J17

Signal Name	Ball Location
uPx_Data[31]	L17
uPx_Data[4]	L4
uPx_Data[5]	N5
uPx_Data[6]	M5
uPx_Data[7]	K5
uPx_Data[9]	L6
uPx_RdN	V6
uPx_RdyN	M1
uPx_Width[0]	U16
uPx_Width[1]	T5
uPx_WrN	T4
VCC	A10
VCC	C12
VDD	D6
VDD	D10
VCC	D11
VDD	D15
VDD	D19
VDD	F4
VDD	F21
VDD	H10
VDD	H15
VDD	J11
VDD	J14
GND	J20
VDD	K4
VDD	K8
VDD	K17
VDD	K21
VDD	L9
VDD	L11
VDD	L14
VDD	L16
VDD	P9
VDD	P11
VDD	P14
VDD	P16
VDD	R4

Signal Name	Ball Location
VDD	R8
VDD	R17
VDD	R21
VDD	T11
VDD	T14
VDD	U10
VDD	U15
VDD	W4
VDD	W21
VDD	AA6
VDD	AA10
VDD	AA15
VDD	AA19
VDD2	B4
VDD2	B8
VDD2	B12
VDD2	D2
VDD2	F8
VDD2	F12
VDD2	H2
VDD2	H6
VDD2	J12
VDD2	M2
VDD2	M6
VDD2	M9
VDD2	M12
VDD3	B13
VDD3	B17
VDD3	B21
VDD3	D23
VDD3	F13
VDD3	F17
VDD3	H19
VDD3	H23
VDD3	J13
VDD3	M13
VDD3	M16
VDD3	M19

Signal Name	Ball Location
VDD3	M23
VDD4	N13
VDD4	N16
VDD4	N19
VDD4	N23
VDD4	T13
VDD4	U19
VDD4	U23
VDD4	W13
VDD4	W17
VDD4	AA23
VDD4	AC13
VDD4	AC17
VDD4	AC21
VDD5	N2
VDD5	N6
VDD5	N9
VDD5	N12
VDD5	T12
VDD5	U2
VDD5	U6
VDD5	W8
VDD5	W12
VDD5	AA2
VDD5	AC4
VDD5	AC8
VDD5	AC12

4.2.2 Balls Listed in Alphabetic Order by Ball Location

Table 7 shows the ball locations and signal names arranged in order by ball location.

Table 7. Ball List in Alphanumeric Order by Ball Location

Ball Location	Signal Name
A1	N/C
A2	N/C
A3	N/C
A4	PLL1_GNDA
A5	PLL1_VDDA
A6	TMOD[0]
A7	TEOP[0]
A8	TERR[0]
A9	DTPA[2]
A10	VCC
A11	TADR[0]
A12	TADR[1]
A13	RENB[0]
A14	RDAT[1]
A15	RDAT[0]
A16	RERR[0]
A17	RDAT[8]
A18	RENB[1]
A19	RFCLK
A20	PLL2_VDDA
A21	PLL2_GNDA
A22	N/C
A23	N/C
A24	N/C
B1	N/C
B2	N/C
B3	TDAT[0]
B4	VDD2
B5	TDAT[6]
B6	GND
B7	TENB[0]
B8	VDD2
B9	TPRTY[2]
B10	GND
B11	PTPA
B12	VDD2
B13	VDD3
B14	RDAT[2]
B15	GND
B16	RSOP[0]
B17	VDD3
B18	RVAL[1]
B19	GND
B20	RDAT[16]
B21	VDD3
B22	RDAT[17]
B23	N/C
B24	N/C
C1	N/C
C2	TDAT[1]
C3	TDAT[2]
C4	TDAT[4]
C5	TDAT[5]
C6	TDAT[7]
C7	TSOP[0]
C8	TDAT[23]
C9	TENB[2]
C10	TSOP[2]
C11	STPA
C12	VCC
C13	RDAT[4]
C14	RDAT[3]
C15	RVAL[0]
C16	REOP[0]
C17	RDAT[9]
C18	RSOP[1]
C19	RENB[2]
C20	RDAT[18]
C21	RDAT[19]
C22	RDAT[20]
C23	REOP[2]
C24	N/C
D1	TDAT[3]
D2	VDD2
D3	DTPA[0]
D4	GND
D5	TPRTY[0]
D6	VDD
D7	TFCLK
D8	GND
D9	TMOD[1]
D10	VDD
D11	VCC
D12	GND
D13	GND
D14	RDAT[5]
D15	VDD
D16	RDAT[10]
D17	GND
D18	REOP[1]
D19	VDD
D20	RERR[2]
D21	GND
D22	RDAT[21]
D23	VDD3
D24	N/C
E1	TSX
E2	TENB[1]
E3	TSOP[1]
E4	TEOP[2]
E5	TDAT[16]

Ball Location	Signal Name
E6	TDAT[17]
E7	TDAT[18]
E8	TDAT[19]
E9	TDAT[20]
E10	TDAT[21]
E11	TERR[2]
E12	N/C
E13	RSX
E14	RDAT[6]
E15	RPRTY[0]
E16	RDAT[11]
E17	RDAT[13]
E18	RDAT[14]
E19	RVAL[2]
E20	RPRTY[2]
E21	RDAT[23]
E22	RDAT[22]
E23	RSOP[2]
E24	RENB[3]
F1	TDAT[8]
F2	GND
F3	TEOP[1]
F4	VDD
F5	TDAT[30]
F6	GND
F7	TDAT[31]
F8	VDD2
F9	TDAT[22]
F10	GND
F11	N/C
F12	VDD2
F13	VDD3
F14	RDAT[7]
F15	GND
F16	RDAT[12]
F17	VDD3
F18	RDAT[15]
F19	GND

Ball Location	Signal Name
F20	RPRTY[3]
F21	VDD
F22	RVAL[3]
F23	GND
F24	RDAT[31]
G1	TDAT[9]
G2	TDAT[10]
G3	TPRTY[1]
G4	TDAT[24]
G5	TDAT[25]
G6	TDAT[26]
G7	TDAT[27]
G8	TDAT[28]
G9	TDAT[29]
G10	uPx_Data[18]
G11	uPx_Data[20]
G12	uPx_Data[22]
G13	RMOD[1]
G14	RMOD[0]
G15	N/C
G16	RPRTY[1]
G17	RERR[1]
G18	RDAT[24]
G19	RDAT[25]
G20	RDAT[26]
G21	RDAT[27]
G22	RDAT[28]
G23	RDAT[29]
G24	RDAT[30]
H1	TDAT[11]
H2	VDD2
H3	TDAT[15]
H4	GND
H5	TEOP[3]
H6	VDD2
H7	N/C
H8	GND
H9	uPx_Data[13]

Ball Location	Signal Name
H10	VDD
H11	uPx_Data[19]
H12	GND
H13	GND
H14	uPx_Data[24]
H15	VDD
H16	uPx_Data[29]
H17	GND
H18	N/C
H19	VDD3
H20	RERR[3]
H21	GND
H22	TMS
H23	VDD3
H24	TDO
J1	TDAT[12]
J2	TDAT[13]
J3	TDAT[14]
J4	TENB[3]
J5	TSOP[3]
J6	TPRTY[3]
J7	DTPA[3]
J8	TERR[3]
J9	uPx_Data[14]
J10	GND
J11	VDD
J12	VDD2
J13	VDD3
J14	VDD
J15	GND
J16	uPx_Data[28]
J17	uPx_Data[30]
J18	RSOP[3]
J19	REOP[3]
J20	GND
J21	N/C
J22	TCLK
J23	TRSTN

Ball Location	Signal Name
J24	TDI
K1	TERR[1]
K2	GND
K3	uPx_Data[1]
K4	VDD
K5	uPx_Data[7]
K6	GND
K7	N/C
K8	VDD
K9	GND
K10	uPx_Data[17]
K11	GND
K12	uPx_Data[21]
K13	uPx_Data[23]
K14	GND
K15	uPx_Data[25]
K16	GND
K17	VDD
K18	N/C
K19	GND
K20	N/C
K21	VDD
K22	N/C
K23	GND
K24	LED_CLK
L1	DTPA[1]
L2	uPx_Data[0]
L3	uPx_Data[2]
L4	uPx_Data[4]
L5	GND
L6	uPx_Data[9]
L7	uPx_Data[10]
L8	uPx_Data[12]
L9	VDD
L10	GND
L11	VDD
L12	GND
L13	GND

Ball Location	Signal Name
L14	VDD
L15	GND
L16	VDD
L17	uPx_Data[31]
L18	N/C
L19	N/C
L20	GND
L21	N/C
L22	LED_LATCH
L23	I2C_CLK
L24	I2C_DATA[0]
M1	UPX_RDYN
M2	VDD2
M3	uPx_Data[3]
M4	GND
M5	uPx_Data[6]
M6	VDD2
M7	N/C
M8	GND
M9	VDD2
M10	uPx_Data[16]
M11	GND
M12	VDD2
M13	VDD3
M14	GND
M15	uPx_Data[27]
M16	VDD3
M17	GND
M18	N/C
M19	VDD3
M20	N/C
M21	GND
M22	LED_DATA
M23	VDD3
M24	I2C_DATA[1]
N1	uPx_Add[1]
N2	VDD5
N3	N/C

Ball Location	Signal Name
N4	GND
N5	uPx_Data[5]
N6	VDD5
N7	uPx_Data[11]
N8	GND
N9	VDD5
N10	uPx_Data[15]
N11	GND
N12	VDD5
N13	VDD4
N14	GND
N15	uPx_Data[26]
N16	VDD4
N17	GND
N18	N/C
N19	VDD4
N20	TxPause_Add[0]
N21	GND
N22	MOD_DEF_INT
N23	VDD4
N24	I2C_DATA[2]
P1	uPx_Addr[2]
P2	N/C
P3	uPx_Addr[0]
P4	N/C
P5	uPx_Data[8]
P6	N/C
P7	N/C
P8	N/C
P9	VDD
P10	GND
P11	VDD
P12	GND
P13	GND
P14	VDD
P15	GND
P16	VDD
P17	N/C

Ball Location	Signal Name
P18	N/C
P19	RX_LOS_INT
P20	TxPause_Add[1]
P21	TxPause_Add[2]
P22	RXP[0]
P23	TX_FAULT_INT
P24	I2C_DATA[3]
R1	uPx_Addr[3]
R2	GND
R3	UPX_CSN
R4	VDD
R5	N/C
R6	GND
R7	GND
R8	VDD
R9	GND
R10	N/C
R11	GND
R12	N/C
R13	N/C
R14	GND
R15	N/C
R16	GND
R17	VDD
R18	RXAV25
R19	GND
R20	N/C
R21	VDD
R22	RXN[0]
R23	GND
R24	RXN[2]
T1	uPx_Addr[4]
T2	UPX_BADDR[0]
T3	uPx_Addr[10]
T4	UPX_WRN
T5	UPX_WIDTH[1]
T6	N/C
T7	N/C

Ball Location	Signal Name
T8	N/C
T9	N/C
T10	GND
T11	VDD
T12	VDD5
T13	VDD4
T14	VDD
T15	GND
T16	RXD_3[4]
T17	RXD_3[5]
T18	RXD_3[6]
T19	RXD_3[7]
T20	TXPAUSE_FR
T21	N/C
T22	N/C
T23	RXAVTT
T24	RXP[2]
U1	uPx_Addr[5]
U2	VDD5
U3	uPx_Addr[9]
U4	GND
U5	N/C
U6	VDD5
U7	N/C
U8	GND
U9	N/C
U10	VDD
U11	N/C
U12	GND
U13	GND
U14	TXAV25
U15	VDD
U16	UPX_WIDTH[0]
U17	GND
U18	N/C
U19	VDD4
U20	RXERR[3]
U21	GND

Ball Location	Signal Name
U22	RXN[1]
U23	VDD4
U24	RXP[3]
V1	uPx_Addr[6]
V2	uPx_Addr[7]
V3	uPx_Addr[8]
V4	RXC[0]
V5	RXDV[0]
V6	UPX_RDN
V7	RXD_0[1]
V8	RXD_0[0]
V9	N/C
V10	N/C
V11	N/C
V12	TXEN[3]
V13	N/C
V14	TXD_3[0]
V15	TXD_3[1]
V16	TXD_3[2]
V17	TXD_3[3]
V18	RXDV[3]
V19	RXD_2[6]
V20	RXD_2[5]
V21	MDIO
V22	RXP[1]
V23	RXC[3]
V24	RXN[3]
W1	TXERR[0]
W2	GND
W3	UPX_BADDR[1]
W4	VDD
W5	RXERR[0]
W6	GND
W7	RXD_0[2]
W8	VDD5
W9	RXD_1[3]
W10	GND
W11	RXD_1[2]

Ball Location	Signal Name
W12	VDD5
W13	VDD4
W14	TXD_3[7]
W15	GND
W16	TXP[2]
W17	VDD4
W18	RXD_3[3]
W19	GND
W20	RXD_2[7]
W21	VDD
W22	RXD_2[4]
W23	GND
W24	MDC
Y1	TXD_0[0]
Y2	TXD_0[1]
Y3	TXD_0[2]
Y4	TXD_0[7]
Y5	RXD_0[5]
Y6	RXD_0[4]
Y7	RXD_0[3]
Y8	TXEN[1]
Y9	RXD_1[0]
Y10	RXD_1[7]
Y11	RXD_1[1]
Y12	RXERR[1]
Y13	TXP[0]
Y14	TXN[0]
Y15	TXD_3[5]
Y16	TXN[2]
Y17	RXD_3[0]
Y18	RXD_3[1]
Y19	RXD_3[2]
Y20	RXD_2[0]
Y21	RXD_2[1]
Y22	RXD_2[2]
Y23	RXD_2[3]
Y24	RXDV[2]
AA1	TXC[0]

Ball Location	Signal Name
AA2	VDD5
AA3	TXD_0[3]
AA4	GND
AA5	CRS[0]
AA6	VDD
AA7	TXD_1[4]
AA8	GND
AA9	CRS[1]
AA10	VDD
AA11	RXD_1[6]
AA12	GND
AA13	GND
AA14	TXD_3[4]
AA15	VDD
AA16	TXD_3[6]
AA17	GND
AA18	TXD_2[7]
AA19	VDD
AA20	TXD_2[6]
AA21	GND
AA22	RXERR[2]
AA23	VDD4
AA24	RXC[2]
AB1	N/C
AB2	TXEN[0]
AB3	TXD_0[4]
AB4	TXD_0[6]
AB5	RXD_0[6]
AB6	COL[0]
AB7	TXD_1[1]
AB8	TXD_1[5]
AB09	TXD_1[2]
AB10	COL[1]
AB11	RXDV[1]
AB12	GND
AB13	TXERR[3]
AB14	TXC[3]
AB15	CRS[2]

Ball Location	Signal Name
AB16	TXAVTT
AB17	COL[3]
AB18	N/C
AB19	TXD_2[5]
AB20	TXD_2[0]
AB21	TXD_2[1]
AB22	TXD_2[2]
AB23	TXD_2[3]
AB24	N/C
AC1	N/C
AC2	N/C
AC3	TXD_0[5]
AC4	VDD5
AC5	RXD_0[7]
AC6	GND
AC7	TXD_1[0]
AC8	VDD5
AC9	TXD_1[7]
AC10	GND
AC11	RXD_1[5]
AC12	VDD5
AC13	VDD4
AC14	GND
AC15	GND
AC16	CRS[3]
AC17	VDD4
AC18	TXP[3]
AC19	GND
AC20	TXC[2]
AC21	VDD4
AC22	TXEN[2]
AC23	N/C
AC24	N/C
AD1	N/C
AD2	N/C
AD3	N/C
AD4	N/C
AD5	N/C

Ball Location	Signal Name
AD6	TXERR[1]
AD7	TXC[1]
AD8	TXD_1[6]
AD9	TXD_1[3]
AD10	RXD_1[4]
AD11	RXC[1]
AD12	SYS_RSTN
AD13	TXP[1]
AD14	TXN[1]
AD15	COL[2]
AD16	TXD_2[4]
AD17	TXERR[2]
AD18	TXN[3]
AD19	CLK125
AD20	PLL3_VDDA
AD21	PLL3_GNDA
AD22	N/C
AD23	N/C
AD24	N/C

5.0 Functional Descriptions

5.1 Media Access Controller (MAC)

The main functional block used in the IXF1104 consists of a 10/100/1000 Mbps Ethernet MAC, which supports the following features:

- 1000 Mbps full-duplex operation in fiber MAC (SerDes with GBIC support)
- 10/100/1000 Mbps full-duplex operation in copper MAC GMII/RGMII
- 10/100 Mbps half-duplex operation in copper MAC RGMII
- Automatic padding of transmitted packets that are less than the minimum frame size
- Broadcast, multicast, and unicast address filtering
- Loopback modes for testing and diagnostics
- Detection of runt and overly large packets
- RMON statistics for dropped packets, packets with errors, etc.
- Cyclic redundancy check (CRC) generation, calculation, and error detection
- Software-programmable option to drop packets with errors
- Compliance with IEEE Spec 802.3x MAC Command Frames
- Receive and execute PAUSE Command Frames
- Pre-padded Rx frames with two bytes to align the Ethernet payload on SPI3 and in network processor memories
- Capable of stripping CRC from Rx frames to keep prepadded minimum packets within a 64-byte burst
- Support for non-standard packet sizes up to 10 kbytes including lossless flow control

Note: The IXF1104 does not support 10/100 Mbps operation when configured in GMII mode

The MAC is fully integrated, designed for use with Ethernet 802.3 frame types, and compliant to all of the IEEE 802.3 MAC requirements.

The MAC adds preamble and Start-of-Frame Delimiter (SFD) to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. CRC is optionally appended to transmit packets. CRC is removed from receive packets after validation, and is not forwarded to SPI3. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped. A bad packet is signaled on SPI3 RERR if it is not dropped.

The MAC operates only in full-duplex mode at 1000 Mbps rates on both SerDes and GMII interface connections. The MAC is capable of operation at 1000 Mbps, full-duplex in RGMII mode, and at full-duplex and half-duplex operation for 10/100 Mbps links.

5.1.1 Features for Fiber and Copper MACs

Section 5.1.1.1 through Section 5.1.1.5 cover MAC functions that are independent of the line-side interface.

5.1.1.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI3 interface and padded up to 64 bytes automatically by the MAC. This feature is enabled by setting bit 7 of the "DiverseConfigWrite Register (Addr: Port_Index + 0x18)".

Note: When the user selects the padding function, the MAC core adds an automatically calculated CRC to the end of the transmitted packet.

5.1.1.2 Automatic CRC Generation

Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any transmit frame. This feature is enabled by setting bit 6 of the "DiverseConfigWrite Register (Addr: Port_Index + 0x18)".

5.1.1.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets through an interaction with the Receive FIFO control.

5.1.1.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the "PacketFilterControl Register (Addr: Port_Index + 0x19)" = 1. Any frame received in this mode that does not match the Station Address (MAC address) is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the "RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)" = 1. Otherwise, all unicast frames are sent to the SPI3 Interface.

5.1.1.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the "PacketFilterControl Register (Addr: Port_Index + 0x19)" = 1. Any frame received in this mode that does not match the Port Multicast Address (reserved multicast address recognized by MAC) is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the "RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)" = 1. Otherwise, all multicast frames are sent to the SPI3 Interface.

5.1.1.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the "PacketFilterControl Register (Addr: Port_Index + 0x19)" = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the "RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)" = 1. Otherwise, all broadcast frames are sent to the SPI3 Interface.

5.1.1.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the "PacketFilterControl Register (Addr: Port_Index + 0x19)" = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the "RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)" = 1. Otherwise, all VLAN frames are sent to the SPI3 Interface.

5.1.1.3.5 Filter Pause Packets

This feature is enabled when bit 4 of the "PacketFilterControl Register (Addr: Port_Index + 0x19)" = 0. Pause frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the "RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)" = 1. Otherwise, all pause frames are sent to the SPI3 Interface.

5.1.1.4 CRC Error Detection

Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI3 interface and may be dropped by the switch or system controller.

Frames transmitted by the MAC are also checked for correct CRC. When an incorrect CRC is detected on a transmitted frame, the Tx Bad CRC RMON statistics counter is incremented for each incorrect frame.

5.1.1.5 Pause Command Frames

The MAC acts on any Pause command frames received from the link partner by checking the entire frame and verifying that it is a valid Pause control frame addressed to either the well-known multicast address or the StationAddress. If the pause frame is valid, the transmit side of the MAC pauses for the required number of Pause Quanta, as specified in IEEE 802.3u, clause 31.

The MAC can be configured to support either symmetrical or asymmetrical pause operation. The default mode is for a symmetrical pause operation.

Note: Pause does not begin until completion of the currently transmitted frame.

5.1.2 Mixed-Mode Operation

The IXF1104 Quad-Port Gigabit Ethernet Media Access Controller gives the user the option of configuring each port for 10/100 Mbps half-duplex copper, 10/100/1000 Mbps full-duplex copper, or 1000 Mbps full-duplex fiber operation simultaneously. This gives the IXF1104 Quad-Port Gigabit Ethernet Media Access Controller the ability to support both copper and fiber operation line-side interfaces operating at the same time within a single device.

The IXF1104 Quad-Port Gigabit Ethernet Media Access Controller provides complete flexibility in line-side connectivity by offering RGMII, integrated SerDes and GMII.

5.1.2.1 Configuration of the IXF1104

The "Intel® IXF1104 Register Map" is logically split into the following two distinct regions:

- Per-Port Registers
- Global Registers.

To achieve a desired configuration for a given port, the relevant per-port registers must be configured correctly by the user. The "Intel® IXF1104 Register Map" also contains registers that affect the operation of all ports, such as the configuration of the SPI3 interface.

See Section 7.0, "Register Set" on page 130 for a complete description of IXF1104 configuration and status registers. Table 45 "Intel® IXF1104 Register Map" on page 132 presents a summary of important configuration registers.

5.1.2.2 Key Configuration Registers

The key registers for selecting the operational mode of a given port are as follows:

Table 8. Operational Mode Configuration Registers

Register Name	Register Address	Description
Desired Duplex Register	0x002 - Port 0 0x082 - Port 1 0x102 - Port 2 0x182 - Port 3	The "DesiredDuplex Register (Addr: Port_Index + 0x02)" defines whether a port is to be configured for full-duplex or half-duplex operation. **Note:** Half-duplex operation is only valid for 10/100 speeds where the RGMII line interface has been selected.
MAC Interface Mode and RGMII Speed Register	0x010 - Port 0 0x090 - Port 1 0x110 - Port 2 0x190 - Port 3	The "MAC Interface Mode and RGMII Speed Register (Addr: Port_Index + 0x10)" determines the MAC operational frequency and mode for a given port. **Note:** This register requires the "Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)" to be set to 0x0 prior to any change in the value of this register. This ensures that a change in the MAC clock frequency is controlled correctly. If the "Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)" is not used correctly, the operation of the MAC may be unpredictable for a short period.
Port Enable Register	0x500 Bit 0 - Port 0 Bit 1 - Port 1 Bit 2 - Port 2 Bit 3 - Port 3	Each bit of the"Port Enable Register (Addr: 0x500)" relates to a port. Set the appropriate bit to 0x1 to enable a port. This should be the last step in the configuration process for a port.
Interface Mode Register	0x501 Bit 0 - Port 0 Bit 1 - Port 1 Bit 2 - Port 2 Bit 3 - Port 3	The "Interface Mode Register (Addr: 0x501)" is used to select whether a port will operate with a copper (RGMII or GMII) line-side interface or use the integrated SerDes fiber line-side interface. For copper operation for a given port, set the relevant bit to 0x1. For fiber operation for a given port, set the relevant bit to 0x0. **Note**: The default mode of operation for the IXF1104 is for all ports to be configured for fiber operation
Clock and Interface Mode Change Register	0x794 Bit 0 - Port 0 Bit 1 - Port 1 Bit 2 - Port 2 Bit 3 - Port 3	The"Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)" indicates to an internal clock generator when to sample the new value of the Interface Clock Mode register (speed) and the Interface Mode register (copper/fiber). When any of these two configuration values are changed for a port, the corresponding bits must be kept in this register under reset by writing 0x0 to the relevant bit.

5.1.3 Fiber MAC

The TX Data path from the MAC is an internal 10-bit interface, as described in the IEEE 802.3z specification. It is connected directly to an internal SerDes block for serialization/deserialization and transmission/reception on the fiber medium to/from the link partner.

The MAC contains all of the PCS (8B/10B encoding and 10B/8B decoding) required to encode and decode the data. The MAC also supports auto-negotiation per the IEEE 802.3z specification via access to the "TXConfigWord Register (Addr: Port_Index + 0x17)" on page 144,"RX Config Word Register Bit Definition (Addr: Port_Index + 0x16)" on page 143, and "DiverseConfigWrite Register (Addr: Port_Index + 0x18)" on page 145.

When configured to use SerDes, the full set of GBIC control and status signals is presented via re-use of GMII pins on a per-port basis (see Section 5.7 on page 80). SerDes mode supports only full-duplex Gigabit operation.

5.1.3.1 Fiber Auto-Negotiation

Hardware- or software-controlled auto-negotiation can be performed by using the "TXConfigWord Register (Addr: Port_Index + 0x17)", "RX Config Word Register Bit Definition (Addr: Port_Index + 0x16)", and "DiverseConfigWrite Register (Addr: Port_Index + 0x18)". When autoneg_enable ("DiverseConfigWrite Register (Addr: Port_Index + 0x18)") is set, the IXF1104 performs hardware-defined auto-negotiation with the "TXConfigWord Register (Addr: Port_Index + 0x17)" used as an "Auto-Negotiation Advertisement Register" and the "RX Config Word Register Bit Definition (Addr: Port_Index + 0x16)" used as an "Auto-Negotiation Link Partner Base Page Ability Register".

Note: While the MAC supports auto-negotiation functions, the IXF1104 does not automatically configure the MAC or other blocks in the device to be consistent with the auto-negotiation results. This configuration is effected by the user and system software.

5.1.3.2 Determining If Link Is Established in Auto-Negotiation Mode

A valid link is established when the (AN_complete) bit is set and the RX_Sync bit reports synchronization has occurred. Both register bits are located in the "RX Config Word Register Bit Definition (Addr: Port_Index + 0x16)".

If the link goes down after auto-negotiation is completed, RX_Sync indicates that a loss of synchronization occurred. The IXF1104 restarts auto-negotiation and attempts to reestablish a link. Once a link has been reestablished, the AN_complete bit is set and the RX_Sync bit shows that synchronization has occurred.

To manually restart auto-negotiation, bit 5 of the Diverse Config Register (AN_enable) must be de-asserted, then re-asserted.

5.1.3.3 Fiber Forced Mode

The fiber operation of the MAC can be forced to operate at 1000 Mbps full-duplex without completion of the auto-negotiation function. In this mode, the MAC Rx path must achieve synchronization with the link partner. Once achieved, the transmit path of the MAC is enabled to allow data transmission. This forced mode is limited to operation with a link partner that operates with a full-duplex link at 1000 Mbps.

5.1.4 Copper MAC

The copper MAC transmits data on the egress path of the RGMII or GMII interface, depending on the port configuration defined by the user. The copper MAC receives data on the ingress path of the RGMII or GMII interface, depending on the port configuration defined by the user. The RGMII interface supports operation at 10/100/1000 Mbps when a full-duplex link is established, and supports 10/100 Mbps when a half-duplex link is established. The GMII interface only supports a 1000 Mbps full-duplex link.

5.1.4.1 Speed

The copper MAC supports 10 Mbps, 100 Mbps, and 1000 Mbps. All required speed adjustments, clocks, etc., are supplied by the MAC. The operating speed of the MAC is programmable via the "MAC Interface Mode and RGMII Speed Register (Addr: Port_Index + 0x10)" (MAC_IF_Mode).

Note: When the IXF1104 is configured to use the GMII interface, the only mode of operation that is supported is 1000 Mbps full-duplex.

If 10/100 Mbps operation is required in either full-duplex or half-duplex, the IXF1104 must be configured to use the RGMII interface.

5.1.4.2 Duplex

The MAC supports full-duplex or half-duplex depending on the line-side interface that is configured by the "MAC Interface Mode and RGMII Speed Register (Addr: Port_Index + 0x10)" (MAC_IF_Mode).

5.1.4.3 Copper Auto-Negotiation

In the copper MAC, auto-negotiation and all other controls of the PHY devices are achieved through the MDIO interface, and are independent of the MAC controller. See Section 5.6, "MDIO Control and Interface" on page 76 for further operation details.

Note: For auto-negotiation in the copper MAC, the IXF1104 does not automatically configure the MAC or other blocks in the device to be consistent with auto-negotiation results. This is done by the user and system software.

5.1.5 Jumbo Packet Support

The IXF1104 supports jumbo frames. The jumbo frame length is dependent on the application and the IXF1104 design is optimized for a 9.6 kbyte jumbo frame length. Larger lengths can be programmed, but limited system performance may lead to data loss during certain flow-control conditions

The value programmed into the"MaxFrameSize Register (Addr: Port_Index + 0x0F)" determines the maximum length frame size the MAC can receive or transmit without activating any error counters, and without truncation.

The"MaxFrameSize Register (Addr: Port_Index + 0x0F)" bits 13:0 set the frame length. The default value programmed into this register is 0x05EE (1518). The value is internally adjusted by +4 if the frame has a VLAN tag. The overall programmable maximum is 0x3FFF or 16383 bytes.

The register should be programmed to 0x2667 for the 9.6 kbyte length jumbo frame, optimized for the IXF1104. The RMON counters are also implemented for jumbo frame support as follows:

5.1.5.1 Rx Statistics

- RxOctetsTotalOK (Addr: Port_Index + 0x20)
- RxPkts1519toMaxOctets (Addr: Port_Index + 0x2B)
- FCSErrors (Addr: Port_Index + 0x2C)
- RxDatatError (Addr: Port_Index = 0x02E)
- AlignErrors (Addr: Port_Index + 0x2F)
- LongErrors (Addr: Port_Index + 0x30)
- JabberErrors (Addr: Port_Index + 0x31)
- VeryLongErrors (Addr: Port_Index + 0x34)

5.1.5.2 TX Statistics

- OctetsTransmittedOK (Addr: Port_Index + 0x40)
- TxPkts1519toMaxOctets (Addr: Port_Index + 0x4B)
- TxExcessiveLengthDrop (Addr: Port_Index + 0x53)
- CRCError (Addr: Port_Index + 0x56)

The IXF1104 checks the CRC for all legal-length jumbo frames (frames between 1519 and the Max Frame Size). On transmission, the MAC can be programmed to append the CRC to the frame or check the CRC and increment the appropriate counter. On reception, the MAC transmits these frames across the SPI3 interface (jumbo frames with a bad CRC cannot be dropped and are sent across the SPI3 interface). If the receive frame has a bad CRC, the appropriate counter is incremented and the RxERR flag is asserted on the SPI3 receive interface.

Jumbo frames also impact flow control. The maximum frame size needs to be taken into account when determining the FIFO watermarks. The current transmission must be completed before a Pause frame is transmitted (needed when the receiver FIFO high watermark is exceeded). If the current transmission is a jumbo frame, the delay may be significant and increase data loss due to insufficient available FIFO space.

5.1.5.3 Loss-less Flow Control

The IXF1104 supports loss-less flow control when the size of a Jumbo packet is restricted to 9.6 kbytes. If this condition is met, the IXF1104 has sufficient memory resources allocated to each MAC port to ensure that, if both the IXF1104 and link partner are required to send Pause packets simultaneously during jumbo packet transfers across a medium of two kilometers of fiber, no packet data should be lost due to FIFO overflows.

5.1.6 Packet Buffer Dimensions

5.1.6.1 TX and RX FIFO Operation

5.1.6.1.1 TX FIFO

The IXF1104 TX FIFOs are implemented with 10 kbytes for each channel. This provides enough space for at least one maximum size (10 kbytes) packet per-port storage and ensures that no under-run conditions occur, assuming that the sending device can supply data at the required data rate.

A transfer to MAC Threshold parameter, which is user-programmable, determines when the FIFO signals to the MAC that it has data to send. This is configured for specific block sizes, and the user must ensure that an under-run does not occur. Also, the threshold can be set above the maximum size of a normal Ethernet packet. This causes the FIFO to send only data to the MAC when this threshold is exceeded or when the End-of-Packet marker is received. This second condition eliminates the possibility of under-run, except when the controlling switch device fails. It can, however, cause idle times on the media.

5.1.6.1.2 RX FIFO

The IXF1104 RX FIFOs are provisioned so that each port has its own 32 kbytes of memory space. This is enough memory to ensure that there is never an over-run on any channel while transferring normal Ethernet frame size data.

The FIFOs automatically generate Pause control frames to halt the link partner when the high watermark is reached and to restart the link partner when the data stored in the FIFO falls below the low-watermark. The RX and TX FIFOs have been sized to support lossless flow control with 10 kbyte packets.

5.1.7 RMON Statistics Support

The IXF1104 supplies RMON statistics through the Microprocessor interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the "Intel® IXF1104 Register Map". Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1104.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Intel switch and router products. This implementation allows the IXF1104 to provide all of the RMON Statistics group as defined by RFC2819. The IXF1104 supports the RMON RFC2819 Group 1 statistics counters. Table 9 notes the differences and additional statistics registers supported by the IXF1104 that are outside the scope of the RMON RFC2819 document.

Table 9. RMON Additional Statistics (Sheet 1 of 2)

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1104-Equivalent Statistics	Type	Definition of RMON Versus IXF1104 Documentation
etherStatsindex	Integer 32	N/A	N/A	N/A
etherStatsDataSource	Object identifier	N/A	N/A	N/A
etherStatsDropEvents	Counter 32	RX/TX Number of Frames Removed	Counter 32	See table note 1
etherStatsOctets	Counter 32	RxOctets TotalOK RxOctets Bad Octets Transmitted OK Octets Transmitted Bad	Counter 32	The IXF1104 has two counters for receive and transmit that use different naming conventions for the total Octets and Octets Bad. These counters need to be combined to meet the RMON definition for this statistic.
etherStatsPkts	Counter32	Rx/Tx UCPks Rx/Tx BCPkts Rx/Tx MCPkts	Counter 32	The IXF1104 has three counters for the etherStatsPkts that need to be combined to give the total packets as defined by the RMON specification.
etherStatsBroadcastPkts	Counter32	Rx/Tx BCPkts	Counter 32	Same as RMON specification
etherStatsMulticastPkts	Counter32	Rx/Tx MCPkts	Counter 32	See table note 2
etherStatsCRCAlignErrors	Counter32	AlignErrors (Rx) FCSErrors (Rx) CRCError (Tx)	Counter 32	The IXF1104 has two counters for the alignment and CRC errors for the Rx side only. The IXF1104 has a CRC Error counter for the Tx side.
etherStatsUndersizedPkts	Counter32	RuntErrors ShortErrors Rx Statistics ONLY	Counter 32	The IXF1104 has two counters, one for Runt errors and the other for ShortErrors.
etherStatsOversizePkts	Counter32	LongErrors (Rx) TxExcessiveLength Drop (Tx)	Counter 32	Same as RMON specification

NOTE: The RMON specification requires that this is “The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The “RX FIFO Number of Frames Removed Register Ports 0 to 3 (Addr: 0x594 – 0x597)" and “TX FIFO Number of Dropped Packets Register Ports 0-3 (Addr: 0x625 – 0x629)"in the IXF1104 support this and increment when either an RX FIFO or TX FIFO has overflowed. If any IXF1104 programmable packet filtering is enabled, the “RX FIFO Number of Frames Removed Register Ports 0 to 3 (Addr: 0x594 – 0x597)" and “TX FIFO Number of Dropped Packets Register Ports 0-3 (Addr: 0x625 – 0x629)" increment with every frame removed in addition to the existing frames counted due to FIFO overflow.

Table 9. RMON Additional Statistics (Sheet 2 of 2)

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1104-Equivalent Statistics	Type	Definition of RMON Versus IXF1104 Documentation
etherStatsFragments	Counter32	RuntErrors	Counter 32	Same as RMON specification
etherStatsJabbers	Counter32	JabberErrors	Counter 32	Same as RMON specification
etherStatsCollisions	Counter32	TxSingleCollision TxMultipleCollision TxLateCollision TxTotalCollision	Counter 32	The TxTotalCollision count value is equivalent to the RMON specification minus the TxLateCollision
etherStatsPkts64Octets	Counter32	Rx/TxPkts64Octets	Counter 32	Same as RMON specification
etherStatsPkts65to127Octets	Counter32	Rx/TxPkts65to127Octets	Counter 32	Same a RMON specification
etherStatsPkts128to255Octets	Counter32	Rx/TxPkts128to255Octets	Counter32	Same a RMON specification
etherStatsPkts256to511Octets	Counter32	Rx/TxPkts256to511Octets	Counter32	Same a RMON specification
etherStatsPkts512to1023Octets	Counter32	Rx/TxPkts512to1023Octets	Counter32	Same a RMON specification
etherStatsPkts1023to1518Octets	Counter32	Rx/ TxPkts1023to1518Octets	Counter32	Same as RMON specification
etherStatOwner	Owner String	N/A	N/A	N/A
etherStatsStatus	Entry Status	N/A/	N/A	N/A

NOTE: The RMON specification requires that this is “The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The “RX FIFO Number of Frames Removed Register Ports 0 to 3 (Addr: 0x594 – 0x597)" and “TX FIFO Number of Dropped Packets Register Ports 0-3 (Addr: 0x625 – 0x629)"in the IXF1104 support this and increment when either an RX FIFO or TX FIFO has overflowed. If any IXF1104 programmable packet filtering is enabled, the “RX FIFO Number of Frames Removed Register Ports 0 to 3 (Addr: 0x594 – 0x597)" and “TX FIFO Number of Dropped Packets Register Ports 0-3 (Addr: 0x625 – 0x629)" increment with every frame removed in addition to the existing frames counted due to FIFO overflow.

5.1.7.1 Conventions

The following conventions are used throughout the RMON Management Information Base (MIB) and its companion documents.

- **Good Packets**: Error-free packets that have a valid frame length. For example, on Ethernet, good packets are error-free packets that are between 64 octets long and 1518 octets long. They follow the form defined in IEEE 802.3, Section 3.2.
- **Bad Packets**: Packets that have proper framing and are recognized as packets, but contain errors within the packet or have an invalid length. For example, on Ethernet, bad packets have a valid preamble and SFD, but have a bad CRC, or are either shorter than 64 octets or longer than 1518 octets.

5.1.7.2 IXF1104 Advantages

The following lists additional IXF1104 registers that support features not documented in RMON:

- MAC (flow) control frames
- VLAN Tagged
- Sequence Errors
- Symbol Errors
- CRC Error

These additional counters allow for differentiation beyond standard RMON probes.

Note: In fiber mode, a packet transfer with an invalid 10-bit symbol does not always update the statistics registers correctly.

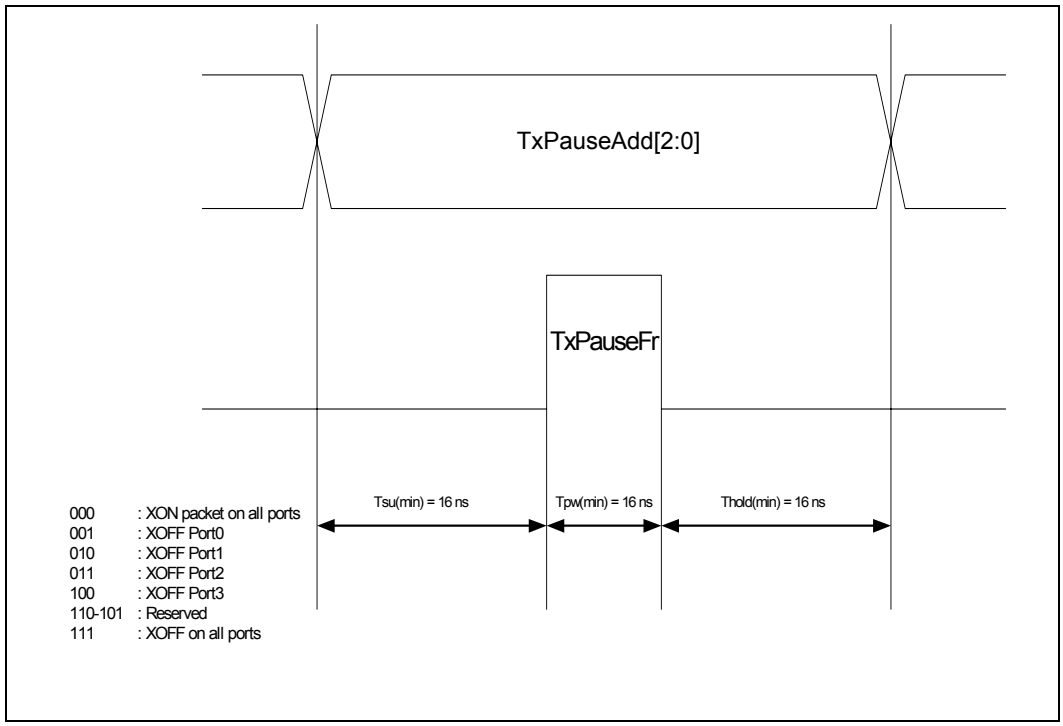
- **Behavior:** The IXF1104 8B10B decoder substitutes a valid code word octet in its place. The packet transfer is aborted and marked as bad. The new internal length of the packet is equal to the byte position where the invalid symbol was. No packet fragments are seen at the next packet transfer.
- **Issue:** If the invalid 10-bit code is inserted in a byte position of 64 or greater, expected RX statistics are reported. However, if the invalid code is inserted in a byte position of less than 64, expected RX statistics are not stored.

5.2 Transmit Pause Control Interface

The Transmit Pause Control interface consists of a 3-bit bus and strobe signal. These signals are asynchronous to the IXF1104 main system clock, which operates at 125 MHz. The user selects the port that requires transmission of the Pause Frame by encoding a value on the 3-bit Pause Control Bus and activating the strobe signal. Internally within the IXF1104, an edge-detect circuit is used to detect a rising-edge event on the strobe signal (TXPauseFr), and a decode of the address currently present on the TXPauseAdd[2:0] bus is performed. Note that there are two additional decodes provided that allow the user to generate either an XOFF frame or XON frame from all ports simultaneously.

The default pause quanta for each port is held by the"FCTxTimerValue Register (Addr: Port_Index + 0x07)"). The default value of this register is 0x05E after reset is applied. Figure 6 illustrates the transmit pause control interface.

Figure 6. Transmit Pause Control Interface



5.3 SPI3 Interface

The SPI3 Interface on the IXF1104 has been implemented to the System Packet Interface Level 3 (SPI3) Physical Layer Interface standard. The function of this interface is to allow the MAC blocks within the IXF1104 to interface to higher-layer network processors or switch fabric.

The transmit interface allows data flows from a network processor or switch fabric device to the IXF1104. The receive interface allows data to flow from the IXF1104 to the network processor or switch fabric device. All signals are active High unless denoted by a trailing "B" as seen in the following example:

SIGNAL = Active High signaling
SIGNAL**B** = Active Low signaling.

This interface receives and transmits data between the PHY and Link Layer with compliant SPI3 interfaces. The SPI3 interface operation is defined in the OIF00.008.3 document (available from the Optical Internet Working Forum [www.oiforum.com]). The OIF specification defines operation for the transfer of data at data rates of up to 3.2 Gbps when operating at a maximum frequency of 104 MHz. The IXF1104 defines operation for the transfer of data at data rates of up to 4.256 Gbps when operating at a maximum frequency of 133 MHz.

The SPI3 interface supports the following two modes of operation:

- MPHY
- SPHY

It can also transfer data in two different ways: byte mode and packet mode.

5.3.1 SPI3 Operation

Since the size of packets is variable, there is no guarantee of the number of bytes available. A selected IXF1104 port-transmit packet is provided on signal STPA and a receive data valid on signal RVAL (in both transmit and receive directions). STPA and RVAL always reflect the status of the selected IXF1104 port to or from the data being transferred. RVAL indicates if valid data is available on the receive data bus and is defined so that data transfers can be aligned with packet boundaries.

The IXF1104 port selection is performed using in-band addressing when the SPI3 interface is used in MPHY mode. In the transmit direction, the network processor device selects an IXF1104 port by sending the address on the TDAT[1:0] bus marked with the TSX signal active and TENB signal inactive. All subsequent TDAT[1:0] bus operations marked with the TSX signal inactive and the TENB active are packet data for the specified port.

In the receive direction, the IXF1104 specifies the selected port by sending the address on the RDAT[1:0] bus marked with the RSX signal active and RVAL signal inactive. All subsequent RDAT[1:0] bus operations marked with RSX inactive and RVAL active are packet data from the specified port.

The data transfer bursts are user-configurable burst lengths of 64, 128, or 256 bytes for data transfers. The IXF1104 also supports interfacing with link layer devices, which transfer data bursts less than the configured maximum burst length in a transfer session where an EOP flag is present in the databurst. (A transfer session is defined as a window for which data is transferred to a selected port prior to switching to another port.) The burst lengths are set in the"SPI3 Transmit and Global Configuration Register (Addr: 0x700)").

Note: The IXF1104 also has a configurable pause interval of zero and two cycles between data transfers in the receive side of the interface. This can be set in the"SPI3 Receive Configuration Register (Addr: 0x701)").

The IXF1104 checks parity on the data bus and is set to odd parity by default. This can be changed to accommodate even parity if desired, and can be set for transmit and receive independently.

5.3.1.1 Bus Widths

SPI3 compatible devices support an 8-bit (SPHY) and/or a 32-bit (MPHY) data bus structure. The bus interface is point-to-point (one output driving only one input load) so a 32-bit data bus would support only one IXF1104. To support multiple network processors with point-to-point connections, an 8-bit data bus structure is defined.

To support variable-length packets, the RMOD[1:0]/TMOD[1:0] signals are defined to specify valid bytes in the 32-bit data bus structure. Each double-word must contain four valid bytes of packet data until the last double-word of the packet transfer, which is marked with the end of packet REOP/TEOP signal. This last double-word of the transfer contains up to four valid bytes specified by the RMOD[1:0]/TMOD[1:0] signals.

5.3.1.2 Clock Rates

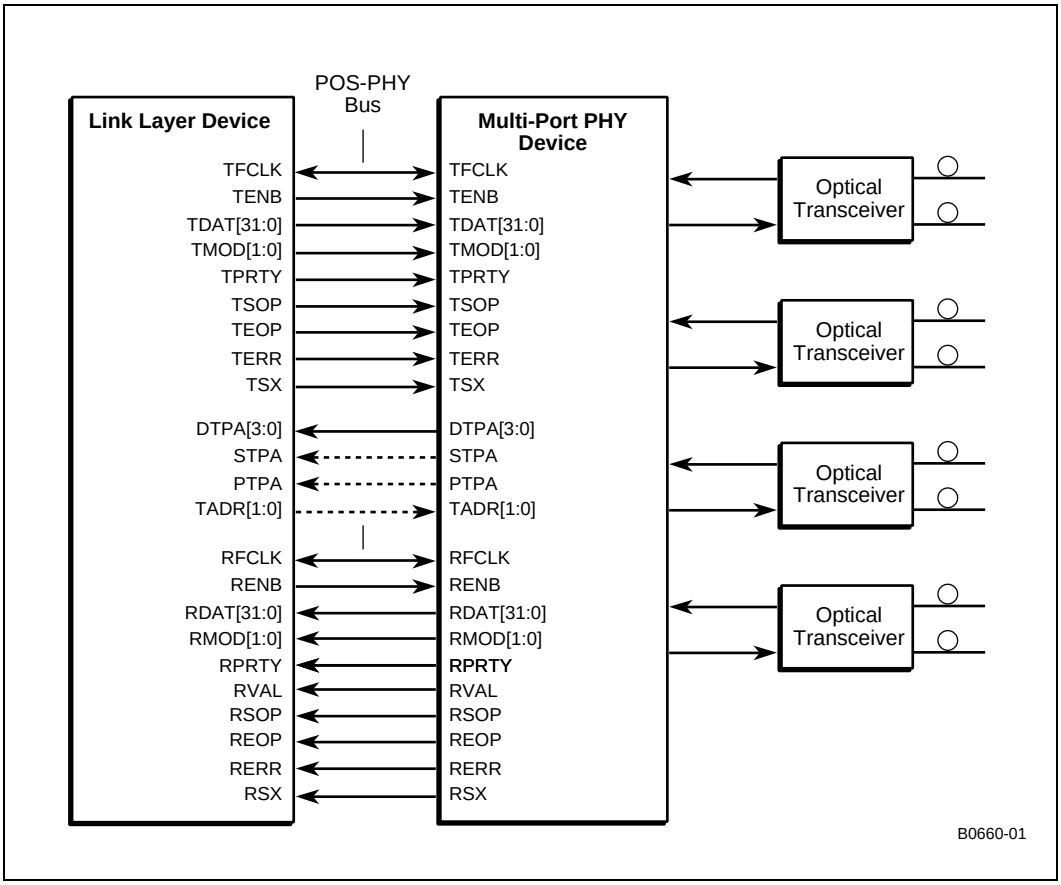
To allow all four ports of the IXF1104 to operate at 1 Gbps, the IXF1104 has been designed to allow this interface to be overclocked. This allows operation for the transfer of data at data rates of up to 4.256 Gbps when operating at an overclocked frequency of 133 MHz.

When operating in SPHY and MPHY mode, the TFCLK and RFCLK can be independent of each other. TFCLK and RFCLK should be common to all the link layer devices. The IXF1104 requires a single clock source for the transmit path, and a single clock source for the receive path of the device.

5.3.1.3 MPHY Mode

When configured in the MPHY mode, the IXF1104 SPI3 interface has a single 32-bit data path (see Figure 7). Since the IXF1104 supports four ports, each port is identified through the use of in-band addressing (TDAT[1:0]). On the transmit side of the interface, there are four addresses that are recognized by the IXF1104 (0, 1, 2 and 3). On the receive side of the interface, the IXF1104 uses a round-robin protocol to service each port dependent upon the enable status of the port and the amount of traffic that needs to be taken from the RX FIFO.

Figure 7. POS-PHY PHY to Link Layer 32-Bit Interface



MPHY mode operates at a maximum clock frequency of 133 MHz (TFCLK and RFCLK). The SPI3 interface in the MPHY mode can operate at a maximum throughput of 4.256 Gbps.

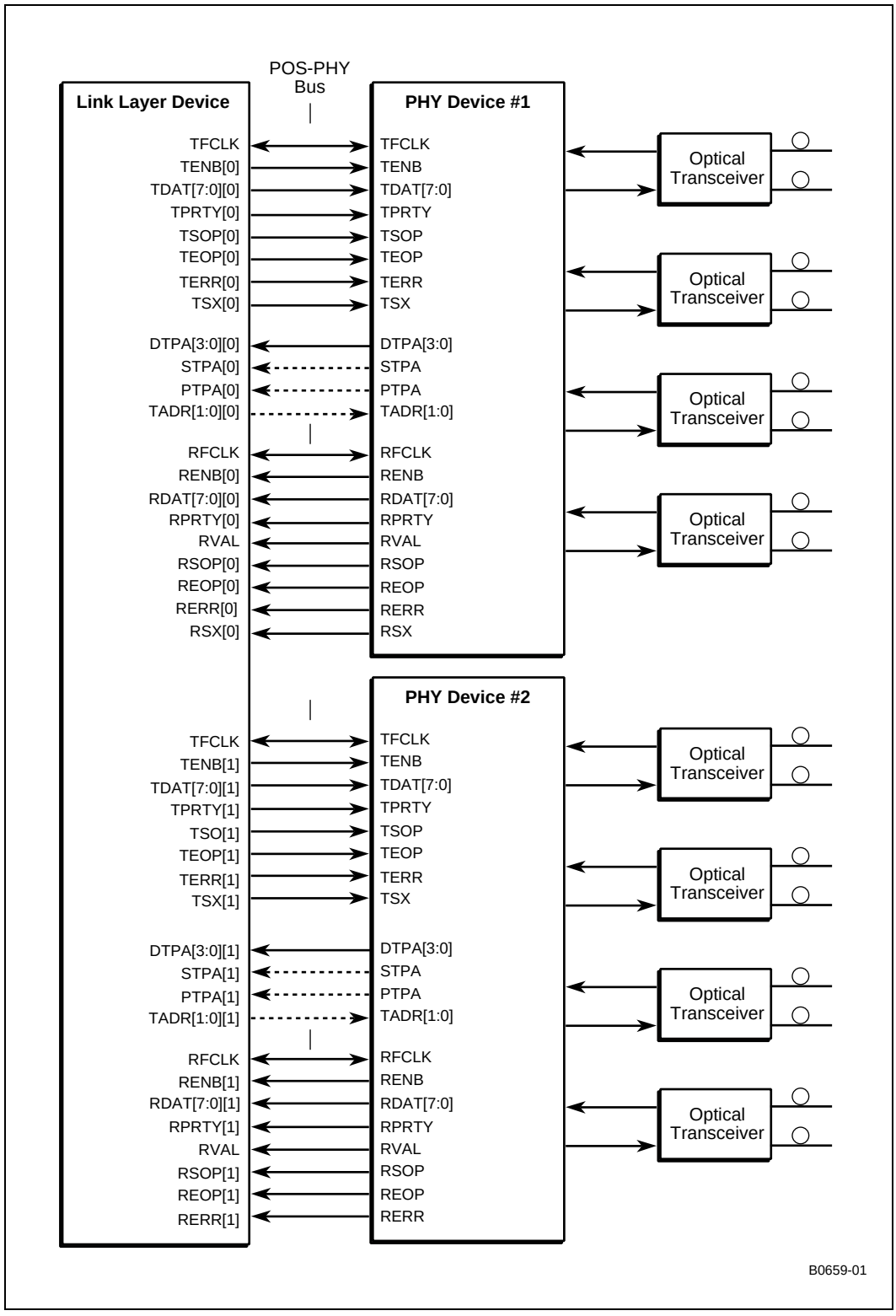
When calculating parity on the data bus, the IXF1104 can be odd or even (the IXF1104 is odd by default). In MPHY mode, only bit 0 in the RX and TX parity sense bits are used. Bits 3:1 are not used.

For configuration of the MPHY mode, refer to the"SPI3 Transmit and Global Configuration Register (Addr: 0x700)".

5.3.1.4 SPHY Mode

When configured in the SPHY mode, the IXF1104 SPI3 interface has four 8-bit data paths that can support four independent 8-bit point-to-point connections for each MAC within the IXF1104 (see Figure 8).

Figure 8. POS-PHY PHY to Link Layer 8-Bit Interface



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SPHY Mode operates at a maximum clock frequency of 125 MHz (TFCLK and RFCLK). The SPI3 interface in the SPHY mode can operate at a maximum throughput of 4.0 Gbps.

When calculating parity on the data bus, the IXF1104 can be odd or even (the IXF1104 defaults to odd). In SPHY mode, the RX and TX parity sense bits have a direct relationship to the port parity.

For configuration of the SPHY mode, refer to theTable 118 “SPI3 Transmit and Global Configuration Register (Addr: 0x700)” on page 183.

5.3.1.5 Packet Flow Control

The SPI3 packet interface supports transmit and receive data transfers at clock rates independent of the line bit rate. As a result, the IXF1104 supports packet rate decoupling using internal FIFOs. These FIFOs are 10 kbytes per port in the transmit direction (egress from the IXF1104 to the line interfaces) and 32 kbytes per port in the receive direction (ingress to the IXF1104 from the line interfaces).

Control signals are provided to the network processor and the IXF1104 to allow either one to exercise flow control. Since the bus interface is point-to-point, the receive interface of the IXF1104 pushes data to the link-layer device. For the transmit interface, the packet available status granularity is byte-based.

In the receive direction, when the IXF1104 has stored an end-of-packet (a complete small packet or the end of a larger packet) or some predefined number of bytes in its receive FIFO, it sends the in-band address followed by FIFO data to the link-layer device (in MPHY mode). The data on the interface bus is marked with the valid signal (RVAL) asserted.

Note: The network processor device can pause the data flow by de-asserting the enable signal (RENB).

In the transmit direction, when the IXF1104 has space for some predefined number of bytes in its transmit FIFO, it informs the network processor device by asserting a transmit packet available (TPA). The network processor device writes the in-band address followed by packet data to the IXF1104 using an enable signal (TENB). The network processor device monitors the TPA signal for a High-to-low transition, which indicates that the transmit FIFO is almost full (the number of bytes left in the FIFO is user-selectable by setting the “RX FIFO High Watermark Register Ports 0 - 3 (Addr: 0x580 – 0x583)", and suspend data transfer to avoid an overflow. The network processor device can pause the data flow by de-asserting the enable signal (TENB).

The addressing of the flow control is determined by pins TADR[1:0] and is used in SPHY and MPHY mode.

5.3.1.6 Packet-Level and Byte-Level Transfers

The IXF1104 can operate with byte-level and packet-level transfer control in the transmit direction.

5.3.1.6.1 Byte Level

In byte-level transfer, FIFO status information is presented on a cycle-by-cycle basis. When using byte-level transfer, direct status indication must be used. The IXF1104 provides the transmit packet available status of the selected port (STPA) in the IXF1104. The IXF1104 provides direct access to the transmit packet available status of all ports (DTPA[3:0]).

5.3.1.6.2 Packet Level

With packet-level transfer, the FIFO status information applies to data segments. The link-layer device is able to do status polling on the transmit direction. The link-layer device can use the transmit port address TADR[1:0] to poll individual ports of the IXF1104, which all respond on a common polled (PTPA) signal.

5.3.2 Pre-Pending Function

The IXF1104 has implemented a pre-pending feature to allow 1518-byte Ethernet packets to be pre-padded with two additional bytes of data so that the packet becomes low-word aligned. The 2-byte pre-pend value is all zeros and is inserted before the destination address of the packet being pre-pended. This value is fixed and cannot be changed.

This function is enabled by writing the appropriate data to the "RX FIFO Padding and CRC Strip Enable Register (Addr: 0x5B3)" for each port.

A standard 1518-byte Ethernet packet would occupy 379 long words (four bytes) with two additional bytes left over (1518/4 = 379.5). To eliminate the memory-management problems for a network processor or switch fabric, the two remaining bytes are dealt with by the addition of two bytes to the start of a packet. This results in a standard 1518-byte Ethernet packet received by the IXF1104 being forwarded to the higher-layer device as a 380-long-word packet. The upper-layer device is responsible for stripping the additional two bytes.

This feature has been added to the IXF1104 to assist in the design of higher-layer memory management. The addition of the two extra bytes is not the default operation of the IXF1104 and must be enabled by the user. The default operation of the IXF1104 SPI3 receive interface forwards data exactly as it is received by the IXF1104 line interface.

5.4 Gigabit Media Independent Interface (GMII)

The IXF1104 supports a subset of the GMII interface standard as defined in IEEE 802.3 2000 Edition for 1 Gbps operation only. This subset is limited to operation at 1000 Mbps full-duplex.

The GMII Interface operates only as a source synchronous interface and does not accept a TxC clock provided by a PHY device when operating at 10/100 Mbps speeds.

Note: The RGMII interface must be used for applications that require 10/100/1000 Mbps operation.

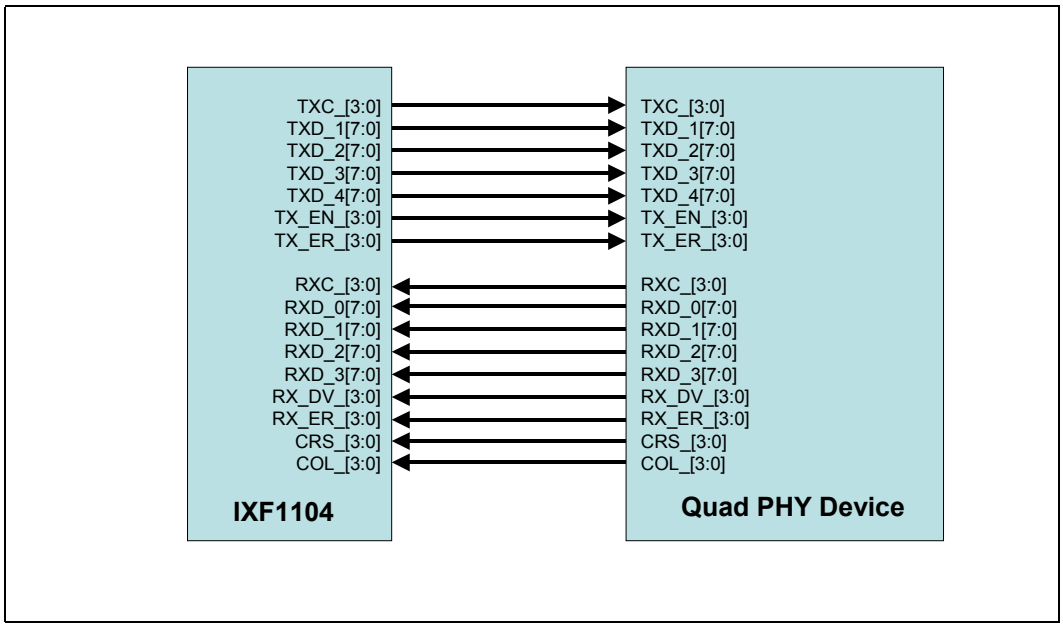
The IXF1104 does NOT support 10/100 Mbps copper PHY devices that are implemented using the MII Interface.

Note: MII operation is not supported by the IXF1104.

The user can select GMII, RGMII, or GBIC/SerDes functionality on a per-port basis. This mode of operation is controlled through a configuration register.

While IEEE 802.3 specifies 3.3 V operation of GMII devices, most PHYs use 2.5 V signaling. The IXF1104 provides a 2.5 V drive and is 3.3 V-tolerant on inputs.

Figure 9. Intel® IXF1104 GMII Interconnect Diagram



5.4.1 GMII Pin Multiplexing

The GMII pins are reassigned using RGMII mode and fiber mode. Table 10 specifies the multiplexing of GMII pins in these modes (see Section 5.1.2, “Mixed-Mode Operation” on page 54 for an explanation of mixed-mode operation).

Table 10. GMII Pin Multiplexing (Sheet 1 of 2)

GMII Pin	RGMII Pin	GBIC Signal
TXC	TXC	N/C
TXD_n[3:0]	TXD_n[3:0]	N/C
TXD_n[4]	N/C	TX_DISABLE
TXD_n[7:5]	N/C	N/C
TX_EN	TX_CTL	N/C
TX_ER	N/C	N/C
RXC	RXC	Pull-down
RXD_n[3:0]	RXD_n[3:0]	Pull-down
RXD_n[4]	N/C	MOD_DEF
RXD_n[5]	N/C	TX_FAULT
RXD_n[6]	N/C	RX_LOS
RXD_n[7]	N/C	Pull-down
RX_DV	RX_CTL	Pull-down

Table 10. GMII Pin Multiplexing (Sheet 2 of 2)

GMII Pin	RGMII Pin	GBIC Signal
RX_ER	N/C	Pull down
CRS	N/C	Pull down
COL	N/C	Pull down

5.4.2 GMII Interface Signal Definition

Table 11 provides the GMII interface signal definitions. For information on 1000BASE-T GMII transmit and receive timing diagrams and tables, please refer to Table 35 “GMII 1000BASE-T Transmit Signal Parameters” on page 117, Figure 35 “1000BASE-T Transmit Interface Timing” on page 117, Figure 36 “1000BASE-T Receive Interface Timing” on page 118, and Table 36 “GMII 1000BASE-T Receive Signal Parameters” on page 118

Table 11. GMII Interface Signal Definitions (Sheet 1 of 2)

IXF1104 Signal	GMII Standard Signal	Source	Description
TXC_0 TXC_1 TXC_2 TXC_3	GTX_CLK	IXF1104	**Transmit Reference Clock:** 125 MHz for Gigabit operation. MII operation for 10/100 Mbps operation is not supported.
TXD_0[7:0] TXD_1[7:0] TXD_2[7:0] TXD_3[7:0]	TXD[7:0]	IXF1104	**Transmit Data Bus:** Width of this synchronous output bus varies with the speed/mode of operation. In 1000 Mbps mode, all 8 bits are used.
TXEN0 TXEN1 TXEN2 TXEN3	TX_EN	IXF1104	**Transmit Enable:** Synchronous input that indicates Valid data is being driven on the TXD[7:0] data bus.
TXER0 TXER1 TXER2 TXER3	TX_ER	IXF1104	**Transmit Error:** Synchronous input to PHY causes the transmission of error symbols in 1000 Mbps links.
RXC_0 RXC_1 RXC_2 RXC_3	RX_CLK	PHY	**Receive Clock:** Continuous reference clock is 125 MHz +/– 100 ppm.
RXD_0[7:0] RXD_1[7:0] RXD_2[7:0] RXD_3[7:0]	RXD<3:0>	PHY	**Receive Data Bus:** Width of the bus varies with the speed and mode of operation. In 1000 Mbps mode, all 8 bits are driven by the PHY device. **Note:** MII operation at 10/100 Mbps is not supported.
RX_DV0 RX_DV1 RX_DV2 RX_DV3	RX_DV	PHY	**Receive Data Valid:** This signal is asserted when valid data is present on the corresponding RXD bus.

Table 11. GMII Interface Signal Definitions (Sheet 2 of 2)

IXF1104 Signal	GMII Standard Signal	Source	Description
RX_ER_0 RX_ER_1 RX_ER_2 RX_ER_3	RX_ER	PHY	**Receive Error:** In 1000 Mbps mode, asserted when error symbols or carrier extension symbols are received. Always synchronous to RX_CLK.
CRS_0 CRS_1 CRS_2 CRS_3	CRS	PHY	**Carrier Sense:** Asserted when valid activity is detected at the line-side interface.
COL_0 COL_1 COL_2 COL_3	COL	PHY	**Collision:** Asserted when a collision is detected and remains asserted for the duration of the collision event. In full-duplex mode, the PHY should force this signal Low.

5.4.3 Electrical Requirements

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output high voltage	I_{OH} = –1.0 mA; V_{CC} = Min	2.0	VDD +10%	V
V_{OL}	Output low voltage	I_{OL} = 1.0 mA; V_{CC} = Min	GND –10%	0.40	V
V_{IH}	Input high voltage	V_{IH} > V_{IH_Min}; V_{CC} = Min	1.70	–	V
V_{IL}	Input low voltage	V_{IH} > V_{IL_Max}; V_{CC} = Min	–	.90	V
I_{IH}	Input high current	V_{CC} = Max; V_{IN} = 2.5V	–	40	µA
I_{IL}	Input low current	V_{CC} = Max; V_{IN} = 0.4V	–600	–	µA

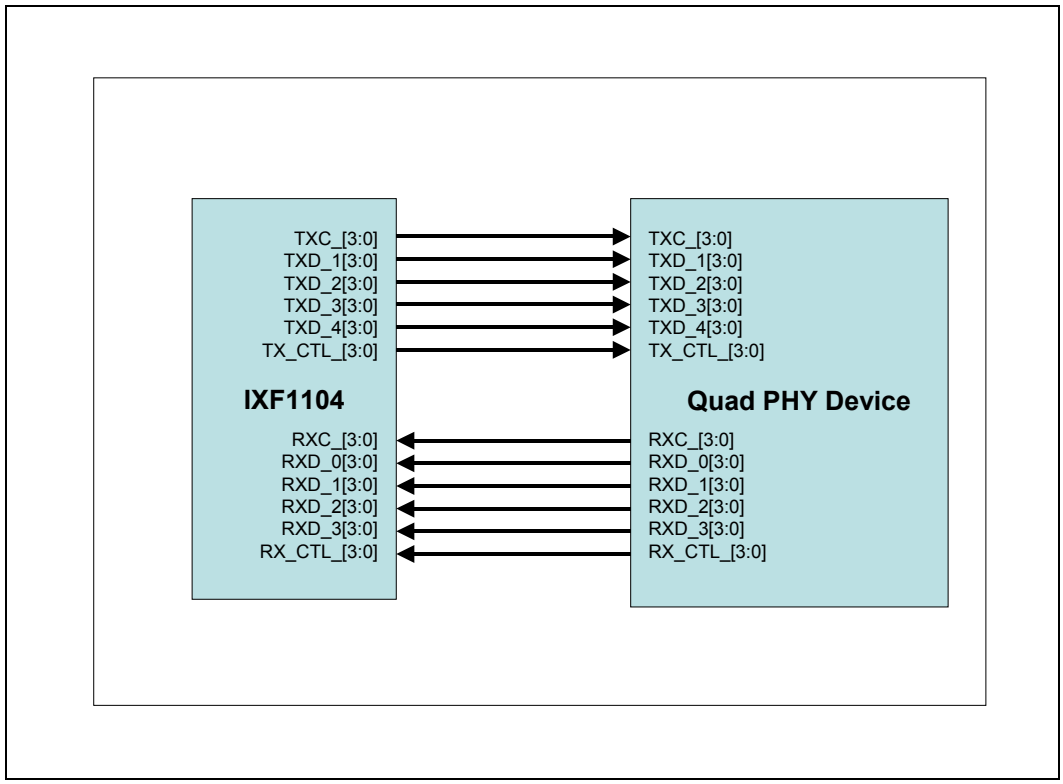
5.5 Reduced Gigabit Media Independent Interface (RGMII)

The IXF1104 supports the RGMII interface standard as defined in the RGMII Version 1.2 specification. The RGMII interface is an alternative to the IEEE 802.3u MII interface.

The RGMII is intended as an alternative to the IEEE 802.3u MII and the IEEE 802.3z GMII. The principle objective of the RGMII is to reduce the number of pins (from a maximum of 28 pins to 12 pins) required to interconnect the MAC and the PHY. This reduction is both cost-effective and technology-independent. To accomplish this objective, the data paths and all associated control signals are reduced, control signals are multiplexed together, and both edges of the clock are used.

- 1000 Mbps operation – clocks operate at 125 MHz
- 100 Mbps operation – clocks operate at 25 MHz
- 10 Mbps operation – clocks operate at 2.5 MHz.

Figure 10. RGMII Interface Diagram



5.5.1 Multiplexing of Data and Control

Multiplexing of data and control information is achieved by utilizing both edges of the reference clocks and sending the lower four bits on the rising edge and the upper four bits on the falling edge. Control signals are multiplexed into a single clock cycle using the same technique. For further information on RGMII multiplexing and timing parameters, see Figure 34 “RGMII Interface Timing” on page 116 and Table 34 “RGMII Interface Timing Parameters” on page 116.

5.5.2 Timing Specifics

The IXF1104 Quad-Port Gigabit Ethernet Media Access Controller RGMII complies with RGMII Rev1.2a requirements. Table 12 provides the timing specifics.

5.5.3 TXERR and RXERR Coding

To reduce interface power, the transmit error condition (TXERR) and the receive error condition (RXERR) are encoded on the RGMII interface to minimize transitions during normal network operation (refer to Table 13 on page 74 for the encoding method). Table 12 provides signal definitions for RGMII.

Table 12. RGMII Signal Definitions

IXF1104 Signal	RGMII Standard Signal	Source	Description
TX_CLK	TXC	MAC	Depending on speed, the transmit reference clock is 125 MHz, 25 MHz, or 2.5 MHz +/– 50ppm.
TXD_[3:0]	TD<3:0>	MAC	Contains register bits 3:0 on the rising edge of TXC and register bits 7:4 on the falling edge of TXC.
TXEN	TX_CTL	MAC	TXEN is on the leading edge of TXC. TXEN xor TXERR is on the falling edge of TXC.
RX_CLK	RXC	PHY	Continuous reference clock is 125 MHz, 25 MHz, or 2.5 MHz +/– 50 ppm.
RXD_[3:0]	RD<3:0>	PHY	Contains register bits 3:0 on the leading edge of RXC and register bits 7:4 on the trailing edge of RXC.
RX_DV	RX_CTL	PHY	RX_DV is on the leading edge of RXC. RX_DV or RXERR is the falling edge of RXC.

The value of RGMII_TX_ER and RGMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way (see Table 13).

Table 13. TXERR and TXERR Coding Description

Condition	Description	
Receiving valid frame, no errors	RX_DV = true Logic High on rising edge of RXC	RXERR = false Logic High on the falling edge of RXC
Receiving valid frame, with errors	RX_DV = true Logic High on rising edge of RXC	RXERR = true Logic Low on the falling edge of RXC
Receiving invalid frame (or no frame)	RX_DV = false Logic Low on rising edge of RXC	RXERR = false Logic Low on the falling edge of RXC
Transmitting valid frame, no errors	TX_EN = true Logic high on rising edge of TXC	TXERR =false Logic High on the falling edge of TXC
Transmitting valid frame with errors	TX_EN = true Logic high on rising edge of TXC	TXERR= true Logic Low on the falling edge of TXC
Transmitting invalid frame (or no frame)	TX_EN = false Logic Low on rising edge of TXC	TX_ERR = false Logic low on the falling edge of TXC
NOTE: Refer to Figure 11 for TX_CTL behavior, and Figure 12 for RX_CTL behavior.		

Figure 11. TX_CTL Behavior Diagram

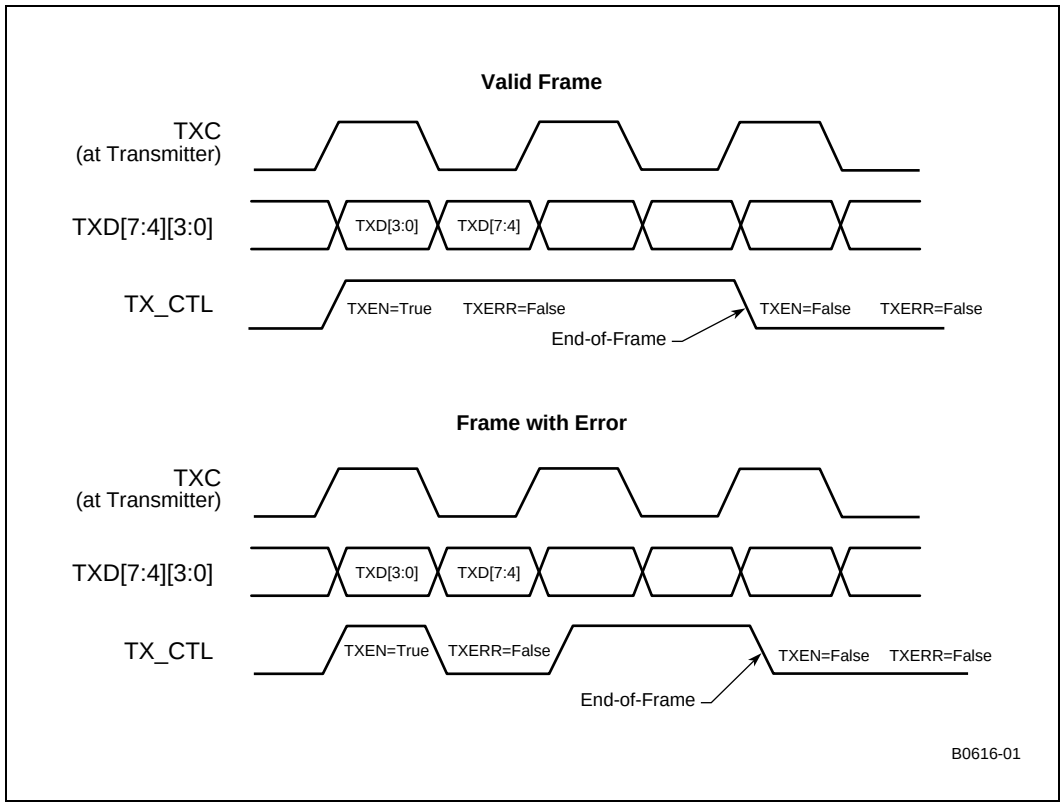
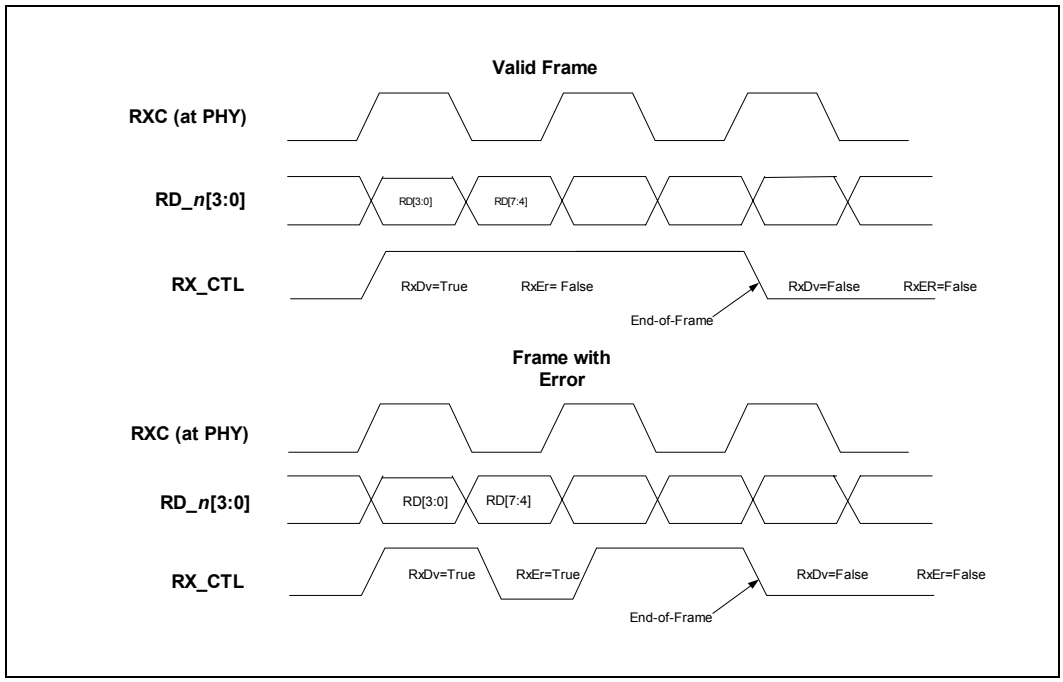


Figure 12. RX_CTL Behavior Diagram



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Revision Number: 006
Revision Date: August 21, 2003

5.5.3.1 In-Band Status

Carrier Sense (CRS) is generated by the PHY when a packet is received from the network interface. CRS is indicated when:

- RXDV = true.
- RXDV = false, RXERR = true, and a value of FF exists on the RXD[7:0] bits simultaneously.
- Carrier Extend, Carrier Extend Error, or False Carrier occurs (please reference the Hewlett-Packard* Version 1.2a RGMII Specification for details.).

Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only. Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

5.5.4 10/100 Mbps Functionality

The RGMII interface implements the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25 MHz for 100 Mbps operation and 2.5 MHz for 10 Mbps. The TXC is generated by the MAC and the RXC is generated by the PHY. During packet reception, the RXC is stretched on either the positive or negative pulse to accommodate transition from the free-running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks is allowed during speed transitions.

This interface operates at 10 Mbps and 100 Mbps speeds in the same manner as 1000 Mbps speed, although the data may be duplicated on the falling edge of the appropriate clock. The MAC holds TX_CTL Low until it is operating at the same speed as the PHY.

Note: The IXF1104 does not support 10/100 Mbps operation when configured in GMII mode

5.6 MDIO Control and Interface

The IXF1104 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows the IXF1104 to monitor and control each of the PHY devices that are connected to the four ports of IXF1104 when those ports are in copper mode.

The MDIO Master Interface block is implemented once in the IXF1104. The MDIO Interface block contains the logic through which the user accesses the registers in PHY devices connected to the MDIO/MDC interface, which is controlled by each port.

The MDIO Master Interface block supports the management frame format, specified by IEEE 802.3, clause 22.2.4.5. This block also supports single MDI access through the Microprocessor interface and an autoscan mode. Autoscan allows the MDIO master to read all 32 registers of the per-port copper PHYs and store the contents in the IXF1104. This provides external-microprocessor-ready access to the PHY register contents through a single microprocessor read without the latency of waiting on the low-speed serial MDIO data bus for each register access.

Scan of a single register with low-frequency operation takes approximately 25.6 µs. Scan of a 32-register block takes approximately 820 µs, or 3.3 µs for all four ports. Autoscan data is not valid until approximately 19.2 µs after enabling scan. These numbers scale by 7/50 for high-frequency operation.

5.6.1 MDI Register Descriptions

For complete information on the MDI registers, refer to the Table 114 “MDI Single Command Register (Addr: 0x680)” on page 181, Table 115 “MDI Single Read and Write Data Register (Addr: 0x681)” on page 181, Table 116 “Autoscan PHY Address Enable Register (Addr: 0x682)” on page 182, and Table 117 “MDI Control Register (Addr: 0x683)” on page 182.

5.6.2 Clear When Done

The MDI Command register bit, in the “MDI Single Command Register (Addr: 0x680)", clears upon command completion and is set by the user to start the requested single MDIO Read or Write operation. This bit is cleared automatically upon operation completion.

5.6.3 MDC Generation

The MDC clock is used for the MDIO/MDC interface. The frequency of the MDC clock is selectable by setting bit 0, MDC Speed, in an IXF1104 configuration register (see Table 117 “MDI Control Register (Addr: 0x683)” on page 182).

5.6.3.1 MDC High-Frequency Operation

The high-frequency MDC is 18 MHz, derived from the 125-MHz system clock by dividing the frequency by 7.

The duty cycle is as follows:

- MDC High duration: 3 x (1/125 MHz) = 3 x 8 ns = 24 ns
- MDC Low duration: 4 x (1/125 MHz) = 4 x 8 ns = 32 ns
- MDC runs continuously after reset

Refer to Figure 38 “MDC High-Speed Operation Timing” on page 120 for the high-frequency MDC timing diagram.

5.6.3.2 MDC Low-Frequency Operation

The low-frequency MDC is 2.5 MHz, which is derived from the 125-MHz system clock by dividing the frequency by 50.

The duty cycle is as follows:

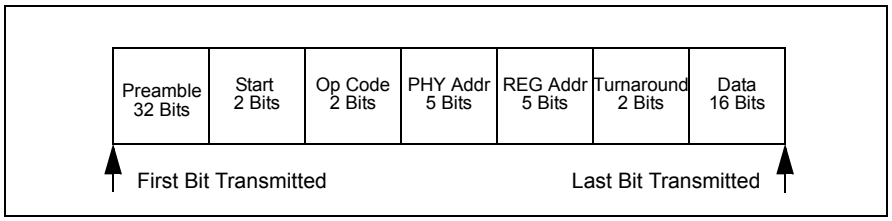
- MDC High duration: 25 x (1/125 MHz) = 25 x 8 ns = 200 ns
- MDC Low duration: 25 x (1/125 MHz) = 25 x 8 ns = 200 ns
- MDC runs continuously after reset

Refer to Figure 39 “MDC Low-Speed Operation Timing” on page 120 for the low frequency MDC timing diagram.

5.6.4 Management Frames

The Management Interface serializes the external register access information into the format specified by IEEE 802.3, Section 22.2.4.5 (see Figure 13).

Figure 13. Management Frame Structure (Single-Frame Format)



5.6.5 Single MDI Command Operation

The Management Data Interface is accessed through the "MDI Single Command Register (Addr: 0x680)" and the "MDI Single Read and Write Data Register (Addr: 0x681)". A single management frame is sent by setting Register 0, bit 20 to logic 1, and is automatically cleared when the frame is completed.

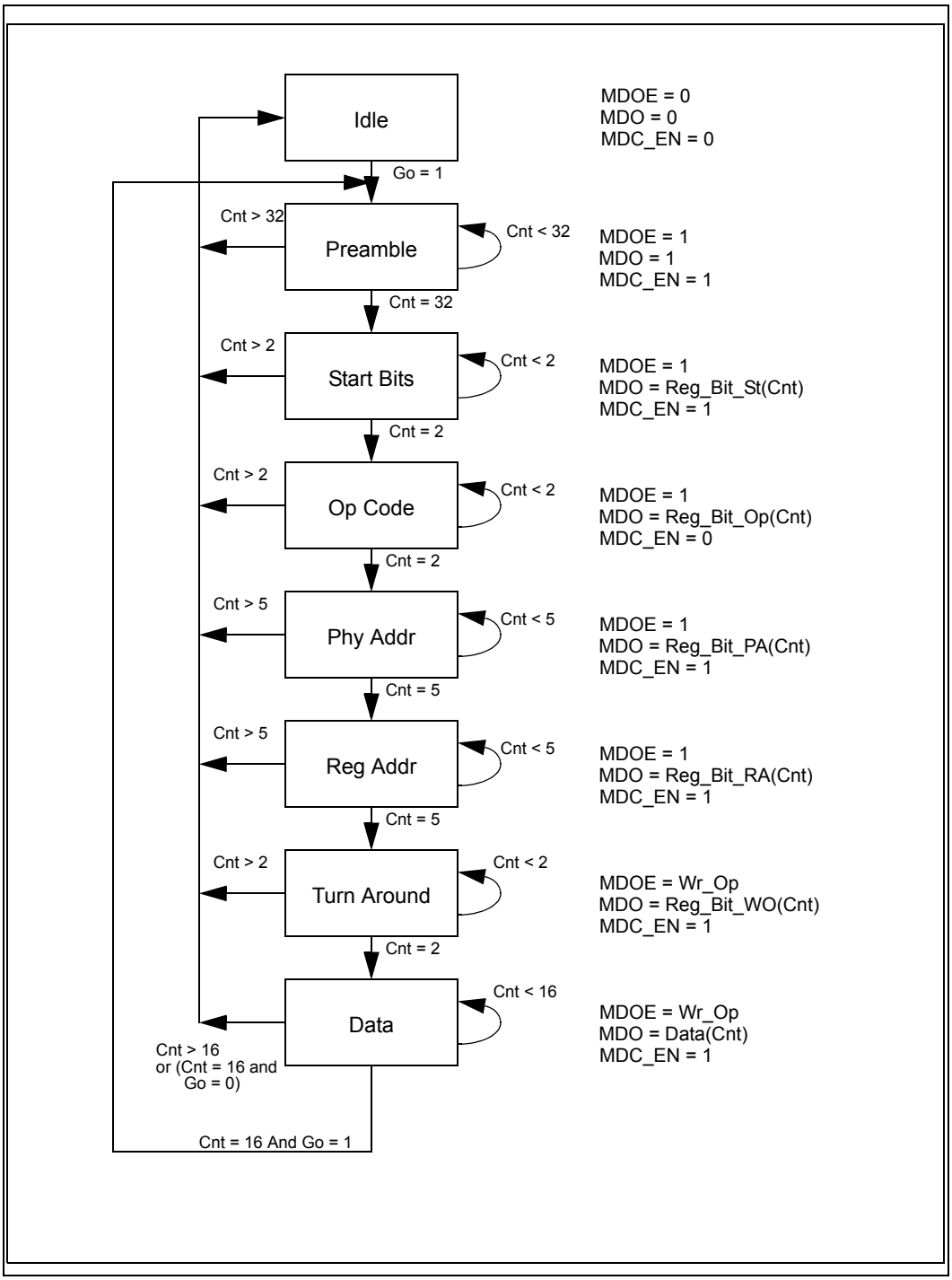
The Write data is first set up in Register 1, bits 15:0 for Write operation. Register 0 is initialized with the appropriate control information (start, op code, etc.) and Register 0, bit 20 is set to logic 1. Register 0, bit 20 is reset to logic 0 when the frame is complete.

The steps are identical for Read operation except that in Register 1, bits 15:0, the data is ignored. The data received from the MDIO is read by the Microprocessor interface from Register 1, bits 31:16.

5.6.6 MDI State Machine

The MDI State Machine sequences the information sent to it by the MDIO control registers and keeps track of the current sequence bit count, enabling or disabling the MDIO driver output (see Figure 14.

Figure 14. MDI State Diagram



5.6.7 Autoscan Operation

The autoscan function allows the 32 registers in each external PHY (up to four) to be stored internally in the IXF1104. Autoscan is enabled by setting bit 1 of the MDI Control register. When enabled, autoscan runs continuously, reading each PHY register. When a PHY register access is instigated through the Microprocessor interface, the current autoscan register Read is completed before the microprocessor register access starts. Upon completion of the microprocessor-induced access, the autoscan functionality restarts from the last autoscan register access.

The"Autoscan PHY Address Enable Register (Addr: 0x682)" determines which PHY addresses are being occupied for each IXF1104 port. The least significant bit (LSB) that is set in the register is Port 0, the next significant bit that is set is assumed to be port 1, and so on. If more than four bits are set, the bits beyond the fourth bit are ignored. If less than four bits are set, the round-robin process returns to the port identified by the LSB being set.

5.7 SerDes Interface

The following sections describe the operations supported by each interface, the configurable options, and register bits that control these options. A full list of the register addresses and full bit definitions are found in Table 45 “Intel® IXF1104 Register Map” on page 132.

The IXF1104 integrates four SerDes interfaces that allow direct connection to optical modules and remove the requirement for external SerDes devices. This increases integration, which reduces the size of the PCB area required to implement this function, reduces total power, reduces silicon and manufacturing costs, and improves reliability.

Each SerDes interface is identical and fully compliant with the relevant IEEE 802.3 specifications, including auto-negotiation. Each port is also compliant with and supports the requirements of the SFF Committee Gigabit Interface Converter (GBIC) standards (SFF-8053, revision 5.2).

5.7.1 Features

The SerDes cores are designed to operate in point-to-point data transmission applications. While the core can be used across various media types, such as PCB or backplanes, it is configured specifically for use in 1000BASE-X Ethernet fiber applications in the IXF1104. The following features are supported:

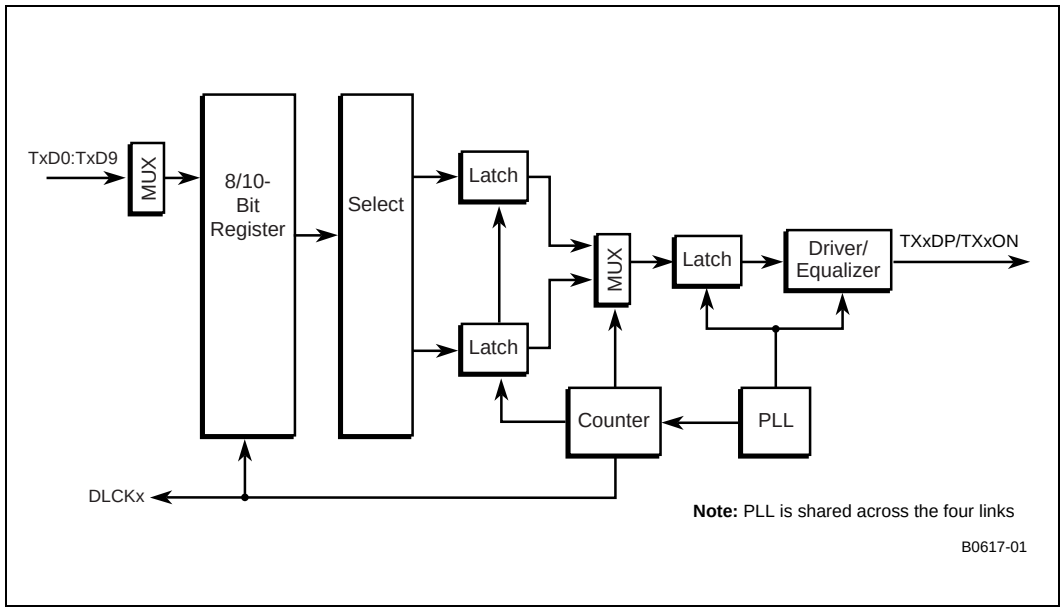
- Line clock frequency of 1.25 GHz +/- 100 ppm
- Low power: Less than 200 mW per channel
- Asynchronous clock-data recovery

5.7.2 Functional Description

5.7.2.1 Transmitter

The transmit core, as seen in Figure 15, shows the PLL input of 625 MHz, multiplied by two, to enable the transmission rate of 1.25 GHz. The 10-bit data is then input at 125 MHz and serialized to the 1.25 GHz differential stream.

Figure 15. Transmitter Concept Diagram



The transmitter structure takes 10-bit data from the data register and synchronously transfers the data two bits at a time to a pair of holding latches. The transferred two-bit data pair is processed by the most significant bit (MSB) first, followed by the next least significant bit (LSB). The counter keeps track of the number of pairs processed and the order of each bit in the pair. When the counter senses that all bit-pairs have been serialized, the interfacing logic is notified to send another word for processing and the 10-bit register is clocked to latch the new data to be processed.

The contents of these latches is transferred in an alternating fashion to a single latch operating at the bit rate. The driver/equalizer receives the bit stream and creates a current-mode differential signal that is frequency equalized for the assumed media channel.

5.7.3 Transmitter Control Interfaces

The transmit core provides multiple control signals to enhance usability in any given application. This section describes the operation of these control signals.

5.7.3.1 AC/DC Coupling

A control input is provided to allow selection of AC or DC coupling on the high-speed link. The AC/DCx control input selects the desired coupling assumption independently for each of the four transmit core drivers.

In AC coupling mode, the driver sources and sinks current to the transmission path and receiver. In DC coupling mode, the driver sinks current from the transmission path. In this mode, the receiver acts as current source to the transmission path. Table 14 provides the AC/DC coupling selection for the transmit core.

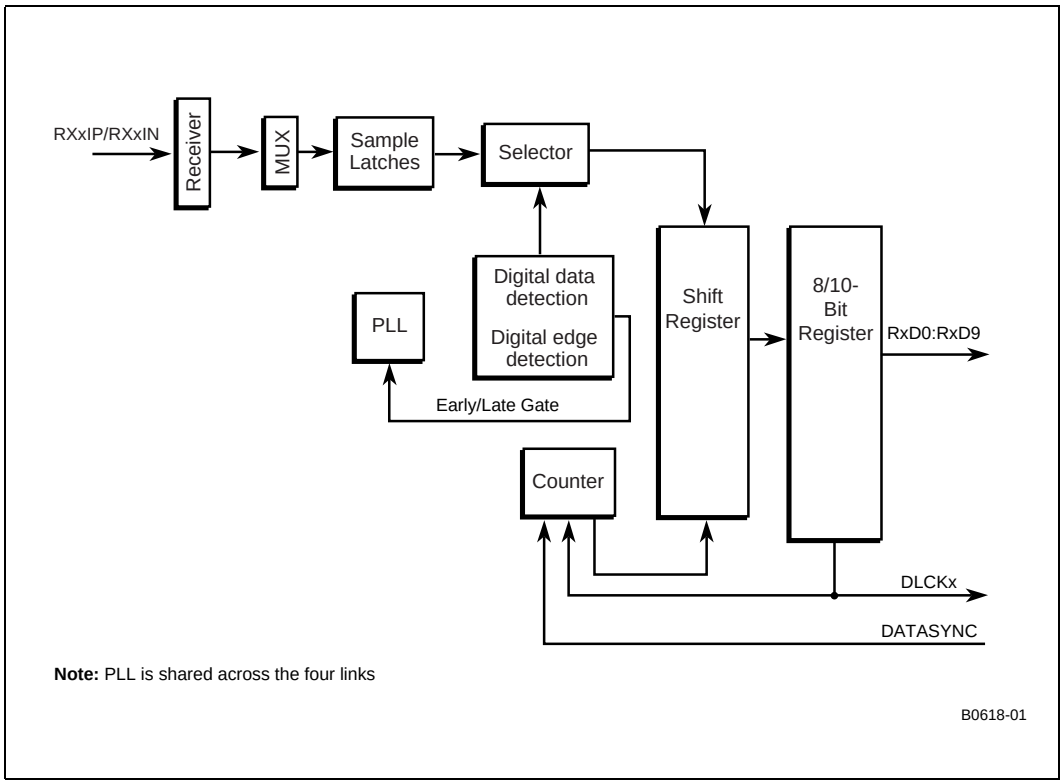
Table 14. AC/DC Coupling Selection for Transmit Core

AC/DCx Input State	Selection
0	AC Coupling
1	DC Coupling

5.7.4 Receiver

The receive core provides the reverse function of the transmit core (see Figure 16).

Figure 16. Receiver Concept Diagram



5.7.4.1 Receiver Operational Overview

5.7.4.1.1 Receiver Operational Overview

The receiver structure performs clock and data recovery (CDR) on the incoming serial data stream. The quality of this operation is a dominant factor for the bit error rate (BER) performance of the system. Feed forward and feedback controls are combined in one receiver architecture for enhanced performance. The data is over-sampled and a digital circuit detects the edge position in the data stream. A feedback loop takes care of low-frequency jitter phenomenon of unlimited amplitude, while a feed forward section suppresses high-frequency jitter having limited amplitude. The static edge position is held at a constant position in the over-sampled data array by a constant adjustment of the sampling phases with the early and late signals.

5.7.4.2 Receiver Control Interfaces

Like the transmitter, the receive core also contains various signals that can configure the receiver core for maximum usability.

5.7.4.3 AC/DC Coupling

A control input is provided to allow selection of AC or DC coupling on the high-speed link. The AC/DCx control input independently selects the desired coupling for each of the receive core drivers. When the AC mode of operation is selected, a common mode reference voltage is applied to the receiver input to provide proper input circuit biasing.

In AC coupling mode, the driver sources and sinks current to the transmission path and receiver. In DC coupling mode, the driver sinks current from the transmission path. in DC mode the receiver acts as a current source to the transmission path.

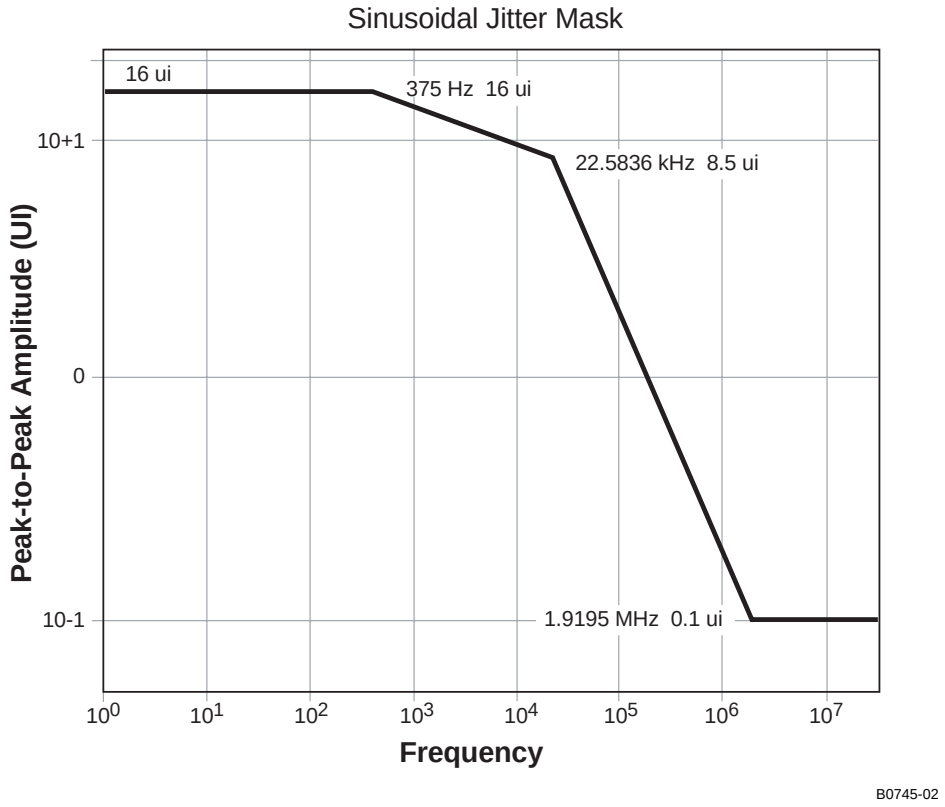
Table 15. AC/DC Coupling Selection for Receive Core

AC/DCx Input State	Selection
0	AC Coupling
1	DC Coupling

5.7.4.4 Receiver Jitter Tolerance

The SerDes receiver architecture is designed to track frequency mismatch, recover phase, and is tolerant of low-frequency data jitter. Figure 17 specifies the SerDes core receiver sinusoidal jitter tracking capabilities.

Figure 17. SerDes Receiver Jitter Tolerance



Note: UI = Unit interval.

5.7.4.5 Transmit Jitter

The SerDes core total transmit jitter, including contributions from the intermediate frequency PLL, is comprised of the following two components:

- A deterministic component attributed to the SerDes core's architectural characteristics
- A random component attributed to random thermal noise effects

Since the thermal noise component is random and statistical in nature, the SerDes core total transmit jitter must be specified as a function of BER.

5.7.4.6 Receive Jitter

The SerDes core total receiver jitter, including contributions from the intermediate frequency PLL, is comprised of the following two components:

- A deterministic component attributed to the SerDes core architectural characteristics
- A random component attributed to random thermal noise effects.

5.7.4.7 System Jitter

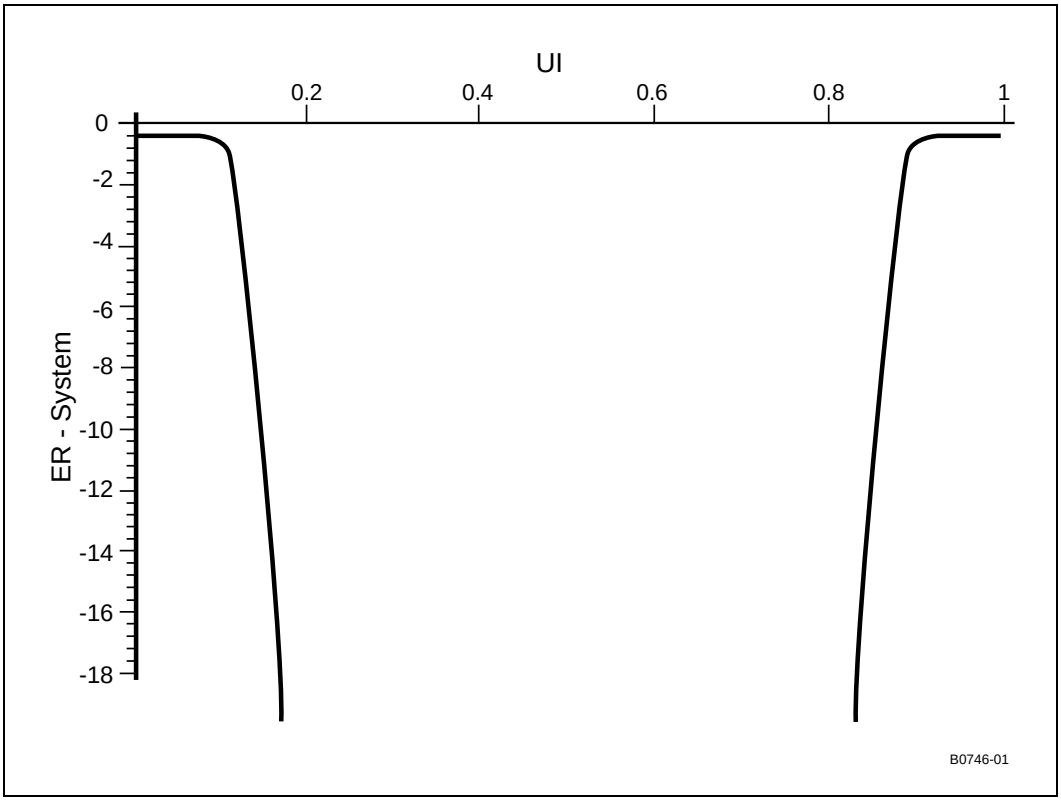
System designers are required to make trade-offs between media jitter attributed to inter-symbol interference (ISI) and system performance. In considering system jitter, Table 16 serves as a useful media budgeting tool.

Table 16. System Jitter

Core Function	Deterministic Jitter DJ ps, p-p	Random Jitter RJ (1-Sigma), ps, rms	Total Jitter (1E-12 ps, p-p (at specified BER)
Transmitter output jitter	68	3.5	118
Receiver internal jitter	90	3.5	140
Receiver jitter tolerance	–	–	660

Figure 18 shows the bathtub curve for the 1.25 Gbps operation of the SerDes core. The distance between the two halves of the curve represents the total jitter that can be apportioned to the transmission media for a given error rate.

Figure 18. SerDes System Jitter



5.8 Gigabit Interface Converter (GBIC) Interface

This section describes the connection of the IXF1104 ports to a GBIC module interface. The minimal connections that are supported for correct operation are detailed. The registers used for write control and read status information are documented.

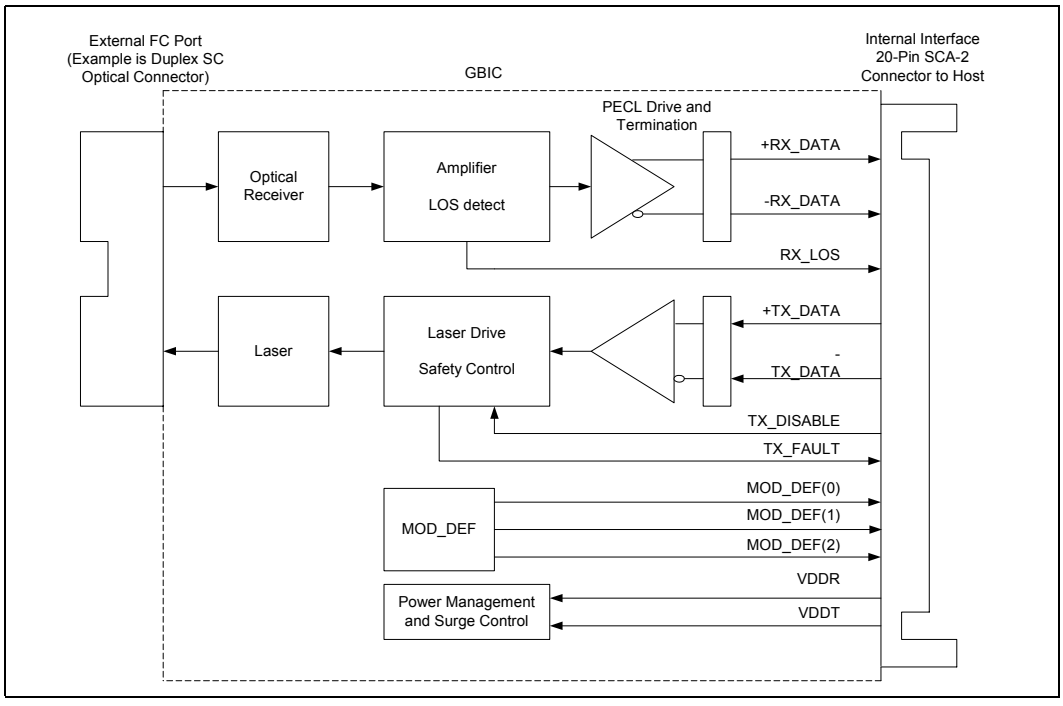
This interface allows the IXF1104 a seamless connection to the GBIC modules that form the system Physical Media connection, eliminating the need for any FPGAs or microprocessors to process this data. All the information required of the GBIC modules is available to the system microprocessor through the IXF1104 microprocessor interface, leading to a more integrated, reliable, and cost-effective system.

GBICs were originally designed for fiber channel applications using the Fiber Channel Arbitrated Loop (FC-AL). The design is practical for point-to-point fiber channel implementations and for other high-performance serial technologies, including 1000 Mbps Ethernet.

There are specific mechanical and electrical requirements for the size, form factor, and connections supported on all GBICs. There are also specific requirements for each GBIC that supports a particular media requirement or interface configuration. These requirements are detailed in the relevant specifications or manufacturers' datasheets.

The IXF1104 supports all the functions required for full compatibility with GBIC modules supporting the SFF Type 4 Module (refer to SFF-8053, revision 5.2). Figure 19 provides typical GBIC module functionality.

Figure 19. Typical GBIC Module Functional Diagram



5.8.1 Intel® IXF1104-Supported GBIC Interface Signals

To describe the GBIC interface operation, three supported signal subgroups are required, allowing a more explicit definition of each function and implementation. The three subgroups are as follows:

- High-Speed Serial Interface
- Low-Speed Status Signaling Interface
- I²C Module Configuration Interface

Table 17 provides descriptions for IXF1104-to-GBIC module connection pins.

Table 17. Intel® IXF1104-to-GBIC Connections

IXF1104 Pin Names	GBIC Module Pin Name	Description	Notes
TxD+_[3:0]	+TX_DAT	Transmit Data, Differential LVDS	Output from the IXF1104
TxD–_[3:0]	–TX_DAT	Transmit Data, Differential LVDS	Output from the IXF1104
RxD+_[3:0]	+RX_DAT	Receive Data, Differential LVDS	Input to the IXF1104
RxD–_[3:0]	–RX_DAT	Receive Data, Differential LVDS	Input to the IXF1104
I²C_CLK	MOD_DEF(1)	I²C_CLK Output from IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (SCL)	Output from the IXF1104
I²C_DATA_[3:0]	MOD_DEF(2)	I²C_DATA I/O (SDA)	Input/Output
MOD_DEF_[3:0]	MOD_DEF(0)	MOD_DEF(0) should be TTL Low level during normal operation.	Input to the IXF1104
TxDISABLE_[3:0]	TX_DISABLE	Transmitter Disable, Logic High, Open collector compatible	Output from the IXF1104
TxFAULT_[3:0]	TX_FAULT	Transmitter Fault, Logic High, Open collector compatible	Input to the IXF1104
Rx_LOS_[3:0]	RX_LOS	Receiver Loss of Signal, Logic High, Open collector compatible	Input to the IXF1104

5.8.2 Functional Descriptions

5.8.2.1 High-Speed Serial Interface

These signals are responsible for transfer of the actual data at 1.25 Gbps. The data is 8B/10B encoded and transmitted differentially at LVDS as seen in Table 28 “DC Specifications” on page 110. This interface may be either AC- or DC-coupled. The default configuration for the IXF1104 is AC-coupled.

The following signals are required to implement the high-speed serial interface:

- TxD+_[3:0]
- TxD–_[3:0]
- RxD+_[3:0]
- RxD–_[3:0]

5.8.2.2 Low-Speed Status Signaling Interface

The following Low-Speed signals indicate the state of the line through the GBIC module:

- MOD_DEF_[3:0]
- Tx_FAULT_[3:0]
- Rx_LOS_[3:0]
- Tx_DISABLE_[3:0]
- MOD_DEF_Int
- Tx_FAULT_Int
- Rx_LOS_Int

5.8.2.2.1 MOD_DEF_[3:0]

These signals are direct inputs to the IXF1104 and are pulled to a logic Low level during normal operation, indicating that a module is present for each channel respectively. If a module is not present, a Logic High is received, which is achieved by a pull-up resistor on the IXF1104 device pad.

The status of each bit (one for each port) is found in bits [3:0] of the "GBIC Status Register Ports 0-3 (Addr: 0x799)" on page 188). Any change in the state of these bits causes a logic Low level on the MOD_DEF_Int output if this operation is enabled.

5.8.2.2.2 Tx_FAULT_[3:0]

These four pins are inputs to the IXF1104. These signals are pulled to a logic Low level by the GBIC module during normal operation. A logic Low level on these signals indicates no fault condition exists. If a fault is present, a logic High is received through the use of an external pull-up resistor on the IXF1104 pad.

The status of each bit (one for each port) can be found in bits [13:10] of the "GBIC Status Register Ports 0-3 (Addr: 0x799)" on page 188. Any change in the state of these bits causes a logic Low level on the Tx_FAULT_Int output if this operation is enabled.

5.8.2.2.3 Rx_LOS_[3:0]

These four pins are inputs to the IXF1104. During normal operation, these signals are pulled to a logic Low level by the GBIC module, which indicates that no loss-of-signal exists. If a loss-of-signal occurs, a logic High is received on these inputs through the use of a pull-up resistor on the IXF1104 pad.

The status of each bit (one for each port) is found in "GBIC Status Register Ports 0-3 (Addr: 0x799)" bits [23:20]. Any change in the state of these bits causes a logic Low level on the Rx_LOS_Int output if this operation is enabled.

5.8.2.2.4 Tx_DISABLE_[3:0]

These four pins are outputs from the IXF1104. During normal operation, these signals are driven to a logic Low level by the IXF1104. This indicates that the GBIC transmitter is enabled. If the GBIC module transmitter is disabled, this signal is switched to a logic High level. On the IXF1104, these outputs are open drain types and pulled up by the 4.7 k to 10 k pull-up resistor at the GBIC module. Each of these signals is controlled through bits [3:0] respectively of the"GBIC Control Register Ports 0-3 (Addr: 0x79A)".

5.8.2.2.5 MOD_DEF_Int

This signal is an open drain type, single output and is active Low. A change in state of any MOD_DEF_[3:0] inputs causes this signal to switch Low and remain in this state until a Read of the "GBIC Status Register Ports 0-3 (Addr: 0x799)". The signal returns to an inactive state.

5.8.2.2.6 Tx_FAULT_Int

This signal is an open-drain type, single output and is active Low. A change in state of any Tx_FAULT_[3:0] inputs causes this signal to switch Low and remain in this state until a Read of the "GBIC Status Register Ports 0-3 (Addr: 0x799)". The signal returns to an inactive state.

5.8.2.2.7 Rx_LOS_Int

RX_LOS_Int is a single output, open-drain type signal and is active low. A change in state of any of the Rx_LOS_[3:0] inputs causes this signal to switch low and remain in this state until a Read of the "GBIC Status Register Ports 0-3 (Addr: 0x799)" has taken place. The signal returns to an inactive state.

Note: The MOD_DEF_Int, TxFAULT_Int, and Rx_LOS_Int are open-drain type outputs. With the three signals on the device, the system can decide which "GBIC Status Register Ports 0-3 (Addr: 0x799)" bits to look at to identify the interrupt condition source port. However, this is achieved at the expense of two device pins.

In systems that cannot support multiple interrupt signals (applications that do not have extra hardware pins), these three outputs can be connected to a single pull-up resistor and used as a single interrupt pin.

5.8.3 I²C Module Configuration Interface

The I²C interface is supported on Type 4 SFF GBIC modules. Details of the operation are found in SFF-8053, Revision 5.2, Annex D, Module Definition "4" GBIC (Serial Identification). This document details the contents of the registers and addresses accessible on a given GBIC module supporting this interface.

SFF-8053 identifies up to 512 8-bit registers that are accessible in each GBIC. The GBIC interface is read-only and supports either sequential or random access to the 8-bit parameters. The maximum clock rate of the interface is 100 kHz. All address-select pins on the internal E²PROM are tied Low to give a device address equal to zero (00h).

Several PHY vendors may offer copper/CAT5-based SFP GBIC compliant modules. To program the internal configuration registers of these modules, the IXF1104 I^2C interface needs to provide the capability to write data to the SFP modules.

The IXF1104 I^2C interface is designed to allow individual writes of byte-wide data to the SFP.

The specific interface in the IXF1104 supports only a subset of the full I²C interface, and only the features required to support the GBIC modules are implemented. This leads to the following support features.

- Single I^2C_CLK pin connected to all GBIC modules, and implemented to save unnecessary pins use.

- Four per-port I²C_DATA pins (I²C Data[3:0]) are required because of the GBIC module requirement that all modules must be addressed as 00h.
- The interface has both read and write functionality.
- Due to the single internal GBIC controller, only one GBIC module may be accessed at any one time. Each access contains a single register Read. Since these register accesses will most likely be done during power-up or discovery of a new module, these restrictions should not affect normal operation.

5.8.3.1 I²C Control and Data Registers

In the IXF1104, the entire I²C interface is controlled through the following two registers:

- Table 127 “I2C Control Register Ports 3-0 (Addr: 0x79B)” on page 189
- Table 128 “I2C Data Register Ports 3-0 (Addr: 0x79F)” on page 189

These registers can be programmed by system software using the Microprocessor interface.

5.8.3.2 I²C Read Operation

To perform a read operation using the I²C interface, use the following sequence:

1. Initialize the Control register by setting the following values:
   a. Enable the I²C Controller by setting bit [25] to 0x1.
   b. Initiate the I²C transfer by setting bit [24] of the control register to 0x1.
   c. Select the port by using bits [17:16].
   d. Select the Read mode of operation by setting bit [15] to 0x1.
   e. Select the Device ID by setting bits [14:11].
   f. Select the register address by setting bits [10:0].

To access the fiber GBIC serial E2PROM, the Device ID field must be set to 0xA and the register address (bits 10:8) must be set to 0x0. Setting the DeviceID field to 0xA, and the Register Address [10:8] to 0x0 permits read-only accesses.

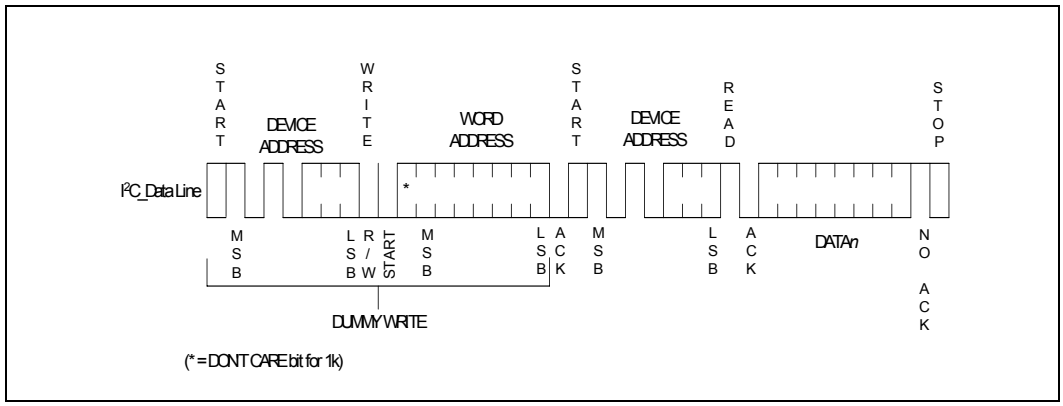
To access the PHY registers, the Device ID field requires to be set to 0xA and the Register Address [10:8] must be set between the values of 0x1 and 0x7.

The user should then poll the Read_Valid field, bit 20. The read data is available when this bit is set to 0x1.

Figure 20 shows an 8-bit read access.

Note: The user software ensures the order of the contiguous accesses required to read the High and Low bytes of 16-bit-wide PHY registers.

Figure 20. I²C Random Read Transaction



Note: Only one GBIC I²C access sequence can be run at any given time. If a second write is carried out to the "I2C Control Register Ports 3-0 (Addr: 0x79B)" and "I2C Data Register Ports 3-0 (Addr: 0x79F)" before a result is returned for the previous write, the data for the first write is lost. An internal state machine completes the GBIC register access for the first write. It attempts to place the data in the DataRead field and checks to see if the WriteCommand bit is 00h. If it is not 00h, it discards the data and signals the I²C access state machine to begin a new cycle using the data from the second write.

5.8.3.3 I²C Write Operation

To perform a write operation using the I²C interface, use the following sequence:

1. Initialize the I²C Control register by setting the following values:
   a. Enable the I²C Controller by setting bit[25] to 0x1.
   b. Initiate the I²C transfer by setting bit[24] of the control register to 0x1.
   c. Select the port by using bits[17:16].
   d. Select the Write mode of operation by setting bit[15] to 0x0.
   e. Select the Device ID by setting bits[14:11]
   f. Select the Register Address by setting bits[10:0]
   g. All other registers should be set to 0x0.

To access the PHY registers, the Device ID field must be set to 0xA and the register address [10:8] must be set between 0x1 and 0x7.

Write requests are not permitted to the embedded fiber GBIC E²PROM. Any attempt to initiate a write to the E²PROM results in no I²C transaction and the WP_ERR bit will be set.

The user should poll the Write_Complete field. The transaction is considered completed when the Write_Complete bit is set to 0x1.

5.8.3.4 I²C Protocol Specifics

This section describes the IXF1104 I²C Protocol behavior, which is controlled by an internal state machine. Specific protocol states are defined below, with an additional description of the hardware pins used on the interface.

The Serial Clock Line (I^2C_CLK) is an output from the IXF1104. The serial data is synchronous with this clock and is driven off the rising edge by the IXF1104 and off the falling edge by the GBIC module. The IXF1104 has only one I^2C_CLK line that drives all of the GBIC modules. I^2C_CLK runs continuously when enabled (I²C Enable = 01h0).

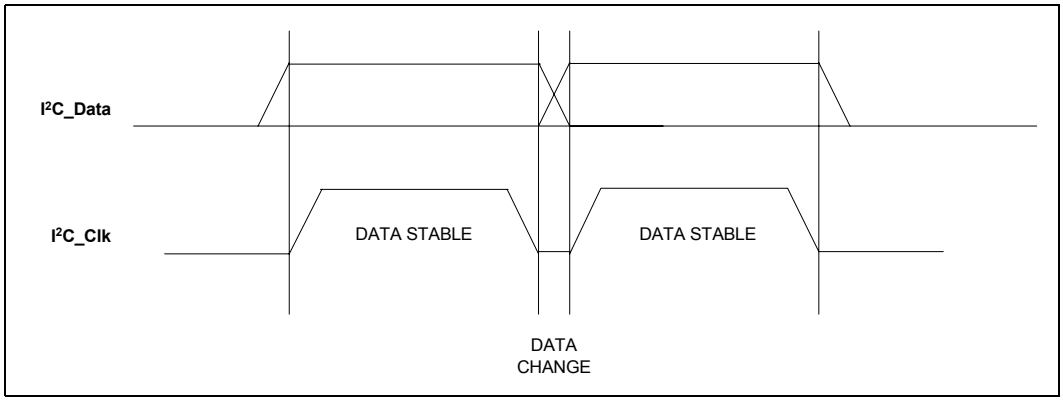
The Serial Data (I^2C_DATA[3:0]) pins (one per port) are bi-directional for serial data transfer. These pins are open drain.

5.8.3.5 Port Protocol Operation

5.8.3.6 Clock and Data Transitions

The I^2C_DATA is normally pulled High with an extra device. Data on the I^2C_DATA pin changes only during the I^2C_CLK Low time periods (see Figure 21). Data changes during I^2C_CLK High periods indicate a start or stop condition.

Figure 21. Data Validity Timing Diagram



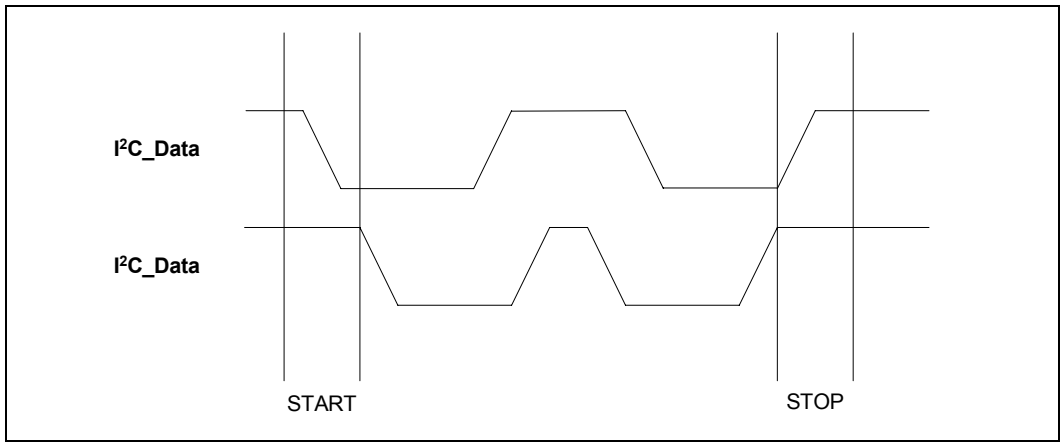
5.8.3.6.1 Start Condition

A High-to-Low transition of I^2C_DATA, with I^2C_CLK High, is a start condition that must precede any other command (see Figure 22).

5.8.3.6.2 Stop Condition

A Low-to-High transition of the I^2C_DATA with I^2C_CLK High is a stop condition. After a Read sequence, the stop command places the E²PROM in the GBIC in a standby power mode (see Figure 22).

Figure 22. Start and Stop Definition Timing Diagram



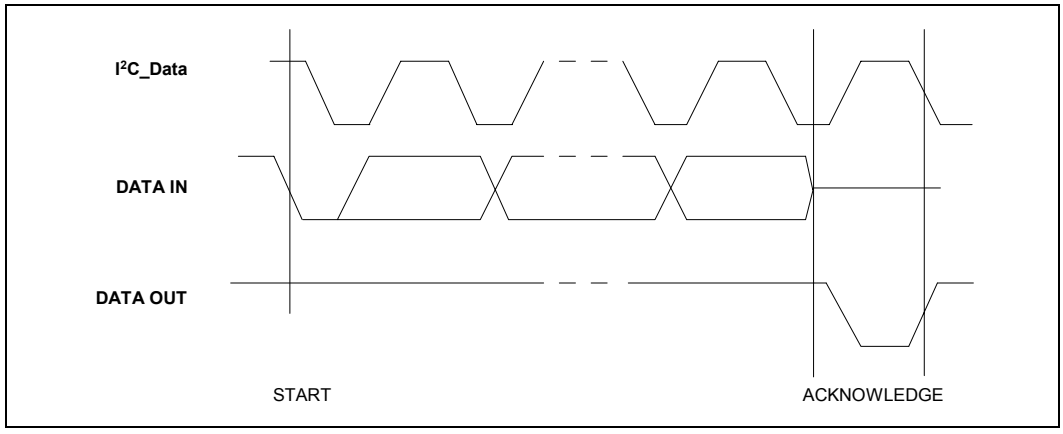
5.8.3.6.3 Acknowledge

All addresses and data words are serially transmitted to and from the GBIC in 8-bit words. The GBIC E²PROM sends a zero to acknowledge that it has received each word, which happens during the ninth clock cycle (see Figure 23).

5.8.3.6.4 Acknowledge

All addresses and data words are serially transmitted to and from the GBIC in 8-bit words. The GBIC E²PROM sends a zero to acknowledge that it has received each word, which happens during the ninth clock cycle (see Figure 23).

Figure 23. Acknowledge Timing Diagram



5.8.3.6.5 Memory Reset

After an interruption in protocol, power loss, or system reset, any 2-wire GBIC can be reset by following three steps:

1. Clock up to 9 cycles

2. Wait for I^2C_DATA High in each cycle while I^2C_CLK is High
3. Initiate a start condition.

5.8.3.6.6 Device Addressing

All E²PROMs in GBIC devices require an 8-bit device address word following a start condition to enable the chip to read or write. The device address word consists of a mandatory one, zero sequence for the four most-significant bits. This is common to all devices. The next three bits are the A2, A1, and A0 device address bits that are tied to zero in a GBIC module. The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is High and a Write operation is initiated if this bit is Low.

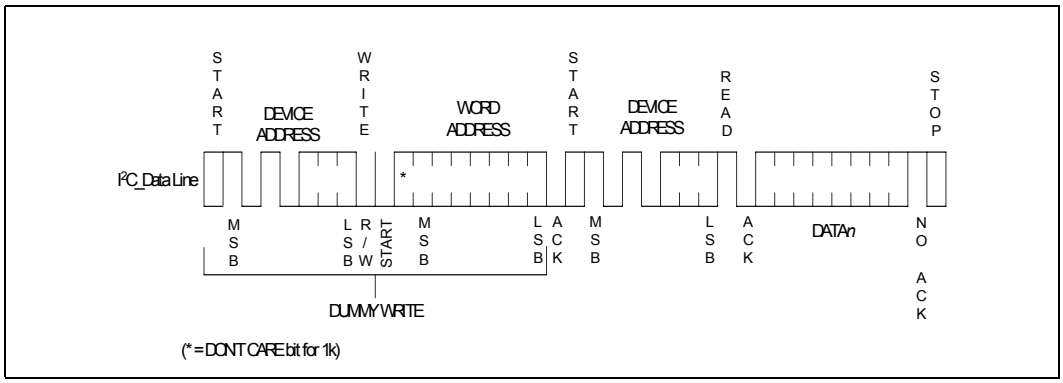
Upon comparison of the device address, the GBIC module outputs a zero. If a comparison is not made, the GBIC E²PROM returns to a standby state.

5.8.3.6.7 Random Read Operation

A random Read requires a “dummy” Byte/Write sequence to load the data word address. The “dummy” write is achieved by first sending the device address word with the Read/Write bit cleared to Low, which signals a Write operation. The GBIC acknowledges receipt of the device address word. The IXF1104 sends the data word address, which is again acknowledged by the GBIC. The IXF1104 generates another start condition. This completes the “dummy” write and sets the GBIC E²PROM pointers to the desired location.

The IXF1104 initiates a current address read by sending a device address with the Read/Write bit set High. The GBIC acknowledges the device address and serially clocks out the data word. The IXF1104 does not respond with a zero but generates a stop condition (see Figure 24).

Figure 24. Random Read



5.9 LED Interface

The IXF1104 uses a Serial interface, consisting of three signals, to provide LED data to some form of external driver. This provides the data for 12 separate direct drive LEDs and allows three LEDs per MAC port.

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in the following sections.

5.9.1 Modes of Operation

There are two modes of operation: Mode 0 and Mode 1. Mode selection is accomplished by using the LED_SEL_MODE bit. This bit is globally selected and controls the operation of all ports (see Table 83 “LED Control Register (Addr: 0x509)” on page 164).

Mode 0: (LED_SEL_MODE = 0 [Default]): This mode selects operations compatible with the SGS Thompson M5450 LED Display Driver device. This device converts the serial data stream, output by the IXF1104, into 30 direct-drive LED outputs. Although the LED interface is capable of driving all 30 LEDs, only twelve will be driven in the four-port IXF1104, three LEDs per port.

Mode 1: (LED_SEL_MODE = 1): This mode is used with standard TTL (74LS599) or HCMOS (74HC599) octal shift registers with latches, providing the most general and cost-effective implementation of the serial data stream conversion.

In addition to these physical modes of operation, there are two types of specific LED data decodes available for fiber and copper modes. This option is a global selection and controls the operation of all ports (see Table 83 “LED Control Register (Addr: 0x509)” on page 164).

5.9.2 LED Interface Signal Description

The IXF1104 LED interface consists of three output signal pins that are 2.5 V CMOS level pads. Table 18 provides LED signal names, pin numbers, and descriptions.

Table 18. LED Interface Signal Descriptions

Pin Name	Pin #	Pin Description
LED_CLK	K24	This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 0.5 MHz. The behavior of this signal remains constant in all modes of operation.
LED_DATA	M22	This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	L22	This is an output pin, and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

5.9.3 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson* M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 25 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 25 shows the 36 clocks that are output on the LED_CLK pin. The data is changed on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device.

The actual data shown in Figure 25 consists of a chain of 36 bits, 12 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 25. Mode 0 Timing Diagram

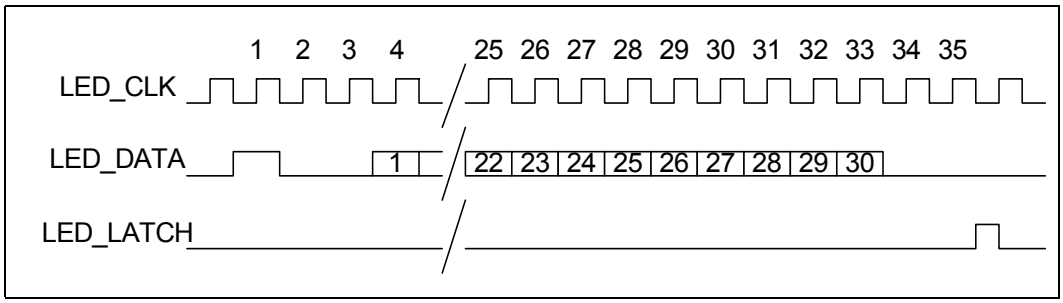


Table 19. Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK Cycle	LED_DATA Name	LED_DATA Description
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 12-bit LED DATA to the required 18-bit frame length. These bits should always be a logic 0.
4:15	LED DATA 1-12	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in Table 21 on page 98. The data is TRUE. Logic 1 (LED ON) = High
36:38	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a logic 0.

When implemented on the board with the M5450 device, the LED DATA bit 1 appears on Output bit 3 of the M5450 and the LED DATA bit 2 appears on Output bit 4, etc. This means that Output bits 1, 2, and 15 through 35 will never have valid data and should not be used.

5.9.4 Mode 1: Detailed Operation

Note: Please refer to generic specifications for 74LS/HC599 for information on device operation.

The operation of the LED Interface in Mode 1 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 26 on page 97 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 26 on page 97 shows the 36 clocks which are output on the LED_CLK pin. The data is changed on the falling edge of the clock and is valid for the almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC599 device. As seen in Figure 26, the LED_LATCH signal is active High during the Low period on the 35th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC599 devices, the LED DATA bit 1 is output on Shift register bit 1, and so on up the chain. Only Shift register bits 31 and 32 do not contain valid data.

The actual data shown in Figure 26 consists of a 36-bit chain, of which 12 bits are valid LED DATA. The 36-bit data chain is built up as shown in Figure 26.

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 26. Mode 1 Timing Diagram

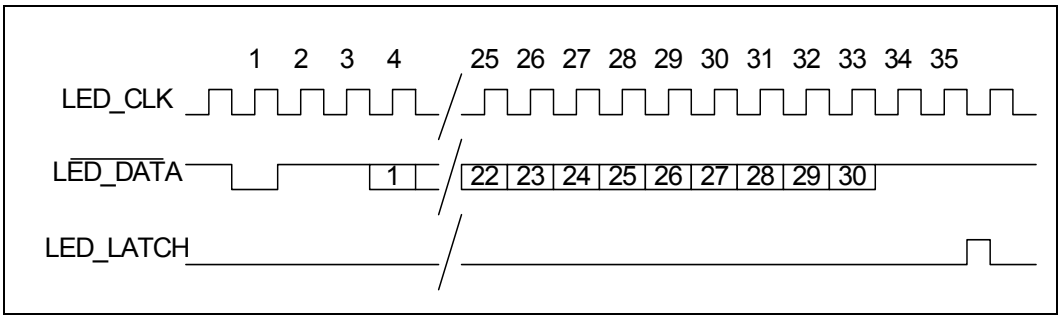


Table 20. Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK Cycle	LED_DATA Name	LED_DATA Description
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 16-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 16-stage shift register chain before the LED_LATCH signal is asserted.
4:15	LED DATA 1-12	These bits are the actual data to be transmitted to the 16-stage shift register chain. The decode for each bit in each mode is defined in Table 21 on page 98. The data is INVERTD. Logic 1 (LED ON) = Low.
36:38	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

5.9.5 Power-On, Reset, Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1104 Quad-Port Gigabit Ethernet Media Access Controller device configuration is completed. This is done by setting the LED_ENABLE bit to a logic 1 (see Table 83 “LED Control Register (Addr: 0x509)” on page 164). The power-on default for this bit is logic 0.

5.9.6 LED DATA Decodes

The data transmitted on the LED_DATA line is determined by programming the global operation mode as either fiber or copper. Table 21 shows the data decode of the data for both fiber and copper MACs.

Note: The data decode of the LED bits is independent of the Physical mode selection.

Table 21. LED_DATA# Decodes

LED_DATA#	MAC Port #	Fiber Designation	Copper Designation
1	0	Rx LED—Amber	Link LED—Amber
2		Rx LED—Green	Link LED—Green
3		Tx LED—Green	Activity LED—Green
4	1	Rx LED—Amber	Link LED—Amber
5		Rx LED—Green	Link LED—Green
6		Tx LED—Green	Activity LED—Green
7	2	Rx LED—Amber	Link LED—Amber
8		Rx LED—Green	Link LED—Green
9		Tx LED—Green	Activity LED—Green
10	3	Rx LED—Amber	Link LED—Amber
11		Rx LED—Green	Link LED—Green
12		Tx LED—Green	Activity LED—Green

5.9.6.1 LED Signaling Behavior

Operation in each mode for the decoded LED data in Table 21 is detailed in Table 22 and Table 23.

5.9.6.1.1 Fiber LED Behavior

Table 22. Intel® IXF1104 LED Behavior (Fiber)

Type	Status	Description
RxLED	Off	Synchronization has occurred but no packets are being received and "LED Control Register (Addr: 0x509)" on page 164 has not been set.
	Amber On	RX Synchronization has not occurred or no optical signal exists.
	Amber Blinking	Port has remote fault and "LED Fault Disable Register (Addr: 0x50B)" on page 164 is not set. Based on remote fault bit setting received in Rx_Config word.
	Green On	RX Synchronization has occurred and the "LED Control Register (Addr: 0x509)" on page 164 bit is set.
	Green Blinking	RX Synchronization has occurred and port is receiving data.
TxLED	Off	Port is not transmitting data or "LED Control Register (Addr: 0x509)" on page 164 is not set.
	Green Blinking	Port is transmitting data and "LED Control Register (Addr: 0x509)" on page 164 bit is set
NOTE: The LED behavior table assumes the port is enabled in the "Port Enable Register (Addr: 0x500)" on page 161 and the LEDs are enabled in the "LED Control Register (Addr: 0x509)" on page 164. If a port is not enabled, all the LEDs for that port will be off. If the LEDs are not enabled, all of the LEDs will be off.		

5.9.6.1.2 Copper LED Behavior

Table 23. Intel® IXF1104 LED Behavior (Copper)

Type	Status	Description
Link LED	Off	Port does not have a Remote Fault and "LED Control Register (Addr: 0x509)" on page 164 bit is not set.
	Amber On	Port has an RGMII RXERR condition detected and "LED Control Register (Addr: 0x509)" on page 164 bit is set
	Amber Blinking	Port has a remote fault and "LED Fault Disable Register (Addr: 0x50B)" on page 164 is not set.
	Green On	"LED Control Register (Addr: 0x509)" on page 164 bit is set and port does not have RGMII RXERR error or Remote Fault condition present.
Activity LED - Green	Off	Port is not transmitting and receiving data.
	Blinking	"LED Control Register (Addr: 0x509)" on page 164 set: Port is transmitting and/or receiving. "LED Control Register (Addr: 0x509)" on page 164 not set: Port is receiving data.
NOTE: The LED behavior table assumes the port is enabled in the "Port Enable Register (Addr: 0x500)" on page 161 and the LEDs are enabled in the "LED Control Register (Addr: 0x509)" on page 164. If a port is not enabled, all the LEDs for that port will be off. If the LEDs are not enabled, all of the LEDs will be off.		

5.10 Microprocessor Interface

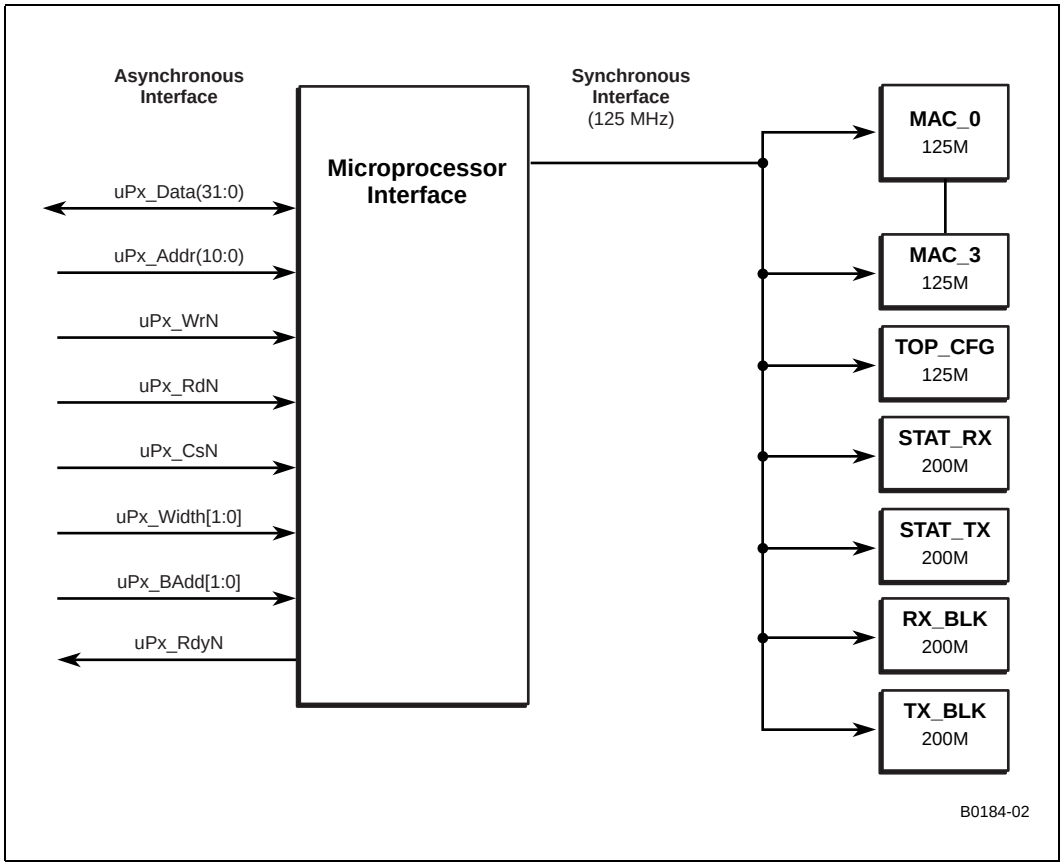
The Microprocessor interface block provides access to registers and statistics in the IXF1104. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to:

- Receive statistics registers
- Transmit statistics registers
- Receive FIFO registers
- Transmit FIFO registers
- Global configuration and control registers
- MAC_0 to MAC_3 registers

The Microprocessor interface width can be configured with the two strap pins (uPx_Width[1:0]) to operate as an 8-bit, 16-bit, or 32-bit bus. All internal accesses to registers are 32-bit (4, 2, or 1 data cycles respectively are required to fully access a register). When operating in 8-bit or 16-bit mode, read data for bytes [3:1] is strobed into read holding registers when byte [0] is read. Subsequent reads of bytes {1, 2, 3} in byte mode or of bytes {2,3} in 16-bit mode are supplied from the holding register independent of the upper address bits. On write accesses in 8-bit mode, the data of bytes {0, 1, 2} is similarly captured in internal write holding registers and the complete 32-bit write is committed when byte[3] is written to the IXF1104. When writing in 16-bit mode, bytes [1:0] are captured, and the double-word is committed when bytes [3:2] are written. The complete address for write is ignored (except for the write which causes the commit operation).

Figure 27 illustrates the internal and external connections of the microprocessor.

Figure 27. Microprocessor — External and Internal Connections



5.10.1 Functional Description

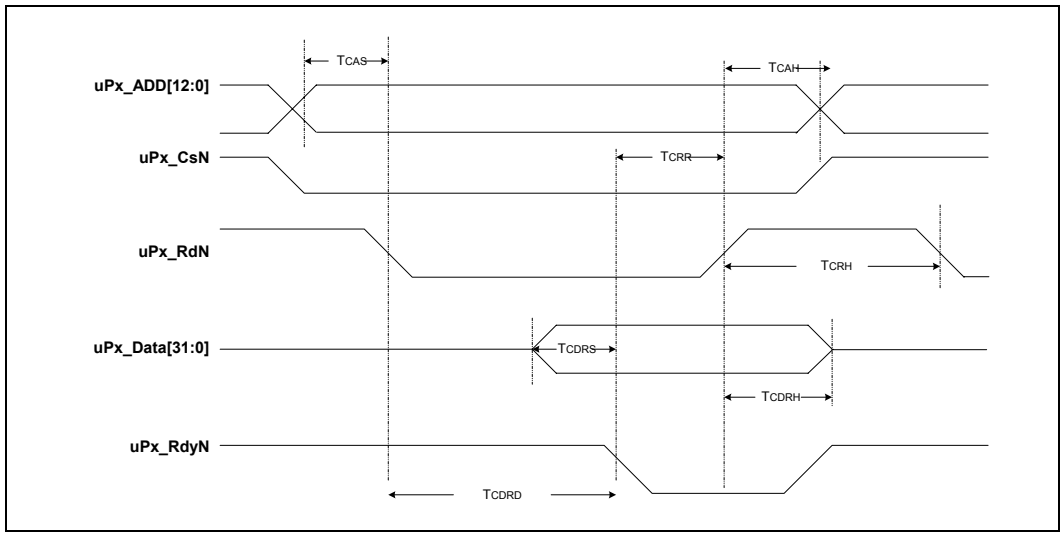
5.10.1.1 Read Access

Read access involves the following:

- Detect assertion of asynchronous Read control signal and latch address
- Generate internal Read strobe
- Drive valid data onto processor bus
- Assert asynchronous Ready signal for required length of time

Figure 28 shows the timing of the asynchronous interface for Read access.

Figure 28. Read Timing Diagram - Asynchronous Interface



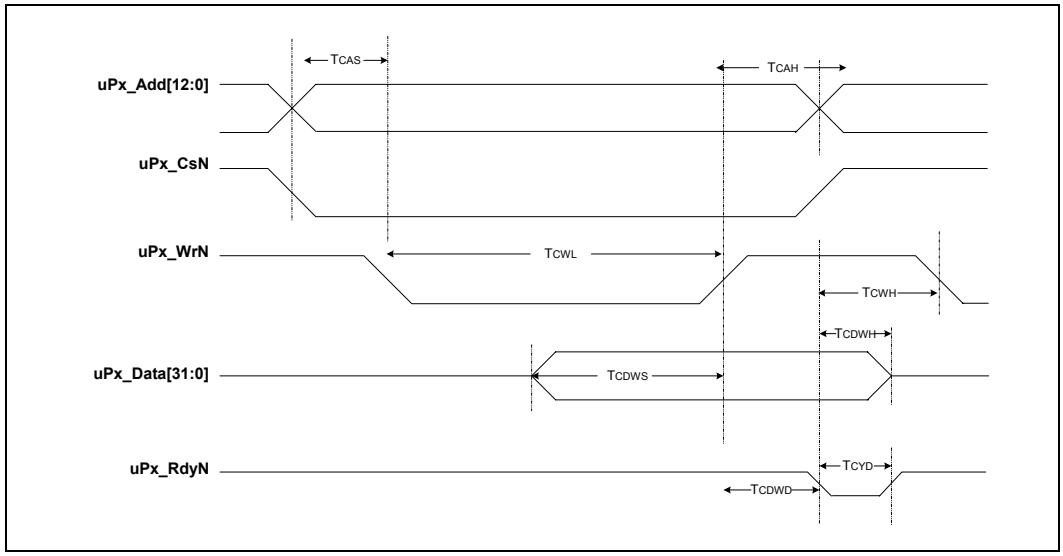
5.10.1.2 Write Access

Write process involves the following:

- Detect assertion of asynchronous Write control signal and latch address
- Detect de-assertion of asynchronous Write control signal and latch data
- Generate internal Write strobe
- Assert asynchronous Ready signal for required length of time

Figure 29 shows the timing of the asynchronous interface for Write accesses.

Figure 29. Write Timing Diagram - Asynchronous Interface



5.10.1.3 Microprocessor Timing Parameters

For information on the microprocessor interface Read and Write cycle AC timing parameters, refer to Figure 43 “Microprocessor Interface Read Cycle AC Timing” on page 124, Figure 44 “Microprocessor Interface Write Cycle AC Timing” on page 124, and Table 40 “Microprocessor Interface Write Cycle AC Signal Parameters” on page 125.

5.10.2 Endian

The Endian of the Microprocessor interface may be changed to allow connection of various microprocessors to the IXF1104 Quad-Port Gigabit Ethernet Media Access Controller. The Endian selection is determined by setting the Endian bit in the “Microprocessor Interface Register (Addr: 0x508)".

The following describes Endianness control:

- There is a byte swapper between the internal 32-bit bus and the external 32-bit bus.
- In 8-bit or 16-bit mode operation, the byte packer/byte unpacker holding registers sink and source data just like the 32-bit external bus in 32-bit mode.
- The “Microprocessor Interface Register (Addr: 0x508)" is used to select Big-Endian or Little-Endian mode.
- The byte swapper causes the behavior seen in Table 24 for accessing a register with data bits data[31:0].

Table 24. Byte Swapper Behavior

Address	Big-Endian			Little-Endian		
	µP[31:0]	µP[15:0]	µP[7:0]	µP[31:0]	µP[15:0]	µP[7:0]
0	data[31:0]	data[31:16]	data[31:24]	[7:0,15:8,23:16,31:24]	[23:16,31:24]	data[7:0]
1	–	–	data[23:16]	–	–	data[15:8]
2	–	data[15:0]	data[15:8]	–	[7:0,15:8]	data[23:16]
3	–	–	data[7:0]	–	–	data[31:24]

5.11 TAP Interface (JTAG)

The IXF1104 includes an IEEE 1149.1 compliant TAP (test access port) interface used during boundary scan testing. The interface consists of the following five pins:

- TDI – serial data input,
- TMS – test mode select
- TCLK– TAP clock
- TRSTN – Active Low asynchronous reset for the TAP
- TDO – serial data output.

TDI, TMS, and TRSTN require external pull-up resistors to float the pins High per the IEEE 1149.1 specification.

5.11.1 TAP State Machine

The TAP pins drive a TAP controller, which implements the 16-state state machine specified by the IEEE 1149.1 specification. Following power-up, the TAP controller must be reset by one of following two mechanisms:

- Asynchronous reset
- Synchronous reset

Asynchronous reset is achieved by pulsing or holding TRSTN Low. Synchronous reset is achieved by clocking TCLK with five clock pulses while TMS is held or floats High. This ensures that the boundary scan cells do not block the pin to core connections in the IXF1104.

5.11.2 Instruction Register and Supported Instructions

The instruction register is a 4-bit register that enacts the boundary scan instructions. After the state machine resets, the default instruction is IDCODE. The decode logic in the TAP controller selects the appropriate data register and configures the boundary scan cells for the current instruction. Table 25 shows the supported boundary-scan instructions.

Table 25. Instruction Register Description

Instruction	Code	Description	Data Register
BYPASS	1111	1-bit Bypass	Bypass
EXTEST	0000	External Test	Boundary Scan
SAMPLE	0001	Sample Boundary	Boundary Scan
IDCODE	0110	ID Code Inspection	ID
HIGHZ	0101	Float Boundary	Bypass
CLAMP	0111	Clamp Boundary	Bypass

5.11.3 ID Register

The ID register is a 32-bit register. The IDCODE instruction connects this register between TDI and TDO. See Table 86 “JTAG ID Register (Addr: 0x50C)” on page 165 for detailed information.

5.11.4 Boundary Scan Register

The Boundary Scan register is a shift register made up of all the boundary scan cells associated with the device pins. The number, type, and order of the boundary scan cells are specified in the IXF1104 BSDL file. The EXTEST and SAMPLE instructions connect this register between TDI and TDO.

5.11.5 Bypass Register

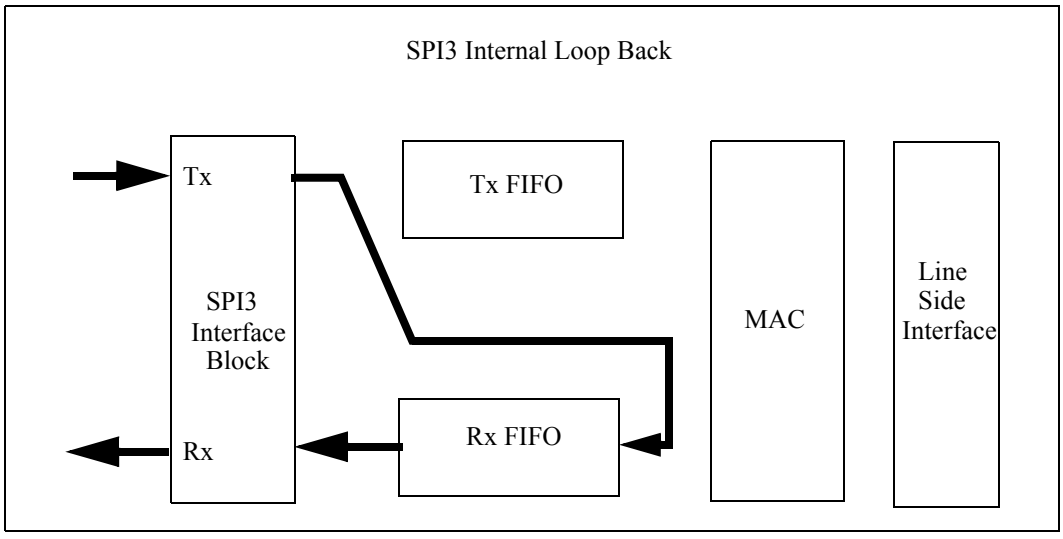
The Bypass register is a 1-bit register that bypasses the IXF1104 to reduce the JTAG chain length when accessing other devices on the chain besides the IXF1104. The BYPASS, HIGHZ, and CLAMP instructions connect this register between TDI and TDO.

5.12 Loopback Modes

The IXF1104 provides two loopback modes for device diagnostic testing when it has been integrated into a user system. A line-side loopback allows the line-side receive interface to be looped back to the transmit line-side interface. A SPI3 loopback mode allows the SPI3 transmit interface to be looped back to the SPI3 receive interface.

5.12.1 SPI3 Interface Loopback

Figure 30. SPI3 Interface Loopback Path



To provide a diagnostic loopback feature on the SPI3 interface, it is possible to configure the IXF1104 to loop back any data written to the IXF1104 through the SPI3 transmit interface back to the SPI3 receive interface. This is accomplished using the datapath shown in Figure 30.

Note: Loopback packets will also appear on the line side TX interface.

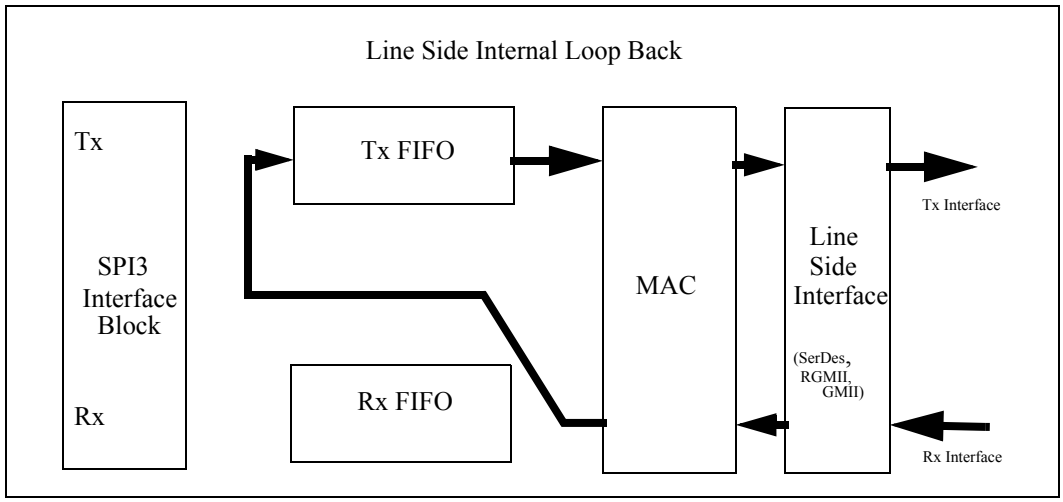
Note: There is a restriction when using this loopback mode. At least one clock cycle is required between a TEoP assertion and a TSoP assertion. This is required when the pre-pend feature of the receive FIFO is enabled to allow the addition of the extra two bytes to the data sent on the transmit interface. Where the pre-pend feature has not been enabled, data can be sent back-to-back on the transmit SPI3 interface with TSoP following TEoP on the next cycle.

To configure the IXF1104 to use the SPI3 loopback mode, the "RX FIFO Loopback Enable for Ports 0 - 3 Register (Addr: 0x5B2)" must be configured. Each IXF1104 port has a unique bit in this register designated to control loopback. It is possible to have individual ports in a loopback mode while other ports continue to operate in a normal mode.

5.12.2 Line Side Interface Loopback

To provide a diagnostic loopback feature on the line-side interfaces, the IXF1104 can be configured to loop back any data received by the IXF1104 through one of the line interfaces back to the corresponding transmit line interface. This is done by using the datapath shown in Figure 31. The line-side interface can be either SerDes, RGMII or GMII. Please note that it is not possible to loop one line-side interface back to a different one (for example, Rx SerDes looped back to transmit RGMII).

Figure 31. Line Side Interface Loopback Path



When the IXF1104 is configured in this loopback mode, all of the MAC functions and features are available, including flow control and pause-packet generation.

To configure the IXF1104 to use the line-side loopback mode, the "Loop RX Data to TX FIFO Register Ports 0 - 3 (Addr: 0x61F)" must be configured. Each IXF1104 port has a unique bit in this register designated to control the loopback. It is possible to have individual ports in a loopback mode while other ports continue to operate in a normal mode.

5.13 Clocks

The IXF1104 system interface has several reference clocks, including the following:

- SPI3 data path input clocks
- RGMII input and output clocks
- MDIO output clock
- JTAG input clock
- GBIC output clock
- LED output clock.

This section details the unique clock source requirements.

5.13.1 System Interface Reference Clocks

The following system interface clock is required by the IXF1104:

- CLK125

5.13.1.1 CLK125

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- +/- 50 ppm
- Maximum duty cycle distortion 40/60

5.13.2 SPI3 Receive and Transmit Clocks

The IXF1104 transmit clock requirements include the following:

- 3.3 V LVTTL drive
- +/- 50 ppm
- Maximum frequency of 133 MHz in MPHY mode
- Maximum frequency of 125 MHz in SPHY mode
- Maximum duty cycle distortion 45/55

The IXF1104 meets the following specifications for the receive clock:

- 3.3 V LVTTL drive
- +/- 50 ppm
- Maximum frequency of 133 MHz in MPHY mode
- Maximum frequency of 125 MHz in SPHY mode
- Maximum duty cycle distortion 45/55

5.13.3 RGMII Clocks

The RGMII interface is governed by the Hewlett-Packard* 1.2a specification. The IXF1104 compliant to this specification with the following:

- 2.5 V CMOS drive
- Maximum duty cycle distortion 40/60
- +/- 100 ppm
- 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps

5.13.4 MDC Clock

The IXF1104 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. The IXF1104 meets the following specifications for this clock:

- 2.5 V CMOS drive
- 2.5/18 MHz operation (selectable by the MDC speed bit in the "MDI Control Register (Addr: 0x683)")
- 50/50 duty cycle for 2.5 MHz operation
- 43/57 duty cycle for 18 MHz operation

5.13.5 JTAG Clock

The IXF1104 supports JTAG. The source of this clock must meet the following specifications:

- 3.3 V CMOS drive
- Maximum clock frequency 11 MHz
- Maximum duty cycle distortion 40/60

5.13.6 GBIC Clock

The IXF1104 supports a single-output GBIC clock to support all 10 GBIC interfaces. The IXF1104 meets the following specifications for this clock:

- 2.5 V CMOS drive
- Maximum clock frequency of 100 MHz

5.13.7 LED Clock

The IXF1104 supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 720 Hz.

The IXF1104 supports a serial LED data stream and meets the following specifications for this clock:

- 2.5 V CMOS drive
- Maximum frequency of 720 Hz
- Maximum duty cycle distortion 50/50

6.0 Electrical Specifications

Table 26 through Table 44 “LED Interface AC Timing Parameters” on page 129 and Figure 32 “SPI3 Receive Interface Timing” on page 112 through Figure 48 “LED AC Interface Timing” on page 129 represent the target specifications of the following IXF1104 interfaces:

- SPI3
- JTAG
- MDIO
- Pause Control
- Microprocessor
- LED
- System
- GMII and RGMII
- SerDes
- GBIC

These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 28 “DC Specifications” on page 110 through Table 44 “LED Interface AC Timing Parameters” on page 129 apply over the recommended operating conditions specified in Table 27.

Table 26. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Comments
Supply voltage		VDD	-0.3	2.2	volts	Core digital power
		VDD2, VDD3	-0.3	4.25	volts	IO digital power
		VDD4, VDD5	-0.3	4.25	volts	IO digital power
		PLL1_VDDA, PLL2_VDDA	-0.3	2.2	volts	PLL analog power
		PLL3_VDDA	-0.3	4.25	volts	PLL analog power
		Tx_AV25, RxAV25	-0.3	2.2	volts	SerDes analog power
		Tx_AVTT, Rx_AVTT	-0.3	2.2	volts	SerDes analog power
Operating temperature	Ambient	TOPA	-40	+85	°C	Copper mode
	Ambient	TOPA	0.0	+70	°C	Fiber mode
Storage temperature		TST	-40	+150	°C	
Caution: Exceeding these values may cause permanent damage to the device. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.						

Table 27. Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Units
Recommended supply voltage		VDD	1.65	–	1.95	Volts
		VDD2, VDD3	3.0	–	3.6	Volts
		VDD4, VDD5	2.3	–	2.7	Volts
		PLL1_VDDA, PLL2_VDDA	1.65	–	1.95	Volts
		PLL3_VDDA	2.3	–	2.7	Volts
		Tx_AV25, RxAV25	2.3	–	2.7	Volts
		Tx_AVTT, Rx_AVTT	1.65	–	1.95	Volts
Operating Current	SerDes Operation Transmitting and receiving in 1000 Mbps mode	VDD, PLL1_VDDA, PLL2_VDDA. Tx_AVTT, Rx_AVTT	–	0.780	–	Amps
		VDD4, VDD5, PLL3_VDDA, Tx_AV25, Rx_AV25	–	0.050	–	Amps
		VDD2, VDD3	–	0.246	–	Amps
Operating Current	RGMII Operation Transmitting and receiving in 1000 Mbps mode	VDD, PLL1_VDDA, PLL2_VDDA. Tx_AVTT, Rx_AVTT	–	0.757	–	Amps
		VDD4, VDD5, PLL3_VDDA, Tx_AV25, Rx_AV25	–	0.224	–	Amps
		VDD2, VDD3	–	0.208	0.235	Amps
Recommended operating temperature	Ambient	TOPA	0	–	70	°C
	Case with heat sink	TOPC-HS	0	–	122	°C
	Case without heat sink	TOPC-NHS	0	–	121	°C
Power consumption	SerDes Operation Transmitting and receiving in 1000 Mbps mode	–	–	2.23	2.72	Watts
	RGMII Operation Transmitting and receiving in 1000 Mbps mode	–	–	2.84	3.4	Watts

6.1 DC Specifications

The IXF1104 supports the following I/O buffer types:

- 2.5 V CMOS
- 3.3 V LVTTL
- LVDS

See Section 5.1.6, "Packet Buffer Dimensions" on page 59 for additional information regarding I/O buffer types. The related driver characteristics are described in this section.

Caution: Please note that IXF1104 input pins are not 5 V tolerant. Devices driving the IXF1104 must provide 3.3 V signal levels or use level-shifting buffers to provide 3.3 V compatible levels. Otherwise, damage to the IXF1104 will occur.

Table 28. DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Comments
2.5V CMOS I/O Cells						
Input high voltage	VIH	1.7	–	–	V	2.5 V I/Os
Input low voltage	VIL	–	–	0.7	V	2.5 V I/Os
Output high voltage	VOH	2.0	–	–	V	2.5 V I/Os
Output low voltage	VOL	–	–	0.4	V	2.5 V I/Os
3.3V I/O Cells						
Input high voltage	VIH	1.7	–	–	V	3.3 V LVTTL I/Os
Input low voltage	VIL	–	–	0.7	V	3.3 V LVTTL I/Os
Output high voltage	VOH	2.4	–	–	V	3.3 V LVTTL I/Os
Output low voltage	VOL	–	–	0.4	V	3.3 V LVTTL I/Os
SerDes Specification						
Transmit differential signal level	TxDfPP	438	525	613	mVpp diff	Tx_AVTT terminated to 1.8V; Rload = 50 ohms
Transmit common mode voltage range	TxCMV	1430	1505	1580	mV	Tx_AVTT terminated to 1.8V; RLoad = 50 ohms; FIR coeffs = 0
Differential signal rise/fall time	Diff rise/ fall	60	96	132	ps	Rload = 50 ohms; 20% to 80% max
Differential output impedance	TxDiffZ	60	105	150	Ω diff	Nominal value = 100 ohms differential
Receiver differential voltage requirement at center of receive eye	RxDiffV	200	–	–	mVp-p diff	–
Receiver common mode voltage range	RxCMV	900	1275	1650	mV	–
Receiver termination impedance	RxZ	40	51	62.5	Ω	–
Signal detect level	RxSigDet	50	125	200	mVp-pdiff	–

6.1.1 Undershoot / Overshoot Specifications

The overshoot figures given in this section represent the maximum voltage that can be applied without affecting the reliability of the device (see Table 29).

Caution: If these limits are exceeded, damage to the device will occur.

Table 29. Undershoot / Overshoot Limits

Pin Type	Undershoot	Overshoot
2.5 V CMOS	-0.60 V	3.9 V
3.3 V LVTTL	-0.60 V	3.9 V

6.1.2 RGMII Electrical Characteristics

The RGMII signals (including MDIO/MDC) are based on 2.5V CMOS interface voltages, as defined by JEDEC EIA/JESD8-5 (see Table 30).

Table 30. RGMII Power

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA; V_{CC} = Min	2.0	VDD +.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA; V_{CC} = Min	GND -.3	0.40	V
V_{IH}	Input High Voltage	V_{IH} > V_{IH_Min}; V_{CC} = Min	–	–	V
V_{IL}	Input Low Voltage	V_{IL} < V_{IL_Max}; V_{CC} = Min	–	.70	V
I_{IH}	Input High Current	V_{CC} = Max; V_{IN} = 2.5V	–	15	µA
I_{IL}	Input Low Current	V_{CC} = Max; V_{IN} = 0.4V	-15	–	µA

6.1.3 Transmitter and Receiver Operating Conditions

Table 31 highlights the operating conditions required by the TX and RX cores to meet specified performance requirements.

Table 31. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply voltage VDD	1.65	1.80	1.95	V
Supply voltage AV25	2.25	2.50	3.60	V
Termination voltage AVTT	1.65	1.80	1.95	V
Ambient temperature	0	–	85	°C
Transmission path characteristic impedance	85	100	115	W diff

6.2 SPI3 AC Timing Specifications

6.2.1 Receive Interface Timing

Figure 32 and Table 32 illustrate and provide SPI3 receive interface timing information.

Figure 32. SPI3 Receive Interface Timing

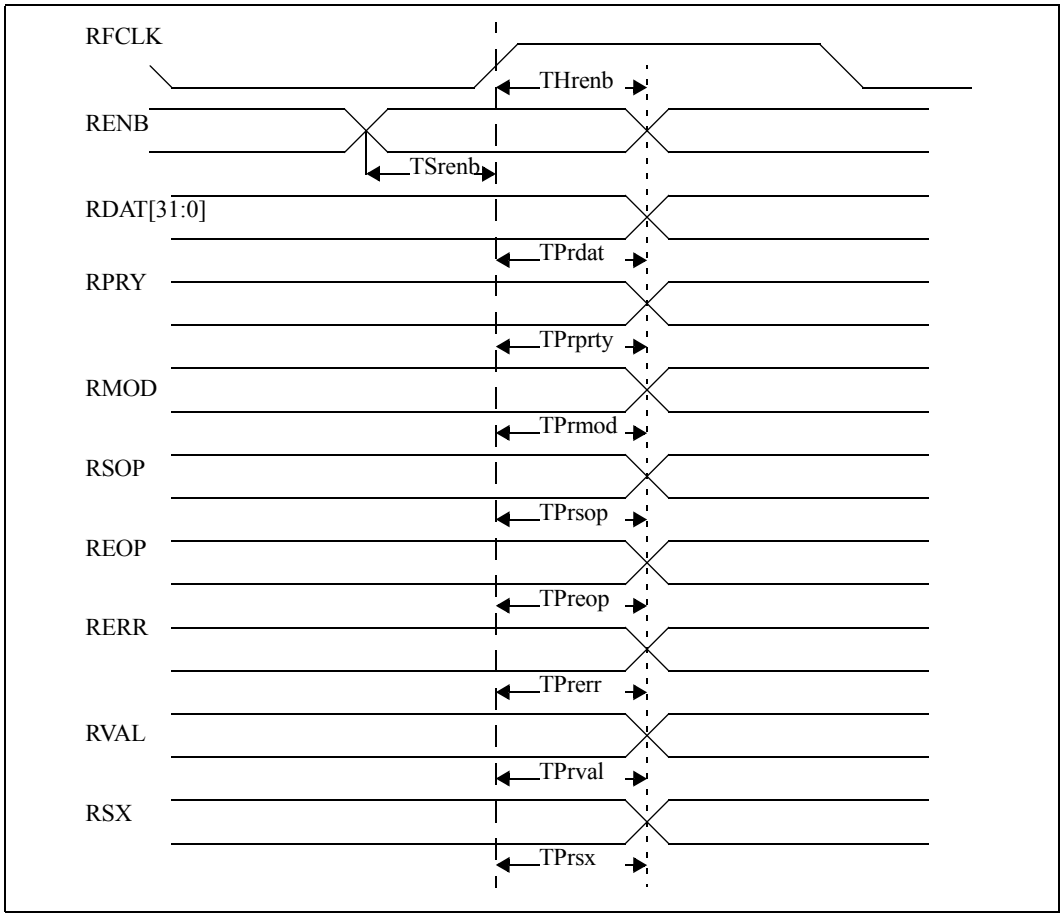


Table 32. SPI3 Receive Interface Signal Parameters

Symbol	Parameter	Min	Max	Units
–	RFCLK frequency	–	133	MHz
–	RFCLK duty cycle	40	60	%
Tsrenb	RENB setup time to RFCLK	1.8	–	ns
Threnb	RENB hold time to RFCLK	0.5	–	ns
TPrdat	RFCLK high to RDAT valid	1.5	3.7	ns
TPrprty	RFCLK high to RPRTY valid	1.5	3.7	ns
TPrsop	RFCLK high to RSOP valid	1.5	3.7	ns
TPreop	RFCLK high to REOP valid	1.5	3.7	ns
TPrmod	RFCLK high to RMOD valid	1.5	3.7	ns
TPrerr	RFCLK high to RERR valid	1.5	3.7	ns
TPrval	RFCLK high to RVAL valid	1.5	3.7	ns
TPrsx	RFCLK high to RSX valid	1.5	3.7	ns

NOTES: Receive I/O Timing

1. When a setup time is specified between an input and a clock, the setup time is the time in nanoseconds from the 1.4-volt point of the input to the 1.4-volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4-volt point of the clock to the 1.4-volt point of the input.
3. Output propagation time is the time in nanoseconds from the 1.4-volt point of the reference signal to the 1.4-volt point of the output.
4. Maximum propagation delays are measured with a 30 pF load when operating OIF-SPI3 standard 104 MHz. Over-clocked rates of 125 MHz or higher are measured using a load of 20 pF.

6.2.2 Transmit Interface Timing

Figure 33 and Table 33 illustrate and provide SPI3 transmit interface timing information.

Figure 33. SPI3 Transmit Interface Timing

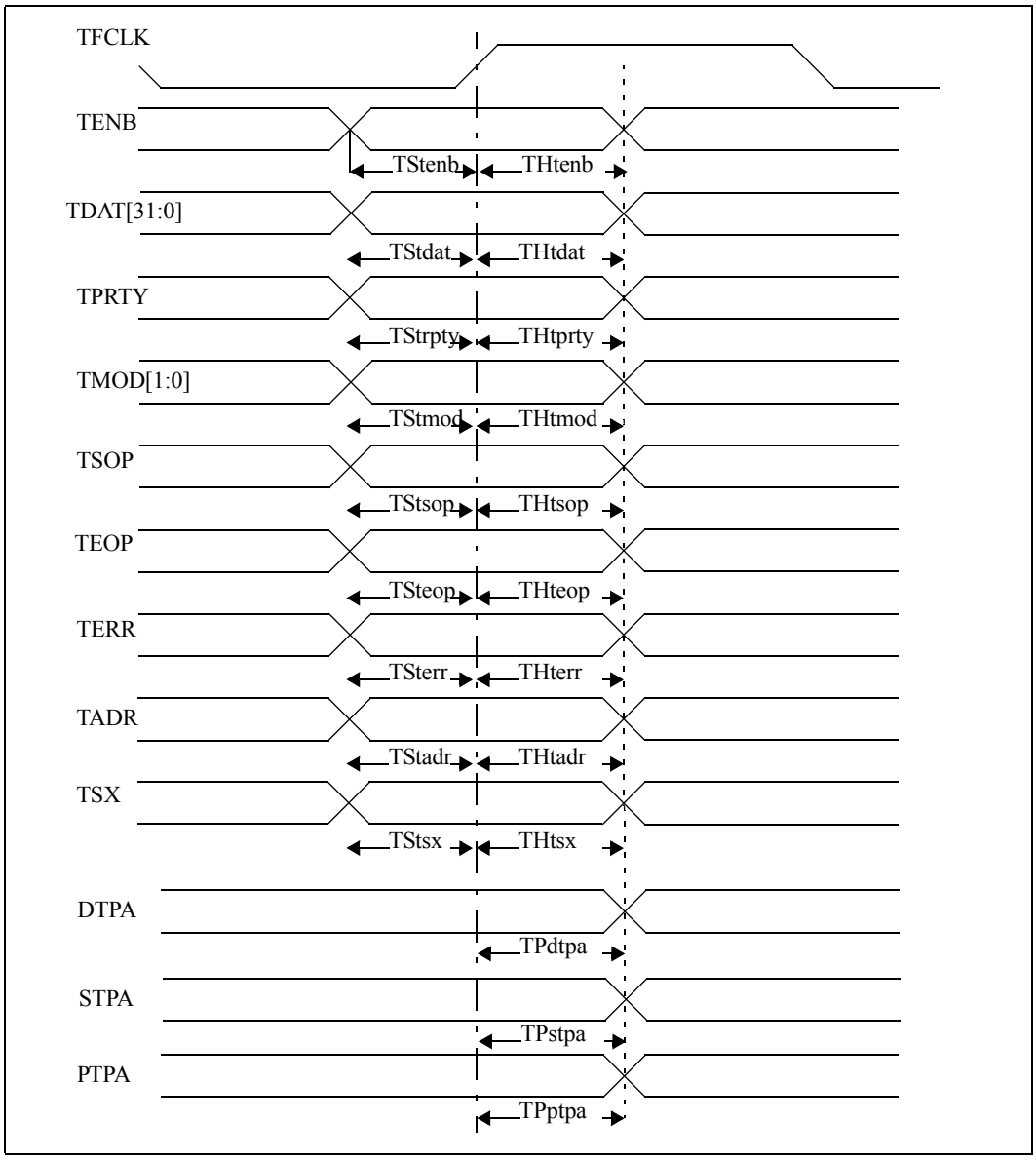


Table 33. SPI3 Transmit Interface Signal Parameters

Symbol	Parameter	Min	Max	Units
–	TFCLK frequency	–	133	MHz
–	TFCLK duty cycle	40	60	%
TStenb	TENB setup time to TFCLK	1.8	–	ns
THtenb	TENB hold time to TFCLK	0.5	–	ns
TStdat	TDAT[31:0] setup time to TFCLK	1.8	–	ns
THtdat	TDAT[31:0} hold time to TFCLK	0.5	–	ns
TStprty	TRPTY setup time to TFCLK	1.8	–	ns
THtprty	TPRTY hold time to TFCLK	0.5	–	ns
TStsop	TSOP setup time to TFCLK	1.8	–	ns
THtsop	TSOP hold time to TFCLK	0.5	–	ns
TSteop	TEOP setup time to TFCLK	1.8	–	ns
THteop	TEOP hold time to TFCLK	0.5	–	ns
TStmod	TMOD setup time to TFCLK	1.8	–	ns
THtmod	TMOD hold time to TFCLK	0.5	–	ns
TSterr	TERR setup time to TFCLK	1.8	–	ns
THterr	TERR hold time to TFCLK	0.5	–	ns
TStsx	TSX setup time to TFCLK	1.8	–	ns
THtsx	TSX hold time to TFCLK	0.5	–	ns
TStadr	TADR setup time to TFCLK	1.8	–	ns
THtadr	TADR hold time to TFCLK	0.5	–	ns
TPdtpa	TFCLK high to DTPA valid	1.5	3.7	ns
TPstpa	TFCLK high to STPA valid	1.5	3.7	ns
TPptpa	TFCLK high to PTPA valid	1.5	3.7	ns

NOTES: Transmit I/O Timing:
1. When a setup time is specified between an input and a clock, the setup time is the time in nanoseconds from the 1.4 V point of the input to the 1.4-volt point of the clock.
2. When a hold time is specified between an input and clock, the hold time is the time in nanoseconds from the 1.4 V point of the clock to the 1.4-volt point of the input.
3. Output propagation delay time is the time in nanoseconds from the 1.4 V point of the reference signal to the 1.4 V point of the output.

6.3 RGMII AC Timing Specification

Figure 34 and Table 34 provide RGMII interface timing parameters.

Figure 34. RGMII Interface Timing

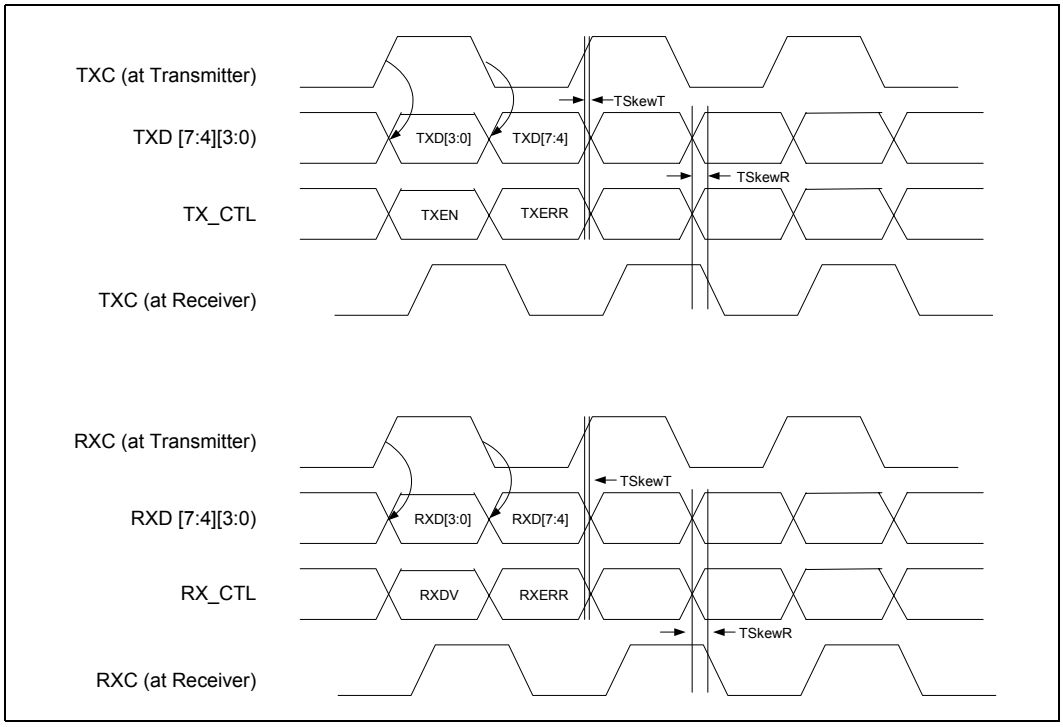


Table 34. RGMII Interface Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data-to-Clock Output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data-to-Clock Input Skew (at Receiver)[1]	1	–	2.8	ns
Tcyc	Clock Cycle Duration[2]	7.2	8	8.8	ns
Duty_T	Duty Cycle for Gigabit[2]	45	50	55	%
Duty_G	Duty Cycle for 10/100T[3]	40	50	60	%
Tr/Tf	Rise/Fall Time (20–80%)	–	–	.75	ns

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
2. For 10 Mbps and 100 Mbps Tcyc scales to 400 ns +/– 40 ns and 40 ns +/– 4 ns respectively.
3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

6.4 GMII AC Timing Specification

6.4.1 1000 Base-T Operation

Figure 35 and Figure 36 and Table 35 and Table 36 provide GMII AC timing specifications.

6.4.1.1 1000 BASE-T Transmit Interface

Figure 35. 1000BASE-T Transmit Interface Timing

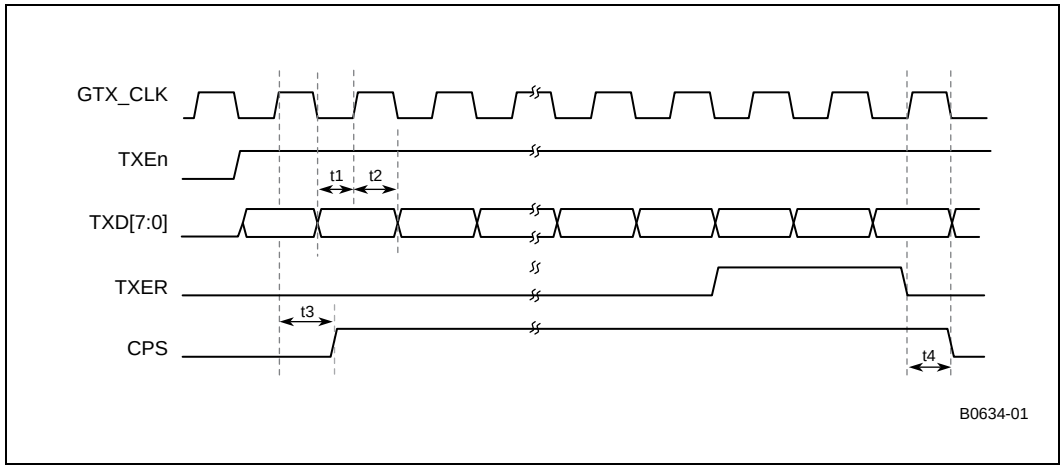


Table 35. GMII 1000BASE-T Transmit Signal Parameters

Symbol	Parameter	Min	Typ[1]	Max	Unit[2]
t1	TXD[7:0], TXEN, TXER Set-up to TXC High	2.0	–	–	ns
t2	TXD[7:0], TXEN, TXER Hold from TXC High	0.0	–	–	ns
t3	TXEN sampled to CRS asserted	–	–	16	BT
t4	TXEN sampled to CRS de-asserted	–	–	16	BT

1. Typical values are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the PHY and is the reciprocal of bit rate. BT for 1000BASE-T = 10^{-9} or 1 ns.

6.4.1.2 1000BASE-T Receive Interface

Figure 36. 1000BASE-T Receive Interface Timing

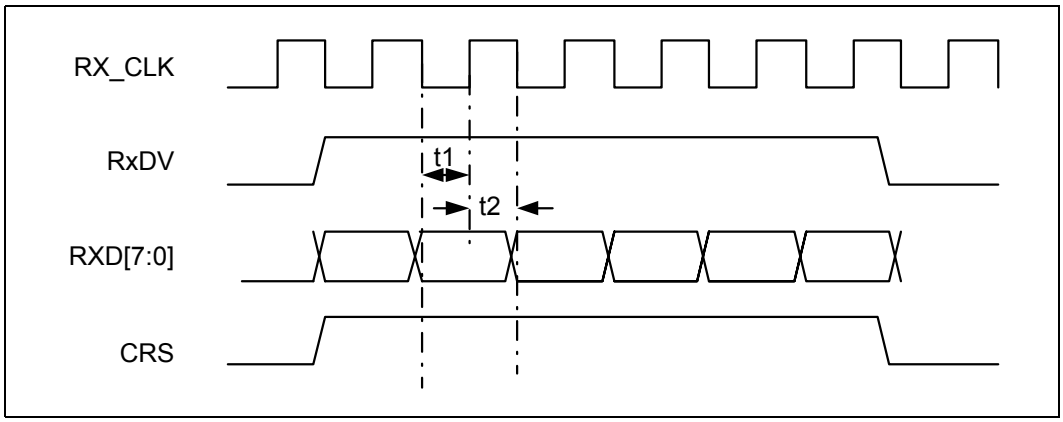


Table 36. GMII 1000BASE-T Receive Signal Parameters

Symbol	Parameter	Min	Typ[1]	Max	Unit[2]
t1	RXD[7:0], RX_DV, RXER Setup to Rx_CLK High	2.5	–	–	ns
t2	RXD[7:0], RX_DV, RXER Hold after Rx_CLK High	0.5	–	–	ns

1. Typical values are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the PHY and is the reciprocal of bit rate. BT for 1000BASE-T = 10^{-9} or 1 ns.

6.5 SerDes AC Timing Specification

Figure 37. SerDes Timing Diagram

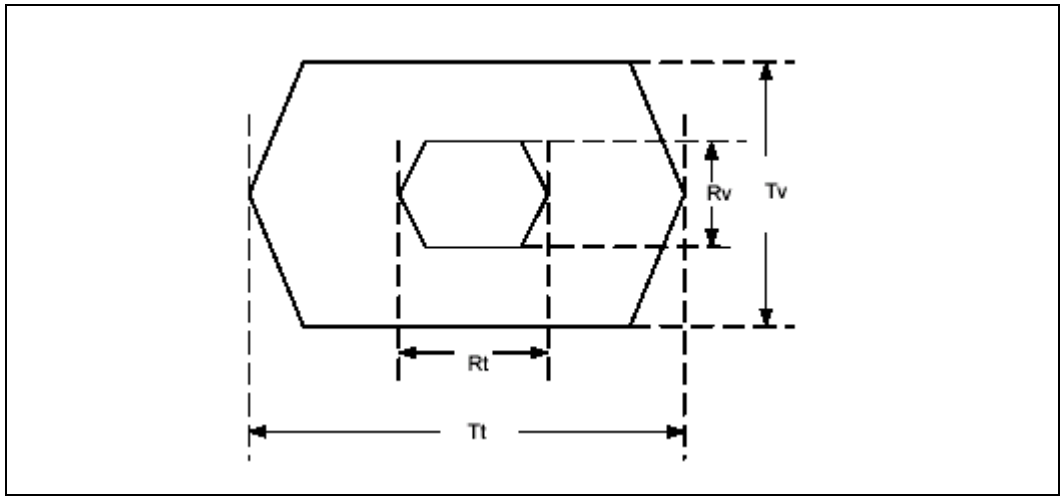


Table 37. SerDes Timing Parameters

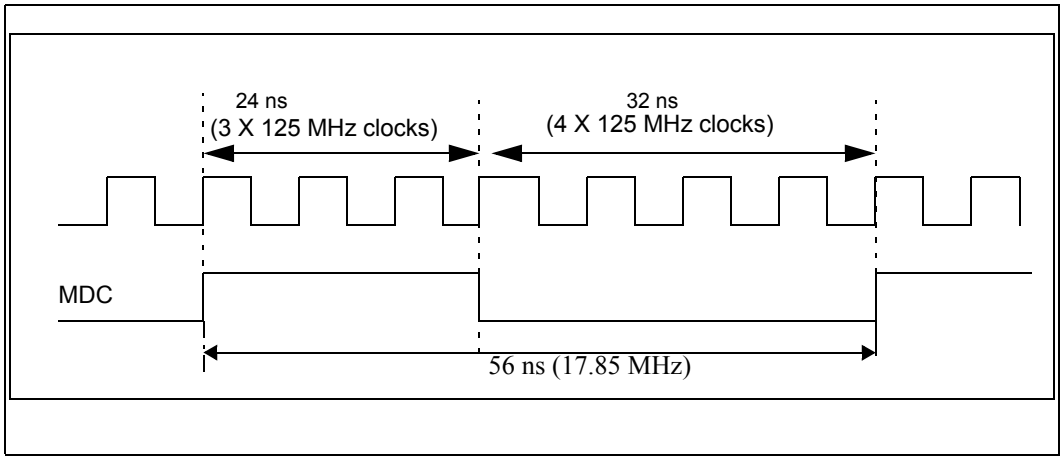
Symbol	Parameter	Min	Max	Units
Tt	Transmit eye width	800	–	pS
Rt	Receiver eye width	280	–	pS
Tv	Transmit amplitude	1000	–	mV
Rv	Receiver amplitude	200	–	mV

6.6 MDIO AC Timing Specification

The MDIO Interface on the IXF1104 can operate in two modes – low-speed and high-speed. In low-speed mode, the MDC clock signal operates at a frequency of 2.5 MHz. In high-speed mode, the MDC clock signal operates at a frequency of 18 MHz. (See Figure 38 through Figure 40 and Table 38.)

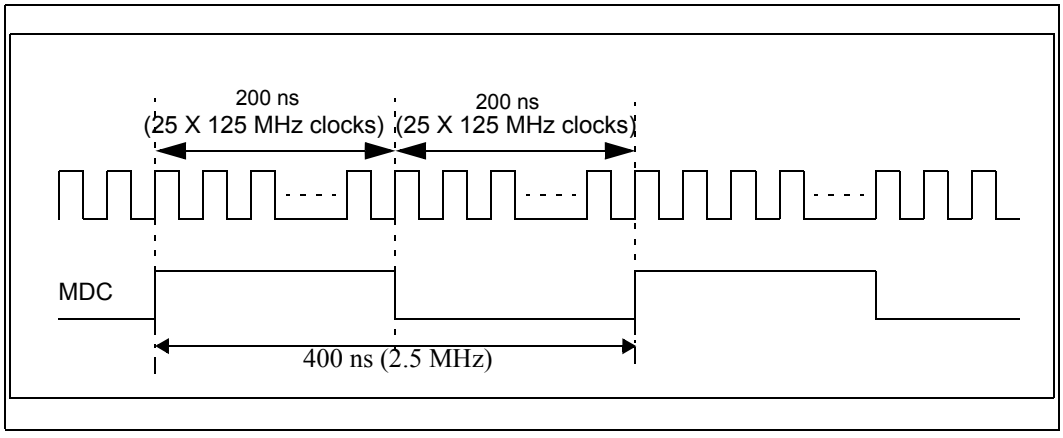
6.6.1 MDC High-Speed Operation Timing

Figure 38. MDC High-Speed Operation Timing



6.6.2 MDC Low-Speed Operation Timing

Figure 39. MDC Low-Speed Operation Timing



6.6.3 MDIO AC Timing

Figure 40. MDIO Timing

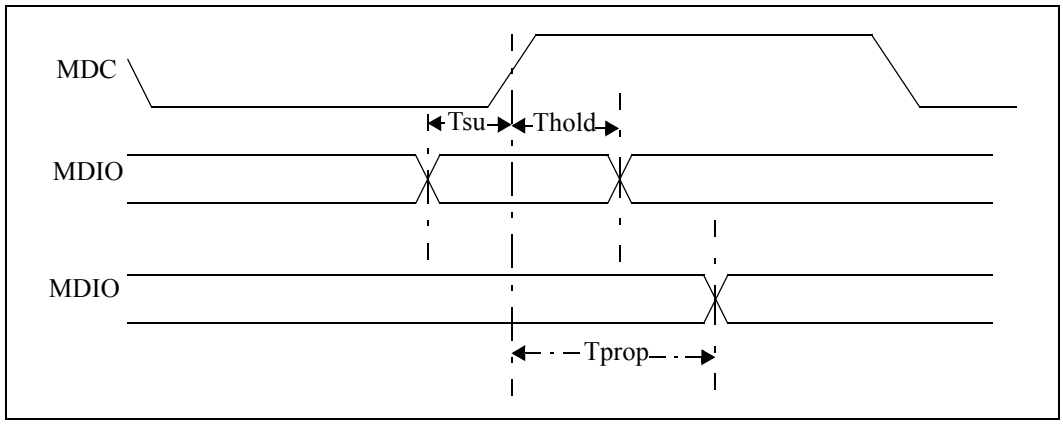


Table 38. MDIO Signal Parameters

Symbol	Parameters	Min	Max	Units
Tsu	MDIO Setup prior to MDC High	10	-	ns
Thold	MDIO Hold after MDC High	10	-	ns
Tprop	MDIO Valid after rising edge of MDC	0	42	ns

6.7 GBIC and I²C AC Timing Specification

6.7.1 I²C Interface Timing

Figure 41 and Figure 42 illustrate bus timing and write cycle, and Table 39 shows the I²C Interface AC timing characteristics.

Figure 41. Bus Timing Diagram

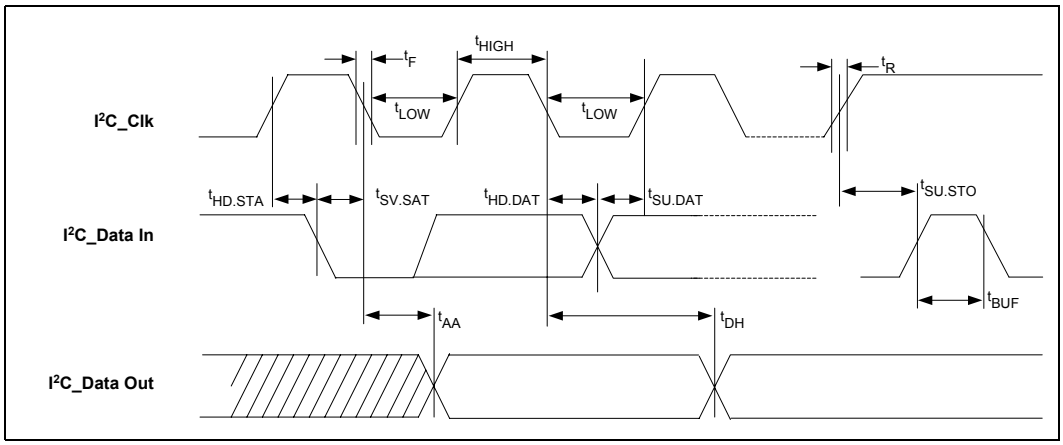


Figure 42. Write Cycle Diagram

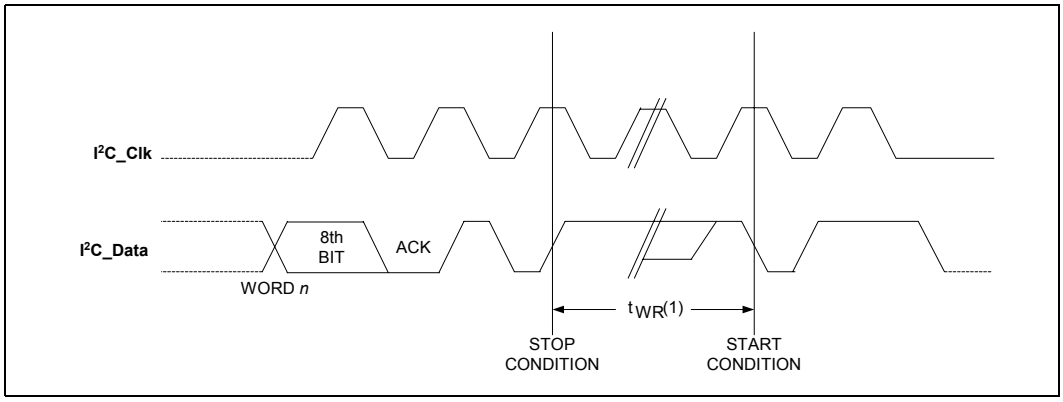


Table 39. I²C AC Timing Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock frequency, SCL	-	100	kHz
t_{LOW}	Clock pulse width low	4.7		µs
t_{HIGH}	Clock pulse width high	4.0		µs
t_I	Noise suppression		100	µs
t_{AA}	Clock low to data valid out	0.1	4.5	µs
t_{BUF}	Time the bus must be free before a new transmission starts	4.7	-	µs
$t_{HD.STA}$	Start hold time	4.0	-	µs

Table 39. I^2C AC Timing Characteristics (Sheet 2 of 2)

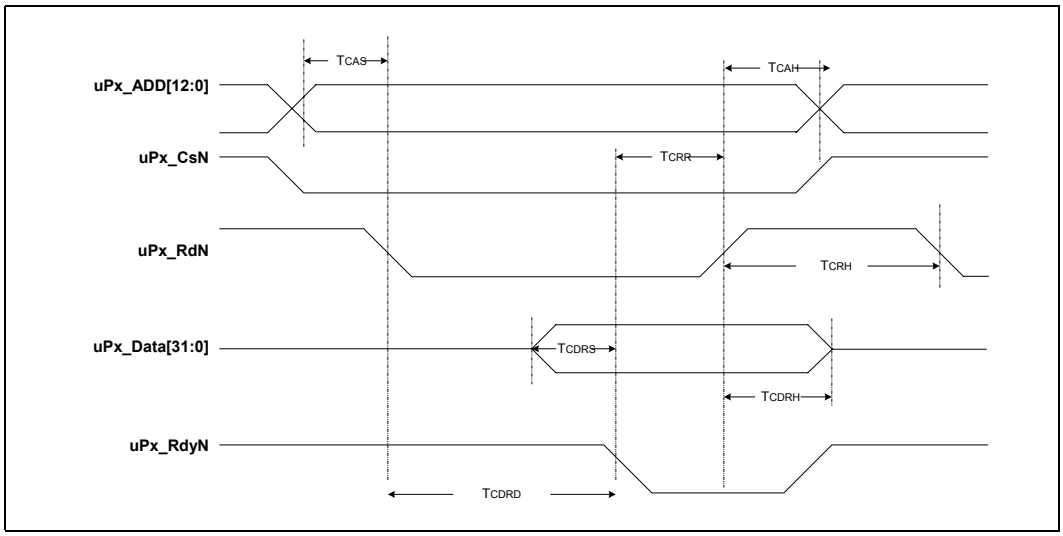
Symbol	Parameter	Min	Max	Units
$t_{SU.STA}$	Start setup time	4.7	–	µs
$t_{HD.DAT}$	Data in hold time	0	–	µs
$t_{SU.DAT}$	Data in setup time	200	–	ns
t_R	Inputs rise time	–	1.0	µs
t_F	Inputs fall time	–	300	ns
$t_{SU.STO}$	Stop setup time	4.7	–	µs
t_{DH}	Data out hold time	100	–	ns
t_{WR}	Write cycle time	–	10	ms

6.8 Microprocessor AC Timing Specification

6.8.1 Microprocessor Interface Read Cycle AC Timing

Figure 43, Figure 44, and Table 40 illustrate the microprocessor interface read and write cycle AC timing.

Figure 43. Microprocessor Interface Read Cycle AC Timing



6.8.2 Microprocessor Interface Write Cycle AC Timing

Figure 44. Microprocessor Interface Write Cycle AC Timing

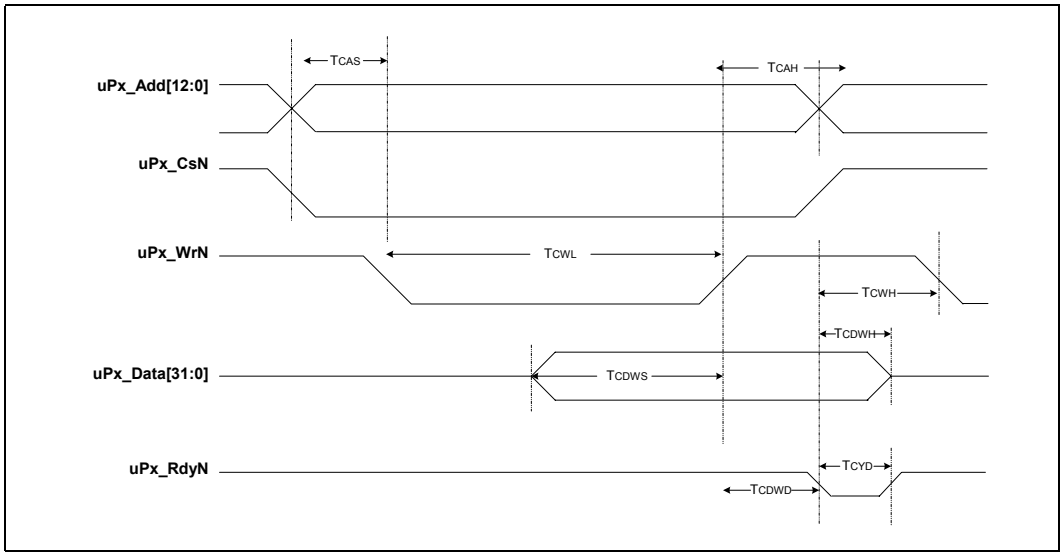


Table 40. Microprocessor Interface Write Cycle AC Signal Parameters

Symbol	Parameter	Min	Max
Tcas	Address, chip select setup time	5 ns	–
Tcah	Address, chip select hold time	10 ns	–
Tcrr	Ready assertion to read de-assertion	10 ns	–
Tcrh	Read high width	24 ns	–
Tcdrs	Read data setup time to ready assertion	10 ns	–
Tcdrh	Read data hold time after read de-assertion	8 ns	32 ns
Tcdrd	Read data driving delay	24 ns	355 ns
Tcwl	Write assertion width	40 ns	–
Tcwh	Ready assertion to write assertion	16 ns	–
Tcdws	Write data setup to write de-assertion	10 ns	–
Tcdwh	Write data hold time after ready assertion	5 ns	–
Tcdwd	Write data sampling delay	8 ns	32 ns
Tcyd	Ready width in write cycle	24 ns	40 ns

6.9 Pause Control AC Timing Specification

Figure 45 and Table 41 show the pause control AC timing specifications. The Pause interface operates as an asynchronous interface relative to the main system clock (CLK125). There is, however, a relationship between the TxPauseAdd bus and the strobe signal (TxPauseFr).

Figure 45. Pause Interface Timing

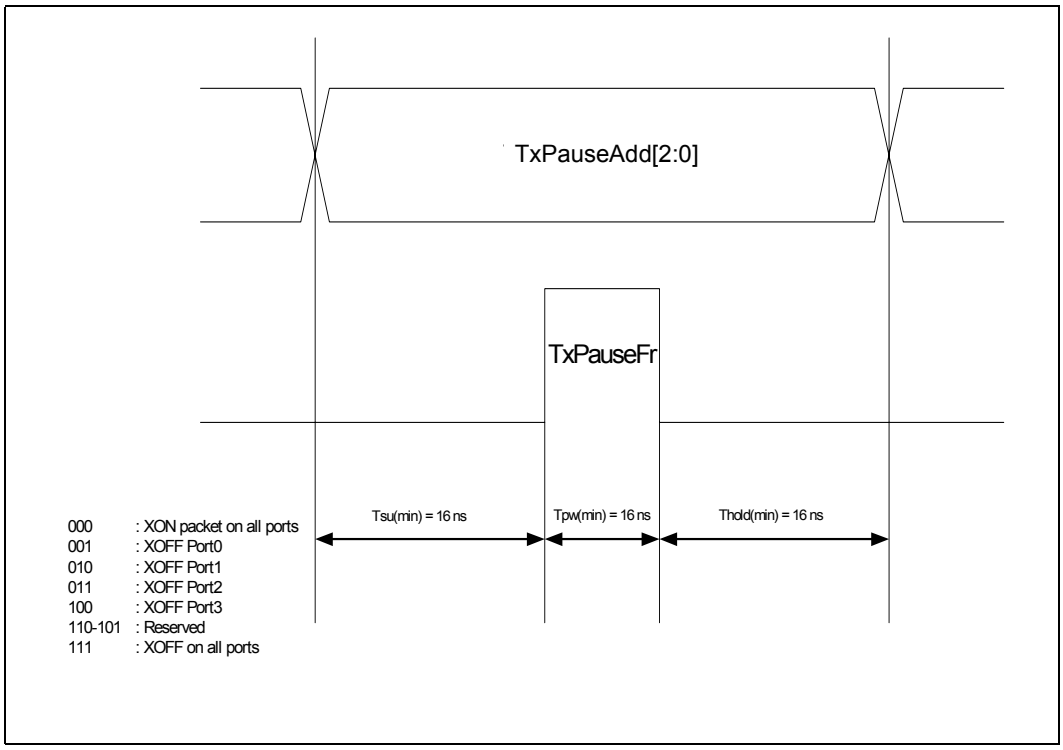


Table 41. Pause Interface Timing Parameters

Symbol	Parameter	Min	Max	Units
Tsu	TxPauseAdd stable prior to TxPauseFr high	16	–	ns
Tpw	TxPauseFr pulse width	16	–	ns
Thold	TxPauseAdd stable after TxPauseFr high	16	–	ns

6.10 JTAG AC Timing Specification

Figure 46 and Table 42 provide the JTAG AC timing specifications.

Figure 46. JTAG AC Timing

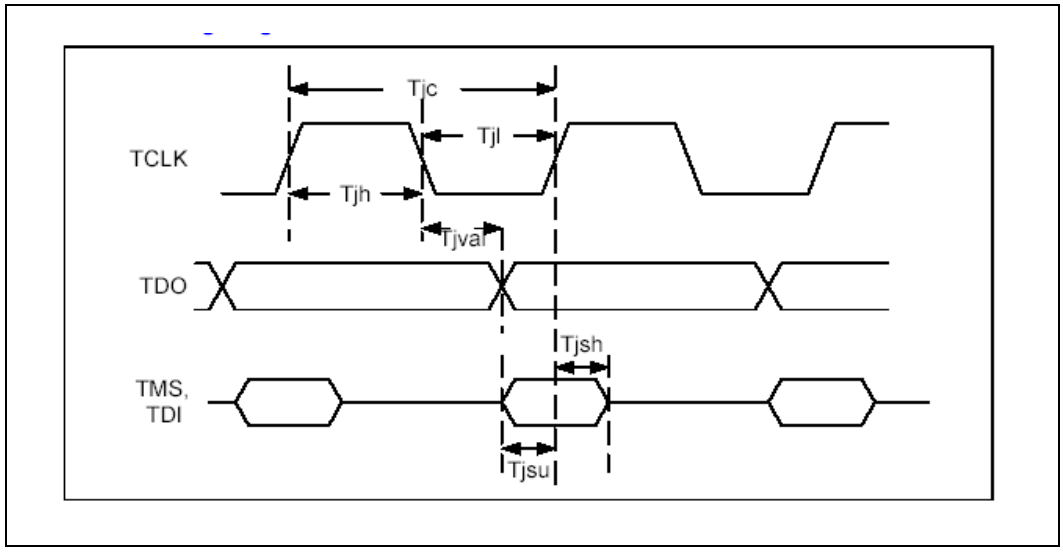


Table 42. JTAG AC Timing Parameters

Symbol	Parameter	Min	Max	Units
Tjc	TCLK cycle time	90	-	ns
Tjh	TCLK high time	0.4 x Tjc	0.6 x Tjc	ns
Tjl	TCLK low time	0.4 x Tjc	0.6 x Tjc	ns
Tjval	TCLK falling edge to TDO valid	-	25	ns
Tjsu	TMS/TDI setup to TCLK	20	-	ns
Tjsh	TMS/TDI hold from TCLK	5	-	ns

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6.11 System AC Timing Specification

Figure 47 and Table 43 illustrate the system reset AC timing specifications.

Figure 47. System Reset AC Timing

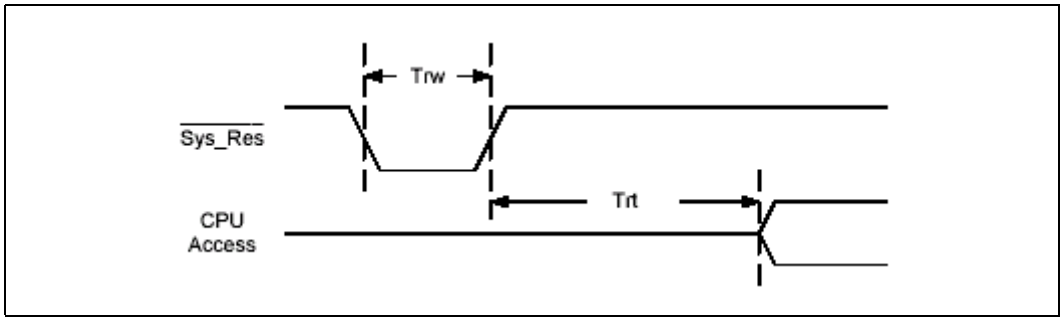

Table 43. System Reset AC Timing Parameters

Symbol	Parameter	Min	Max	Units
Trw	Reset pulse width	1.0	-	µs
Trt	Reset recovery time	200	-	µs

6.12 LED AC Timing Specification

Figure 48 and Table 44 provide the LED AC timing specifications.

Figure 48. LED AC Interface Timing

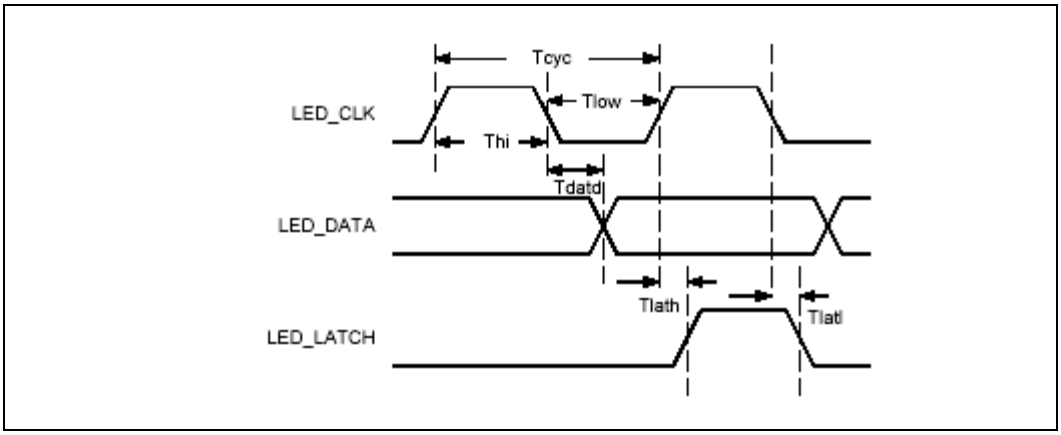

Table 44. LED Interface AC Timing Parameters

Symbol	Parameter	Min	Max	Units
Tcyc	LED_CLK cycle time	1.36	1.40	ms
Thi	LED_CLK high time	680	700	µs
Tlow	LED_CLK low time	680	700	µs
Tdatd	LED_CLK falling edge to LED_DATA valid	2	5	ns
Tlath	LED_CLK rising edge to LED_LATCH rising edge	690	700	µs
Tlatl	LED_CLK falling edge to LED_LATCH falling edge	690	700	µs

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Revision Number: 006
Revision Date: August 21, 2003

7.0 Register Set

The registers shown in this section provide access for configuration, alarm monitoring, and control of the chip. Table 45 shows the register map. The registers are listed by ascending address in the table.

7.1 Document Structure

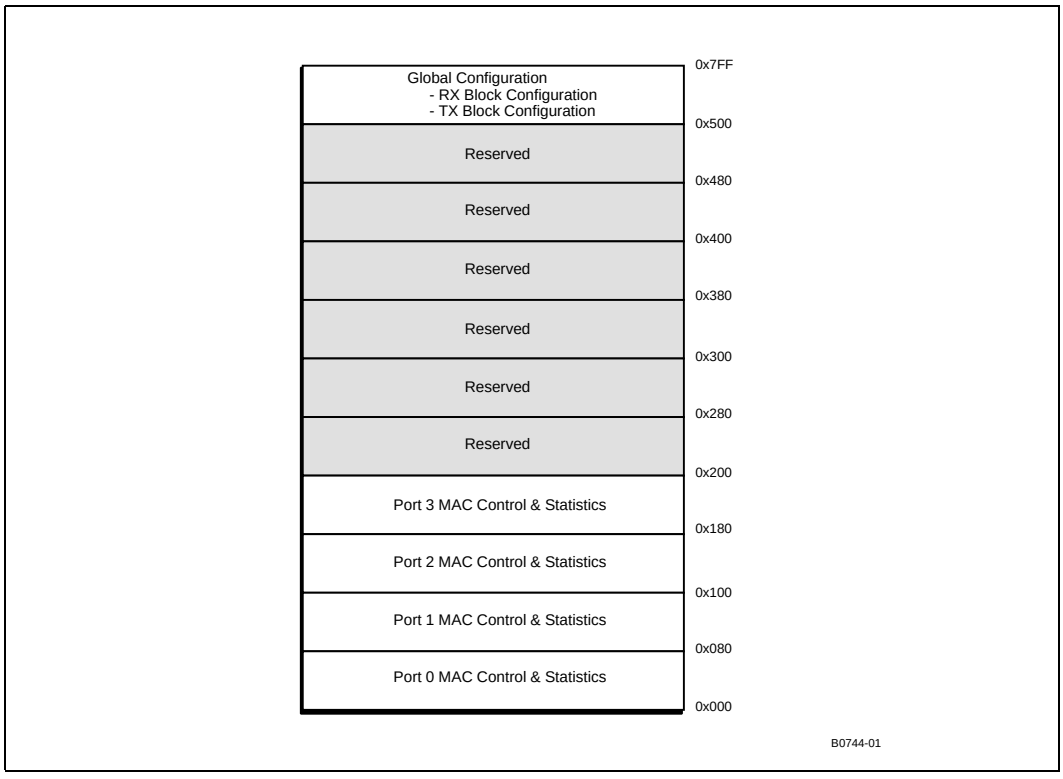
The following sections are structured to provide a general overview of the register map. Later sections provide detailed descriptions of each register segment or bit.

All registers are accessed and addressed as 32-bit doublewords. When accessed using 8- or 16-bit accesses, the microprocessor interface packs or unpacks the partial accesses into a 32-bit register value.

7.2 Graphical Representation

Figure 49 represents an overview of the IXF1104 global control status registers that are used to configure or report on all ports. All register locations shown in Figure 49 represent a 32-bit double word.

Figure 49. Memory Overview Diagram

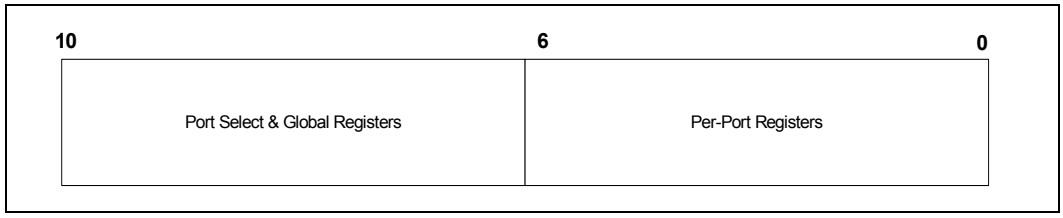


7.3 Per Port Registers

Section 7.4 covers all of the registers that are replicated in each port of the IXF1104. These registers perform an identical function in each port.

The address vector for the IXF1104 is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 50.

Figure 50. Register Overview Diagram



7.4 Register Map

Table 45 presents the IXF1104 memory map. Global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All IXF1104 registers are 32-bit registers.

Table 45. Intel® IXF1104 Register Map (Sheet 1 of 6)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
StationAddressLow	32	R/W	138	0x00
StationAddressHigh	32	R/W	138	0x01
DesiredDuplex	32	R/W	138	0x02
FDFCType	32	R/W	138	0x03
Reserved	32	R	–	0x04
CollisionDistance	32	R/W	139	0x05
CollisionThreshold	32	R/W	139	0x06
FCTxTimerValue	32	R/W	139	0x07
FDFCAddressLow	32	R/W	139	0x08
FDFCAddressHigh	32	R/W	139	0x09
IPGReceiveTime1	32	R/W	140	0x0A
IPGReceiveTime2	32	R/W	140	0x0B
IPGTransmitTime	32	R/W	140	0x0C
Reserved	–	RO	–	0x0D
PauseThreshold	32	R/W	140	0x0E
MaxFrameSize	32	R/W	140	0x0F
MacIFMode	32	R/W	141	0x10
FlushTX	32	R/W	141	0x11
FCEnable	32	R/W	142	0x12
FCBackPressureLength	32	R/W	142	0x13
ShortRuntsThreshold	32	R/W	143	0x14
DiscardUnknownControlFrame	32	R/W	143	0x15
RxConfigWord	32	RO	143	0x16
TxConfigWord	32	R/W	144	0x17
DiverseConfigWrite	32	R/W	145	0x18
PacketFilterControl	32	R/W	146	0x19
PortMulticastAddressLow	32	R/W	147	0x1A
PortMulticastAddressHigh	32	R/W	147	0x1B

Table 45. Intel® IXF1104 Register Map (Sheet 2 of 6)

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RxOctetsTotalOK	32	R	148	0x20
RxOctetsBAD	32	R	148	0x21
RxUCPckts	32	R	148	0x22
RxMCPkts	32	R	148	0x23
RxBCPkts	32	R	148	0x24
RxPkts64Octets	32	R	148	0x25
RxPkts65to127Octets	32	R	148	0x26
RxPkts128to255Octets	32	R	148	0x27
RxPkts256to511Octets	32	R	148	0x28
RxPkts512to1023Octets	32	R	148	0x29
RxPkts1024to1518Octets	32	R	148	0x2A
RxPkts1519toMaxOctets	32	R	148	0x2B
FCSErrors	32	R	148	0x2C
Tagged	32	R	148	0x2D
RxDataError	32	R	148	0x2E
Align Errors	32	R	148	0x2F
LongErrors	32	R	148	0x30
JabberErrors	32	R	148	0x31
PauseMacControlReceivedCounter	32	R	148	0x32
UnknownMacControlFrameCounter	32	R	148	0x33
VeryLongErrors	32	R	148	0x34
RuntErrors	32	R	148	0x35
ShortErrors	32	R	148	0x36
CarrierExtendError	32	R	148	0x37
SequenceErrors	32	R	148	0x38
SymbolErrors	32	R	148	0x39
MAC TX Statistics Registers (Port Index + Offset)				
OctetsTransmittedOK	32	R	152	0x40
OctetsTransmittedBad	32	R	152	0x41
TxUCPkts	32	R	152	0x42
TxMCPkts	32	R	152	0x43
TxBCPkts	32	R	152	0x44
TxPkts64Octets	32	R	152	0x45
TxPkts65to127Octets	32	R	152	0x46
TxPkts128to255Octets	32	R	152	0x47
TxPkts256to511Octets	32	R	152	0x48

Table 45. Intel® IXF1104 Register Map (Sheet 3 of 6)

Register	Bit Size	Mode[1]	Ref Page	Offset
TxPkts512to1023Octets	32	R	152	0x49
TxPkts1024to1518Octets	32	R	152	0x4A
TxPkts1519toMaxOctets	32	R	152	0x4B
DeferredTx	32	R	152	0x4C
TxTotalCollisions	32	R	152	0x4D
TxSingleCollisions	32	R	152	0x4E
TxMultipleCollisions	32	R	152	0x4F
TxLateCollisions	32	R	152	0x50
ExcessiveCollisionErrors	32	R	152	0x51
ExcessiveDeferralErrors	32	R	152	0x52
TxExcessiveLengthDrop	32	R	152	0x53
TxUnderrun	32	R	152	0x54
Tagged	32	R	152	0x55
CRCError	32	R	152	0x56
TxPauseFrames	32	R	152	0x57
FlowControlCollisionsSend	32	R	152	0x58
PHY Autoscan Registers (Port Index + Offset)				
PHY Control	32	RO	155	0x60
PHY Status	32	RO	156	0x61
PHY Identification 1	32	RO	157	0x62
PHY Identification 2	32	RO	157	0x63
Auto-Negotiation Advertisement	32	RO	158	0x64
Auto-Negotiation Link Partner Base Page Ability	32	RO	159	0x65
Auto-Negotiation Expansion	32	RO	160	0x66
Auto-Negotiation Next Page Transmit	32	RO	160	0x67
Reserved	32	RO	–	0x68 - 0x6F
Vendor Specific	32	RO	–	0x70 - 0x7F
Global Status and Configuration Registers (0x500 + Offset)				
Port Enable	32	R/W	161	0x500
Interface Mode	32	R/W	161	0x501
Link LED Enable	32	R/W	–	0x502
Reserved	32	RO		0x503 - 0x504
MAC Soft Reset	32	R/W	162	0x505
MDIO Soft Reset	32	R/W	163	0x506
Reserved	32	RO		0x507
Microprocessor Interface	32	R/W	163	0x508
LED Control	32	R/W	164	0x509

Table 45. Intel® IXF1104 Register Map (Sheet 4 of 6)

Register	Bit Size	Mode[1]	Ref Page	Offset
LED Flash Rate	32	R/W	164	0x50A
LED Fault Disable	32	R/W	164	0x50B
JTAG ID (Device Revision)	32	R	165	0x50C
RX FIFO Registers (0x580 + Offset)				
RX FIFO High Watermark Port 0	32	R/W	166	0x580
RX FIFO High Watermark Port 1	32	R/W	166	0x581
RX FIFO High Watermark Port 2	32	R/W	166	0x582
RX FIFO High Watermark Port 3	32	R/W	166	0x583
Reserved	32	RO	–	0x584 - 0x589
RX FIFO Low Watermark Port 0	32	R/W	167	0x58A
RX FIFO Low Watermark Port 1	32	R/W	167	0x58B
RX FIFO Low Watermark Port 2	32	R/W	167	0x58C
RX FIFO Low Watermark Port 3	32	R/W	167	0x58D
Reserved	32	RO	–	0x58E - 0x593
RX FIFO Number of Frames Removed Port 0	32	R	168	0x594
RX FIFO Number of Frames Removed Port 1	32	R	168	0x595
RX FIFO Number of Frames Removed Port 2	32	R	168	0x596
RX FIFO Number of Frames Removed Port 3	32	R	168	0x597
Reserved	32	RO	–	0x598 - 0x59D
RX FIFO Port Reset	32	R/W	168	0x59E
RX FIFO Errored Frame Drop Enable	32	R/W	169	0x59F
RX FIFO Overflow Event	32	R	169	0x5A0
RX FIFO Number of Error Packets Dropped Port 0	32	R	170	0x5A2
RX FIFO Number of Error Packets Dropped Port 1	32	R	170	0x5A3
RX FIFO Number of Error Packets Dropped Port 2	32	R	170	0x5A4
RX FIFO Number of Error Packets Dropped Port 3	32	R	170	0x5A5
Reserved	32	RO	–	0x5A6 - 0x5B1
RX FIFO Loopback Enable	32	R/W	170	0x5B2
RX FIFO Padding and CRC Strip Enable	32	R/W	170	0x5B3
Reserved	32	R	–	0x5B4 - 0x5B7
RX FIFO Jumbo Packet Size Port 0	32	R/W	171	0x5B8
RX FIFO Jumbo Packet Size Port 1	32	R/W	172	0x5B9
RX FIFO Jumbo Packet Size Port 2	32	R/W	172	0x5BA
RX FIFO Jumbo Packet Size Port 3	32	R/W	172	0x5BB
Reserved	32	R	–	0x5BC - 0x5BF
TX FIFO Registers (0x600 + Offset)				
TX FIFO High Watermark Port 0	32	R/W	173	0x600

Table 45. Intel® IXF1104 Register Map (Sheet 5 of 6)

Register	Bit Size	Mode[1]	Ref Page	Offset
TX FIFO High Watermark Port 1	32	R/W	173	0x601
TX FIFO High Watermark Port 2	32	R/W	173	0x602
TX FIFO High Watermark Port 3	32	R/W	173	0x603
Reserved	32	RO	–	0x604 - 0x609
TX FIFO Low Watermark Port 0	32	R/W	174	0x60A
TX FIFO Low Watermark Port 1	32	R/W	174	0x60B
TX FIFO Low Watermark Port 2	32	R/W	174	0x60C
TX FIFO Low Watermark Port 3	32	R/W	174	0x60D
Reserved	32	RO	–	0x60E - 0x613
TX FIFO MAC Threshold Port 0	32	R/W	175	0x614
TX FIFO MAC Threshold Port 1	32	R/W	175	0x615
TX FIFO MAC Threshold Port 2	32	R/W	175	0x616
TX FIFO MAC Threshold Port 3	32	R/W	175	0x617
Reserved	–	RO	–	0x618 - 0x61D
TX FIFO Overflow/Underflow Event/Out of Sequence	32	R	176	0x61E
Loop RX Data to TX FIFO	32	R/W	177	0x61F
TX FIFO Port Reset	32	R/W	177	0x620
TX FIFO Number of Frames Removed Port 0	32	R	178	0x621
TX FIFO Number of Frames Removed Port 1	32	R	178	0x622
TX FIFO Number of Frames Removed Port 2	32	R	178	0x623
TX FIFO Number of Frames Removed Port 3	32	R	178	0x624
TX FIFO Number of Dropped Packets Port 0	32	R	179	0x625
TX FIFO Number of Dropped Packets Port 1	32	R	179	0x626
TX FIFO Number of Dropped Packets Port 2	32	R	179	0x627
TX FIFO Number of Dropped Packets Port 3	32	R	179	0x628
Reserved	32	R	–	0x629 - 0x62C
TX FIFO Occupancy Counter for Port 0	32	R	179	0x62D
TX FIFO Occupancy Counter for Port 1	32	R	179	0x62E
TX FIFO Occupancy Counter for Port 2	32	R	179	0x62F
TX FIFO Occupancy Counter for Port 3	32	R	179	0x630
TX FIFO Mini Frame Size for MAC and Padding Enable Port 0 to 3	32	R/W	180	0x63E
Reserved	32	R	–	0x631 - 0x63E
MDIO Registers (0x680 + Offset)				
MDI Single Command	32	R/W	181	0x680
MDI Single Read and Write Data	32	R/W	181	0x681

Table 45. Intel® IXF1104 Register Map (Sheet 6 of 6)

Register	Bit Size	Mode[1]	Ref Page	Offset
Autoscan PHY Address Enable	32	R/W	182	0x682
MDI Control	32	R/W	182	0x683
SPI3 Registers (0x700 + Offset)				
SPI3 Transmit and Global Configuration	32	R/W	183	0x700
SPI3 Receive Configuration	32	R/W	184	0x701
Reserved	32	R	–	0x702 - 0x705
Address Parity Error Packet Drop Counter	32	R	185	0x70A
Reserved	32	R	–	0x70B - 0x716
SerDes Registers (0x780 + Offset)				
Tx and Rx ACDC Coupling Selection	32	R/W	186	0x780
Reserved	32	RO	–	0x781 - 0x783
Reserved	32	RO	–	0x784 - 0x792
Rx Signal Detect Level Ports 0-3	32	RO	186	0x793
Clock and IF Mode Change Enable Ports 0-3	32	R/W	187	0x794
Reserved	32	RO	–	0x795 - 0x798
GBIC Registers (0x780 + Offset)				
GBIC Status Ports 0-3	32	R	188	0x799
GBIC Control Ports 0-3	32	R/W	188	0x79A
I²C Control Ports 0-3	32	R/W	189	0x79B
Reserved	32	RO	–	0x79C - 0x79E
I²C Data Ports 0-3	32	R/W	189	0x79F

7.4.1 MAC Control Registers

Table 46 through Table 66 "Port Multicast Address Register (Addr: Port_Index +0x1A – +0x1B)" on page 147 provide details on the control and status registers associated with each MAC port. The register address is 'Port_index + 0x**', where the port index is set at any value from 0x0 through 0x5. All registers are 32-bit. The unused bits of the registers are read-only and are set permanently to zero.

Table 46. StationAddress Register (Addr: Port_Index +0x00 – +0x01)

Name	Description	Address	Type[1]	Default
StationAddressLow	**Source MAC address bit 31-0.** This address is inserted in the source address field when transmitting pause frames, and is also used to compare against unicast pause frames at the receiving side.	Port_Index + 0x00	R/W	0x0000000
StationAddressHigh	**Source MAC address bit 47-32.** This address is inserted in the source address field when transmitting pause frames, and is also used to compare against unicast pause frames at the receiving side. Bits 15:0 of this register are assigned to bits 47:32 of the station address.	Port_Index + 0x01	R/W	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 47. DesiredDuplex Register (Addr: Port_Index + 0x02)

Bit	Name	Description	Type[1]	Default
Register Description: Chooses between half-duplex and full-duplex operation mode. In copper mode, the bit PHY duplex in the "DiverseConfigWrite Register (Addr: Port_Index + 0x18)" on page 145 overrides this value when Force Duplex in that register is not set. In fiber mode, the matching duplex capability with the link partner, obtained through auto-negotiation, overrides this value when auto-negotiation is enabled.				0x00000001
31:1	Reserved	Reserved	R	0x00000000
0	Duplex Select	0 = Half-duplex 1 = Full-duplex **NOTE:** Half-duplex operation applies only to 10/100 Mbps speed on copper media. Gigabit speed on either media requires full-duplex.	R/W	1

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 48. FDFCType Register (Addr: Port_Index + 0x03)

Name	Description	Address	Type[1]	Default
FDFCType	This value is used to fill the Type field of the Transmitted Pause frames. Only bits 15:0 of this register are used.	Port_Index + 0x03	R/W	0x00008808

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 49. CollisionDistance Register (Addr: Port_Index + 0x05)

Name	Description	Address	Type[1]	Default
Collision Distance	This is a 10-bit value that sets the limit for late collision. Collisions happening at byte times beyond the configured value are considered to be late collisions. (Only valid in half-duplex).	Port_Index + 0x05	R/W	0x00000043

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 50. CollisionThreshold Register (Addr: Port_Index + 0x06)

Name	Description	Address	Type[1]	Default
Collision Threshold	This is a 4-bit value that sets the limit for excessive collisions. When the number of transmission attempts performed for a packet exceeds this value, it is considered to be an excessive collision and the frame is dropped. (Only valid in half-duplex).	Port_Index + 0x06	R/W	0x0000000F

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 51. FCTxTimerValue Register (Addr: Port_Index + 0x07)

Name	Description	Address	Type[1]	Default
FCTxTimerValue	The 16-bit pause length inserted in the flow control pause frame sent to the receiving station. The value is in 512-bit times.	Port_Index + 0x07	R/W	0x0000005E

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 52. FDFCAddress Register (Addr: Port_Index + 0x08 – + 0x09)

Name	Description	Address	Type[1]	Default
FDFCAddressLow	The lowest 32 bits of the 48-bit globally assigned multicast pause frame destination address.	Port_Index + 0x08	R/W	0xC2000001
FDFCAddressHigh	The highest 16 bits (47:32) of the globally assigned multicast pause frame destination address. The higher 16-bit address is derived from bits 15:0 of this register.	Port_Index + 0x09	R/W	0x00000180

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 53. IPG Receive and Transmit Time Register (Addr: Port_Index + 0x0A – + 0x0C)

Name	Description	Address	Type[1]	Default
IPGReceiveTime1	Sets the period inserted between packets to allow contention for access to the transmission medium in half-duplex mode.	Port_Index + 0x0A	R/W	0x00000008
IPGReceiveTime2	Sets the period inserted between packets to allow contention for access to the transmission medium in half-duplex mode.	Port_Index + 0x0B	R/W	0x00000007
IPGTransmitTime	This is a 10-bit value configuring IPG time for back-to-back transmissions.	Port_Index + 0x0C	R/W	0x00000008

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

NOTE: The IPG in bit times = (n + 4) x 8 [n = register value].

Table 54. PauseThreshold Register (Addr: Port_Index + 0x0E)

Name	Description	Address	Type[1]	Default
Pause Threshold	When a pause frame has been sent, an internal timer checks when the next pause frame must be scheduled for transmission to keep the link partner in pause mode (this is required only if the flow control has to be extended for one more session). The pause threshold value is a 16-bit value that sets the time in terms of 512-bit quantum after the previous pause frame when the next pause frame has to be sent. This ensures that the link partner is kept in pause mode continuously.	Port_Index + 0x0E	R/W	0x0000002F

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 55. MaxFrameSize Register (Addr: Port_Index + 0x0F)

Name	Description	Address	Type[1]	Default
MaxFrameSize	This is a 14-bit value configuring the maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. This value is excluding the 4-byte CRC in the transmit direction when CRC append is enabled in the MAC. Hence, this value has to be set four bytes less when CRC append is enabled in the MAC. The maximum frame size is internally adjusted by +4 if the frame is VLAN tagged.	Port_Index + 0x0F	R/W	0x000005EE

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 56. MAC Interface Mode and RGMII Speed Register (Addr: Port_Index + 0x10)

Bit	Name	Description	Type[1]	Default
Register Description – MACIFMode: Determines the MAC operation frequency and mode per port. Changes to the data setting of this register must be made in conjunction with the "Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)" to ensure a safe transition to a new operational mode.				0x00000003
31:3	Reserved	Reserved	R	0x00000000
2:0	Port Mode	These bits are used to define the clock mode and the RGMII/GMII mode of operation. 000 = Reserved 001 = Reserved 010 = GMII 1000 Mbps operation 011 = Reserved 100 = RGMII 10 Mbps operation 101 = RGMII 100 Mbps operation 11x = RGMII 1000 Mbps operation	R/W	011

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 57. Flush TX Register (Addr: Port_Index + 0x11)

Bit	Name	Description	Type[1]	Default
Register Description: Used to flush all TX data. It is used if all traffic sent to a port should be stopped.				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	FlushTX	This bit is used to flush all TX data. It is used if all the traffic sent to a port should be stopped.	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 58. FC Enable Register (Addr: Port_Index + 0x12)

Bit	Name	Description	Type[1]	Default
Register Description: Indicates which flow control mode is used for the RX and TX MAC.				0x00000007
31:3	Reserved	Reserved	R	0x00000000
2	TXHDFC	When TXHDFC is enabled (half-duplex mode only), the MAC generates deliberate collisions on incoming packets when the RX FIFO occupancy crosses a higher watermark (flow control). 0 = Disable TX half-duplex flow control 1 = Enable TX half-duplex flow control	R/W	1
1	TXFDFC	0 = Disable TX full-duplex flow control 1 = Enable TX full-duplex flow control	R/W	1
0	RXFDFC	0 = Disable RX full-duplex flow control 1 = Enable RX full-duplex flow control	R/W	1
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 59. FC Back Pressure Length Register (Addr: Port_Index + 0x13)

Name	Description	Address	Type[1]	Default
FCBackPressureLength	This register sets number the byte cycles for which the collision has to be applied. The 6-bit configuration holds the value in bytes, which applies to the minimum length/duration of back pressure in half-duplex mode. Flow control in the receive path is executed by deliberately colliding the incoming packets in half-duplex mode. Register bits 5:0 are used alone.	Port Add + 0x13	R/W	0x0000000C
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 60. Short Runts Threshold Register (Addr: Port_Index + 0x14)

Name	Description	Address	Type[1]	Default
ShortRunts Threshold	The 5-bit configuration holds the value in bytes, which applies to the threshold in determining between runts and short. The bits 4:0 of this register are alone used. A received packet is reported as a short packet when the length (excluding Preamble and SFD) is less than this value. A received packet is reported as a runt packet when the length (excluding Preamble and SFD) is equal to or greater than this value and less than 64-bytes. **NOTE:** This register is only relevant when the IXF1104 port is configured for copper operation (the line side interface is configured for either RGMII or GMII).	Port_Index + 0x14	R/W	0x00000008

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 61. Discard Unknown Control Frame Register (Addr: Port_Index + 0x15)

Bit	Name	Description	Type[1]	Default
Register Description: Discards or forwards unknown control frames. Known control frames are pause frames.				0x00000000
31:1	Reserved	Reserved	R	0x00000000
0	DiscardUnknown ControlFrame	0 = Forward unknown control frames 1 = Discard unknown control frames	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 62. RX Config Word Register Bit Definition (Addr: Port_Index + 0x16) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in fiber MAC only for auto-negotiation and to report the receive status. The contents of this register are the “config_reg” received from the link partner, as described in IEEE 802.3 2000 Edition, Section 37.2.1.				0x00000000
31:22	Reserved	Reserved	RO	0x000
31:22	Reserved	Reserved	RO	0x000
21	An_complete	Auto-negotiation complete. This bit remains cleared from the time auto-negotiation is reset until auto-negotiation reaches the “LINK_OK” state. It remains set until auto-negotiation is disabled or restarted. This bit is only valid if auto-negotiation is enabled.	RO	0
20	Rx Sync	0 = Loss of synchronization 1 = Bit synchronization. The bit remains Low until the register is read.	RO	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 62. RX Config Word Register Bit Definition (Addr: Port_Index + 0x16) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
19	RxConfig	0 = Receiving idle/data stream 1 = Receiving /C/ ordered sets	RO	0
18	ConfigChanged	0 = RxConfigWord has changed since last read 1 = RxConfigWord has not changed since last read. This bit remains High until the register is read.	R	0
17	InvalidWord	0 = Have not received an invalid symbol 1 = Have received an invalid symbol This bit remains High until the register is read.	RO	0
16	CarrierSense	0 = Device is not receiving idle characters; carrier sense is true. 1 = Device is receiving idle characters; carrier sense is false.	RO	0
15	NextPage	Next Page request	RO	0
14	Reserved	Reserved	RO	0
13:12	RemoteFault[1:0]	Remote fault definitions	RO	00
11:9	Reserved	Reserved	RO	000
8	AsymPause	Asym Pause. The ability to send pause frames.	RO	0
7	SymPause	Sym Pause. The ability to send and receive pause frames.	RO	0
6	HalfDuplex	Half-duplex	RO	0
5	FullDuplex	Full-duplex	RO	0
4:0	Reserved	Reserved	RO	0x0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 63. TXConfigWord Register (Addr: Port_Index + 0x17) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in fiber MAC for auto-negotiation only. The contents of this register are sent as the config_word. The contents of this register are the “config_reg” sent to the link partner, as described in IEEE 802.3 2000 Edition, subclause 37.2.1.				0x0001A0
31:16	Reserved	Reserved	RO	0x0000
15	NextPage	Next Page request	R/W	0
14	Reserved	Reserved	RO	0
13:12	RemoteFault[1:0]	Remote fault definitions	R/W	00
11:9	Reserved	Reserved	RO	000
8	AsymPause	Asym Pause. The ability to send pause frames.	R/W	1
7	SymPause	Sym Pause. The ability to send and receive pause frames.	R/W	1

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

NOTE: A value of 0x0 must be written to all reserved bits of the TX Config Word Register.

Table 63. TXConfigWord Register (Addr: Port_Index + 0x17) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
6	HalfDuplex	Half-duplex	R/W	1
5	FullDuplex	Full-duplex	R/W	1
4:0	Reserved	Reserved	RO	0x00

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

NOTE: A value of 0x0 must be written to all reserved bits of the TX Config Word Register.

Table 64. DiverseConfigWrite Register (Addr: Port_Index + 0x18)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains various configuration bits for general use.				0x00110D
31:8	Reserved	Reserved	RO	0x000000
31:8	Reserved	Reserved	RO	0x000000
7	pad_enable	0 = Normal operation 1 = Enable padding of undersized packets **Note:** Assertion of this bit results in the automatic addition of a CRC to the padded packet.	R/W	0
6	crc_add	0 = Normal operation 1 = Enable automatic CRC appending	R/W	0
5	autoneg_enable	Enable auto-negotiation (used for fiber operation only) to be performed by the hardware state machines in the MAC. The hardware auto-negotiation (AN) state machine controls the config words transmitted when this bit is set.	R/W	0
4	Reserved	Reserved	RO	0
3	phy_duplex	To set the duplex capability of the PHY device in Copper mode. 0 = Full-duplex 1 = Half-duplex	R/W	1
2	Force_duplex	Forces the duplex mode set in the "DesiredDuplex Register (Addr: Port_Index + 0x02)"). This overrides the value set in the PHY duplex register. This bit provides an option for the user to override the PHY duplex capability.	R/W	1
1	send_config	Send Configuration. This bit allows the software to perform auto-negotiation without involving the hardware state machines. When this bit is set, the transmitter sends the value configured in the "TXConfigWord Register (Addr: Port_Index + 0x17)".	R/W	0
0	Reserved	Reserved		

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 65. PacketFilterControl Register (Addr: Port_Index + 0x19)

Bit	Name	Description	Type[1]	Default
Register Description: This register allows for specific packet types to be marked for filtering and is used in conjunction with the RX FIFO Errored Frames Drop Enable register.				0x00000000
31:6	Reserved	Reserved		0
5	PassBad	This bit enables a global filter on frames with layer-2 errors. 0 = All bad frames are dropped. 1 = All bad frames are passed to the SPI3 Interface.	R/W	0
4	PauseFramePass	This bit enables a Global filter on Pause frames. 0 = All pause frames are dropped. 1 = All pause frames are passed to the SPI3 Interface.	R/W	0
3	VLANDropEn	This bit enables a global filter on VLAN frames. 0 = All VLAN frames are passed to the SPI3 Interface. 1 = All VLAN frames are dropped.	R/W	0
2	B/CastDropEn	This bit enables a Global filter on broadcast frames. 0 = All broadcast frames are passed to the SPI3 Interface. 1 = All broadcast frames are dropped.	R/W	0
1	M/CastMatchEn	This bit enables a filter on multicast frames. 0 = All muticast frames are good and passed to the SPI3 Interface. 1 = Only multicast frames with a destination address that matches the PortMulticastAddress are forwarded. All other muticast frames are dropped.	R/W	0
0	U/CastMatchEn	This bit enables a filter on unicast frames. 0 = All unicast frames are good and are passed to the SPI3 Interface. 1 = Only unicast frames with a Destination Address that matches the Station Address are forwarded. All other unicast frames are dropped.	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 66. Port Multicast Address Register (Addr: Port_Index +0x1A – +0x1B)

Name	Description	Address	Type*	Default
PortMulticast AddressLow	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	Port_Index + 0x1A	R/W	0x0000000
PortMulticast AddressHigh	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	Port_Index + 0x1B	R/W	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

7.4.2 MAC RX Statistics Register Overview

The MAC RX Statistics registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 67 covers the RX statistics for the four MAC ports. Port_Index is the port number (0, 1, 2, or 3).

Table 67. RX Statistics Registers (Addr: Port_Index + 0x20 – + 0x39) (Sheet 1 of 4)

Name	Description	Address	Type[1]	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the cyclic redundancy check (CRC). The initial preamble and Start of Frame Delimiter (SFD) bytes are not counted.	Port_Index + 0x20	R	0x00000000
RxOctetsBAD[2]	Counts the bytes received in all bad frames with legal size (frames with CRC error, alignment errors, or code violations), including all bytes from the destination MAC address to (and including) the CRC. The initial preamble and SFD bytes are not counted. Frames with illegal size do not add to this counter (shorts, runts, longs, jabbers, and very longs). **Note:** This register does not count octets on undersized received packets.	Port_Index + 0x21	R	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets). **Note:** This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting Management Information Base (MIB) information.	Port_Index + 0x22	R	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets) **Note:** This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	R	0x00000000
RxBCPkts	The total number of Broadcast packets received (excluding bad packets).	Port_Index + 0x24	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. When sending in large frames, the counters can only handle certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent upon where maxframesize is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

NOTE: This register is only relevant when the IXF1104 port is configured for copper-based operation (the line side interface is configured for RGMII or GMII based operation). The register will not increment when the IXF1104 port is configured for fiber operation using the SerDes interface.

Table 67. RX Statistics Registers (Addr: Port_Index + 0x20 – + 0x39) (Sheet 2 of 4)

Name	Description	Address	Type[1]	Default
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field.	Port_Index + 0x25	R	0x00000000
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were 65-127 octets in length. Incremented for tagged packets with a length of 65-127 bytes, including tag field.	Port_Index + 0x26	R	0x00000000
RxPkts128t0255 Octets	The total number of packets received (including bad packets) that were 128-255 octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field.	Port_Index + 0x27	R	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were 256-511 octets in length. Incremented for tagged packets with a length of 256-511 bytes, including tag field.	Port_Index + 0x28	R	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were 512-1023 octets in length. Incremented for tagged packets with a length of 512-1023 bytes, including tag field.	Port_Index + 0x29	R	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were 1024-1518 octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag.	Port_Index + 0x2A	R	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were greater than 1518 octets in length. Incremented for tagged packet with a length between 1526-max, including the tag.	Port_Index + 0x2B	R	0x00000000
FCSErrors	Number of frames received with legal size, but with wrong CRC field (also called Frame Check Sequence (FCS) field).	Port_Index + 0x2C	R	0x00000000
Tagged	Number of OK frames with VLAN tag. (Type field = 0x8100)	Port_Index + 0x2D	R	0x00000000
RxDataError	Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII).	Port_Index + 0x2E	R	0x00000000
AlignErrors	Frames with a legal frame size, but containing less than eight additional bits. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, then the frame is not counted but treated as an OK frame.	Port_Index + 0x2F	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. When sending in large frames, the counters can only handle certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent upon where maxframesize is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

NOTE: This register is only relevant when the IXF1104 port is configured for copper-based operation (the line side interface is configured for RGMII or GMII based operation). The register will not increment when the IXF1104 port is configured for fiber operation using the SerDes interface.

Table 67. RX Statistics Registers (Addr: Port_Index + 0x20 – + 0x39) (Sheet 3 of 4)

Name	Description	Address	Type[1]	Default
LongErrors[2]	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets. Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*maxframesize and 50,000 bits are not counted here, but they are counted in the VeryLongError counter.	Port_Index + 0x30	R	0x00000000
JabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*maxframesize and 50,000 bits are not counted here, but they are counted in the VeryLongError counter.	Port_Index + 0x31	R	0x00000000
PauseMacControl ReceivedCounter	Number of Pause MAC control frames received.	Port_Index + 0x32	R	0x00000000
UnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause).	Port_Index + 0x33	R	0x00000000
VeryLongErrors[2]	Frames bigger than the larger of 2*maxframesize and 50,000 bits	Port_Index + 0x34	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. When sending in large frames, the counters can only handle certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent upon where maxframesize is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

NOTE: This register is only relevant when the IXF1104 port is configured for copper-based operation (the line side interface is configured for RGMII or GMII based operation). The register will not increment when the IXF1104 port is configured for fiber operation using the SerDes interface.

Table 67. RX Statistics Registers (Addr: Port_Index + 0x20 – + 0x39) (Sheet 4 of 4)

Name	Description	Address	Type[1]	Default
RuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times, which corresponds to a 4-byte frame with a well-formed preamble and SFD. This is the shortest fragment and can be transmitted in case of a collision event on a half-duplex segment. This counter indicates fragment sizes, which is expected on half-duplex segments but not on full-duplex links, and the counter is only fully updated after receipt of a good frame following a fragment. **NOTE:** The ShortRuntsThreshold register controls the byte count used to determine the difference between Runts and Shorts and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames. **NOTE:** This counter is only valid when the selected port within the IXF1104 is operating in copper (RGMII or GMII) mode. The RuntError counter is not updated when the selected port within the IXF1104 is configured to operated in fiber (SerDes) mode.	Port_Index + 0x35	R	0x00000000
Short Errors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well-formed preamble and SFD. This counter indicates fragment sizes illegal in all modes and is only fully updated after reception of a good frame following a fragment. **NOTE:** This register is only relevant when the IXF1104 port is configured for copper operation (the line side interface is configured for either RGMII or GMII operation). This register will not increment when the IXF1104 port is configured for fiber operation using the SerDes interface.	Port_Index + 0x36	R	0x00000000
Carrier Extend Error	Not applicable.	Port_Index + 0x37	R	0x00000000
SequenceErrors	Records the number of sequencing errors that occur in fiber mode.	Port_Index + 0x38	R	0x00000000
SymbolErrors	Records the number of symbol errors encountered by the PHY.	Port_Index + 0x39	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. When sending in large frames, the counters can only handle certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*maxframesize, dependent upon where maxframesize is set. If maxframesize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1.

NOTE: This register is only relevant when the IXF1104 port is configured for copper-based operation (the line side interface is configured for RGMII or GMII based operation). The register will not increment when the IXF1104 port is configured for fiber operation using the SerDes interface.

7.4.3 MAC TX Statistics Register Overview

The MAC TX Statistics registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 68 covers all four MAC ports TX statistics. Port_Index is the port number (0, 1, 2, or 3).

Table 68. STAT-TX Registers (Addr: Port_Index +0x40 – +0x58) (Sheet 1 of 4)

Name	Description	Address	Type[1]	Default
OctetsTransmittedOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. Any initial collided transmission attempts before a successful frame transmission do not add to this counter.	Port_Index + 0x40	R	0x00000000
OctetsTransmittedBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. Late collision counted: The count is close to the actual number of bytes transmitted before the frame is discarded. Excessive collision counted: The count is close to the actual number of bytes transmitted before the frame is discarded. TX under-run counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded. TX CRC error counted: All bytes not sent with success are counted by this counter. Any initial collided transmission attempts before a successful frame transmission do not add to this counter.	Port_Index + 0x41	R	0x00000000
TxUCPkts	The total number of unicast packets transmitted (excluding bad packets).	Port_Index + 0x42	R	0x00000000
TxMCPkts	The total number of multicast packets transmitted (excluding bad packets). **NOTE:** This count includes pause control packets, which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 68. STAT-TX Registers (Addr: Port_Index +0x40 – +0x58) (Sheet 2 of 4)

Name	Description	Address	Type[1]	Default
TxBCPkts	The total number of broadcast packets transmitted (excluding bad packets).	Port_Index + 0x44	R	0x00000000
TxPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field.	Port_Index + 0x45	R	0x00000000
Txpkts65to127Octets	The total number of packets transmitted (including bad packets) that were 65-127 octets in length. Incremented for tagged packets with a length of 65-127 bytes, including tag field.	Port_Index + 0x46	R	0x00000000
Txpkts128to255Octets	The total number of packets transmitted (including bad packets) that were 128-255 octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field.	Port_Index + 0x47	R	0x00000000
Txpkts256to511Octets	The total number of packets transmitted (including bad packets) that were 256-511 octets in length. Incremented for tagged packets with a length of 256-511 bytes, including tag field.	Port_Index + 0x48	R	0x00000000
Txpkts512to1023Octets	The total number of packets transmitted (including bad packets) that were 512-1023 octets in length. Incremented for tagged packets with a length of 512-1023 bytes, including tag field.	Port_Index + 0x49	R	0x00000000
Txpkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were 1024-1518 octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag.	Port_Index + 0x4A	R	0x00000000
Txpkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were greater than 1518 octets in length. Incremented for tagged packet with a length between 1526-max, including the tag.	Port_Index + 0x4B	R	0x00000000
DeferredTx	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. TxTotalCollisions. **NOTE:** N/A - half-duplex only	Port_Index + 0x4C	R	0x00000000
TxTotal Collisions	Sum of all collision events. **NOTE:** N/A - half-duplex only	Port_Index + 0x4D	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 68. STAT-TX Registers (Addr: Port_Index +0x40 – +0x58) (Sheet 3 of 4)

Name	Description	Address	Type[1]	Default
TxSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. **NOTE:** N/A - half-duplex only	Port_Index + 0x4E	R	0x00000000
TxMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. **NOTE:** N/A - half-duplex only	Port_Index + 0x4F	R	0x00000000
TxLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. **NOTE:** N/A - half-duplex only	Port_Index + 0x50	R	0x00000000
ExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions **NOTE:** N/A - half-duplex only	Port_Index + 0x51	R	0x00000000
ExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize because of another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. **NOTE:** N/A - half-duplex only	Port_Index + 0x52	R	0x00000000
TxExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	R	0x00000000
TxUnderrun	Internal TX error that causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 68. STAT-TX Registers (Addr: Port_Index +0x40 – +0x58) (Sheet 4 of 4)

Name	Description	Address	Type[1]	Default
Tagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	R	0x00000000
CRCError	Number of frames transmitted with a legal size but with the wrong CRC field (also called FCS field).	Port_Index + 0x56	R	0x00000000
TxPauseFrames	Number of pause MAC frames transmitted.	Port_Index + 0x57	R	0x00000000
FlowControlCollisionsSend	Intentionally generates collisions to curb reception of incoming traffic due to insufficient memory available for additional frames. The port must be in half-duplex mode with flow control enabled. **NOTE:** To receive a correct statistic, a last frame may have to be transmitted after the last flow control collisions send. **NOTE:** N/A - half-duplex only	Port_Index + 0x58	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

7.4.4 PHY Autoscan Registers

Table 69. PHY Control Register (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15	Reset	PHY Soft Reset. Resets the PHY registers to their default value. This register bit self-clears after the reset is complete. 0 = Normal Operation 1 = PHY reset	RO	0
14	Loopback	0 = Disable loopback mode 1 = Enable loopback mode	RO	0
13	Speed Selection	0.6 (Speed<1> 0.13 (Speed<0>) 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps (manual mode not allowed) 11 = Reserved	RO	0[2]
12	Auto-Negotiation Enable	0 = Disable auto-negotiation process 1 = Enable auto-negotiation process This register bit must be enabled for 1000BASE-T operation.	RO	1
11	Power-Down	0 = Normal operation 1 = Power-down	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. This register is ignored if auto-negotiation is enabled.

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Table 69. PHY Control Register (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
10	Isolate	0 = 1 = Electrically isolate PHY from GMII	RO	0
9	Restart Auto-Negotiation	0 = Normal operation 1 = Restart auto-negotiation process	RO	0
8	Duplex Mode	0 = Half-duplex mode 1 = Full-duplex mode	RO	1[2]
7	Collision Test	0 = Disable COL signal test 1 = Enable COL signal test This register bit is ignored unless loopback is enabled (Register bit 0.14 = 1)	RO	0
6	Speed Selection 1000 Mbps	0.6 (Speed<1>) 0.13 (Speed<0>) 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps (manual mode now allowed) 11 = Reserved	RO	0[2]
5:0	Reserved	Reserved	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. This register is ignored if auto-negotiation is enabled.

Table 70. PHY Status Register (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0
15	100BASE-T4	0 = PHY not able to operate in 100BASE-T4 1 = PHY able to operate in 100BASE-T4	RO	0
14	100BASE-X Full-Duplex	0 = PHY not able to operate in 100BASE-X in full-duplex mode 1 = PHY able to operate in 100BASE-X in full-duplex mode	RO	1
13	100BASE-X Half-Duplex	0 = PHY not able to operate in 100BASE-X in half-duplex mode 1 = PHY able to operate in 100BASE-X in half-duplex mode	RO	1
12	10 Mbps Full-Duplex	0 = PHY not able to operate in 10 Mbps in full-duplex mode 1 = PHY able to operate in 10 Mbps in full-duplex mode	RO	1
11	10 Mbps Half-Duplex	0 = PHY not able to operate in 10 Mbps in half-duplex mode 1 = PHY able to operate in 10 Mbps in half-duplex mode	RO	1
10	100BASE-T2 Full-Duplex	0 = PHY not able to operate in 10BASE-T2 in full-duplex mode (not supported) 1 = PHY able to operate in 100BASE-T2 in full-duplex mode	RO	0

1. R = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 70. PHY Status Register (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
9	100BASE-T2 Half-Duplex	0 = PHY not able to operate in 100BASE-T2 in half-duplex mode 1 = PHY able to operate in 100BASE-T2 in half-duplex mode	RO	0
8	Extended Status	0 = No extended status information in Register 15 1 = Extended status information in Register 15	RO	1
7	Reserved	Reserved	RO	0
6	MF Preamble Suppression	0 = PHY will not accept management frames with preamble suppressed 1 = PHY will accept management frames with preamble suppressed	RO	0
5	Reserved	Reserved	RO	0
4	Remote Fault	0 = 1 = Remote fault condition detected	RO	0
3	Auto-Negotiation Ability	0 = 1 = PHY is able to perform auto-negotiation	RO	1
2	Link Status	0 = Link is down 1 = Link is up	RO	0
1	Jabber Detect	0 = Jabber condition not detected 1 = Jabber condition detected	RO	0
0	Extended Capability	0 = No extended register capabilities 1 = Extended register capabilities	RO	1
1. R = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 71. PHY Identification 1 Register

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0
15:0	PHY ID Number	The PHY identifier is composed of register bits 18.3 of the OUI (Organizationally Unique Identifier)	RO	h0013
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 72. PHY Identification 2 Register

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0
15:10	PHY ID Number	The PHY identifier is composed of register bits 24:19 of the OUI (Organizationally Unique Identifier)	RO	011110
9:4	Manufacturer's Model	Six bits containing the manufacturer's part number	RO	010000
3:0	Manufacturer's Revision Number	Four bits containing the manufacturer's revision number	RO	0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 73. Auto-Negotiation Advertisement Register

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0
15	Next Page	0 = 1 = Manual control of Next Page (software)	RO	0
14	Reserved	Reserved	RO	0
13	Remote Fault	0 = No remote fault 1 = Remote fault	RO	0
12	Reserved	Reserved	RO	0
11	ASM_DIR	Advertise Asymmetric Pause Direction register bit. This register bit is used in conjunction with Pause (Register bit 4.10) 0 = Link partner is not capable of asymmetric pause 1 = Link partner is capable of asymmetric pause	RO	1
10	Pause	Advertise to link partner that Pause operation is desired (IEEE 802.3x Standard)	RO	0
9	100BASE-T4	0 = 100BASE-T4 capability is not available 1 = 100BASE-T4 capability is available The IXF1104 does not support 100BASE-T4, but allows this register bit to be set to advertise in auto-negotiation sequence for 100BASE-T4 operation. If this capability is desired, an external 100BASE-T4 transceiver can be switched in.	RO	0
8	100BASE-TX Full-Duplex	0 = DTE is not 100BASE-TX, full-duplex mode capable 1 = DTE is 100BASE-TX, full-duplex mode capable	RO	1
7	100BASE-TX Half-Duplex	0 = DTE is not 100BASE-TX, half-duplex mode capable 1 = DTE is 100BASE-TX, half-duplex mode capable	RO	1
6	10BASE-T Full-Duplex	0 = DTE is not 10BASE-T, full-duplex mode capable 1 = DTE is 10BASE-T, full-duplex mode capable	RO	1
5	10BASE-T Half-Duplex	0 = DTE is not 10BASE-T, half-duplex mode capable 1 = DTE is 10BASE-T, half-duplex mode capable	RO	1
4:0	Selector Field, S[4:0]	00001 =IEEE 802.3 00010 =IEEE 802.9 ISLAN-16T 00000 =Reserved for future auto-negotiation development 11111 =Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted Setting this field to a value other than 00001 will most likely cause auto-negotiation to fail	RO	00001

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 74. Auto-Negotiation Link Partner Base Page Ability Register

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0
15	Next Page	0 = Link partner has no ability to send multiple pages 1 = Link partner has the ability to send multiple pages	RO	N/A
14	Acknowledge	0 = Link partner has not received Link Code Word from the IXF1104 1 = Link partner has received Link Code Word from the IXF1104	RO	N/A
13	Remote Fault	0 = No remote fault 1 = Remote fault	RO	N/A
12	Reserved	Reserved	RO	0
11	ASM_DIR	Advertise Asymmetric Pause Direction Register bit. This register bit is used in conjunction with Pause (Register bit 4.10) 0 = Link partner is not capable of asymmetric pause 1 = Link partner is capable of asymmetric pause	RO	1
10	Link Partner Pause	Link partner wants to utilize Pause Operation as defined in IEEE 802.3x Standard	RO	0
9	1000BASE-T4	0 = Link partner is not 100BASE-T4 capable 1 = Link partner is 100BASE-T4 capable	RO	0
8	100BASE-TX Full-Duplex	0 = Link partner is not 100BASE-TX, full-duplex mode capable 1 = Link partner is 100BASE-TX, full-duplex mode capable	RO	1
7	100BASE-TX Half-Duplex	0 = Link partner is not 100BASE-TX, half-duplex mode capable 1 = Link partner is 100BASE-TX, half-duplex mode capable	RO	1
6	10BASE-T Full-Duplex	0 = Link partner is not 10BASE-T, full-duplex mode capable 1 = Link partner is 10BASE-T, full-duplex mode capable	RO	1
5	10BASE-T Half-Duplex	0 = Link partner is not 10BASE-T, half-duplex mode capable 1 = Link partner is 10BASE-T, half-duplex mode capable	RO	1
4:0	Selector Field, S[4:0]	00001 =IEEE 802.3 00010 =IEEE 802.9 ISLAN-16T 00000 =Reserved for future auto-negotiation development 11111 =Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted Setting this field to a value other than 00001 will most likely cause auto-negotiation to fail	RO	00001

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 75. Auto-Negotiation Expansion Register

Bit	Name	Description	Type[1]	Default
31:6	Reserved	Reserved	RO	0
5	Base Page	This register bit indicates the status of the auto-negotiation variable, base page. It flags synchronization with the auto-negotiation state diagram allowing detection of interrupted links. This register bit is only used if Register bit 16.1 (alternate Next Page feature) is set. 0 = base_page = false 1 = base_page = true	RO	0
4	Parallel Detection Fault	0 = Parallel detection fault has not occurred 1 = Parallel detection fault has occurred	RO	0
3	Link Partner Next Page Able	0 = Link partner is not Next Page able 1 = Link partner is Next Page able	RO	0
2	Next Page Able	0 = Local device is not Next Page able 1 = Local device is Next Page able	RO	0
1	Page Received	Indicates that a new page has been received and the received code word has been loaded into Register 5 (base pages) or Register 8 (next pages) as specified in the EEE 802.3 Standard. This bit clears on Read.	RO	0
0	Link Partner Auto-Negotiation Able	0 = Link partner is not auto-negotiation able 1 = Link partner is auto-negotiation able	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 76. Auto-Negotiation Next Page Transmit Register

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0
15	Next Page (NP)	0 = Last page 1 = Additional Next Pages follow	RO	0
14	Reserved	Reserved	RO	0
13	Message Page (MP)	0 = Unformatted page 1 = Message page	RO	0
12	Acknowledge 2	0 = Cannot comply with message 1 = Complies with message	RO	0
11	Toggle (T)	0 = Previous value of the transmitted Link Code Word was logic one 1 = Previous value of the transmitted Link Code Word was logic zero	RO	0
10:0	Message/Unformatted Code Field	11-bit message code field See IEEE 802.3 Annex 28C	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

7.4.5 Global Status and Configuration Register Overview

Table 77 through Table 86 "JTAG ID Register (Addr: 0x50C)" on page 165 provide an overview for the Global Control and Status Registers.

Table 77. Port Enable Register (Addr: 0x500)

Bit	Name	Description	Type*	Default
Register Description: A control register for each port in the IXF1104. Port ID = bit position in the register. To make a port active, the bit must be set High. For example, Port 2 active implies a register value of 0000.0100. Setting the bit to 0 de-asserts the enable. The default state for this register is for all four ports to be active.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	0
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	0
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	0
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 78. Interface Mode Register (Addr: 0x501) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: If_Mode – Four bits of this register determines the PHY interface mode. 0 = Fiber 1 = Copper Changes to the data setting of this register must be made in conjunction with the "Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)" to ensure a safe transition to a new operational mode. The Enable clock mode change bit has to be set back to 1 after the configuration change takes effect.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Port 3 Interface Mode	0 = Fiber mode 1 = Copper mode	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 78. Interface Mode Register (Addr: 0x501) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	Port 2 Interface Mode	0 = Fiber mode 1 = Copper mode	R/W	0
1	Port 1 Interface Mode	0 = Fiber mode 1 = Copper mode	R/W	0
0	Port 0 Interface Mode	0 = Fiber mode 1 = Copper mode	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 79. Link LED Enable Register (Addr: 0x502)

Bit	Name	Description	Type[1]	Default
Register Description: Per port bit should be set upon detection of link to enable proper operation of the link LEDs.				0x00000000
31:4	Reserved	Reserved	R/W	0x00000
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 80. MAC Soft Reset Register (Addr: 0x505) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port software-activated reset of the MAC core.				0x00000000
31:4	Reserved	Reserved	R/W	0x00000
3	Software Reset MAC 3	Port 3 0 = Reset inactive 1 = Enable	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 80. MAC Soft Reset Register (Addr: 0x505) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	Software Reset MAC 2	Port 2 0 = Reset inactive 1 = Enable	R/W	0
1	Software Reset MAC 1	Port 1 0 = Reset inactive 1 = Enable	R/W	0
0	Software Reset MAC 0	Port 0 0 = Reset inactive 1 = Enable	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 81. MDIO Soft Reset Register (Addr: 0x506)

Bit	Name	Description	Type[1]	Default
Register Description: Software-activated reset of the MDIO module.				0x00000000
31:1	Reserved	Reserved	RO	0x00000000
0	Software MDIO Reset	0 = Reset inactive 1 = Reset active	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 82. Microprocessor Interface Register (Addr: 0x508)

Bit	Name	Description	Type[1]	Default
Register Description: Microprocessor Interface Endian select. Allows the user to select the Endian of the microprocessor interface to allow for various microprocessors to be connected to the IXF1104.				0x00000000
31:25	Reserved	Reserved	RO	0x00
24	Microprocessor Endian	Reserved in Little Endian Valid in Big endian 0 = Little Endian 1 = Big Endian	R/W	0
23:1	Reserved	Reserved	RO	0x000000
0	Microprocessor Endian Control	Reserved in Big Endian Valid in Little Endian 0 = Little Endian 1 = Big Endian	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write **NOTE:** Since the Endianess of the bus is unknown when writing to this register, write 0x01000001 to set the bit and 0x0 to clear it.				

Table 83. LED Control Register (Addr: 0x509)

Bit	Name	Description	Type[1]	Default
Register Description: Global selection of LED mode.				0x00000000
31:2	Reserved	Reserved	RO	0x00000000
1	LED Enable	0 = Disable LED Block 1 = Enable LED Block	R/W	0
0	LED Control	0 = Enable LED Mode 0 for use with SGS Thomson M5450 LED driver (Default) 1 = LED Mode 1 for use with Standard Octal Shift register	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 84. LED Flash Rate Register (Addr: 0x50A)

Bit	Name	Description	Type[1]	Default
Register Description: Global selection of LED flash rate.				0x00000000
31:3	Reserved	Reserved	RO	0x00000000
2:0	LED Flash Rate Control	000 =100 ms flash rate 001 =200 ms flash rate 010 =300 ms flash rate 011 = 400 ms flash rate 100 = 500 ms flash rate 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 85. LED Fault Disable Register (Addr: 0x50B) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port fault disable. Disables the LED flashing for local or remote faults.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	LED Port 3 Fault Control	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 85. LED Fault Disable Register (Addr: 0x50B) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	LED Port 2 Fault Control	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Port 1 Fault Control	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Port 0 Fault Control	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 86. JTAG ID Register (Addr: 0x50C)

Bit	Name	Description	Type[1]	Default
Register Description: The value of this register follows the same scheme as the device identification register found in the IEEE 1149.1 specification. The upper four bits correspond to silicon stepping. The next 16 bits store a Part ID Number. The next 11 bits contain a JEDEC manufacturer ID. Bit zero = 1 if the chip is the first in a stack. The encoding scheme used for the Product ID field is implementation-dependent.				0x10450013
31:28	Version	Version	RO	0001^{2}
27:12	Part ID	Part ID	RO	0000010001 010000
11:8	JEDEC Continuation Characters	JEDEC Continuation Characters	RO	0000
7:1	JEDEC ID	JEDEC ID	RO	0001001
0	Fixed	Fixed	RO	1

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. These bits vary with stepping.

7.4.6 RX FIFO Register Overview

Table 87 through Table 94 provide an overview of the RX FIFO registers, which include the RX FIFO High and Low watermarks.

Table 87. RX FIFO High Watermark Register Ports 0 - 3 (Addr: 0x580 – 0x583)

Name	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 0	**High watermark for RX FIFO port 0.** The default value of 0x0E6 represents 230 eight-byte locations. This equates to 1840 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO exceeds the high watermark, flow control is automatically initiated within the MAC to avoid an overflow condition.	0x580	R/W	0x0E6
RX FIFO High Watermark Port 1	**High watermark for RX FIFO port 1.** The default value of 0x0E6 represents 230 eight-byte locations. This equates to 1840 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO exceeds the high watermark, flow control is automatically initiated within the MAC to avoid an overflow condition.	0x581	R/W	0x0E6
RX FIFO High Watermark Port 2	**High watermark for RX FIFO port 2.** The default value of 0x0E6 represents 230 eight-byte locations. This equates to 1840 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO exceeds the high watermark, flow control is automatically initiated within the MAC to avoid an overflow condition.	0x582	R/W	0x0E6
RX FIFO High Watermark Port 3	**High watermark for RX FIFO port 3.** The default value of 0x0E6 represents 230 eight-byte locations. This equates to 1840 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO exceeds the high watermark, flow control is automatically initiated within the MAC to avoid an overflow condition.	0x583	R/W	0x0E6

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 88. RX FIFO High Watermark Register Ports 0 - 3 Bit Definitions

Bit	Name	Description	Type[1]	Default
31:12	Reserved	Reserved	RO	0x00000
11: 0	RX FIFO High Watermark	The high water mark value. **NOTE:** Must be greater than the Low Watermark/ jumbo frame size.	R/W	0x0E6

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 89. RXFIFO Low Watermark Register Ports 0 - 3 (Addr: 0x58A – 0x58D)

Name	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 0	**Low watermark for RX FIFO port 0.** The default value of 0x072 represents 114 eight-byte locations. This equates to 912 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO falls below the Low Watermark, flow control is automatically de-asserted within the MAC to allow more line-side data to be captured by the RX FIFO.	0x58A	R/W	0x072
RX FIFO Low Watermark Port 1	**Low watermark for RX FIFO port 1.** The default value of 0x072 represents 114 eight-byte locations. This equates to 912 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO falls below the Low Watermark, flow control is automatically de-asserted within the MAC to allow more line-side data to be captured by the RX FIFO.	0x58B	R/W	0x072
RX FIFO Low Watermark Port 2	**Low watermark for RX FIFO port 2.** The default value of 0x072 represents 114 eight-byte locations. This equates to 912 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO falls below the Low Watermark, flow control is automatically de-asserted within the MAC to allow more line-side data to be captured by the RX FIFO.	0x58C	R/W	0x072
RX FIFO Low Watermark Port 3	**Low watermark for RX FIFO port 3.** The default value of 0x072 represents 114 eight-byte locations. This equates to 912 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the RX FIFO falls below the Low Watermark, flow control is automatically de-asserted within the MAC to allow more line-side data to be captured by the RX FIFO.	0x58D	R/W	0x072

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 90. RX FIFO Low Watermark Register Port 0 to 3 Bit Definitions

Bit	Name	Description	Type[1]	Default
31:12	Reserved	Reserved	RO	0x00000
11: 0	RX FIFO Low Watermark	The High Watermark value **Note:** Should never be greater or equal to the High Watermark.	R/W	0x072

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 91. RX FIFO Number of Frames Removed Register Ports 0 to 3 (Addr: 0x594 – 0x597)

Name	Description	Address	Type[1]	Default
Number of frames removed on port 0	When RX FIFO on port 0 becomes full or reset, the number of frames lost/removed on this port are shown in this register. This register gets updated after one cycle of sw_reset is applied.	0x594	R	0x00000000
Number of frames removed on port 1	When RX FIFO on port 1 becomes full or reset, the number of frames lost/removed on this port are shown in this register. This register gets updated after one cycle of sw_reset is applied.	0x595	R	0x00000000
Number of frames removed on port 2	When RX FIFO on port 2 becomes full or reset, the number of frames lost/removed on this port are shown in this register. This register gets updated after one cycle of sw_reset is applied.	0x596	R	0x00000000
Number of frames removed on port 3	When RX FIFO on port 3 becomes full or reset, the number of frames lost/removed on this port are shown in this register. This register gets updated after one cycle of sw_reset is applied.	0x597	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 92. RX FIFO Port Reset Register (Addr: 0x59E)

Bit	Name	Description	Type[1]	Default
Register Description: The soft reset register for each port in the RX block. Port ID = bit position in the register. To make the reset active, the bit must be set High. For example, reset of port 1 implies register value = 0000_0018. Setting the bit to 0 de-asserts the reset.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Reset RX FIFO for Port 3	Port 3 0 = De-assert reset 1 = Reset	R/W	0
2	Reset RX FIFO for Port 2	Port 2 0 = De-assert reset 1 = Reset	R/W	0
1	Reset RX FIFO for Port 1	Port 1 0 = De-assert reset 1 = Reset	R/W	0
0	Reset RX FIFO for Port 0	Port 0 0 = De-assert reset 1 = Reset	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 93. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used to configure dropping of error packets (DEBAD). **Note:** Jumbo packets are not dropped.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Rx FIFO Drop Error Frames Enable Port 3	This bit is used in conjunction with MAC filter bits. This allows the user to select whether the errored packets are to be dropped or not. 1 = Frame Drop Enable 0 = Frame Drop Disable	R/W	0
2	Rx FIFO Drop Error Frames Enable Port 2	This bit is used in conjunction with MAC filter bits. This allows the user to select whether the errored packets are to be dropped or not. 1 = Frame Drop Enable 0 = Frame Drop Disable	R/W	0
1	Rx FIFO Drop Error Frames Enable Port 1	This bit is used in conjunction with MAC filter bits. This allows the user to select whether the errored packets are to be dropped or not. 1 = Frame Drop Enable 0 = Frame Drop Disable	R/W	0
0	Rx FIFO Drop Error Frames Enable Port 0	This bit is used in conjunction with MAC filter bits. This allows the user to select whether the errored packets are to be dropped or not. 1 = Frame Drop Enable 0 = Frame Drop Disable	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 94. RX FIFO Overflow Event Register (Addr: 0x5A0)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a status if a FIFO-full situation has occurred—for example, a FIFO overflow. The bit position equals the port number. This register is cleared on Read.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	RX FIFO Overflow Event on Port 3	Port 3 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
2	RX FIFO Overflow Event on Port 2	Port 2 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
1	RX FIFO Overflow Event on Port 1	Port 1 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
0	RX FIFO Overflow Event on Port 0	Port 0 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 95. RX FIFO Dropped Packet Counter for Ports 0 to 3 Register (Addr: 0x5A2 - 0x5A5)

Name	Description	Address	Type	Default
Number of dropped packets on Port 0	This register gives the number of packets dropped by the RX FIFO 0, due to various errors. This register is cleared on Read.	0x5A2	R	0x00000000
Number of dropped packets on Port 1	This register gives the number of packets dropped by the RX FIFO 1, due to various errors. This register is cleared on Read.	0x5A3	R	0x00000000
Number of dropped packets on Port 2	This register gives the number of packets dropped by the RX FIFO 2, due to various errors. This register is cleared on Read.	0x5A4	R	0x00000000
Number of dropped packets on Port 3	This register gives the number of packets dropped by the RX FIFO 3, due to various errors. This register is cleared on Read.	0x5A5	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 96. RX FIFO Loopback Enable for Ports 0 - 3 Register (Addr: 0x5B2)

Bit	Name	Description	Type[1]	Default
Register Description: Enables TX SPI3 Port to pump packets into the RX_FIFO instead of into the TX FIFO.				0x00000000
31:12	Reserved	Reserved	RO	0x00000
11	Loopback enable for Port 3	0 = Disabled 1 = Enabled	R/W	0x0
10	Loopback enable for Port 2	0 = Disabled 1 = Enabled	R/W	0x0
9	Loopback enable for Port 1	0 = Disabled 1 = Enabled	R/W	0x0
8	Loopback enable for Port 0	0 = Disabled 1 = Enabled	R/W	0x0
7:0	Reserved	Reserved	RO	0x00

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 97. RX FIFO Padding and CRC Strip Enable Register (Addr: 0x5B3) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: This control register enables to pre-pend every packet with two extra bytes and also enables the CRC stripping of a packet.				0x00000000
31:8	Reserved	Reserved	RO	0x000000
7	CRC Stripping Enable for Port 3	CRC stripping is enabled for Port 3. 0 = Disabled 1 = Enabled	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. Pre-pending should not be enabled in loopback mode.

Table 97. RX FIFO Padding and CRC Strip Enable Register (Addr: 0x5B3) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
6	CRC Stripping Enable for Port 2	CRC stripping is enabled for Port 2. 0 = Disabled 1 = Enabled	R/W	0
5	CRC Stripping Enable for Port 1	CRC stripping is enabled for Port 1. 0 = Disabled 1 = Enabled	R/W	0
4	CRC Stripping Enable for Port 0	CRC stripping is enabled for Port 0. 0 = Pre-pending Disabled 1 = Pre-pending Enabled	R/W	0
3	Pre-pending Enable[1] Port 3	Enables pre-pending of two bytes at the start of every packet – Port 3. 0 = Disabled 1 = Enabled	R/W	0
2	Pre-pending Enable[1] Port 2	Enables pre-pending of two bytes at the start of every packet – Port 2. 0 = Disabled 1 = Enabled	R/W	0
1	Pre-pending Enable[1] Port 1	Enables pre-pending of two bytes at the start of every packet – Port 1. 0 = Disabled 1 = Enabled	R/W	0
0	Pre-pending Enable[1] Port 0	Enables pre-pending of two bytes at the start of every packet – Port 0. 0 = Disabled 1 = Enabled	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write
2. Pre-pending should not be enabled in loopback mode.

Table 98. RX FIFO Jumbo Packet Size 0-3 Register (Addr: 0x5B8 – 0x5BB

Name	Description	Address	Type	Default
Jumbo Packet size for port_0	Jumbo Packet size for port 0 in 8 byte location	0x5B8	R/W	0x000000BE
Jumbo Packet size for port_1	Jumbo Packet size for port 1 in 8 byte location	0x5B9	R/W	0x000000BE
Jumbo Packet size for port_2	Jumbo Packet size for port 2 in 8 byte location	0x5BA	R/W	0x000000BE
Jumbo Packet size for port_3	Jumbo Packet size for port 3 in 8 byte location	0x5BB	R/W	0x000000BE

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 99. RX FIFO Jumbo Packet Size Port 0 Register Bit Definitions (Addr: 0x5B8)

Bit	Name	Description	Type	Default
31:12	Reserved	Reserved	RO	0x00000
11:0	Jumbo Packet Size	Jumbo Packet size for port 0. This must be less than the FIFO high water mark.	R/W	0x0BE
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 100. RX FIFO Jumbo Packet Size Port 1 Register Bit Definitions (Addr: 0x5B9)

Bit	Name	Description	Type	Default
31:12	Reserved	Reserved	RO	0x00000
11:0	Jumbo Packet Size	Jumbo Packet size for port 1. This must be less than the FIFO high water mark.	R/W	0x0BE
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 101. RX FIFO Jumbo Packet Size Port 2 Register Bit Definitions (Addr: 0x5BA)

Bit	Name	Description	Type	Default
31:12	Reserved	Reserved	RO	0x00000
11:0	Jumbo Packet Size	Jumbo Packet size for port 2. This must be less than the FIFO high water mark.	R/W	0x0BE
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 102. RX FIFO Jumbo Packet Size Port 3 Register Bit Definitions (Addr: 0x5BB)

Bit	Name	Description	Type	Default
31:12	Reserved	Reserved	RO	0x00000
11:0	Jumbo Packet Size	Jumbo Packet size for port 3. This must be less than the FIFO high water mark.	R/W	0x0BE
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

7.4.7 TX FIFO Register Overview

Table 103 through Table 110 provide an overview of the TX FIFO registers, which include the TX FIFO High and Low watermark.

Table 103. TX FIFO High Watermark Register Ports 0 to 3 (Addr: 0x600 – 0x603)

Name	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 0	**High watermark for TX FIFO Port 0.** The default value of 0x3E0 represents 992 8-byte locations. This equates to 7936 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO exceeds the high watermark, flow control is automatically initiated on the SPI3 interface to request that the switch fabric stops data transfers to avoid an overflow condition.	0x600	R/W	0x000003E0
TX FIFO High Watermark Port 1	**High watermark for TX FIFO Port 1.** The default value of 0x3E0 represents 992 8-byte locations. This equates to 7936 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO exceeds the high watermark, flow control is automatically initiated on the SPI3 interface to request that the switch fabric stops data transfers to avoid an overflow condition.	0x601	R/W	0x000003E0
TX FIFO High Watermark Port 2	**High watermark for TX FIFO Port 2.** The default value of 0x3E0 represents 992 8-byte locations. This equates to 7936 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO exceeds the high watermark, flow control is automatically initiated on the SPI3 interface to request that the switch fabric stops data transfers to avoid an overflow condition.	0x602	R/W	0x000003E0
TX FIFO High Watermark Port 3	**High watermark for TX FIFO Port 3.** The default value of 0x3E0 represents 992 8-byte locations. This equates to 7936 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO exceeds the high watermark, flow control is automatically initiated on the SPI3 interface to request that the switch fabric stops data transfers to avoid an overflow condition.	0x603	R/W	0x000003E0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 104. TX FIFO Low Watermark Register Ports 0 to 3 (Addr: 0x60A – 0x60D)

Name	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 0	**Low watermark for TX FIFO Port 0.** The default value of 0x0D0 represents 208 8-byte locations. This equates to 1664 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO falls below the low watermark, flow control is automatically de-asserted on the SPI3 interface to allow further data to be sent by the switch fabric to the IXF1104.	0x60A	R/W	0x000000D0
TX FIFO Low Watermark Port 1	**Low watermark for TX FIFO Port 1.** The default value of 0x0D0 represents 208 8-byte locations. This equates to 1664 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO falls below the low watermark, flow control is automatically de-asserted on the SPI3 interface to allow further data to be sent by the switch fabric to the IXF1104.	0x60B	R/W	0x000000D0
TX FIFO Low Watermark Port 2	**Low watermark for TX FIFO Port 2.** The default value of 0x0D0 represents 208 8-byte locations. This equates to 1664 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO falls below the low watermark, flow control is automatically de-asserted on the SPI3 interface to allow further data to be sent by the switch fabric to the IXF1104.	0x60C	R/W	0x000000D0
TX FIFO Low Watermark Port 3	**Low watermark for TX FIFO Port 3.** The default value of 0x0D0 represents 208 8-byte locations. This equates to 1664 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO falls below the low watermark, flow control is automatically de-asserted on the SPI3 interface to allow further data to be sent by the switch fabric to the IXF1104.	0x60D	R/W	0x000000D0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 105. TX FIFO MAC Threshold Register Ports 0 to 3 (Addr: 0x614 – 0x617)

Name	Description	Address	Type[1]	Default
TX FIFO MAC Threshold Port 0	**MAC threshold for TX FIFO Port 0.** The default value of 0x1BE represents 446 8-byte locations. This equates to 3568 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO reaches this threshold, data is forwarded to the MAC core and line-side interfaces for onward transmission. By setting the threshold to an appropriate value, the user can configure the TX FIFO to operate in a “cut-through” mode rather than the default “store and forward” operation mode.	0x614	R/W	0x000001BE
TX FIFO MAC Threshold Port 1	**MAC threshold for TX FIFO Port 1.** The default value of 0x1BE represents 446 8-byte locations. This equates to 3568 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO reaches this threshold, data is forwarded to the MAC core and line-side interfaces for onward transmission. By setting the threshold to an appropriate value, the user can configure the TX FIFO to operate in a “cut-through” mode rather than the default “store and forward” operation mode.	0x615	R/W	0x000001BE
TX FIFO MAC Threshold Port 2	**MAC threshold for TX FIFO Port 2.** The default value of 0x1BE represents 446 8-byte locations. This equates to 3568 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO reaches this threshold, data is forwarded to the MAC core and line-side interfaces for onward transmission. By setting the threshold to an appropriate value, the user can configure the TX FIFO to operate in a “cut-through” mode rather than the default “store and forward” operation mode.	0x616	R/W	0x000001BE
TX FIFO MAC Threshold Port 3	**MAC threshold for TX FIFO Port 3.** The default value of 0x1BE represents 446 8-byte locations. This equates to 3568 bytes of data. A unit entry in this register equates to 8 bytes of data. When the amount of data stored in the TX FIFO reaches this threshold, data is forwarded to the MAC core and line-side interfaces for onward transmission. By setting the threshold to an appropriate value, the user can configure the TX FIFO to operate in a “cut-through” mode rather than the default “store and forward” operation mode.	0x617	R/W	0x000001BE

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 106. TX FIFO Overflow/Underflow/Out of Sequence Event Register Bit Definition (Addr: 0x61E) (Sheet 1 of 2)

Bit	Name	Description	Type[1]	Default
Register Description: TX FIFO Out of Sequence Event: These register bits provide status information, and indicate if out-of-sequence data has been received. The bit position equals the port number + 8. These bits are cleared on Read.				0x0
Register Description: TX FIFO Underflow Event: This register provides a status that a FIFO Empty situation has occurred (for example, a FIFO under-run). The bit position equals the port number + 4. This register is cleared on Read.				0x0
Register Description: TX FIFO Overflow Event: This register provides a status that a FIFO full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x0
31:12	Reserved	Reserved	RO	0x00000
11	FOSE3	Port 3 0 = FIFO out of sequence event did not occur 1 = FIFO out of sequence event occurred	R	0
10	FOSE2	Port 2 0 = FIFO out of sequence event did not occur 1 = FIFO out of sequence event occurred	R	0
9	FOSE1	Port 1 0 = FIFO out of sequence event did not occur 1 = FIFO out of sequence event occurred	R	0
8	FOSE0	Port 0 0 = FIFO out of sequence event did not occur 1 = FIFO out of sequence event occurred	R	0
7	FUE3	Port 3 0 = FIFO underflow event did not occur 1 = FIFO underflow event occurred	R	0
6	FUE2	Port 2 0 = FIFO underflow event did not occur 1 = FIFO underflow event occurred	R	0
5	FUE1	Port 1 0 = FIFO underflow event did not occur 1 = FIFO underflow event occurred	R	0
4	FUE0	Port 0 0 = FIFO underflow event did not occur 1 = FIFO underflow event occurred	R	0
3	FOE3	Port 3 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 106. TX FIFO Overflow/Underflow/Out of Sequence Event Register Bit Definition (Addr: 0x61E) (Sheet 2 of 2)

Bit	Name	Description	Type[1]	Default
2	FOE2	Port 2 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
1	FOE1	Port 1 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
0	FOE0	Port 0 0 = FIFO overflow event did not occur 1 = FIFO overflow event occurred	R	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 107. Loop RX Data to TX FIFO Register Ports 0 - 3 (Addr: 0x61F)

Bit	Name	Description	Type[1]	Default
Register Description: This register enables data received from the line-side receive interface through the MAC to be sent to the TX FIFO and back to the line-side transmit interface.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Port 3 Loop RX data to TX FIFO	0 = Disable loopback 1 = Enable loopback	R/W	0
2	Port 2 Loop RX data to TX FIFO	0 = Disable loopback 1 = Enable loopback	R/W	0
1	Port 1 Loop RX data to TX FIFO	0 = Disable loopback 1 = Enable loopback	R/W	0
0	Port 0 Loop RX data to TX FIFO	0 = Disable loopback 1 = Enable loopback	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 108. TX FIFO Port Reset Register (Addr: 0x620)

Bit	Name	Description	Type[1]	Default
Register Description: This is a port reset register for each port in the TX block. Port ID = bit position in the register. To make the port active, the bit must be set to Low. (For example, reset of Port 3 implies register value = 1000, setting the bit to 1 asserts the port reset).				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Port 3 Reset	Port 3 0 = De-assert Reset 1 = Assert Reset	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 108. TX FIFO Port Reset Register (Addr: 0x620) (Continued)

Bit	Name	Description	Type[1]	Default
2	Port 2 Reset	Port 2 0 = De-assert Reset 1 = Assert Reset	R/W	0
1	Port 1 Reset	Port 1 0 = De-assert Reset 1 = Assert Reset	R/W	0
0	Port 0 Reset	Port 0 0 = De-assert Reset 1 = Assert Reset	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 109. TX FIFO Number of Frames Removed Register Ports 0-3 (Addr: 0x621 – 0x624)

Name	Description	Address	Type*	Default
TX FIFO number of frames removed on Port 0	When TX FIFO on Port 0 becomes full or reset, the number of frames lost or removed on this port is shown in this register. This register is cleared on Read.	0x621	R	0x00000000
TX FIFO number of frames removed on Port 1	When TX FIFO on Port 1 becomes full or reset, the number of frames lost or removed on this port is shown in this register. This register is cleared on Read.	0x622	R	0x00000000
TX FIFO number of frames removed on Port 2	When TX FIFO on Port 2 becomes full or reset, the number of frames lost or removed on this port is shown in this register. This register is cleared on Read.	0x623	R	0x00000000
TX FIFO number of frames removed on Port 3	When TX FIFO on Port 3 becomes full or reset, the number of frames lost or removed on this port is shown in this register. This register is cleared on Read.	0x624	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 110. TX FIFO Number of Dropped Packets Register Ports 0-3 (Addr: 0x625 – 0x629)

Name	Description	Address	Type*	Default
TX FIFO number of dropped packets on Port 0	This register provides the number of packets dropped by the TX FIFO due to the following: Data Parity Errors Short SOPs Small Packets (9-14 bytes) **NOTE:** This register is cleared on Read.	0x625	R	0x00000000
TX FIFO number of dropped packets on Port 1	This register provides the number of packets dropped by the TX FIFO due to the following: Data Parity Errors Short SOPs Small Packets (9-14 bytes) **NOTE:** This register is cleared on Read.	0x626	R	0x00000000
TX FIFO number of dropped packets on Port 2	This register provides the number of packets dropped by the TX FIFO due to the following: Data Parity Errors Short SOPs Small Packets (9-14 bytes) **NOTE:** This register is cleared on Read.	0x627	R	0x00000000
TX FIFO number of dropped packets on Port 3	This register provides the number of packets dropped by the TX FIFO due to the following: Data Parity Errors Short SOPs Small Packets (9-14 bytes) **NOTE:** This register is cleared on Read.	0x628	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 111. TX FIFO Occupancy Counter for Ports 0 - 3 Registers (Addr: 0x62D – 0x630)

Name	Description	Address	Type	Default
Occupancy for Tx FIFO Port 0	This register gives the Occupancy for TX FIFO Port 0. This is a Read only register	0x62D	R	0x00000000
Occupancy for Tx FIFO Port 1	This register gives the Occupancy for TX FIFO Port 1. This is a Read only register	0x62E	R	0x00000000
Occupancy for Tx FIFO Port 2	This register gives the Occupancy for TX FIFO Port 2. This is a Read only register	0x62F	R	0x00000000
Occupancy for Tx FIFO Port 3	This register gives the Occupancy for TX FIFO Port 3. This is a Read only register	0x630	R	0x00000000

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 112. TX FIFO Port Drop Enable Register (Addr: 0x63D)

Bit	Name	Description	Type	Default
Register Description: Independently enables the individual TX FIFOs to drop erroneous packets.				0x0000000f
31:4	Reserved	Reserved	RO	0x000000
3	Port 3 Drop	0 = Disable hard discard of error packets in Tx FIFO 1 = Enable hard discard of error packets in Tx FIFO	R/W	1
2	Port 2 Drop	0 = Disable hard discard of error packets in Tx FIFO 1 = Enable hard discard of error packets in Tx FIFO	R/W	1
1	Port 1 Drop	0 = Disable hard discard of error packets in Tx FIFO 1 = Enable hard discard of error packets in Tx FIFO	R/W	1
0	Port 0 Drop	0 = Disable hard discard of error packets in Tx FIFO 1 = Enable hard discard of error packets in Tx FIFO	R/W	1
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 113. TX FIFO Mini Frame Size for MAC and Padding Enable Port 0 to 3 Register (Addr: 0x63E)

Bit	Name	Description	Type	Default
Register Description: This register is used to independently enable the different minimum packet lengths to be transmitted to the MAC. These values are used to pad the short packets, if padding is enabled. The allowed values allowed (A, B, C, D and E) correspond to 80,88,96,102, and 110 packet bytes. Any other value is not written and the last programmed value is retained.				0x000FAAAA
31:20	Reserved	Reserved	RO	0x000000
19	Port 3 Pad Enable	0 = 1 =Disable padding of short packets for port 3 1 = Enable padding of short packets for port 3	R/W	1
18	Port 2 Pad Enable	0 = Disable padding of short packets for port 2 1 = Enable padding of short packets for port 2	R/W	1
17	Port 1 Pad Enable	0 = Disable padding of short packets for port 1 1 = Enable padding of short packets for port 1	R/W	1
16	Port 0 Pad Enable	0 = Disable padding of short packets for port 0 1 = Enable padding of short packets for port 0	R/W	1
15:12	Port 3 Minimum Size	If the programmed value is ‘N’, the minimum number of bytes in a packet is equal to ‘N * 8’ bytes (N = A, B, C, D and E).	R/W	A
11:8	Port 2 Minimum Size	If the programmed value is ‘N’, the minimum number of bytes in a packet is equal to ‘N * 8’ bytes (N = A, B, C, D and E).	R/W	A
7:4	Port 1 Minimum Size	If the programmed value is ‘N’, the minimum number of bytes in a packet is equal to ‘N * 8’ bytes (N = A, B, C, D and E).	R/W	A
3:0	Port 0 Minimum Size	If the programmed value is ‘N’, the minimum number of bytes in a packet is equal to ‘N * 8’ bytes (N = A, B, C, D and E).	R/W	A
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

7.4.8 MDIO Register Overview

Table 114 through Table 117 "MDI Control Register (Addr: 0x683)" on page 182 provide an overview of the MDIO registers.

Table 114. MDI Single Command Register (Addr: 0x680)

Bit	Name	Description	Type[1]	Default
Register Description: Gives the microprocessor the ability to perform single MDIO read and write accesses.				0x00010319
31:21	Reserved	Reserved	RO	00000000000
20	MDI Command	Performs the MDI operation. Cleared when done. 0 = MDI ready, operation complete 1 = Perform operation	R/W	0
19:18	Reserved	Reserved	RO	00
17:16	OP Code	MDIO Op Code; two bits identify operation to be performed: 00 = Reserved 01 = Write operation (as defined in IEEE 802.3, clause 22.2.4.5) 10 = Read operation (as defined in IEEE 802.3, clause 22.2.4.5) 11 = Reserved	R/W	01
15:10	Reserved	Reserved	RO	000000
9:8	PHY Address	Address of external PHY device	R/W	11
7:5	Reserved	Reserved	RO	000
4:0	REG Address	Five-bit address to one among 32 registers in an addressed PHY device.	R/W	11001
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 115. MDI Single Read and Write Data Register (Addr: 0x681)

Bit	Name	Description	Type[1]	Default
Register Description: MDI read and write data.				0x00000000
31:16	MDI Read Data	MDI Read data from external device.	RO	0000H
15:0	MDI Write Data	MDI Write data from external device.	R/W	0000H
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 116. Autoscan PHY Address Enable Register (Addr: 0x682)

Bit	Name	Description	Type[1]	Default
Register Description: Defines valid PHY addresses. Each bit enables the corresponding PHY address. 0 = Disable the PHY address 1 = Enable the PHY address				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3:0	Autoscan PHY Address	Autoscan PHY address enable 1 = Enable address 0 = Disable address	R/W	1111
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 117. MDI Control Register (Addr: 0x683)

Bit	Name	Description	Type[1]	Default
Register Description: Miscellaneous control bits.				0x00000000
31:20	Reserved	Reserved	RO	0x000
19:16	Remote Fault	Remote fault status	RO	0000
15:4	Reserved	Reserved	RO	0x000
3	MDI Progress	MDI progress. This bit reflects the status of MDI operation.	RO	0
2	MDI Enable	MDI enable. 1 = Enable MDI 0 = Disable MDI	R/W	0
1	Autoscan Enable	Autoscan enable. 1 = Enable Autoscan 0 = Disable Autoscan	R/W	0
0	MDC Speed	MDC speed. 1 = MDC runs at 18 MHz 0 = MDC runs at 2.5 MHz	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

7.4.9 SPI3 Register Overview

Table 118 through Table 120 "Address Parity Error Packet Drop Counter Register (Addr: 0x70A)" on page 185 provide an overview of the SPI3 registers.

Table 118. SPI3 Transmit and Global Configuration Register (Addr: 0x700)

Bit	Name	Description	Type[1]	Default
Register Description: This register gives the configuration related to the SPI3 Transmitter and Global configuration (4 x 8 mode).				0x0020000F
31:24	Reserved	Reserved	RO	0x00
23	SPI3 Transmitter Soft Reset	1 = The SPI3 TX block is reset.	R/W	0
22	SPI3 Receiver Soft Reset	1 = The SPI3 RX block is reset.	R/W	0
21	4x8_mode	0 = Indicates that SPI3 block operates in 32-bit MPHY mode. 1 = Indicates that the SPI3 block operates in 4 x 8 SPHY mode. This configuration affects both the SPI3 transmitter and receiver functionality.	R/W	1
20	Tx_ad_prtyer_drop	Indicates whether to drop packets received with parity error during the address selection phase (Tsx and nTenb High) should be dropped. 0 = Do not drop packets with address parity error 1 = Drop packets with address parity error This is applicable only in MPHY mode of operation. This bit is ignored in 4 x 8 mode as there will be no address selection.	R/W	0
19:16	Dat_prtyer_drp[3:0]	Indicates whether to drop packets with data parity error for each of the ports. 0 = Do not drop packets with data parity error (default) 1 = Drop packets with data parity error	R/W	0x0
15:8	Reserved	Write as 0, ignore on Read.	R/W	00000000
7:4	Tx_parity_sense [3:0]	Indicates the parity sense to check the parity on TDAT bus for each port. Bit 0 is used in MPHY mode. 0 = Odd Parity 1 = Even Parity	R/W	0x0
3:0	Tx_port_enable [3:0]	Enables the individual Transmit ports when set. 0 = Port disable 1 = Port enable	R/W	0xF
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 119. SPI3 Receive Configuration Register (Addr: 0x701)

Bit	Name	Description	Type[1]	Default
Register Description: This register gives the configuration related to the SPI3 receiver.				0x00000F80
31:28	Reserved	Reserved	RO	0x0
27:24	B2B_PAUSE [3:0]	Indicates the number of pause cycles to be introduced between back-to-back transfers. The 4-bits are for four ports. In MPHY mode port 0's setting is used. 0 = Zero pause cycles 1 = Two pause cycles	R/W	0x0
23:22	RX_BURST_3[1:0]	Selects maximum burst size on the TX and RX path for ports [3:0]. MPHY mode uses port[0]'s configuration. 0x = 64 bytes maximum burst size 10 = 128 bytes maximum burst size 11 = 256 bytes maximum burst size	R/W	0x0
12:20	RX_BURST_2[1:0]		R/W	0x0
19:18	RX_BURST_1[1:0]		R/W	0x0
17:16	RX_BURST_0[1:0]		R/W	0x0
15:12	Rx_parity_sense[3:0]	Indicates the parity sense to check the parity on RDAT bus for each port. Bit 0 is used in MPHY mode. 0 = Odd Parity 1 = Even Parity	R/W	0x0
11:8	Rx_port_enable[3:0]	Enables the individual Rx logical ports in MPHY mode when set. This enable is local to SPI3 block. The packet from the disabled ports will not be sent on the Rx SPI3 In 4 x 8 mode it enables the individual SPI3 Rx paths.	R/W	0xF
7	Rx_core_enable[3:0]	When set enables the core operating in MPHY mode. Used only in MPHY mode of operation.	R/W	0x1
6:1	IBA[5:0]	Sets the 6-bit value appended to the 2-bit address during the port address selection. This is applicable only in MPHY mode of operation.	R/W	0x00
0	SIG_BAD	If this bit is '1' and the Packet Filter Control Register bit PassBad is also '1' then frames containing Layer-2 errors are indicated with RERR on SPI3.	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

Table 120. Address Parity Error Packet Drop Counter Register (Addr: 0x70A)

Bit	Name	Description	Type[1]	Default
Register Description: This register counts the number of packets dropped due to parity error detection during the address selection cycle.				0x00000000
31:8	Reserved	Reserved	RO	0x000000
7:0	Address Parity Error Packet Drop Counter	This is an 8-bit counter that counts the number of packets dropped due to parity error detection during the address selection cycle. This gets cleared when read and saturates at 8'hFF. There is only one counter for address parity drop as address will be used only in MPHY mode of operation. The counter gets cleared once the register is read.	R	0x00

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

7.4.10 SerDes Register Overview

Table 121 through Table 124 "Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)" on page 187 define the contents of the SerDes registers at base location 0x780, which contain the control and status for the four SerDes interfaces on the IXF1104.

Table 121. Tx and Rx ACDC Coupling Selection Register (Addr: 0x780)

Bit	Name	Description	Type[1]	Default
Register Description: Allows selection of AC or DC coupling on the output of each SerDes port (Tx and RX are independent).				0x00000000
31:8	Reserved	Reserved	RO	0x000000
7	RxACDC3	Selects line coupling mode, AC = 0, DC = 1	R/W	0
6	TxACDC3	Selects line coupling mode, AC = 0, DC = 1	R/W	0
5	RxACDC2	Selects line coupling mode, AC = 0, DC = 1	R/W	0
4	TxACDC2	Selects line coupling mode, AC = 0, DC = 1	R/W	0
3	RxACDC1	Selects line coupling mode, AC = 0, DC = 1	R/W	0
2	TxACDC1	Selects line coupling mode, AC = 0, DC = 1	R/W	0
1	RxACDC0	Selects line coupling mode, AC = 0, DC = 1	R/W	0
0	TxACDC0	Selects line coupling mode, AC = 0, DC = 1	R/W	0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 122. Tx and Rx Power-Down Register (Addr: 0x787)

Bit	Name	Description	Type	Default
Register Description: Power-Down Tx and Rx power-down bits to allow per-port power-down of unused ports				0x00000000
31:14	Reserved	Reserved	RO	0x0000000
13:10	TPWRDWN[3:0]	Tx power-down for Ports 3-0 (1 = Power-down)	R/W	0000
9:4	Reserved	Reserved		0x00
3:0	RPWRDWN[3:0]	Rx Power-Down for Ports 3-0 (1 = Power-down)	R/W	0000
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 123. Rx Signal Detect Level Ports 0-3 Register (Addr: 0x793)

Bit	Name	Description	Type[1]	Default
Register Description: This register shows the status of the Rx input in relation to the level of the signal being received from the line. This register is meant for debug and test use.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3:0	SIGDET[3:0]	Signal Detect for Ports 0-3 0 = Noise 1 = Signal	RO	0x0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 124. Clock and Interface Mode Change Enable Ports 0-3 Register (Addr: 0x794)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used when a change to the operational mode or speed of the IXF1104 is required. This register ensures that when a change is made that the internal clocking of the IXF1104 is managed correctly and no unexpected effects of the operational or speed change are observable on the line interfaces. Prior to any change in either speed or copper/fiber mode, the appropriate port of this register should be set to 0x1. Once this has been performed, the "Interface Mode Register (Addr: 0x501)" or the "MAC Interface Mode and RGMII Speed Register (Addr: Port_Index + 0x10)" can be altered. Once the changes have been made, this register should be written to, setting the appropriate port bit to 0x0. The port should then be ready to begin operation in its newly configured mode.				0x00000000
31:4	Reserved	Reserved	RO	0x0000000
3	Enable clock mode change_3	Enables internal clock generator for Port 3 to sample the interface clock mode and Interface mode. To be set to zero when the clock mode or the interface mode is to be changed for Port 3. Otherwise, the bit has to be set to 1 for the change in the configuration to take effect.	R/W	0
2	Enable clock mode change_2	Enables internal clock generator for Port 2 to sample the interface clock mode and Interface mode. To be set to zero when the clock mode or the interface mode is to be changed for Port 2. Otherwise, the bit has to be set to 1 for the change in the configuration to take effect.	R/W	0
1	Enable clock mode change_1	Enables internal clock generator for Port 1 to sample the interface clock mode and Interface mode. To be set to zero when the clock mode or the interface mode is to be changed for Port 1. Otherwise, the bit has to be set to 1 for the change in the configuration to take effect.	R/W	0
0	Enable clock mode change_0	Enables internal clock generator for Port 0 to sample the interface clock mode and Interface mode. To be set to zero when the clock mode or the interface mode is to be changed for Port 0. Otherwise, the bit has to be set to 1 for the change in the configuration to take effect.	R/W	0

1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write

7.4.11 GBIC Register Overview

Table 125 through Table 128 "I2C Data Register Ports 3-0 (Addr: 0x79F)" on page 189 provide an overview of the GBIC registers.

Table 125. GBIC Status Register Ports 0-3 (Addr: 0x799)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a means to control and monitor the interface to the GBIC Modules when used in SerDes mode.				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:20	Rx_LOS_3:0	Rx_LOS inputs for Ports 0-3	R	0x0
19:14	Reserved	Reserved		
13:10	Tx_FAULT_3:0	Tx_FAULT inputs for Ports 0-3	R	0x0
9:4	Reserved	Reserved		
3:0	MOD_DEF_3:0	MOD_DEF inputs for Ports 0-3	R	0x0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 126. GBIC Control Register Ports 0-3 (Addr: 0x79A)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a means to control and monitor the interface to the GBIC Modules when used in SerDes mode.				0x00000000
31:17	Reserved	Reserved	RO	0x0000
16:13	I^2c_port_enable	When set, individually enables the four I^2C ports.	R/W	0xf
12	Rx_LOS_En	Enable for Rx_LOS_Int operation (Enabled = 1)	R/W	0
11	Tx_FAULT_En	Enable for Tx_FAULT_Int operation (Enabled = 1)	R/W	0
10	MOD_DEF_En	Enable for MOD_DEF_Int operation (Enabled = 1)	R/W	0
9:4	Reserved	Reserved		
3:0	Tx_DISABLE_3:0	Tx_DISABLE outputs for Ports 0-3	R/W	0x0
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 127. I²C Control Register Ports 3-0 (Addr: 0x79B)

Bit	Name	Description	Type[1]	Default
Register Description: This register controls and monitors the interface to the GBIC modules when used in SerDes mode.				0x00000000
31:28	Reserved	Reserved	RO	0x0
27	wp_err	An attempt to write to the protected E²PROM has occurred.	R	0
26	no_ack_err	This bit is set to 1 when a write and subsequent read from a GBIC has failed. This signal should be used to validate the data being read. Data is only valid if this bit is equal to zero.	R	0
25	I²C_enable	Enable the I²C block.	R/W	0
24	I²C_start	Start the I²C transfer.	R/W	0
23	Reserved	Reserved	RO	0
22	write_complete	Bit is asserted when write access is complete.	R	0
21	Reserved	Reserved	RO	0
20	Read_complete	Bit asserted when read access is complete.	R	0
19:18	Reserved	Reserved	RO	0
17:16	Port Select	Selects the port for which the I²C transaction is targeted. Valid range is 0 to 3.	R/W	00
15	Read/Write	0 = Write transaction 1 = Read transaction	R/W	0
14:11	Device ID	Most-significant four bits of device address field.	R/W	0x0
10:0	Register Address	Bits 10:8 select the least-significant three bits of the device address field Bits 7:0 select the word/register address	R/W	0x000
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

Table 128. I²C Data Register Ports 3-0 (Addr: 0x79F)

Bit	Name	Description	Type[1]	Default
Register Description: These registers hold data bytes that are read and written using the I²C interface to GBICs connected to each port of the IXF1104 Quad-Port Gigabit Ethernet Media Access Controller.				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:16	Write Data	Bit 23=MSB, Bit 16 = LSB Data to be written to the GBIC module.	R/W	0X00
15:8	Reserved	Reserved	RO	0x00
7:0	Read Data	Bit 7 = MSB, Bit 0 = LSB Data read from the GBIC module.	R/W	0X00
1. RO = Read Only, No clear on Read; R = Read, Clear on Read; W = Write only; R/W = Read/Write, No clear; R/W/C = Read/Write, Clear on Write				

8.0 Mechanical Specifications

The IXF1104 is packaged in a 576-ball BGA package with 6 balls removed diagonally from each corner, for a total of 552 balls used measuring 25 mm x 25 mm. The pitch of the balls on the package is 1 mm.

8.1 Overview

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications with high noise immunity requirements.

8.1.1 Features

- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power-zone offering supports core and four additional voltages
- JEDEC-compliant package

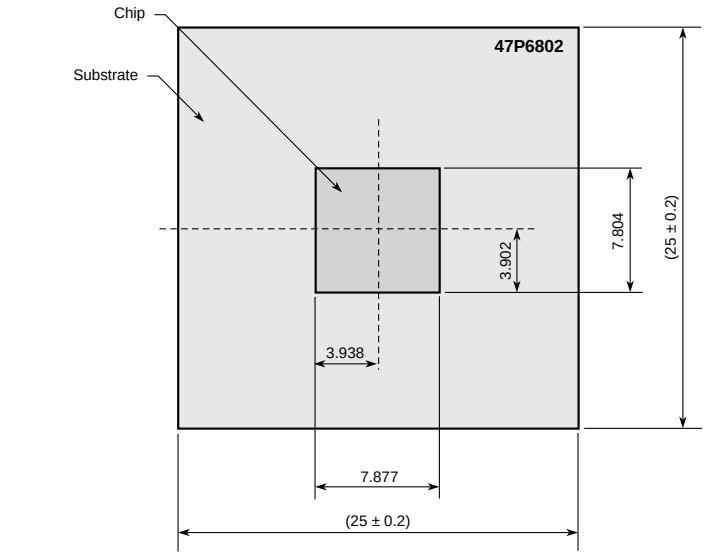
8.2 Package Specifics for the IXF1104

The IXF1104 uses the following package:

- 576-ball BGA package with 6 balls removed diagonally from each corner, for a total of 552 balls used
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

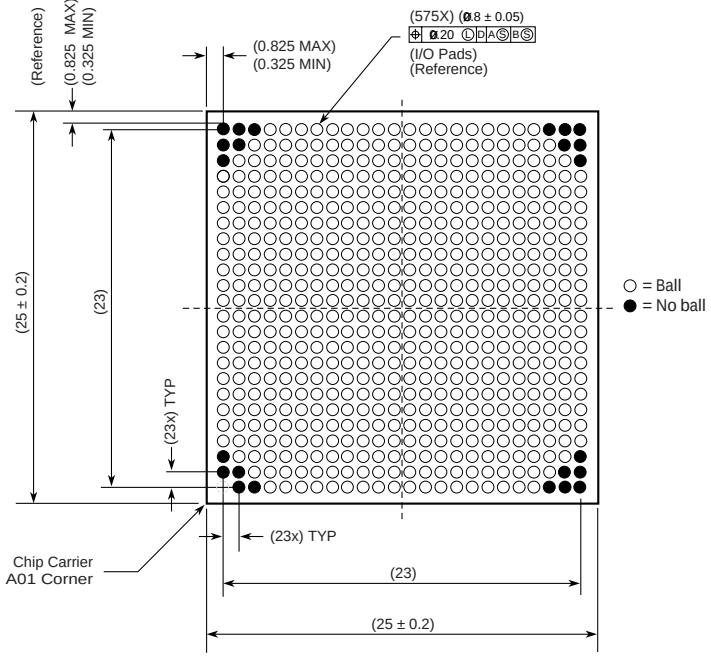
8.3 Package Information

Figure 51. CBGA Package Diagram



Note: All dimensions are in mm.

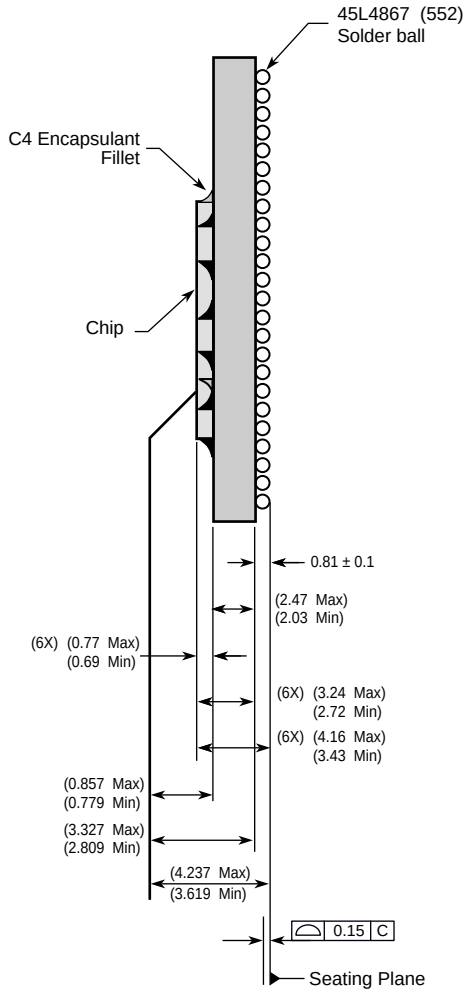
B0034-01



Note: All dimensions are in mm.

B0035-03

Figure 52. CBGA Package Side View Diagram

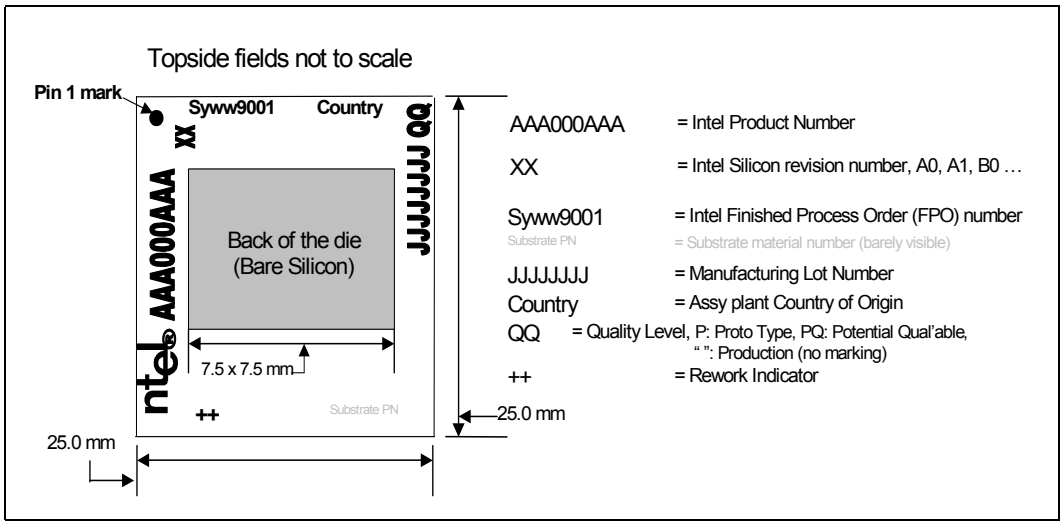


Note: All dimensions are in mm.

B0555-01

8.3.1 Example Package Marking

Figure 53. Intel® IXF1104 Example Package Marking



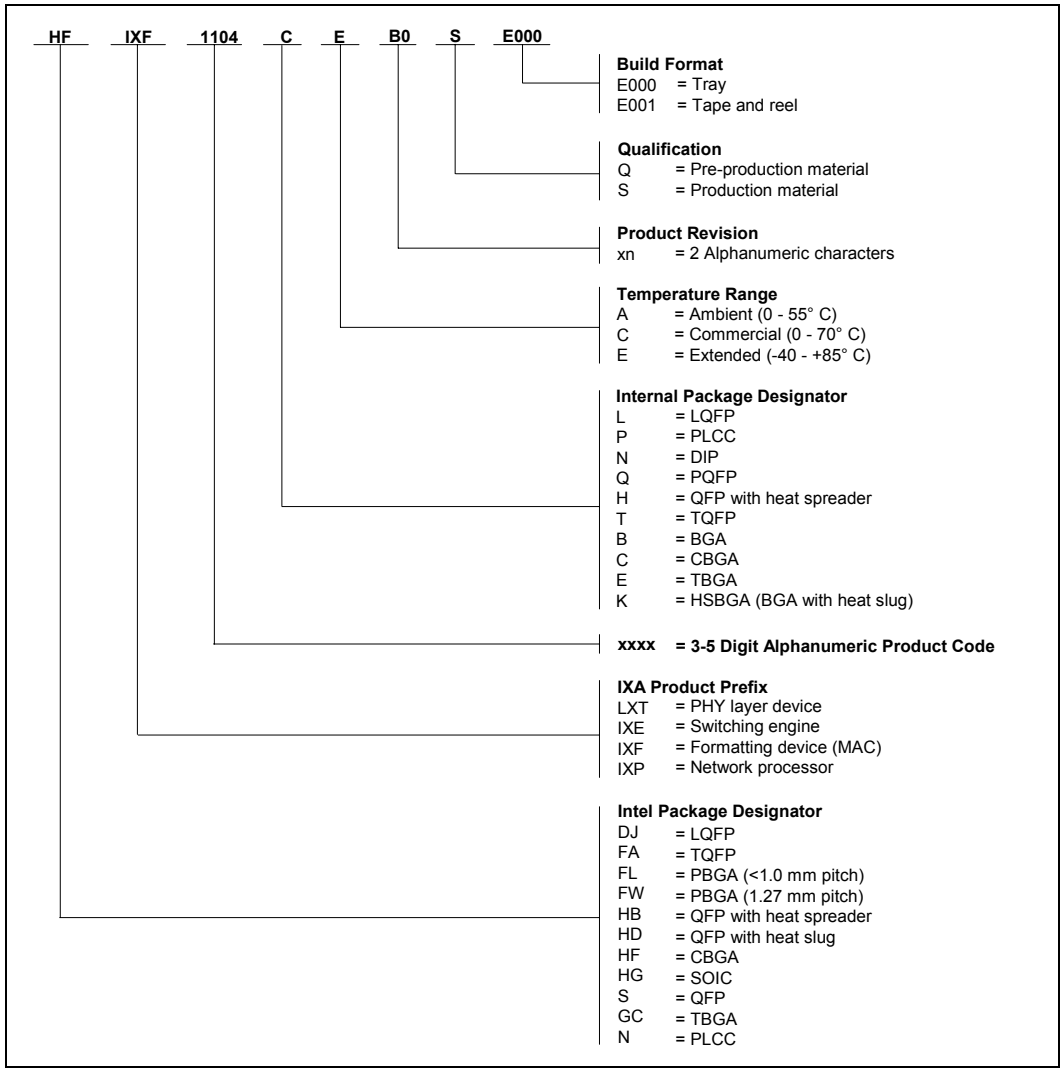
9.0 Product Ordering Information

Table 129 and Figure 54 provide IXF1104 product ordering information.

Table 129. Product Information

Number	Revision	Qualification	MM Number	Ship Media
HFIXF1104CE.B0 S 853714	B0	S	853714	Tray

Figure 54. Ordering Information – Sample



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