

CMOS PRESET TABLE DIVIDE-BY-N COUNTER

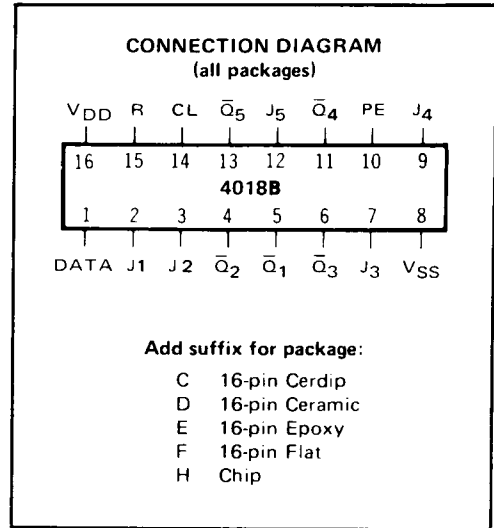
FEATURES

- ◆ Divide by any Number Between 2 and 10 with One External Gate
- ◆ Johnson Counter Configuration for Spike-Free Counting
- ◆ Fully Static operation - DC to 5MHz @ 10Vdc

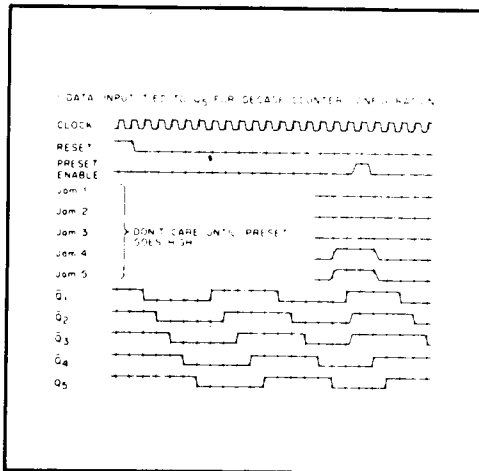
DESCRIPTION

The 4018B consists of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. Clock, Reset, Data, Preset Enable, and 5 individual Jam inputs are provided. Divide-by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the Q5, Q4, Q3, Q2, Q1 signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by use of a single SCL4081B gate to properly gate the feedback connections to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple 4018B units. The counter is advanced one count at the positive clock-signal transition. A high Reset signal clears the counter to an all-zero condition. A high Preset-Enable signal allows information on the Jam inputs to preset the counter. Reset and Preset gating is provided to assure the proper counting sequence.

This device is particularly useful in frequency-division and control applications.



TIMING DIAGRAM

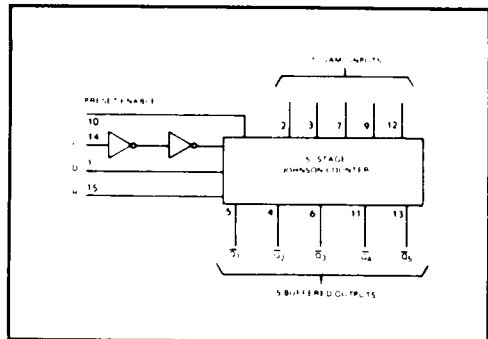


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C
E Device			

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	-	5	-	0.05	5	-	150	μA _{dc}
			-	10	-	0.1	10	-	300	
			-	15	-	0.2	20	-	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

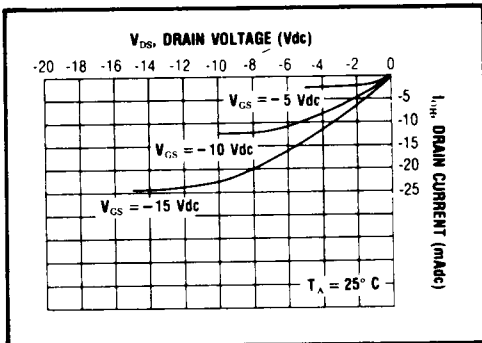
T_{HIGH} = +125°C for C, D, F, H device.

= +85°C for E device.

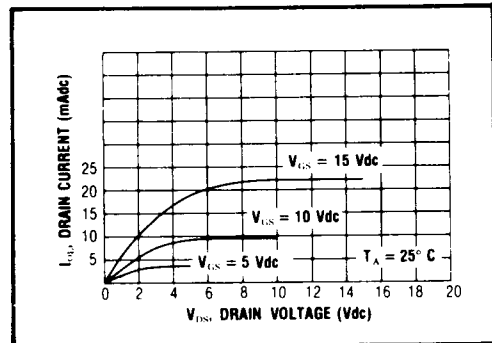
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION					
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	-	500	1000
		10	-	150	300
		15	-	120	240
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	-	130	260
		10	-	65	130
		15	-	50	100
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	-	200	400
		10	-	100	200
		15	-	80	160
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	-
		10	2.5	5.0	-
		15	3.0	6.0	-
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	-	-
		10	15	-	-
		15	5	-	-
MINIMUM DATA INPUT SETUP TIME	t _{setup}	5	-	200	400
		10	-	100	200
		15	-	80	160
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	-	0	100
		10	-	0	50
		15	-	0	40
PRESET OR RESET OPERATION					
PROPAGATION DELAY TIME From PE or Reset Input	t _{PLH} , t _{PHL}	5	-	500	1000
		10	-	250	500
		15	-	200	400
MINIMUM PRESET OR RESET PULSE WIDTH	PW _{PR} , PW _R	5	-	200	400
		10	-	100	200
		15	-	80	160
MINIMUM JAM INPUT SETUP TIME	t _{setup}	5	-	200	400
		10	-	100	200
		15	-	80	160
PRESET OR RESET REMOVAL TIME	t _{rem}	5	-	375	750
		10	-	125	250
		15	-	90	180

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the clock outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

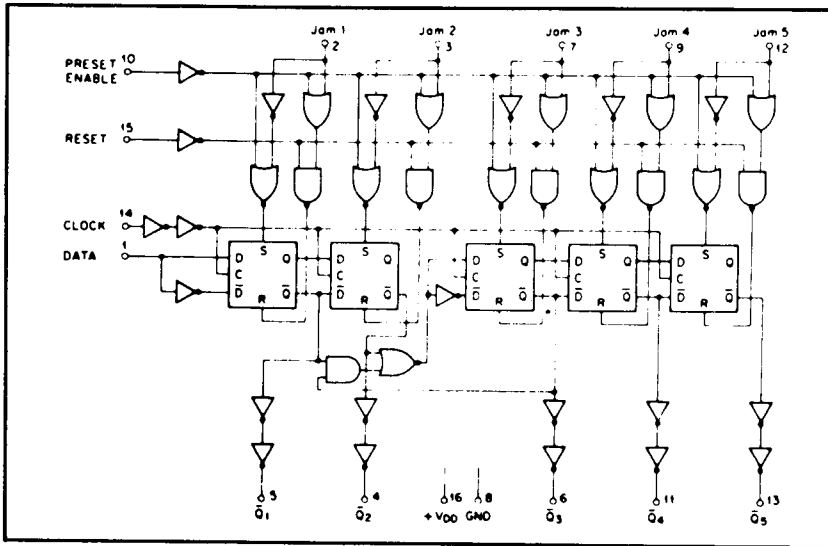


Typical P-Channel
Source Current Characteristics

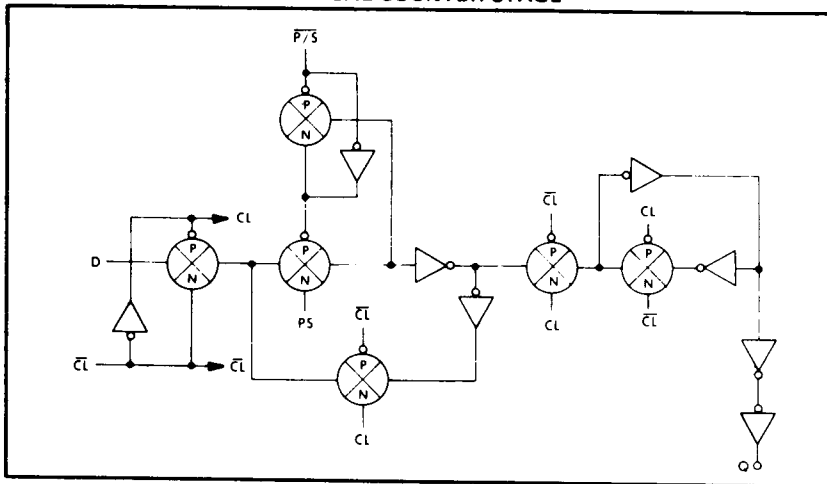


Typical N-Channel
Sink Current Characteristics

LOGIC DIAGRAM



TYPICAL COUNTER STAGE



EXTERNAL CONTROL CONNECTIONS

