L29C525
Dual Pipeline Register

FEATURES

- Dual 8-Deep Pipeline Register
- Configurable to Single 16-Deep
- Low Power CMOS Technology
- Replaces AMD Am29525
- Load, Shift, and Hold Instructions
- Separate Data In and Data Out Pins
- Three-State Outputs
- DECC SMD No. 5962-91696
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C525** is a high-speed, low power CMOS pipeline register. It is pin-for-pin compatible with the AMD Am29525. The L29C525 can be configured as two independent 8-level pipelines or as a single 16-level pipeline. The configuration implemented is determined by the instruction code (I_{1-0}) as shown in Table 2.

The I_{1-0} instruction code controls the internal routing of data and loading of each register. For instruction I_{1-0} = 00 (Push A and B), data applied at the D_{7-0} inputs is latched into register A0 on the rising edge of CLK. The contents of A0 simultaneously move to register A1, A1 moves to A2, and so on. The contents of register A7 are wrapped back to register B0. The registers on the B side are similarly shifted, with the contents of register B7 lost.

Instruction I_{1-0} = 01 (Push B) acts similarly to the Push A and B instruction, except that only the B side registers are shifted. The input data is applied to register B0, and the contents of register B7 are lost. The contents of the A side registers are unaffected. Instruction I_{1-0} = 10 (Push A) is identical to the Push B instruction, except that the A side registers are shifted and the B side registers are unaffected.

Instruction I_{1-0} = 11 (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

The contents of any of the registers is selectable at the output through the use of the S_{3-0} control inputs. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_{3-0} controls is given in Table 3.

L29C525 Block Diagram

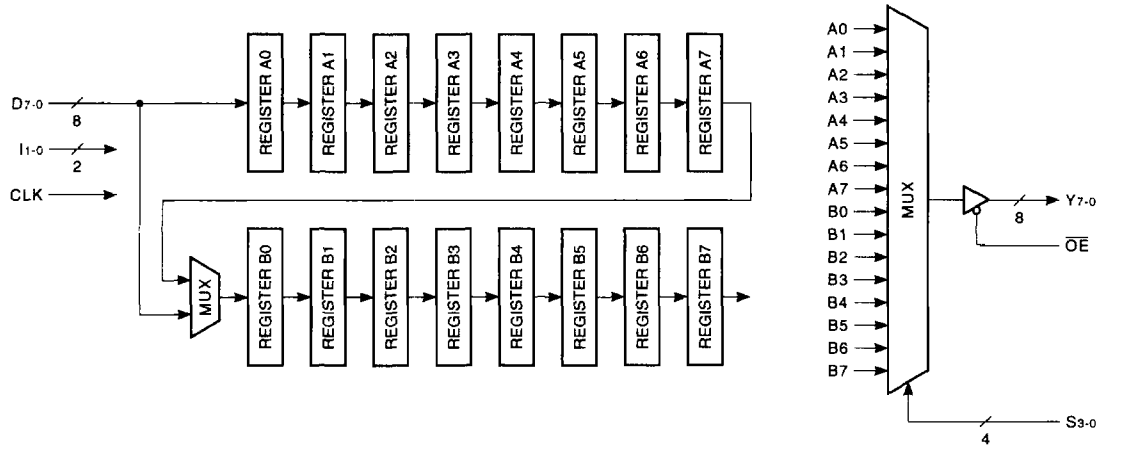


Table 1. Register Load Operations

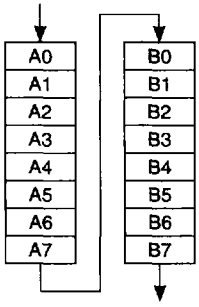
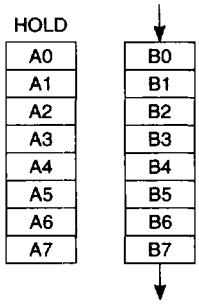
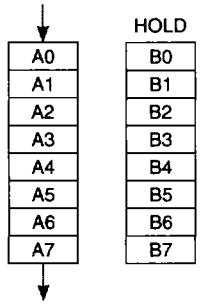
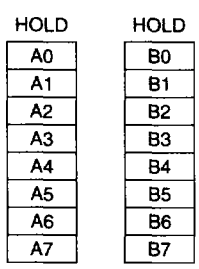
Single 16 Level	Dual 8 Level		
Push A and B	**Push B**	**Push A**	**Hold All Registers**
			

Table 2. Instruction Set

Mnemonics	Inputs I_1	Inputs I_0	Description
Shift	0	0	Push A and B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	Hold All Registers

Table 3. Output Select

S_3	S_2	S_1	S_0	Y_{7-0}
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	0	A6
0	1	1	1	A7
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	0	B6
1	1	1	1	B7

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –12 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

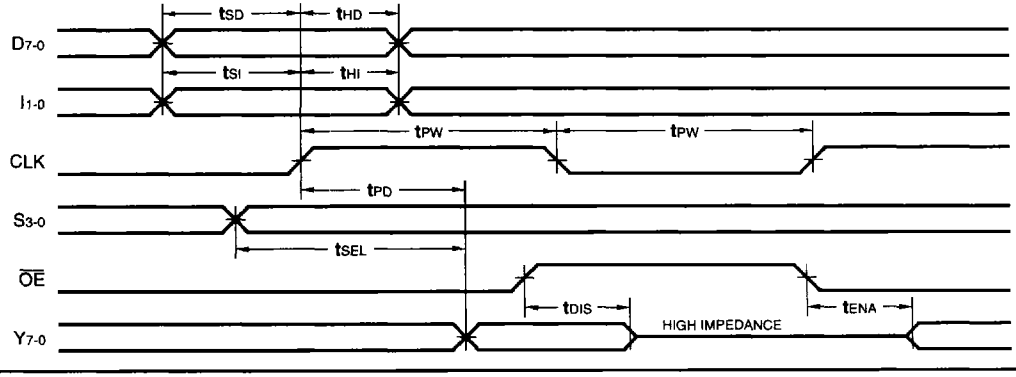
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C525–			
		20		15	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		20		15
t_{SEL}	Select to Output Delay		20		15
t_{PW}	Clock Pulse Width	12		10	
t_{SD}	Data Setup Time	7		5	
t_{HD}	Data Hold Time	0		0	
t_{SI}	Instruction Setup Time	7		5	
t_{HI}	Instruction Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C525–			
		25		20	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		25		20
t_{SEL}	Select to Output Delay		25		20
t_{PW}	Clock Pulse Width	12		12	
t_{SD}	Data Setup Time	7		7	
t_{HD}	Data Hold Time	2		2	
t_{SI}	Instruction Setup Time	7		7	
t_{HI}	Instruction Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

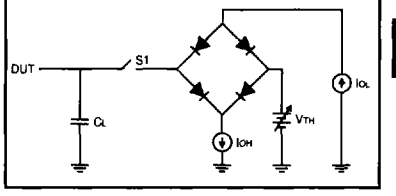
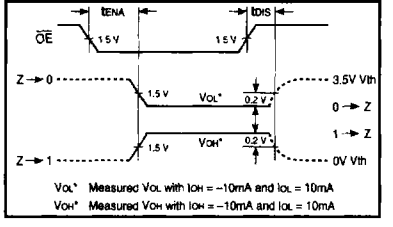


FIGURE B. THRESHOLD LEVELS



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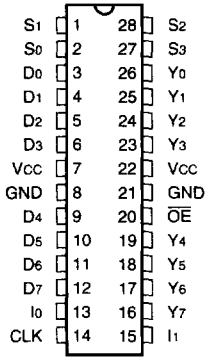
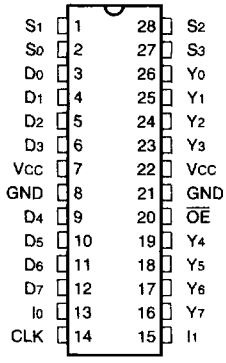
ORDERING INFORMATION

28-pin — 0.3" wide



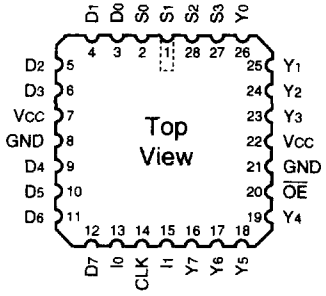
28-pin — 0.4" wide



Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Ceramic DIP (C10)
	0°C to +70°C — Commercial Screening		
20 ns	L29C525PC20	L29C525CC20	L29C525IC20
15 ns	L29C525PC15	L29C525CC15	L29C525IC15
	–55°C to +125°C — Commercial Screening		
25 ns		L29C525CM25	L29C525IM25
20 ns		L29C525CM20	L29C525IM20
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns		L29C525CMB25	L29C525IMB25
20 ns		L29C525CMB20	L29C525IMB20

ORDERING INFORMATION

28-pin



Speed	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)	
	0°C to +70°C — Commercial Screening		
20 ns 15 ns	L29C525JC20 L29C525JC15		
	–55°C to +125°C — Commercial Screening		
	–55°C to +125°C — MIL-STD-883 Compliant		
25 ns 20 ns		L29C525KMB25 L29C525KMB20	

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