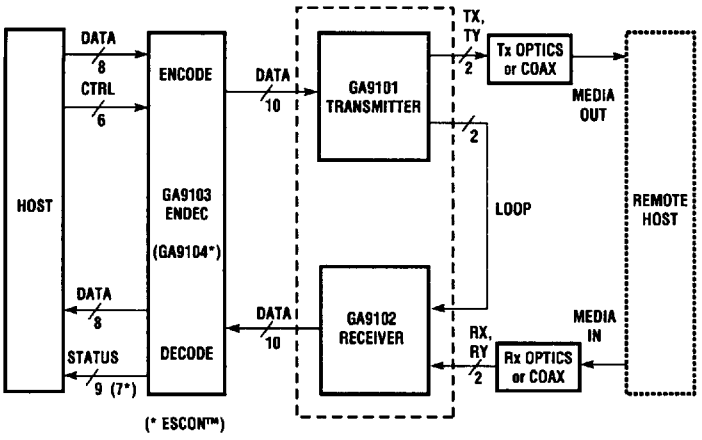

TriQuint's GA9101 Transmitter and GA9102 Receiver, in conjunction with either the GA9103 ENDEC or the GA9104 ENDEC, provide a comprehensive electrical and physical interface in compliance with the Fiber Channel Specification of the Accredited Standards Committee (ASCX3T9.3) or the Enterprise Systems Connection Architecture (ESCON™). These chip sets can also be used for ATM local area network applications operating at serial data rates of 194.4 Megabaud (payload at 155.52 Megabits/sec).

The Fiber Channel Specification is intended as a standard I/O channel interface for either serial interconnection of peripherals to computers or for communication between computers. With the Fiber Channel, users may communicate over distances of up to 10 kilometers at baud rates of 132.8125 Megabaud to 1.0625 Gigabaud. The GA9101 and GA9102 are designed to operate at serial baud rates of 194.4, 200.0, and 265.625 Megabaud.

The Fiber Channel standard provides a variety of physical media and data rates to accommodate different cost/performance needs. The framing protocol also provides flexibility so different implementations can use various features of the standard in order to optimize the overall performance of the system.

The GA9103 CMOS ENDEC chip implements the data, ordered-set, and line-state encoding and decoding functions of the Fiber Channel Physical Layer standard (FC_PH). In addition, it performs 32-bit CRC and parity generate/check functions.

The ESCON I/O interface provides an optical-fiber communication link between I/O devices and main storage of IBM or compatible computers implementing Enterprise Systems Architecture/390 ™ (ESA/390 ™).

The GA9104 CMOS ENDEC chip implements the data and control encoding/decoding functions of the ESCON standard. In addition, it performs 16-bit CRC and parity generate/check functions.

GA9101/GA9102

Fiber Channel ESCON™ ATM Transmitter, Receiver

Data Comm

Features

- *Fiber Channel, ESCON, and ATM compatible*
- *With fiber optics and ENDEC, a complete FC-0, FC-1 solution*
- *TTL-compatible 10-bit-wide data bus with 19.44, 20.00, or 26.5625 MHz byte clock*
- *Serial rate of 194.4, 200.0, or 265.625 Mbaud with on-chip bit clock generation*
- *On-chip clock-and-data-recovery PLL*
- *Automatic byte alignment to 8b/10b code*
- *Low power dissipation – 700 mW per chip, typical*
- *28-pin surface-mount package*

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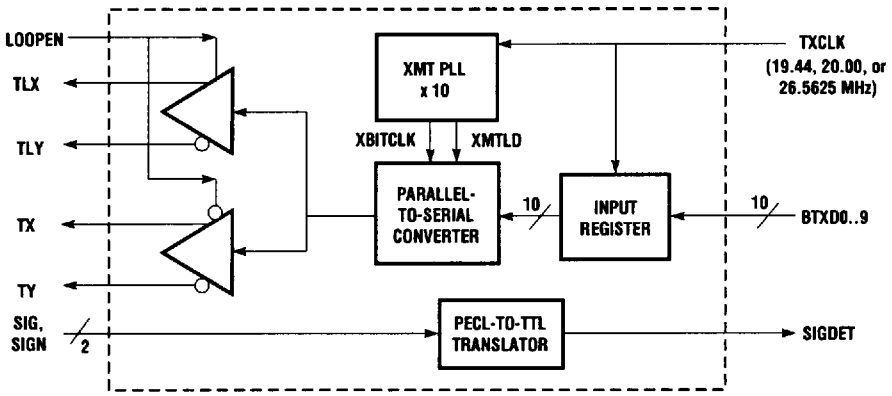
The ENDECs (GA9103, GA9104) interface to TriQuint's GA9101 and GA9102 Transmitter and Receiver and to either the device link protocol controller or the fabric.

The Transmitter/Receiver chips, GA9101 and GA9102, are designed using TriQuint's proprietary 0.7 micron One-Up™GaAs process, and interface either directly to the electrical medium or to the fiber-optic interface. The chips implement parallel-to-serial conversion, bit clock generation, receive clock/data recovery, and serial-to-parallel conversion.

Along with a fiber-optic module, the Fiber Channel chip set will provide complete FC-0 and FC-1 solutions for a Fiber Channel data link.

In addition to ESCON and Fiber Channel applications, the GA9101 and GA9102 can also be used for serial SCSI, point-to-point serial communication, ATM networks and other network applications.

GA9101 – Transmitter



Functional Description – GA9101 Transmitter

The XMT PLL block synthesizes the reference bit clock, XBITCLK, which is derived from the transmit clock input, TXCLK. The frequency of TXCLK is 19.44, 20.00, or 26.5625 MHz, which is multiplied by 10 through an internal Phase-Locked Loop to obtain an XBITCLK of 194.4, 200.0, or 265.625 MHz, respectively. The XBITCLK is used to provide the bit timing to the transmit path.

The INPUT REGISTER loads the 10-bit-wide input data, BTXD0..9 from the ENDEC on the positive edge of TXCLK. It sends out the data to the PARALLEL-TO-SERIAL block.

The XMTLD signal strobes in the 10-bit-wide data into the PARALLEL-TO-SERIAL CONVERTER functional block. This data is then serialized using the XBITCLK from the PLL block. During serialization, the most significant bit, BTXD9, is transmitted first, followed by BTXD8 . . BTXD0. The serial data is sent out using the differential PECL driver. The transmit output is selected by the LOOPEN input signal as shown in the table. The unselected differential outputs are forced to a logic LOW state.

The SIG and SIGN differential PECL signals originate from the optical receiver and, when active, indicate the presence of input optical signals. SIGDET is an active-HIGH TTL signal derived from SIG and SIGN, through the PECL-to-TTL TRANSLATOR

As required by the Fiber Channel standard, the GA9101/GA9102 provide a Loopback mode for a system test at speed. When LOOPEN = 1, the TLX and TLY outputs of the GA9101 are enabled and are transmitted to the RLX and RLY inputs of the local receiver. In the normal mode (LOOPEN = 0), the TX and TY outputs of the transmitter are enabled.

Transmit Output Selection Table

LOOPEN	*Tx Output*
0	TX, TY
1	TLX, TLY

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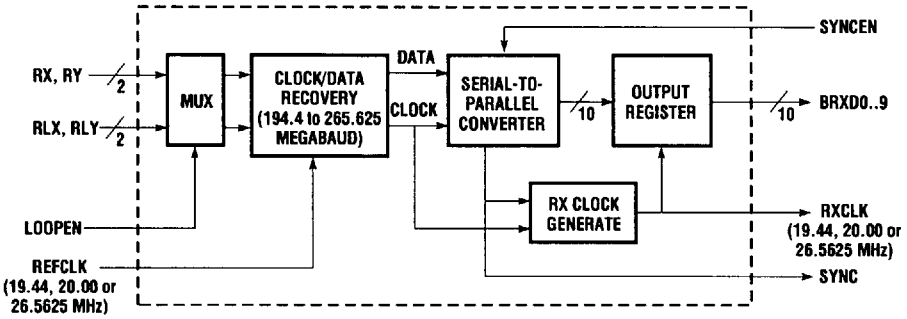
GA9102 – Receiver



Functional Description – GA9102 Receiver

The MUX block receives its inputs from the RX, RY differential inputs and the looped transmit outputs connected to RLX and RLY. Its output goes to the CLOCK/DATA RECOVERY block. The MUX output is selected by the LOOPEN pin as outlined in the Selection Table below.

Clock Recovery Input Selection Table

LOOPEN	*MUX Output*
0	RX, RY
1	RLX, RLY

The CLOCK/DATA RECOVERY (CDR) circuit recovers the clock information from the input data, at the serial transmission rate of 194.4, 200.0, or 265.625 Megabaud. The CDR block uses the REFCLK to aid in frequency acquisition of the recovered clock, called CLOCK, which is then used to retime the data, removing any jitter components. If REFCLK is present, the initial receiver bit-synchronization time to valid incoming data is less than 200 microseconds. The receiver is guaranteed to have valid outputs 1 ms after valid REFCLK and serial data are applied. Once synchronized, if a phase discontinuity occurs in the incoming data, the receiver resynchronizes in less than 2500 bit times, (with 95% probability) . The recovered data is converted to a 10-bit data word by the SERIAL-TO-PARALLEL CONVERTER (SPC) logic. The CLOCK signal is used by the SPC and the RX CLOCK GENERATE blocks to provide the necessary bit timing.

The SERIAL-TO-PARALLEL CONVERTER block does the serial-to-parallel conversion. The parallel conversion is to 10 bits, which corresponds to the undecoded byte output of the 8b/10b coding scheme. The output of this block is sent to the OUTPUT REGISTER. The SPC also generates the SYNC signal upon receipt of a K28.5 byte, (001111 1010 or 110000 0101), provided the SYNCEN pin is HIGH. The SYNC signal is always LOW if SYNCEN is inactive. When the SYNCEN signal is LOW, the device retains the previous alignment for the incoming K28.5 byte. The SYNCEN signal is useful when the host decides to disable byte alignment to the incoming K28.5. Using this pin, the host may decide to align only under certain circumstances, such as power up or loss of word synchronization (see the GA9103 ENDEC data sheet). The SYNCEN pin can also be of use in non-Fiber Channel applications where byte alignment to a different pattern may be done by the interfacing logic.

The RX CLOCK GENERATE block is used to generate the Receive Byte Clock, RXCLK. RXCLK is 19.44, 20.00, or 26.5625 MHz, corresponding to the serial baud rate of 194.4, 200.0, or 265.625 Megabaud, respectively. The RXCLK is realigned synchronous to the SYNC signal from the SERIAL-TO-PARALLEL CONVERTER. On power up, the RXCLK provides arbitrary alignment for the incoming data until the arrival of the first K28.5 byte while SYNCEN is HIGH.

The OUTPUT REGISTER takes in the 10-bit-wide output from the SERIAL-TO-PARALLEL CONVERTER block and generates output data BRXD0..9. BRXD0..9 interfaces to the ENDEC chip and can be strobed on the negative edge of RXCLK. The received bit sequence within each 10 bits of serial data is BRXD9 . . BRXD0.

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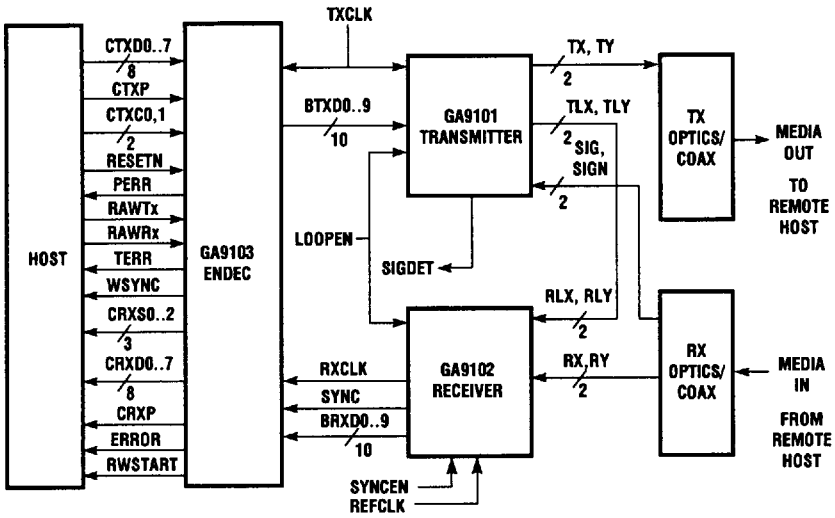
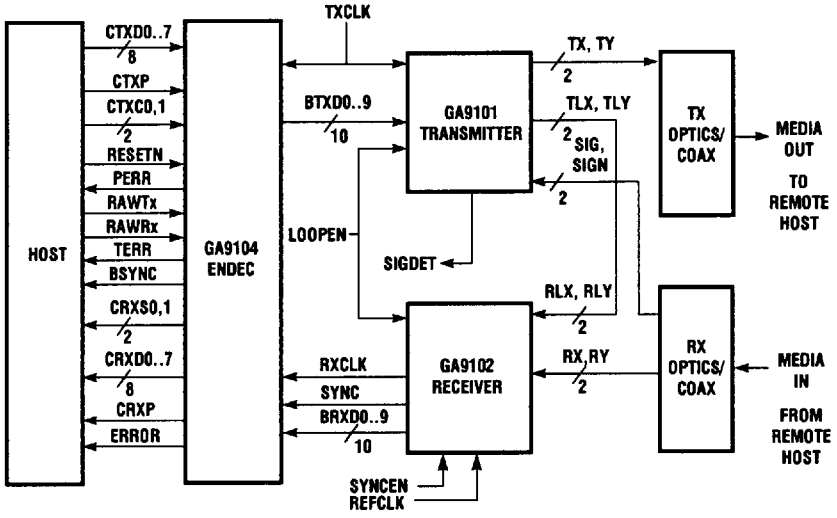
System Block Diagram – Fiber Channel



System Block Diagram – ESCON/ATM



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Guide to Specifications

A substantial number of specifications define the operation of the ESCON/Fiber Channel Transmitter/Receiver. They have been segmented for quick reference:

Conditions
- Absolute maximum ratings
- Operating conditions
- Test conditions

DC Specifications (Receiver)
- TTL-level pins
- PECL-level pins

DC Specifications (Transmitter)
- TTL-level pins
- PECL-level pins

AC Specifications (Receiver)
- Bus timing
- Serial interface timing

AC Specifications (Transmitter)
- Bus timing
- Serial interface timing

Absolute Maximum Ratings

Exceeding the absolute maximum ratings may damage the device.

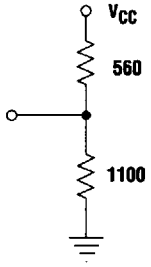
Storage temperature	-65°C to +150°C
Case temperature	-55°C to +125°C
Supply voltage to ground	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (VCC +0.5 V)
DC input current	-30 mA to +5 mA

Operating Conditions

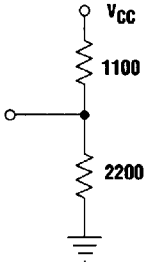
Proper functionality is guaranteed under these conditions:

Supply voltage	5V ±5%
Ambient temperature	0-70°C

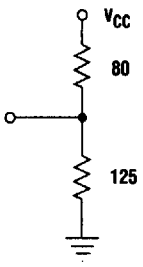
TTL Test Load, RXCLK



TTL Test Load, All Other TLL Outputs



PECL Test Load



Capacitance*

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance	V_{IN} = 2.0 V at f = 1 MHz		6		pF
C_{OUT}	Output capacitance	V_{OUT} = 2.0 V at f = 1 MHz		9		pF

Note: These parameters are not 100% tested, but are periodically sampled.

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DC Characteristics (Over operating range unless otherwise specified.)

GA9101 Transmitter TTL Signals (BTXD0..9, TXCLK, SIGDET, LOOPEN)

Symbol	Description	Test Conditions	Limits[1] Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min I_{OH} = -1.6 mA V_{IN}[2] = V_{IH} or V_{IL}	2.4	3.7		V
V_{OL}	Output LOW voltage	V_{CC} = Min I_{OL} = 4 mA V_{IN}[2] = V_{IH} or V_{IL}		0.2	0.5	V
I_{SC}[4]	Output short-circuit current	V_{CC} = Max V_{OUT} = 0.5 V	-15		-100	mA
I_{IL}	Input LOW current	V_{CC} = Max V_{IN} = 0.40 V			- 400	µA
I_{IH}	Input HIGH current	V_{CC} = Max V_{IN} = 2.7 V			25	µA
I_I	Input HIGH current	V_{CC} = Max V_{IN} = 5.5 V			1	mA
V_{IH}[3]	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}[3]	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input clamp voltage	V_{CC} = Min I_{IN} = -18 mA			-1.2	V
I_{CC}	Power supply current	V_{CC} = Max		115	160	mA

GA9101 Transmitter PECL Signals (TX, TY, TLX, TLY, SIG, SIGN)

Symbol	Description	Test Conditions	Limits[1] Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min PECL load	V_{CC} - 1.025		V_{CC} - 0.50	V
V_{OL}	Output LOW voltage	V_{CC} = Min PECL load	V_{CC} - 2.00		V_{CC} - 1.62	V
V_{CMO}	Output common mode voltage		V_{CC} - 1.60		V_{CC} -1.20	V
ΔV_{OUT}	Output differential voltage		0.75		1.2	V
I_{IL}	Input LOW current	V_{CC} = Max V_{IN} =2.4V	0.5			µA
I_{IH}	Input HIGH current	V_{CC} = Max V_{IN} = V_{CC} - 0.5 0V			250	µA
V_{IHS}	Highest Input HIGH voltage	V_{CC} = Min			V_{CC} - 0.50	V
V_{ILS}	Lowest Input LOW voltage	V_{CC} = Max	2.4			V
V_{DIF}	Differential Input voltage	V_{CC} = Min	0.4		1.2	V
V_{ICM}	Input Common Mode voltage	V_{CC} = Min	2.8		V_{CC} - 0.70	V

Notes: 1. *Typical limits are: V_{CC} = 5.0 V and T_A = 25° C.*
2. *The TTL inputs could be HIGH or LOW.*
3. *These are absolute values with respect to device ground.*
4. *No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.*

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DC Characteristics (Over operating range unless otherwise specified.)

GA9102 Receiver TTL Signals (BRXD0..9, RXCLK, SYNC, REFCLK, LOOPEN)

Symbol	Description	Test Conditions		Limits[1] Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min V_{IN}[2] = V_{IH} or V_{IL}	I_{OH} = -1.6 mA = -3.2 mA[3]	2.4	3.7		V
V_{OL}	Output LOW voltage	V_{CC} = Min V_{IN}[2] = V_{IH} or V_{IL}	I_{OL} = 4 mA = 8 mA[3]		0.2	0.5	V
I_{SC}[5]	Output short-circuit current	V_{CC} = Max	V_{OUT} = 0.5V	-15		-120	mA
I_{IL}	Input LOW current	V_{CC} = Max	V_{IN} = 0.40 V			-400	µA
I_{IH}	Input HIGH current	V_{CC} = Max	V_{IN} = 2.7 V			25	µA
I_I	Input HIGH current	V_{CC} = Max	V_{IN} = 5.5 V			1	mA
V_{IH}[4]	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}[4]	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input clamp voltage	V_{CC} = Min	I_{IN} = -18 mA			-1.2	V
I_{CC}	Power supply current	V_{CC} = Max			150	180	mA

GA9102 Receiver PECL Signals (RX, RY, RLX, RLY)

Symbol	Description	Test Conditions		Limits[1] Min.	Typ.	Max.	Unit
I_{IL}	Input LOW current	V_{CC} = Max	V_{IN} = 2.4 V	0.5			µA
I_{IH}	Input HIGH current	V_{CC} = Max	V_{IN} = V_{CC} -0.50 V			250	µA
V_{IHS}	Highest Input HIGH voltage	V_{CC} = Max				V_{CC} - 0.50	V
V_{ILS}	Lowest Input LOW voltage	V_{CC} = Min		2.4			V
V_{DIF}	Differential input voltage	V_{CC} = Min		0.4		1.2	V
V_{ICM}	Input common mode voltage	V_{CC} = Min		2.8		V_{CC} - 0.7	V

Notes: 1. *Typical limits are: V_{CC} = 5.0 V and T_A = 25°C.*
2. *The TTL inputs could be HIGH or LOW.*
3. *The RXCLK signal has an 8 mA I_{OL}. All other outputs have a 4 mA I_{OL}.*
4. *These are absolute values with respect to device ground.*
5. *No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.*

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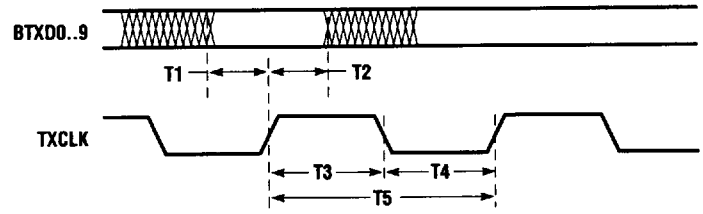
AC Specifications – GA9101 Transmitter

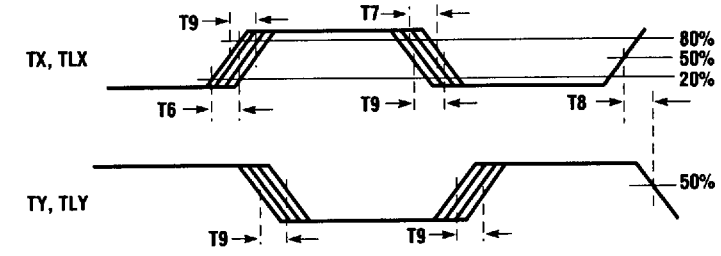
Parameter	Description	Min.	Typ.	Max.	Units
T_1	BTXD0..9 Setup Time	2.50			ns
T_2	BTXD0..9 Hold Time	2.50			ns
T_3	TXCLK Pulse Width HIGH	15.00			ns
T_4	TXCLK Pulse Width LOW	15.00			ns
T_5[1]	TXCLK Period (T)	37.30		52.00	ns
T_6	TX, TY, TLX, TLY Rise Time	250		750	ps
T_7	TX, TY, TLX, TLY Fall Time	250		750	ps
T_8	TX – TY or TLX – TLY Skew			60	ps
T_9[2]	TX , TY or TLX , TLY Output Jitter – Deterministic Jitter (DJ)			60	ps
	– Random Jitter (RJ)			275	ps
T_{10}	Propagation Delay SIG, SIGN to SIGDET			20	ns

Notes: 1. TXCLK period = (10/baud rate) ±0.01%, where baud rate is 194.4, 200.0, or 265.625 Megabaud.
2. These numbers are measured single-ended, using the High Gain Method @ 25 MHz. Please see Application Note C-7 on Jitter for more details.
3. The jitter numbers are for a BER of 10^{-12}.

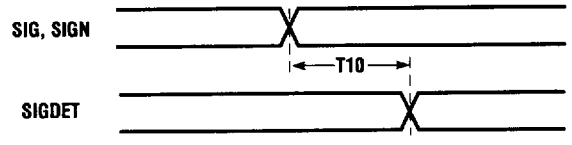
Bus Timing – GA9101 Transmitter



Serial Output Timing – GA9101



Serial Output Timing – GA9101



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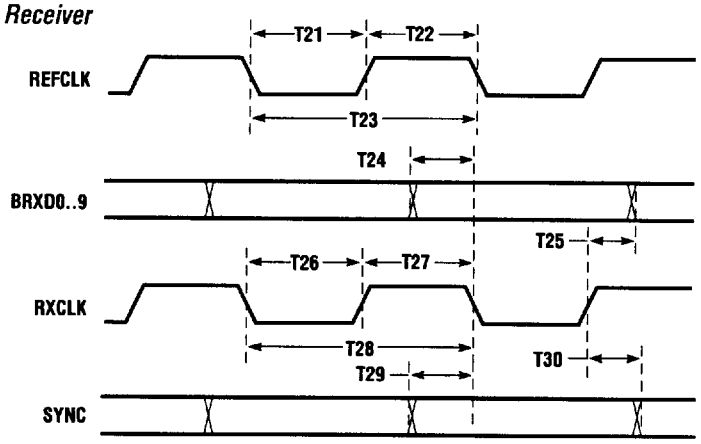
AC Specifications – GA9102 Receiver

Parameter	Description	Min.	Typ.	Max.	Units
T_{21}	REFCLK Pulse width LOW	15.00			ns
T_{22}	REFCLK Pulse width HIGH	15.00			ns
T_{23}[1]	REFCLK Period	37.30		52.00	ns
T_{24}	BRXD0..9 Valid to RXCLK ↓	$T_{28}/5$			ns
T_{25}	BRXD0..9 Time from RXCLK ↑	2.00			ns
T_{26}	RXCLK Pulse width HIGH	$(T_{28}/2)$ -2.50			ns
T_{27}	RXCLK Pulse width LOW	$(T_{28}/2)$ -2.50			ns
T_{28}[1]	RXCLK Period	37.30		52.00	ns
T_{29}	SYNC Valid to RXCLK ↓	$T_{28}/5$			ns
T_{30}	SYNC Time from RXCLK ↑	2.00			ns
T_{31}[2]	RX, RY, RLX, RLY Rise time			1.50	ns
T_{32}[2]	RX, RY, RLX, RLY Fall time			1.50	ns
T_{33}	RX – RY or RLX – RLY Skew			0.60	ns
T_{34}	RX, RY, RLX, RLY Peak-to-peak input jitter[3]	$0.07 * T_{28}$			ns

Notes: 1. REFCLK and RXCLK period = (10/baud rate) ±0.01%, where baud rate is 194.4, 200.0, or 265.625 Megabaud.
2. Measured at $V_{DIFF} = 0.4$ V.
3. The jitter numbers are for a BER of 10^{-12}.

Bus Timing – GA9102 Receiver



Synchronization Times

Description	Min.	Typ.	Max.	Units
Power Up or application of REFCLK			1	ms
Application of valid data			200	µs
Resynchronization after phase shift on data			2500	bit time

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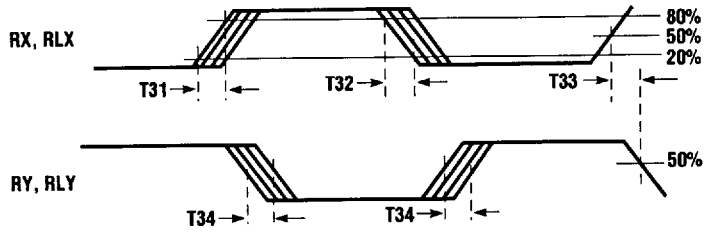
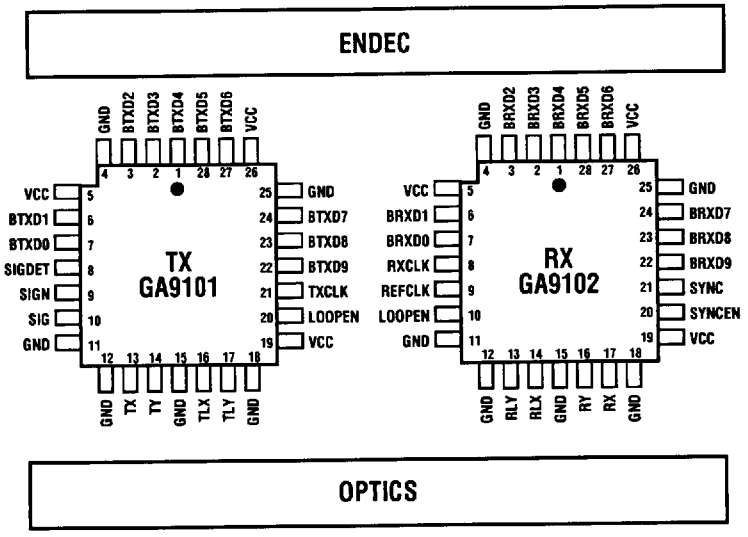
Serial Input Timing – GA9102



Pinouts for GA9101 and GA9102

The pinouts for the Transmitter and Receiver have been selected for easy interface to the ENDEC and the optics.



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Pin Definitions GA9101

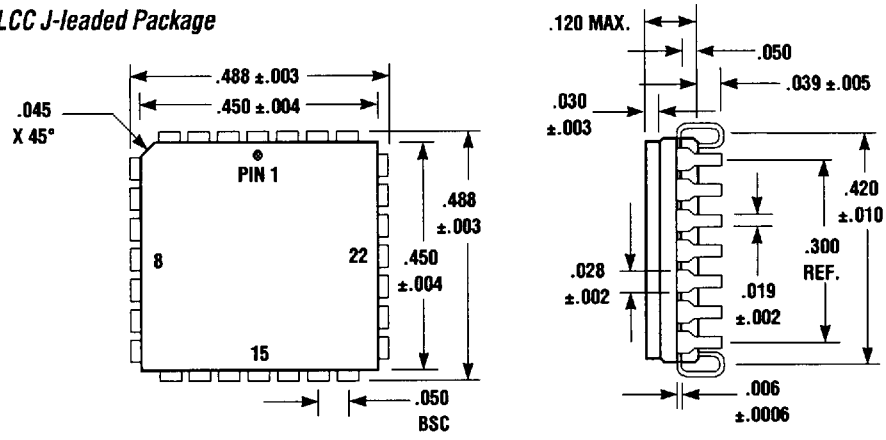
Symbol	Pin #	I/O	Qty.	Logic Level	Active	Description
TX, TY	13, 14	OUTPUT	2	PECL	NRZ	Differential Serial Data Output
TLX, TLY	16, 17	OUTPUT	2	PECL	NRZ	Diff. Serial Data Output, Loopback
SIGN, SIG	9, 10	INPUT	2	PECL	HIGH	Optical Signal Present
BTXD0..9	7, 6, 3-1, 28, 27, 24-22	INPUT	10	TTL	HIGH	Transmit Data Input
TXCLK	21	INPUT	1	TTL	HIGH	Transmit Clock
LOOPEN	20	INPUT	1	TTL	HIGH	Enable Loopback
SIGDET	8	OUTPUT	1	TTL	HIGH	Signal Detected
VCC	5, 19, 26	INPUT	3	N/A	N/A	+5 Volt Supply
GND	4, 11, 12, 15, 18, 25	INPUT	6	N/A	N/A	Ground

Pin Definitions GA9102

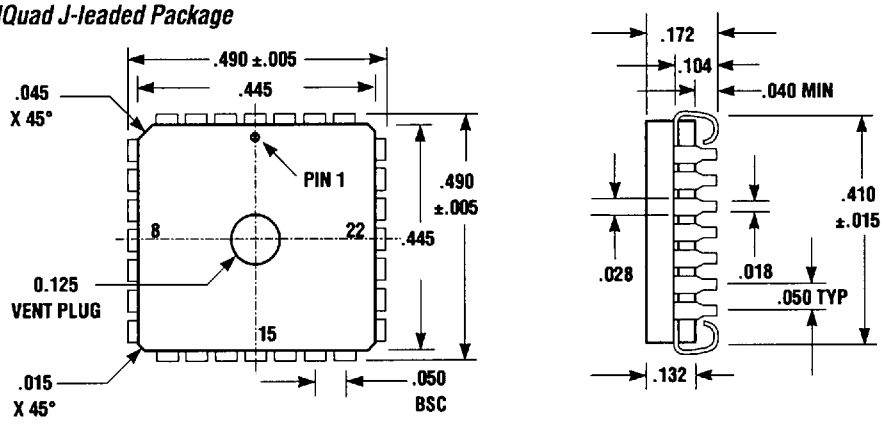
Symbol	Pin #	I/O	Qty.	Logic Level	Active	Description
RX, RY	17, 16	INPUT	2	PECL	NRZ	Differential Serial Data Input
RLX, RLY	14, 13	INPUT	2	PECL	NRZ	Diff. Serial Data Input, Loopback
BRXD0..9	7, 6, 3-1, 28, 27, 24-22	OUTPUT	10	TTL	HIGH	Receive Output Data
RXCLK	8	OUTPUT	1	TTL	HIGH	Receive Clock
SYNC	21	OUTPUT	1	TTL	HIGH	Receive Byte Sync
LOOPEN	10	INPUT	1	TTL	HIGH	Enable Loopback
REFCLK	9	INPUT	1	TTL	HIGH	Oscillator Clock (19.44, 20.00, 26.5625 MHz)
SYNCEN	20	INPUT	1	TTL	HIGH	Align to K28.5
VCC	5, 19, 26	INPUT	3	N/A	N/A	+5 Volt Supply
GND	4, 11, 12, 15, 18, 25	INPUT	6	N/A	N/A	Ground

8906218 0000874 229

28-Pin CLCC J-leaded Package



28-Pin MQuad J-leaded Package



Ordering Information

For Fiber Channel applications, order the chip set as FC-265. **FC–265**

GA9101 - 2CC – Transmitter
GA9102 - 2CC – Receiver
GA9103 - 2CC – ENDEC

For ESCON/ATM applications, order the chip set as FC-200. **FC–200**

GA9101 - 2CC – Transmitter
GA9102 - 2CC – Receiver
GA9104 - 2CC – ENDEC

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Section 6 - Packaging

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Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$P_D = (T_J - T_A) / \theta J_A, \text{ where:}$$

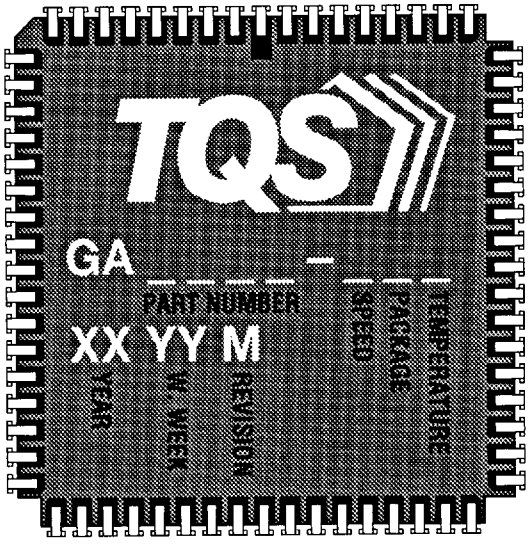
P_D = power dissipation at ambient operating temperature
T_J = maximum junction operating temperature (150°C is typically used)
T_A = maximum ambient operating temperature (free air)
θJ_A = typical thermal resistance of junction to ambient (°C/W)

Packaging Notes

Unless otherwise indicated, all thermal impedances listed are typical range values or values in still air for the package only. These impedances will vary when additional heat sinking capability is provided through PCB solder attachment or air flow.

Device Markings

TriQuint's Standard Device Markings



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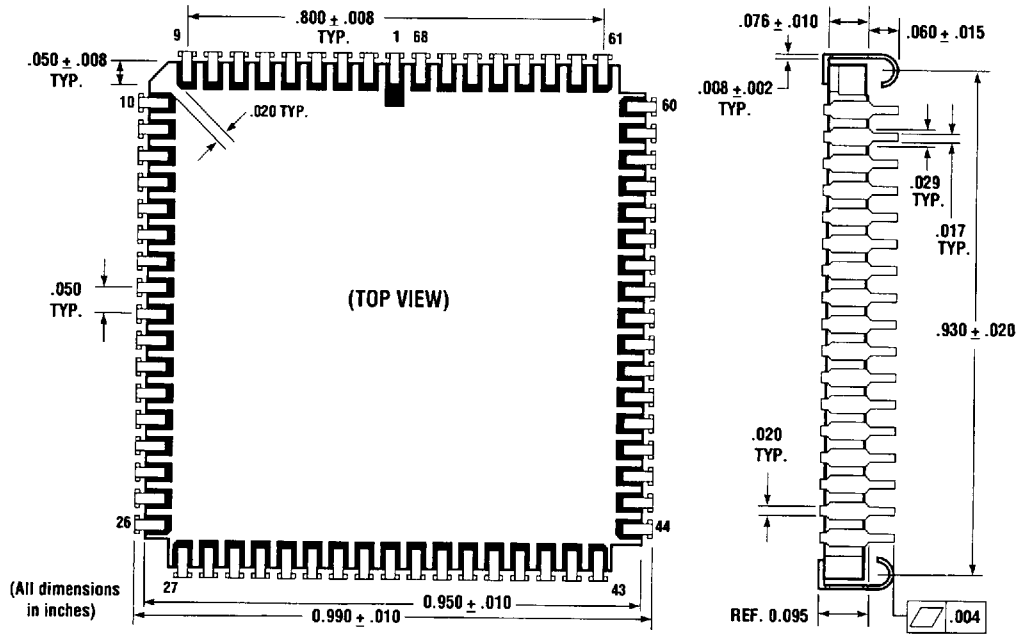
Package Outlines

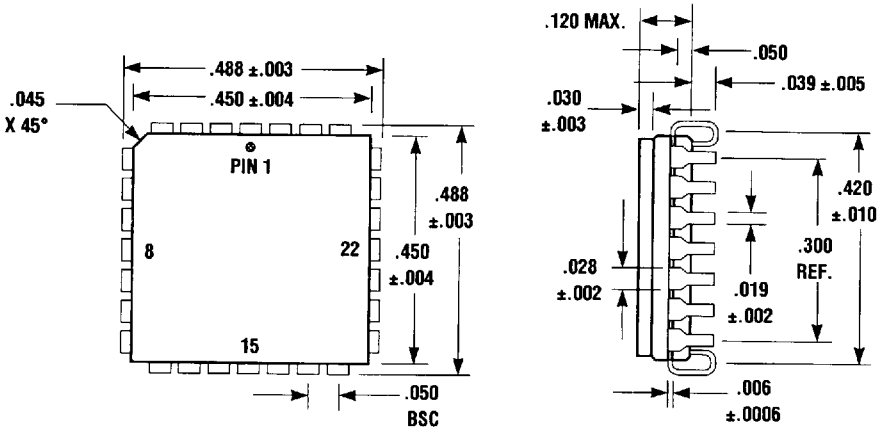
68-Pin J-Lead (CLCC) Package

Packaging for: GA9011, GA9012 (θJ_A = 25°C/Watt)



28-Pin J-Lead CerQuad Package

Packaging for: GA9101, GA9102 (θJ_A = 60°C/Watt)



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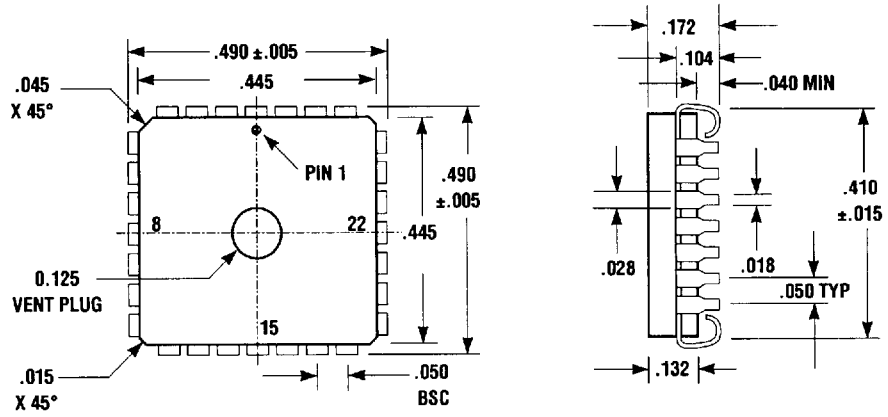
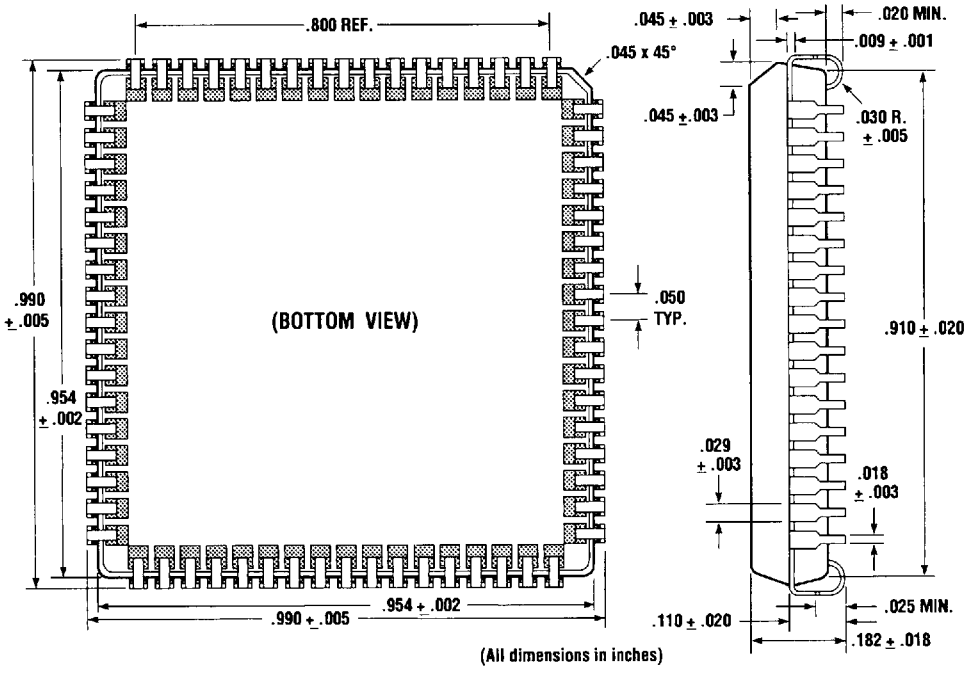
28-Pin J-Lead MQuad Package

Packaging for: GA9101, GA9102 (θJ_A = 42°C/Watt)



68-Pin PLCC Package

Packaging for: GA9103, GA9104 (θJ_A = 47°C/Watt)



(All dimensions in inches)

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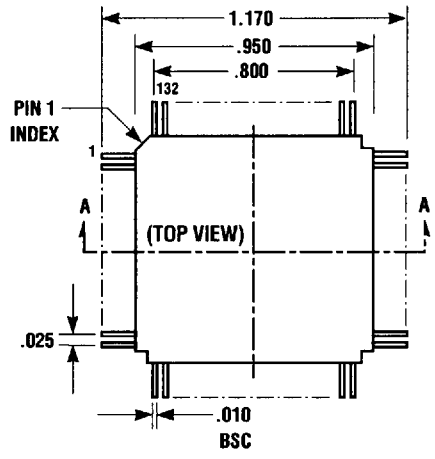
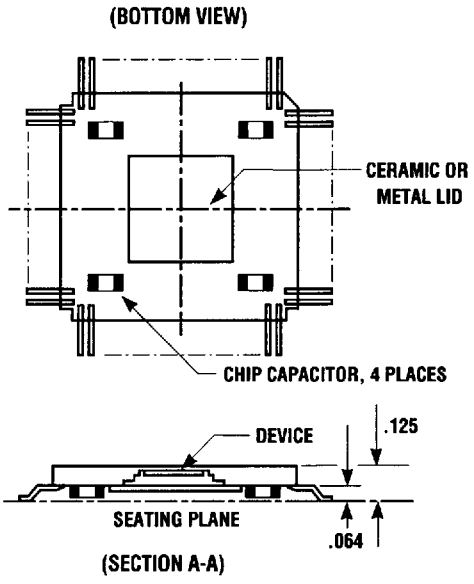
132-Pin Leaded Ceramic Chip Carrier

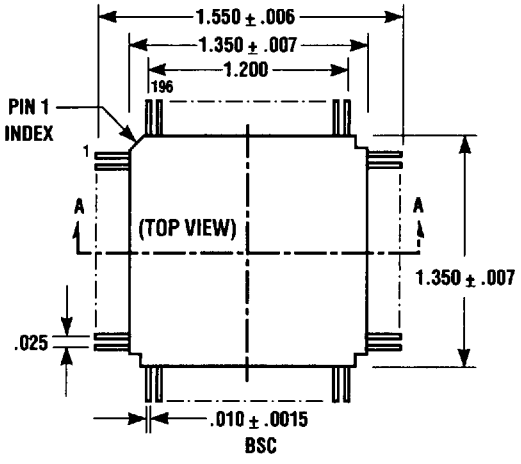
Packaging for: TQ8016 (Heat sink required, θJ_C = 8°C/Watt)

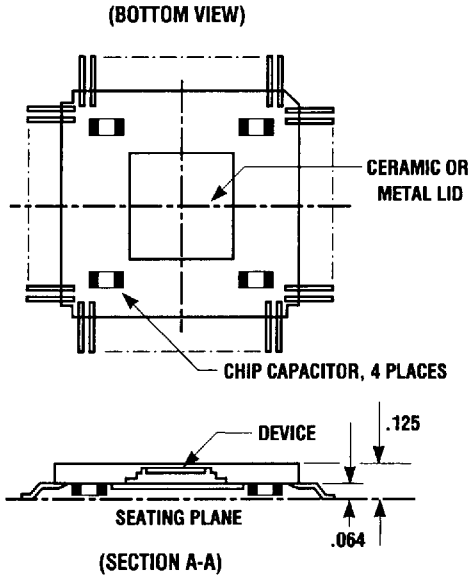




196-Pin Leaded Ceramic Chip Carrier

Packaging for: TQ8032 (Heat sink required, θJ_C = 8°C/Watt)





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