

Motor Driver IC Series for Tape Record System

3 in 1 Motor Driver

for Digital Video Camera

BD6637KV/KS, BD6300KU



●Description

The low power consumption, 3 in 1 motor driver, utilizes a DMOS linear output driver. It integrates the capstan, cylinder, loading motor driver, and amplifier of each sensor signal that is required for digital video camera systems.

●Features

- 3-phase motor driver for capstan
 - 1) 3-phase full wave drive system (pseudo-linear)
 - 2) Output stage DMOS drive system
 - 3) Built-in torque ripple canceling circuit
 - 4) Built-in output Tr saturation preventing circuit (lower)
 - 5) Equipped with a VM power supply control terminal
 - 6) Built-in normal, reverse, and short brake function
 - 7) Built-in FG sensor amplifier

- 3-phase sensor-less motor driver for cylinder
 - 1) Soft switching drive system
 - 2) Output stage DMOS drive system
 - 3) Built-in output Tr saturation preventing circuit (lower)
 - 4) Equipped with a VM power supply control terminal
 - 5) Built-in startup circuit
 - 6) Built-in FG/PG sensor amplifier

- Reversible motor driver for loading
 - 1) Output stage DMOS drive system
 - 2) Normal/Reverse rotation and braking 3 mode output
 - 3) Any setting of output voltage with L_REF terminal available

- Built-in TSD
- Built-in voltage rise circuit
- Power saving function

●Applications

Portable video equipment, such as digital video cameras, VTR, and 8-mm video cameras.

●Product lineup

Item	BD6637KV/KS	BD6300KU
Capstan	3-phase pseudo-linear drive (DMOS linear drive)	3-phase pseudo-linear drive (DMOS linear drive)
Cylinder	3-phase sensor-less soft switching drive (DMOS linear drive)	3-phase sensor-less soft switching drive (DMOS linear drive)
Loading	DMOS H bridge drive	DMOS H bridge drive
Sensor Amplifier	Capstan FG signal, Cylinder PG signal (coil sense), Cylinder FG signal waveform coordinate	Capstan FG signal, Cylinder PG signal (hall sense), Cylinder FG signal, Reel sensor signal waveform coordinate
Package	VQFP64/SQFP56	UQFP64

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limit	Unit
Supply voltage		VCC	7	V
		UNREG	15	V
		C_VM	10	V
		D_VM	10	V
		L_VM	7	V
Power dissipation	BD6637KV/KS	Pd	1250 *	mW
	BD6300KU		1750 *	mW
Operate temperature		T _{opr}	-25~+75	°C
Storage temperature		T _{stg}	-40~+150	°C
Junction temperature		T _{jmax}	150	°C
Output max current	BD6637KV/KS	I _{omax}	1000 * *	mA
	BD6300KU		800 *	mA

* 70mm × 70mm × 1.6mm glass epoxy board. Reduced by 14mW/°C when Ta=25°C

* * However, do not exceed Pd, ASO and T_j=150°C(Common to 3 drivers)

●Operating conditions

Supply voltage	VCC	2.7 ~ 4.5	V
	UNREG	5 ~ 12 *	V
	C_VM	0 ~ 8 *	V
	D_VM	0 ~ 8 *	V
	L_VM	4.5 ~ 5.5	V

* UNREG ≥ C_VM
UNREG ≥ D_VM
L_VM ≥ VCC

●Electrical characteristics

BD6637KV/KS (Unless otherwise specified Ta=25°C, VCC=3V, C_VM=D_VM=L_VM=5V, UNREG=7.2V)

Parameter	Symbol	Limit			Unit	Conditions	Fig No.
		Min.	Typ.	Max.			
<TOTAL>							
VCC Circuit current 1	I _{CC1}	6	13	20	mA	Power save OFF	Fig.1
VCC Circuit current 2	I _{CC2}	—	—	5	μA	Power save ON	Fig.2
UNREG stand by current	I _{UNREG}	—	—	5	μA	Power save ON	Fig.3
PS input switching level	PS	0.6	1.4	2	V		—
VG voltage	VG	9.5	11	12.5	V		Fig.4,5
<CAPSTAN OUTPUT>							
Output H voltage	C_VO _H	—	0.35	0.55	V	I _{OUT} =-400mA	Fig.6
Output L voltage	C_VO _L	—	0.4	0.65	V	I _{OUT} =400mA, C _{RNF} =0.33Ω	Fig.7
<CAPSTAN HALL AMP>							
In-phase input voltage range	C_V _{CM}	1.2	—	VCC-1.1	V		—
Hall input offset range	C_V _{HOF}	-15	—	15	mV		—
<CAPSTAN F/B/R>							
Forward rotation control	C_V _{FWD}	—	—	0.7	V		—
Brake voltage range	C_V _{BRK}	1.3	1.5	1.7	V		—
Reverse rotation control	C_V _{REV}	2.3	—	—	V		—
<CAPSTAN TORQUE CONTROL>							
EC input bias current	C_I _{EC}	—	3	7.5	μA	C_EC=VCC	—
Torque control input/output gain	C_G _{IO}	0.35	0.5	0.65	A/V	C _{RNF} =0.33Ω, C _{RCC} =3.3kΩ	Fig.8
Torque control start voltage	C_V _{ECOFFS}	1.05	1.2	1.35	V		Fig.8
Current limit voltage	C_C _{limit}	0.2	0.24	0.28	V	C _{RNF} =0.33Ω, C _{RCC} =3.3kΩ	Fig.8
Ripple cancel ratio	C_V _{RCC}	8	20	32	%	I _{OUT} =400mA, C _{RCC} =3.3kΩ	—
<CAPSTAN VS>							
Voltage gain	C_G _{VS}	7	8	9	TIMES		—
Output H voltage	C_V _{VS_{OH}}	—	0.5	0.8	V	I _{ovs} =1mA,	—
Output L voltage	C_V _{VS_{OL}}	—	0.13	0.2	V	I _{ovs} =50 μA	—
VS offset voltage	C_V _{VS_{OFFS}}	0.12	0.25	0.38	V	DC/DC × 3 in use	—
<CAPSTAN FGAMP>							
Input offset voltage	C_V _{FG_{OFFS}}	-12	—	12	mV		—
DC bias voltage	C_V _{FG}	1.3	1.5	1.7	V		—
Voltage gain 1	C_A _{V1}	50	59	—	dB	f=3kHz	Fig.20
Voltage gain 2	C_A _{V2}	30	36	—	dB	f=50kHz	Fig.20
In-phase input voltage range	C_V _{FG_{CM}}	0.35	—	VCC-1.1	V		—
Output H voltage	C_V _{FG_{A_{OH}}}	—	0.3	0.5	V	I _{OH} =0.2mA,	—
Output L voltage	C_V _{FG_{A_{OL}}}	—	0.1	0.3	V	I _{OL} =1mA	—
<CAPSTAN FG _{HYS} >							
C _{FG} hysteresis width	C_V _{FG_{HYS}}	±30	±46	±62	mV		Fig.22
DC bias voltage	C_V _{FG+}	1.3	1.5	1.7	V		—
Output L voltage	C_V _{FG_{SOL}}	—	0.1	0.3	V	I _{OL} =1mA	Fig.21
<CYLINDER OUTPUT>							
Output H voltage	D_VO _H	—	0.3	0.5	V	I _{OUT} =-400mA	Fig.9
Output L voltage	D_VO _L	—	0.4	0.65	V	I _{OUT} =400mA, C _{RNF} =0.33Ω	Fig.10
<CYLINDER TORQUE CONTROL>							
EC input bias current	D_I _{EC}	—	2	5	μA	D_EC=VCC	—
Torque control input/output gain	D_G _{IO}	0.45	0.66	0.87	A/V	D _{RNF} =0.33Ω	Fig.11
Torque control start voltage	D_V _{ECOFFS}	1.05	1.2	1.35	V		Fig.11
Current limit voltage	D_C _{limit}	0.217	0.274	0.332	V	D _{RNF} =0.33Ω	Fig.11

Parameter	Symbol	Limit			Unit	Conditions	Fig No.
		Min.	Typ.	Max.			
<CYLINDER STARTING/DETECTION/SLOPE>							
DETECT terminal charge current	D_IDETO	2	5	10	μA		Fig.12
DETECT terminal discharge current	D_IDETI	2	5	10	μA		Fig.12
DETECT terminal H voltage	D_VDETH	1.1	1.3	1.5	V		Fig.13
DETECT terminal L voltage	D_VDETL	0.5	0.65	0.8	V		Fig.13
ISET voltage	D_VISET	0.32	0.4	0.48	V	R _{D_ISET} =18kΩ	Fig.14
SL1,2 charge current	D_ISLO	16	22	28	μA	R _{D_ISET} =18kΩ	Fig.15
SL1,2 discharge current	D_ISLI	17	24	31	μA	R _{D_ISET} =18kΩ	Fig.15
SL1,2 H voltage	D_VSLH	2.5	2.8	—	V		Fig.16
SL1,2 L voltage	D_VSLL	0.85	1	1.15	V		Fig.16
SL1,2 charge and discharge current ratio	D_RSL	0.82	0.89	0.96			—
SL switching EC level	D_VECSL	1.6	2	2.4	V		—
< CYLINDER VS>							
Voltage gain	D_Gvs	7	8	9	TIMES		—
Output H voltage	D_VVSOH	—	0.5	0.8	V	I _{ovs} =1mA, between VCC and output	—
Output L voltage	D_VVSOL	—	0.13	0.2	V	I _{ovs} =50 μA	—
VS offset voltage	D_VVSOFs	0.12	0.25	0.38	V	DC/DC × 3 in use	—
<CYLINDER FGAMP>							
Input offset voltage	D_VFGOFs	-12	—	12	mV		—
DC bias voltage	D_VFG+	1.3	1.5	1.7	V		—
Voltage gain 1	D_FAV1	50	59	—	dB	f=3kHz	Fig.20
Voltage gain 2	D_FAV2	30	36	—	dB	f=50kHz	Fig.20
In-phase input voltage range	D_VFGCM	0.35	—	VCC-1.1	V		—
Output H voltage	D_VFGAOH	—	0.3	0.5	V	I _{OH} =-0.2mA, between VCC and output	—
Output L voltage	D_VFGAOL	—	0.15	0.35	V	I _{OL} =1mA	—
<CYLINDER FGHYS>							
D_FG hysteresis width	D_VFGHYS	±84	±110	±136	mV	Measure D_FGAMP at 1K feed back resistance	Fig.24
DC bias voltage	D_VFG+	1.3	1.5	1.7	V	Measure D_FGAMP at 1K feed back resistance	—
Output L voltage	D_VFGSOL	—	0.1	0.3	V	I _{OL} =1mA	Fig.21
<CYLINDER PGAMP>							
Input offset voltage	D_VPGOFs	-12	—	17	mV		—
DC bias voltage	D_VPG+	1.3	1.5	1.7	V		—
Voltage gain 1	D_PAV1	50	59	—	dB	f=3kHz	Fig.20
Voltage gain 2	D_PAV2	30	36	—	dB	f=50kHz	Fig.20
In-phase input voltage range	D_VPGCM	0.35	—	VCC-1.1	V		—
Output H voltage	D_VPGAOL	—	0.3	0.5	V	I _{OH} =-0.2mA, between VCC and output	—
Output L voltage	D_VPGAOL	—	0.15	0.35	V	I _{OL} =1mA	—
<CYLINDER PGHYS>							
D_PG hysteresis width	D_VPGHYS	±118	±144	±170	mV		Fig.23
DC bias voltage	D_VPG+	1.3	1.5	1.7	V		—
Output L voltage	D_VPGSOL	—	0.1	0.3	V	I _{OL} =1mA	Fig.21
<LOADING>							
Output saturation voltage	L_VSAT	—	0.3	0.5	V	I _{OUT} =200mA, L_REF=L_VM Total saturation voltage of low and high side output transistor	Fig. 17, 18
L_REF pin input current	L_IREF	—	0.3	2	μA		—
Vout-L_REF offset	L_VOFs	0	100	200	mV		Fig.19
Forward rotation control voltage range	L_VFWD	—	—	0.7	V		—
Brake voltage range	L_VBRK	1.3	1.5	1.7	V		—
Reverse rotation control voltage range	L_VREV	2.3	—	—	V		—
L_REF output open voltage	L_VREF	—	—	1.3	V		—

●Electrical characteristics

BD6300KU (Unless otherwise specified Ta=25°C, VCC=3V, C_VM=D_VM=L_VM=5V, UNREG=7.2V)

Parameter	Symbol	Limit			Unit	Conditions	Fig No.
		Min.	Typ.	Max.			
<TOTAL>							
VCC Circuit current 1	Icc1	5	11	17	mA	Power save OFF	Fig.25
VCC Circuit current 2	Icc2	1	4	7	mA	Power save ON	Fig.26
VG voltage	VG	9.5	11	12.5	V		Fig. 28,29
<CAPSTAN OUTPUT>							
Output H voltage 1	C_VOH1	—	0.1	0.16	V	I _{OUT} =-200mA	Fig.31
Output H voltage 2	C_VOH2	—	0.2	0.32	V	I _{OUT} =-400mA	Fig.31
Output L voltage	C_VOL	—	0.2	0.32	V	I _{OUT} =200mA, C _{RNF} =0.33Ω	Fig.32
<CAPSTAN HALL AMP>							
In-phase input voltage range	C_VCM	1.2	—	VCC-1.1	V		—
Hall input offset range	C_VHOF	-15	—	15	mV		—
<CAPSTAN PS, F/B/R>							
C_PS input threshold level	C_PS	0.7	1.4	2	V		—
Forward rotation control voltage range	C_VFWD	—	—	0.7	V		—
Brake voltage range	C_VBRK	1.3	1.5	1.7	V		—
Reverse rotation control voltage range	C_VREV	2.3	—	—	V		—
<CAPSTAN TORQUE CONTROL>							
EC input bias current	C_IEC	—	3	7.5	μA	C_EC=VCC	—
Torque control input/output gain	C_GIO	0.42	0.6	0.78	A/V	C _{RNF} =0.33Ω, C _{RCC} =3.3kΩ	Fig.30
Torque control start voltage	C_VECOFS	1.05	1.2	1.35	V		Fig.30
Current limit voltage	C_Climit	0.25	0.33	0.41	V	C _{RNF} =0.33Ω, C _{RCC} =3.3kΩ	Fig.30
Ripple cancel ratio	C_VRCC	22	45	68	%	I _{OUT} =100mA, C _{RCC} =3.3kΩ C _{RNF} =0.33Ω	—
<CAPSTAN VS>							
Voltage gain	C_Gvs	7	8	9	TIMES		—
Output H voltage	C_VVSOH	—	0.5	0.8	V	I _{OV} =1mA, between VCC and output	—
Output L voltage	C_VVSOL	—	0.13	0.2	V	I _{OV} =50μA	—
<CAPSTAN FGAMP>							
In-phase input voltage range	C_VFGCM	0.35	—	VCC-1.1	V		—
Input bias current	C_IFG	—	—	1	μA		—
Output H voltage	C_VFGSOH	2.8	—	—	V		—
Output L voltage	C_VFGSOL	—	0.1	0.3	V	I _{OL} =1mA	Fig.44
<CYLINDER OUTPUT>							
Output H voltage	D_VOH	—	0.3	0.48	V	I _{OUT} =-400mA	Fig.34
Output L voltage	D_VOL	—	0.28	0.4	V	I _{OUT} =100mA, C _{RNF} =0.33Ω	Fig.35
<CYLINDER OUTPUT>							
D_PS input threshold level	D_PS	0.7	1.4	2	V		—
<CYLINDER TORQUE CONTROL>							
EC input bias current	D_IEC	—	2	5	μA	D_EC=VCC	—
Torque control input/output gain	D_GIO	0.45	0.66	0.87	A/V	D _{RNF} =0.33Ω	Fig.33
Torque control start voltage	D_VECOFS	1.05	1.2	1.35	V		Fig.33
Current limit voltage	D_Climit	0.217	0.274	0.332	V	D _{RNF} =0.33Ω	Fig.33
<CYLINDER STARTING/DETECTION>							
DETECT terminal charge current	D_IDETO	2	5	10	μA		Fig.36
DETECT terminal discharge current	D_IDETI	2	5	10	μA		Fig.36
DETECT terminal H voltage	D_VDETH	1.1	1.3	1.5	V		Fig.37
DETECT terminal L voltage	D_VDETL	0.5	0.65	0.8	V		Fig.37

Parameter	Symbol	Limit			Unit	Conditions	Fig No.
		Min.	Typ.	Max.			
<CYLINDER SLOPE>							
ISET voltage	D_V _{ISET}	0.32	0.4	0.48	V	R _{D_ISET} =18kΩ	Fig.38
SL1,2 charge current	D_I _{SLO}	16	22	28	μA	R _{D_ISET} =18kΩ	Fig.39
SL1,2 discharge current	D_I _{SLI}	17	24	31	μA	R _{D_ISET} =18kΩ	Fig.39
SL1,2 H voltage	D_V _{SLH}	2.5	2.8	—	V		Fig.40
SL1,2 L voltage	D_V _{SLL}	0.85	1	1.15	V		Fig.40
SL1,2 charge and discharge current ratio	D_R _{SL}	0.82	0.89	0.96			—
< CYLINDER VS>							
Voltage gain	D_G _{vs}	7	8	9	TIME		—
Output H voltage	D_V _{VSOH}	—	0.5	0.8	V	I _{ovs} =-1mA, between VCC and output	—
Output L voltage	D_V _{VSOL}	—	0.13	0.2	V	I _{ovs} =50A	—
<CYLINDER FGAMP/SMT>							
DC bias voltage	D_V _{FG+}	1.3	1.5	1.7	V		—
In-phase input voltage range	D_V _{FGCM}	0.35	—	VCC-1.1	V		—
DC bias current	D_I _{FG}	—	—	1	μA		—
Output H voltage	D_V _{FGSO}	2.8	—	—	V		—
Output L voltage	D_V _{FGSO}	—	0.1	0.3	V	I _{oL} =1mA	Fig.45
<CYLINDER PGAMP>							
DC bias voltage	D_V _{PG+}	1.3	1.5	1.7	V		—
In-phase input voltage range	D_V _{PGC}	0.35	—	VCC-1.1	V		—
Output H voltage	D_V _{PGSO}	2.8	—	—	V		—
Output L voltage	D_V _{PGSO}	—	0.14	0.3	V		Fig.46
<LOADING>							
Output saturation voltage	L_V _{SAT}	—	0.3	0.5	V	I _{OUT} =200mA, L_REF=L_VM Total saturation voltage of low and high side output transistor	Fig. 41,42
L_REF pin input current	L_I _{REF}	—	0.3	2	μA	L_REF=L_VM	—
V _{out} -L_REF offset	L_V _{OFS}	—	100	200	mV		Fig.43
Forward rotation control voltage range	L_V _{FWD}	—	—	0.7	V		—
Brake voltage range	L_V _{BRK}	1.3	1.5	1.7	V		—
Reverse rotation control voltage range	L_V _{REV}	2.3	—	—	V		—
L_REF output open voltage	L_V _{REF}	—	—	1.3	V		—
<REEL AMP>							
Input bias current	R_I _{IN}	—	—	1	μA		—
Input offset voltage	R_V _{OFS}	-8	—	8	mV		—
In-phase input voltage range	R_V _{INCM}	0.35	—	VCC-1.1	V		—
Output L voltage	R_V _{SOL}	—	0.1	—	V	I _{oL} =1mA	Fig.47

●Reference data

BD6637KV/KS Characteristic data

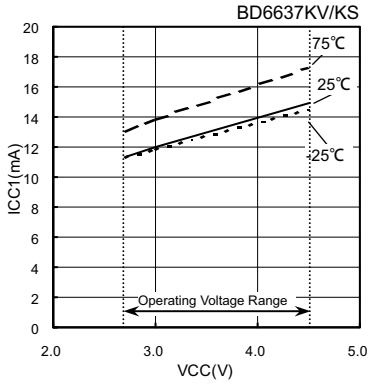


Fig.1 VCC Circuit current 1

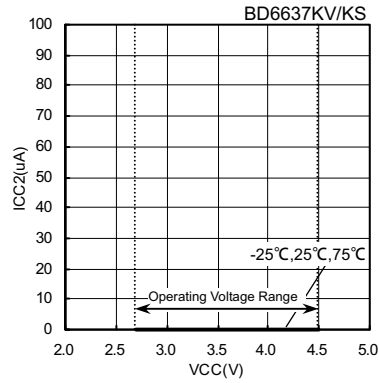


Fig.2 VCC Circuit current 2

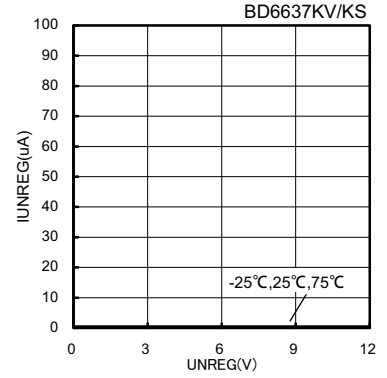


Fig.3 UNREG stand by current

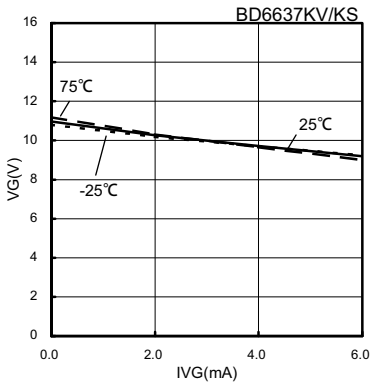


Fig.4 VG voltage
(Temperature characteristics)

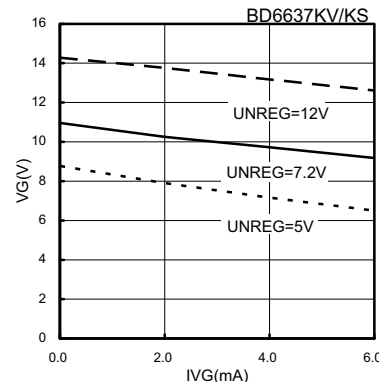


Fig.5 VG voltage
(Voltage characteristics)

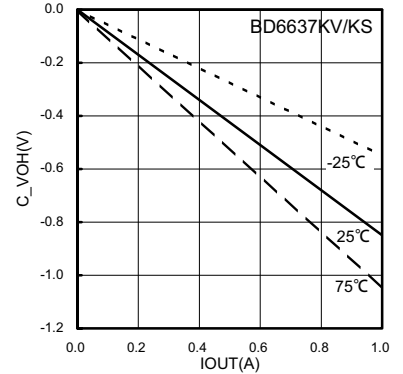


Fig.6 CAPSTAN Output High-voltage

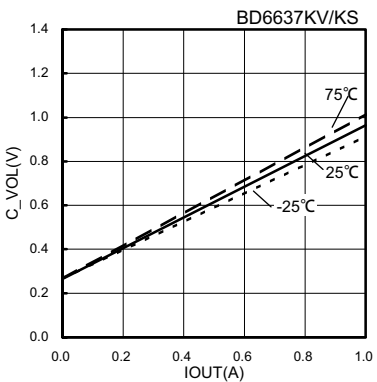


Fig.7 CAPSTAN Output High-voltage

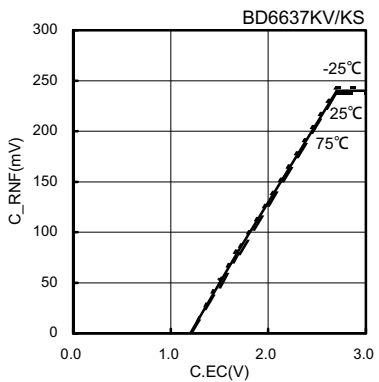


Fig.8 CAPSTAN Torque control
input/output gain

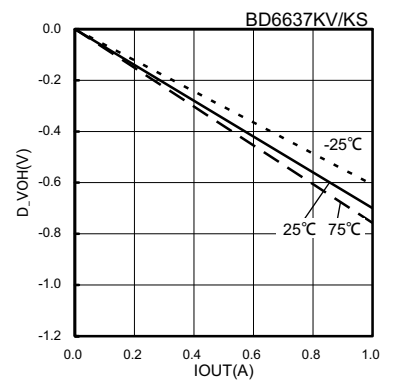


Fig.9 CYLINDER Output
High-voltage

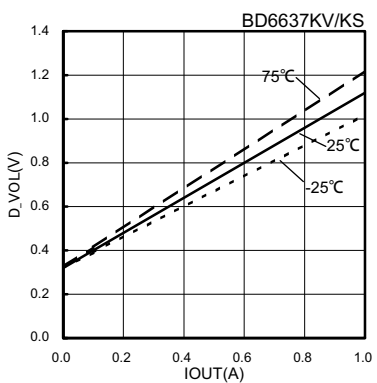


Fig.10 CYLINDER
Output Low-voltage

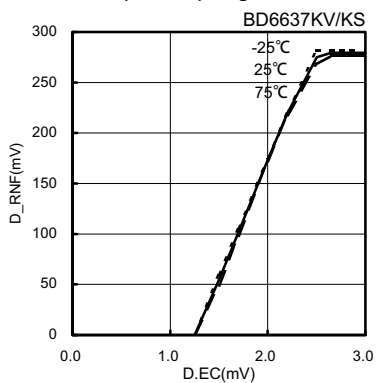


Fig.11 CYLINDER Torque control
input/output gain

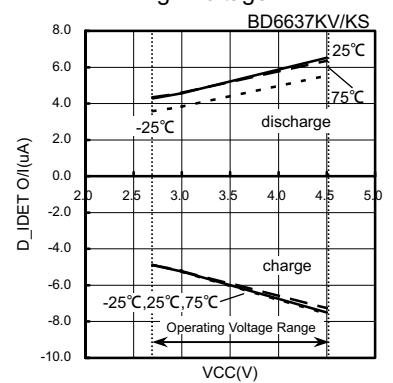


Fig.12 DETECT terminal
charge/discharge current

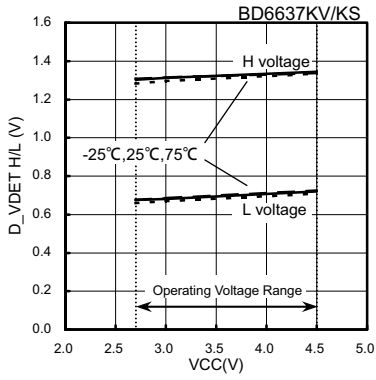


Fig.13 DETECT terminal H/L voltage

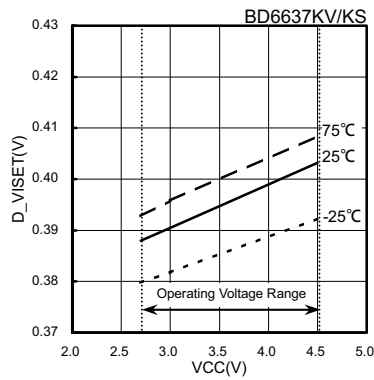


Fig.14 ISET voltage

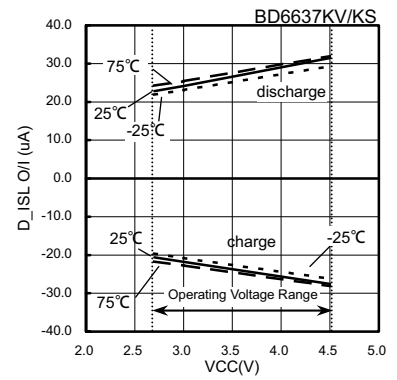


Fig.15 SL1,2 charge/discharge current

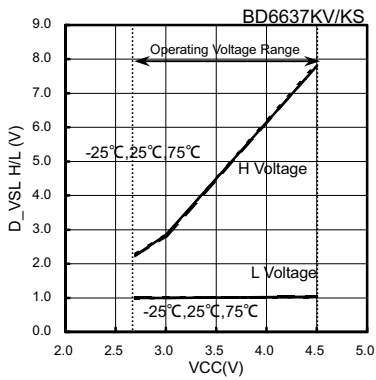


Fig.16 SL1,2 H/L voltage

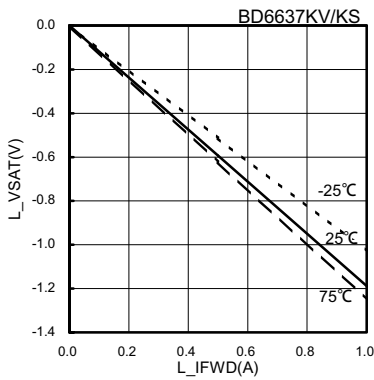


Fig.17 LOADING Output High-voltage

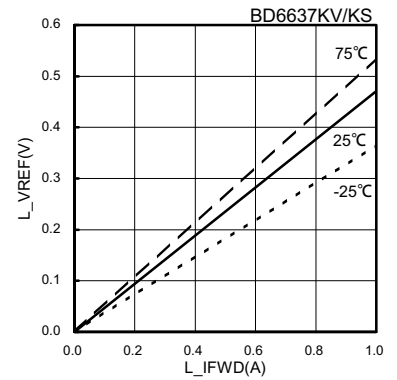


Fig.18 LOADING Output Low-voltage

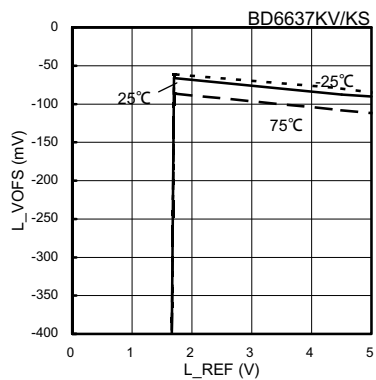


Fig.19 Vout-L_REF offset

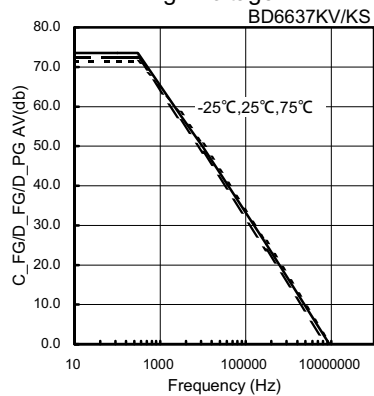


Fig.20 C_FG/D_FG/D_PG Voltage gain

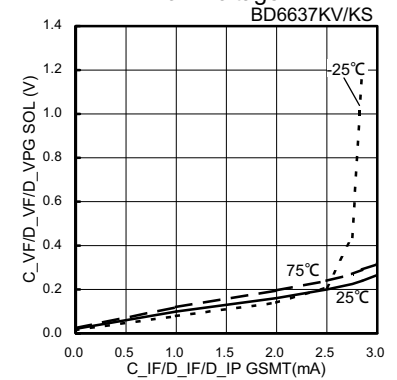


Fig.21 C_FG/D_FG/D_PG Output Low-voltage

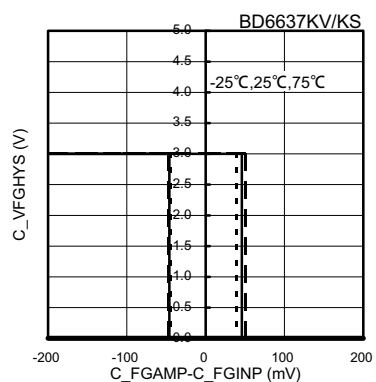


Fig.22 C_FG hysteresis width

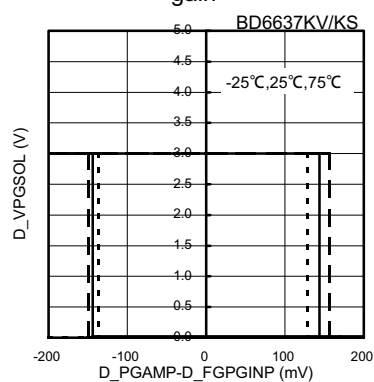


Fig.23 D_PG hysteresis width

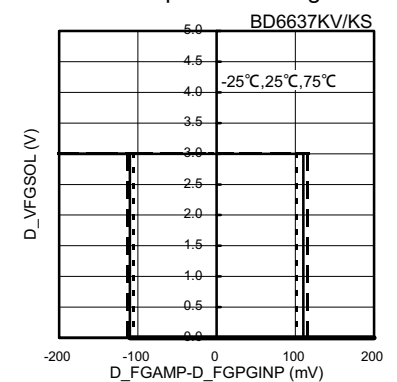


Fig.24 D_FG hysteresis width

●Reference data

BD6300KU Characteristic data

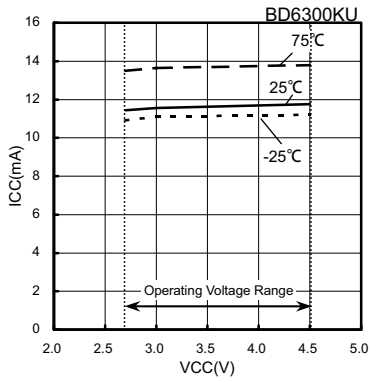


Fig.25 VCC Circuit current 1

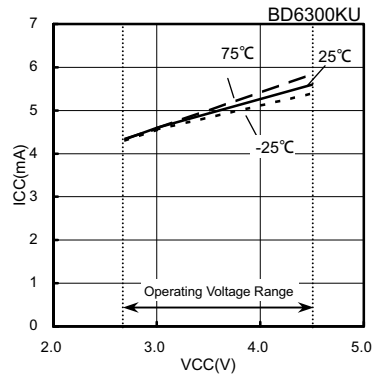


Fig.26 VCC Circuit current 2

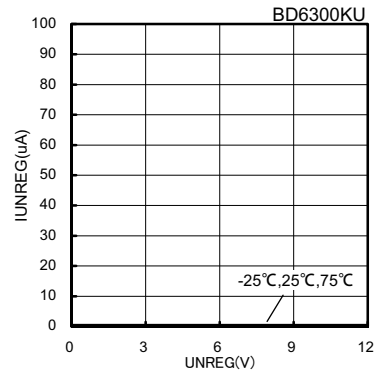


Fig.27 UNREG stand by current

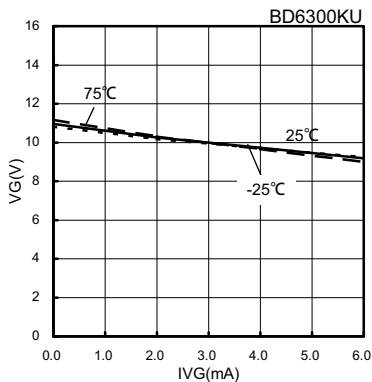


Fig.28 VG voltage
(Temperature characteristics)

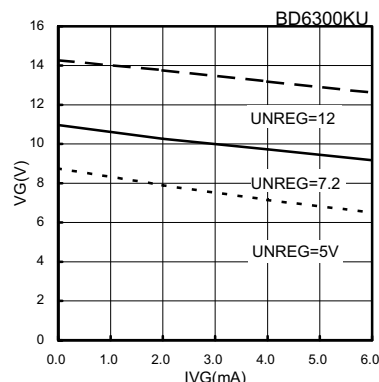


Fig.29 VG voltage
(Voltage characteristics)

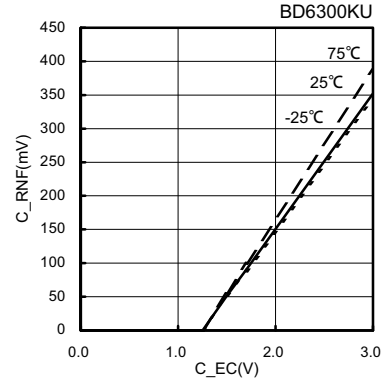


Fig.30 CAPSTAN
Torque control input/output gain

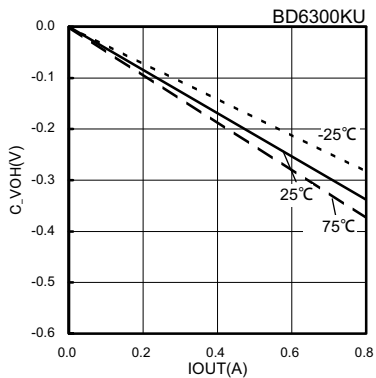


Fig.31 CAPSTAN Output
High-voltage

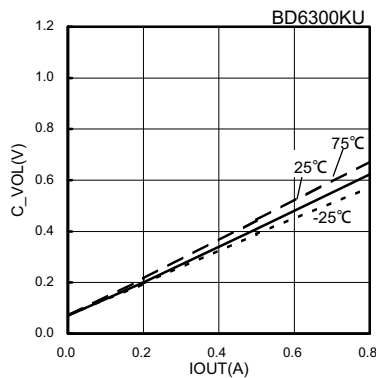


Fig.32 CAPSTAN Output
Low-voltage

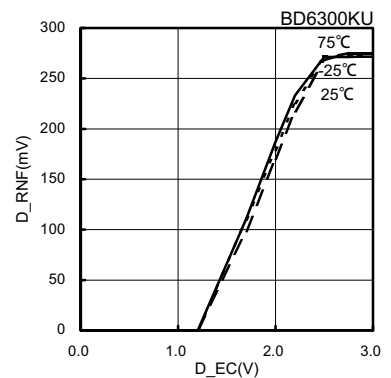


Fig.33 CYLINDER Torque control
input/output gain

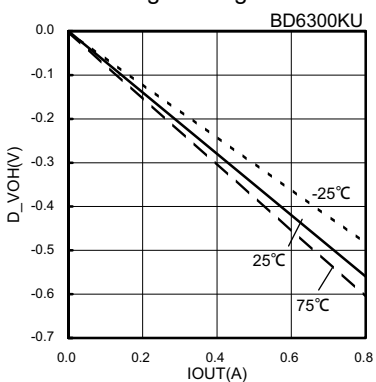


Fig.34 CYLINDER Output
High-voltage

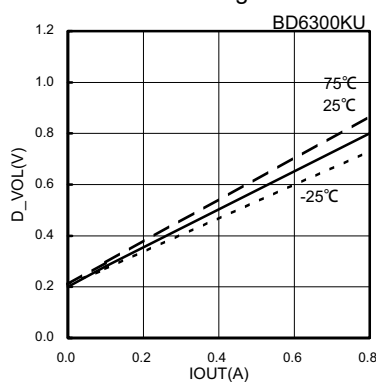


Fig.35 CYLINDER Output
Low-voltage

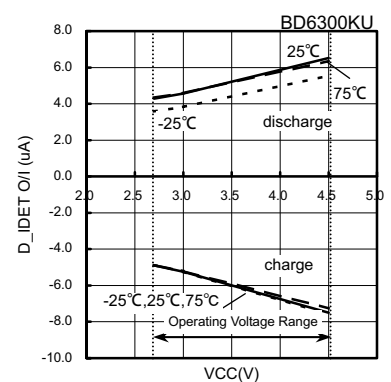


Fig.36 DETECT terminal
charge/discharge current

BD6300KU Characteristic data

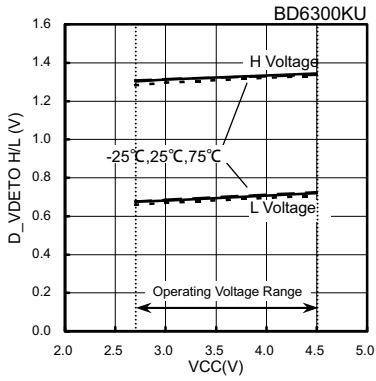


Fig.37 DETECT terminal H/L voltage

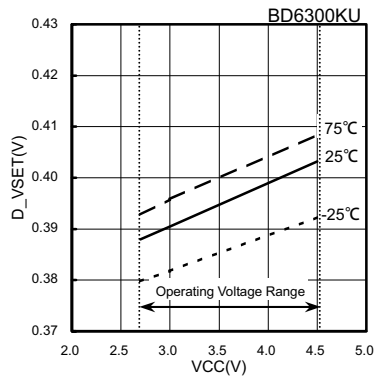


Fig.38 ISET voltage

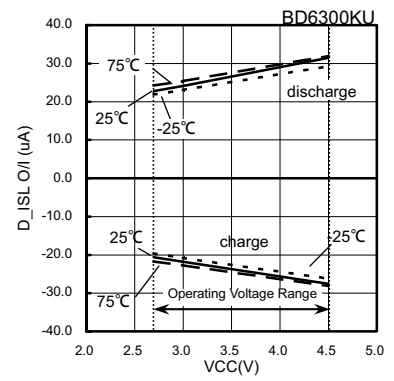


Fig.39 SL1,2 charge/discharge current

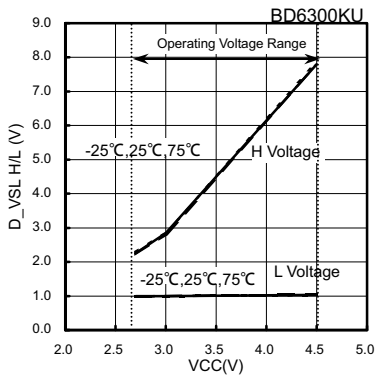


Fig.40 SL1,2 H/L voltage

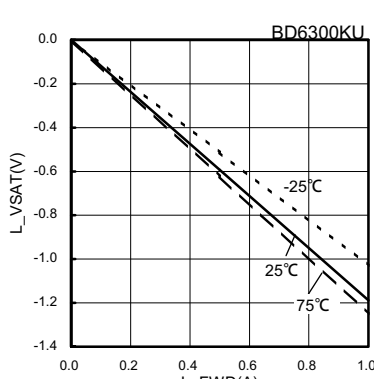


Fig.41 LOADING Output High-voltage

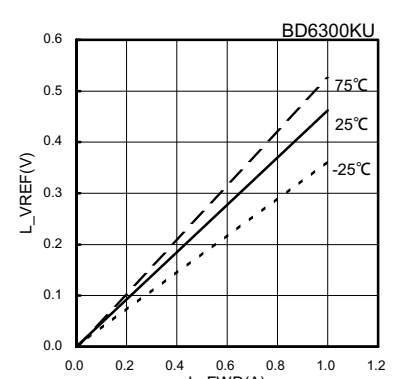


Fig.42 LOADING Output Low-voltage

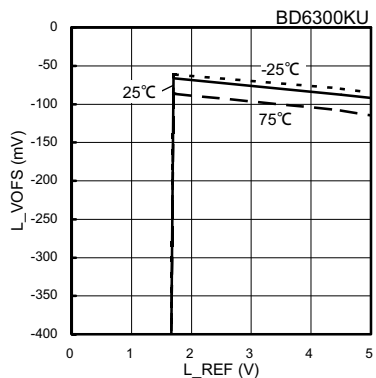


Fig.43 Vout-L_REF offset

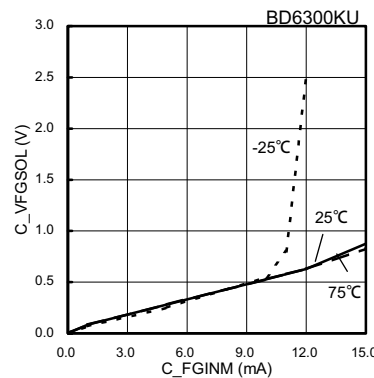


Fig.44 C_FGSMT Output Low-voltage

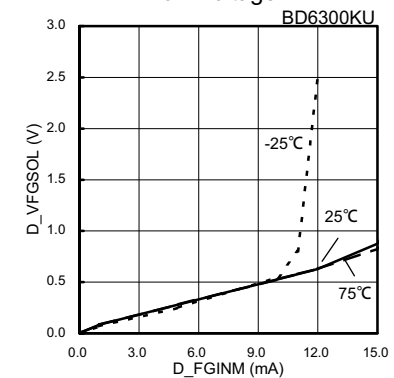


Fig.45 D_FGSMT Output Low-voltage

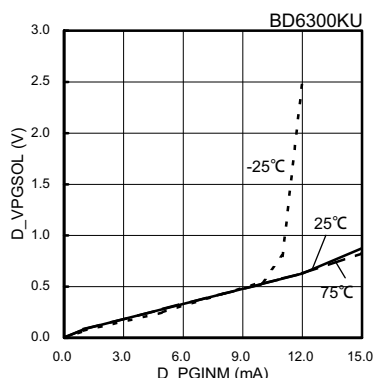


Fig.46 D_PGSM T Output L voltage

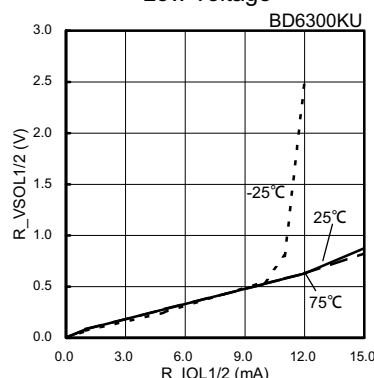
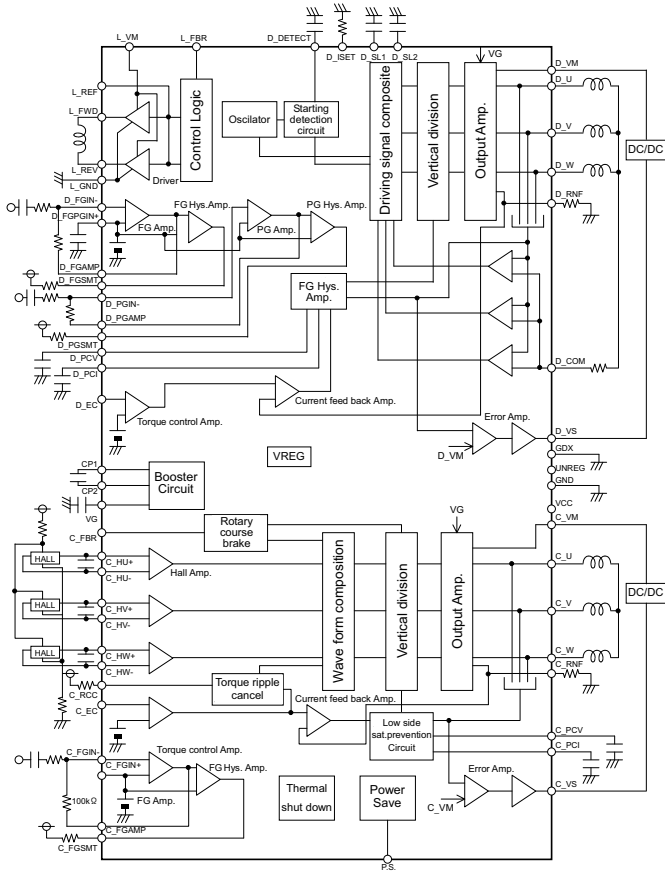


Fig.47 R_OUT1/2 Output L voltage

●Block diagram

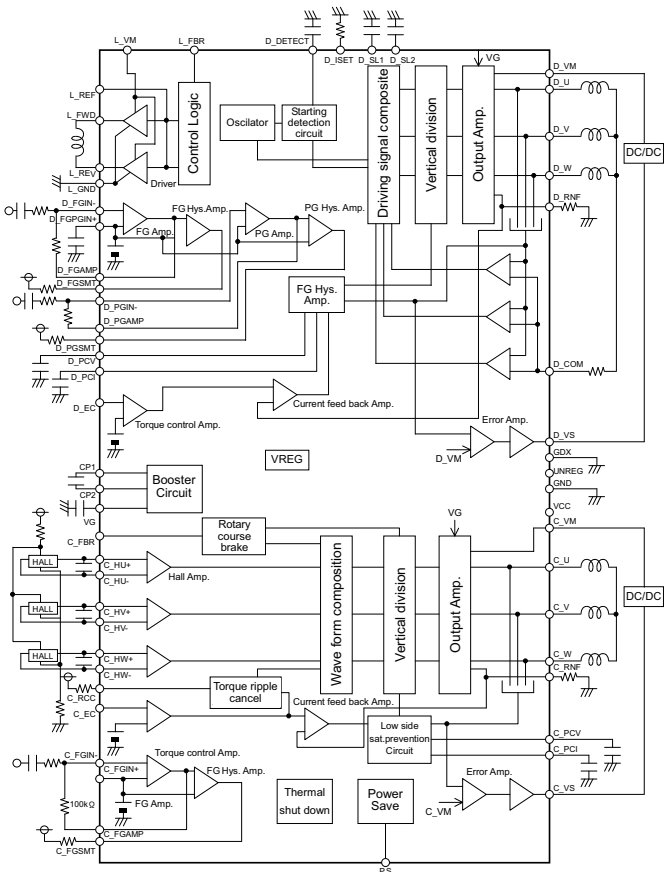
BD6637KV/KS



Terminal function table

PIN NO.	PIN Name (KV)	PIN Name (KS)	PIN NO.	PIN Name (KV)	PIN Name (KS)
1	N.C.	C_U	33	D_COM	D_W
2	C_U	C_V	34	D_U	L_FBR
3	C_V	C_RNF	35	D_V	L_REF
4	C_RNF	C_W	36	D_RNF	L_FWD
5	C_W	C_HU+	37	D_W	L_GND
6	N.C.	C_HU-	38	N.C.	L_REV
7	N.C.	C_HV+	39	L_FBR	L_VM
8	C_HU+	C_HV-	40	L_REF	C_FGIN+
9	C_HU+	C_HW+	41	L_FWD	C_FGIN-
10	C_HV+	C_HW-	42	N_C	C_FGAMP
11	C_HV-	D_PGSM	43	L_GND	C_FGSMT
12	C_HW+	D_PGAMP	44	L_REV	VG
13	C_HW-	D_PGIN-	45	L_VM	CP1
14	D_PGSM	D_FGPGIN+	46	C_FGIN+	CP2
15	D_PGAMP	D_FGIN-	47	C_FGIN-	GND
16	D_PGIN-	D_FGAMP	48	C_FGAMP	GDX
17	D_FGPGIN+	D_FGSMT	49	C_FGSMT	PS
18	D_FGIN-	VCC	50	N.C.	C_RCC
19	D_FGAMP	D_DETECT	51	VG	C_FBR
20	D_FGSMT	D_ISET	52	CP1	C_VM
21	VCC	D_SL1	53	CP2	C_VS
22	D_DETECT	D_SL2	54	N.C.	C_EC
23	D_ISET	UNREG	55	GND	C_PCI
24	D_SL1	D_VM	56	GDX	C_PCV
25	D_SL2	D_VS	57	PS	
26	UNREG	D_EC	58	C_RCC	
27	N.C.	D_PCI	59	C_FBR	
28	D_VM	D_PCV	60	C_VM	
29	D_VS	D_COM	61	C_VS	
30	D_EC	D_U	62	C_EC	
31	D_PCI	D_V	63	C_PCI	
32	D_PCV	D_RNF	64	C_PCV	

BD6300KU



Terminal function table

PIN NO.	PIN Name	PIN NO.	PIN Name
1	D_PH	33	R_IN+2
2	D_FGIN-	34	R_IN-2
3	D_FGPGIN+	35	R_OUT2
4	D_PGIN-	36	VG
5	D_FGSMT	37	CP2
6	VCC	38	CP1
7	D_DETECT	39	GND
8	D_ISET	40	GDX
9	D_SL1	41	D_PS
10	D_SL2	42	C_PS
11	UNREG	43	C_FBR
12	D_VM	44	C_VM
13	D_VS	45	C_VS
14	D_EC	46	C_EC
15	D_PCI	47	C_PCI
16	D_PCV	48	C_PCV
17	D_COM	49	FGND1
18	D_U	50	C_U
19	D_V	51	C_V
20	D_RNF	52	C_RNF
21	D_W	53	C_W
22	N.C.	54	C_RCC
23	FGND2	55	C_HV-
24	L_FBR	56	C_HV+
25	L_REF	57	C_HU-
26	L_FWD	58	C_HU+
27	L_GND	59	C_HW+
28	L_REV	60	C_HW-
29	L_VM	61	C_FGIN+
30	R_IN+1	62	C_FGIN-
31	R_IN-1	63	C_FGSMT
32	R_OUT1	64	D_PGSM

●Description of operations

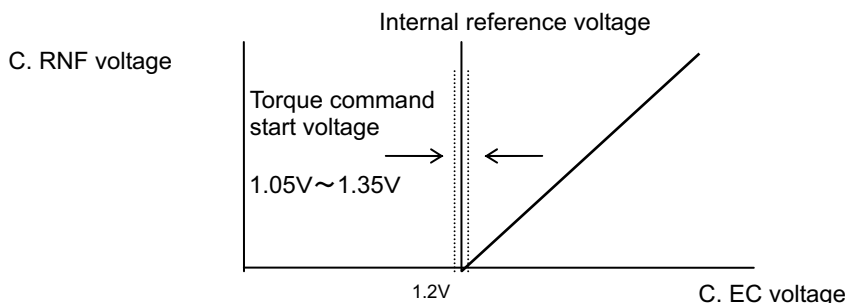
▪ Description of capstan operation

1. Hall input - output

The Hall sensor input signal of the three-phase, is amplified by the Hall amplifier to produce a drive signal waveform. This drive signal is amplified, once again, by the output amplifier to supply a drive current for the motor coil. Output current is a trapezoidal waveform. Due to the trapezoidal waveform, gaps are generated in the magnetic field by the three-phase coil, which causes a slight irregularity of rotation. In operation, the triangle wave is superimposed upon the trapezoidal output waveform. (Torque ripple cancellation)

2. Torque control

Output current can be controlled by the voltage applied to C.EC (torque control terminal).



3. Brake

When the C.FBR terminal is set to M, each output voltage becomes low and the brake is applied.

Brake command voltage: C.FBR 1.3V to 1.7V

4. Motor power supply control function

In order to use power effectively (as well as to prevent exceeding permissible dissipation of IC), it is required to change supply voltage according to output current, i.e. to reduce supply voltage when current output is low, and increase when current output is high, thereby preventing extra voltage from being applied between Drain and Source of output stage MOS. Power supply control function (VS terminal) is installed for this purpose. In this function, the voltage between Drain and Source of upper MOS of output stage is detected, and output to VS terminal as a power supply control signal. This gain signal is multiplied several times by DC/DC, for controlling motor power supply.

5. Output TR saturation preventing circuit

This circuit is used to operate output MOS in linear region. It has good dynamic range from a low to high current, and provides a good rotating performance under overload, etc.

▪ Description of cylinder operation

1. Back electromotive force detecting comparator (BEMF)

Compares the output voltage of the motor with the midpoint potential BEMF and detects the position of the rotor and stator (magnet and coil). Further, the BEMF is provided with hysteresis, which can be set by resistor RD.com, connected to D.COM terminal.

2. Phase switching logic

Synthesizes the output from three-phase BEMF force detecting comparator. The noise pulse of BEMF by the motor is eliminated by MASK signal, generated by D.SL terminal 1 and 2 with reference to each position-detected signal. Only the rising edge of masked synthetic output is used as a signal for the secondary counter. While output from secondary and drive signal is synthesized, FG signal is generated every 60 degrees (electric angle).

3. Slope

D.SL terminal 1 and 2 are charged and discharged in synchronization with the timing of the internal FG signal. For driving soft switching, slope is applied to output current waveform by the slope rate of D.SL terminal 1 and 2.

MASK signal is generated by charging and discharging waveform of D.SL terminal 1 and 2. MASK signal L is output only when the charging and discharging waveform of D.SL terminal 1 and 2 is clamped at L level, when MASK is canceled. Otherwise, H is output and MASK is applied, and noise pulse by back electromotive force of motor is removed.

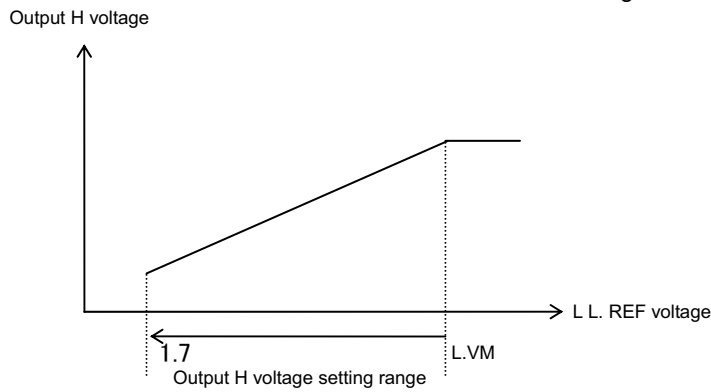
4. Detection circuit - start signal synthesizing

When a capacitor is connected to D.DETECT terminal, charging and discharging are performed. When the motor is stopped, D.DETECT terminal repeats charging and discharging between Low-level and High-level. Only the rising edge of square wave (SEL) that is synchronized with D.DETECT terminal, is compared with rising edge of synthesized output of BEMF detecting comparator. When the motor is stopped, BEMF detecting comparator is not output. Therefore, the edge of SEL signal is input to secondary counter and attempts to force the motor to rotate (synchronized mode). Before the motor rotates and D.DETECT terminal reaches High-level, BEMF detecting comparator detects BEMF motor. When synthetic output of BEMF detection comparator is output, D.DETECT terminal starts discharging on the corresponding edge. When Low-level is reached, charging is started again, and discharging is started on the edge of BEMF detecting comparator output. Here the edge of synthetic output of BEMF comparator is input to secondary counter, and the motor rotates. (BEMF mode)

5. Torque control
Output current can be controlled by the voltage applied to D.EC (torque control terminal), as with capstan assembly.
6. Motor power supply control function
In order to use power effectively (as well as to prevent exceeding permissible dissipation of IC), it is required to control supply voltage according to output current. For example, reduce supply voltage when current output is low, and increase when current output is high, thereby preventing extra voltage from being applied between Drain and Source of output stage MOS. Power supply control function (VS terminal) is used for this purpose. In this function, the voltage between Drain and Source of upper MOS of output stage is detected, and sent to VS terminal as a power supply control signal. This gain signal is multiplied several times by DC/DC, for controlling motor power supply.
7. Output TR saturation preventing circuit
This circuit is used to operate output MOS in linear region. It has good dynamic range from a low to high current, and provides a good rotating performance under overload, etc.

- Description of loading assembly operation

1. L.FBR input - output
Output (L.REV and L.FWD) is three-mode output for forward/reverse rotation and braking, depending on the voltage input to L.FBR.
2. Loading assembly output H voltage control
Output High-voltage of loading assembly can be set by the voltage input to L.RFF terminal. Output High-voltage V_{OH} can be represented by the formula below:
L.REF voltage where the formula above holds true is 1.7 V - L. VM voltage.

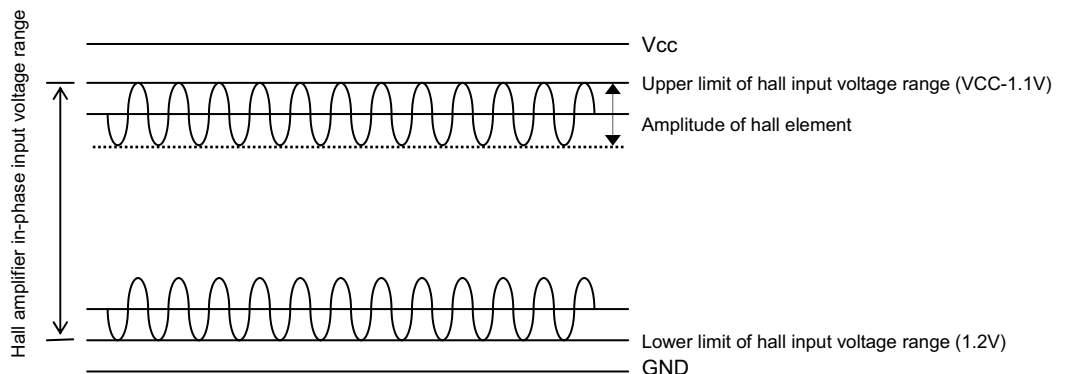


●Application part selecting procedure

Selection of constant in the example of recommended circuit is shown below:

- 1) Capstan hall bias resistor (R_{H1} and R_{H2})

The amplitude and bias point of hall element can be set by hall bias resistor. Hall amplitude varies with hall element in use even when the same bias resistor is used, therefore adjust the bias resistor so that the amplitude of hall element is 50 - 100mvp-p as well as within the range of hall amplifier in-phase input voltage range of capstan assembly (1.2 - V_{CC}-1.1V).



- 2) Capstan C.RCC resistor

Canceling rate of torque ripple canceling circuit of capstan assembly can be adjusted by the resistor equipped externally on C.RCC terminal. Select the optimum value, considering the vibrations, when the IC is mounted to the motor. The optimum value depends on the motor, while 2k Ω to 4k Ω is recommended.

- 3) Cylinder D.COM terminal connection terminal

By inserting a resistor in the middle point of D.COM terminal and motor, the BEMF detecting comparator can also generate hysteresis, thereby preventing any noise from causing malfunction. Hysteresis width can be calculated as follows:

$$\text{Hysteresis width} = \pm R.D.COM \times 20 \mu A \text{ (Typ. value)}$$

The optimum value depends on the motor, while 200 Ω to 300Ω is recommended.

4) Cylinder and output current slope setting capacitor (CSL1, CSL2)

Triangle wave is output from D.SL terminal 1 and 2 for normal rotation of the cylinder. Level 1 is output for Low-level of the triangle wave. The level determined by cylinder rotating speed is output for High-level. Adjust the capacitor of terminal D.SL1 and D.SL2 and the resistance of ISET terminal so that this High-level is approximately 1.8V. It can be set as follows:

Example: When normal rotation speed of cylinder is 9000 rpm, capacitor of terminal D.SL1 and D.SL2 0.047μF and resistance 18 k Ω are recommended.

$$C_{SL1,CSL2} = \frac{185\mu s \times I_{SL}}{0.8V} (\mu F) \quad (\text{where } I_{SL} = \frac{\text{ISET terminal voltage (Typ.:0.4V)}}{R_{ISET}})$$

5) Setting of drive signal frequency in cylinder startup

Drive signal frequency in cylinder startup can be controlled by changing the capacitor of D.DETECT terminal. Adjust the optimum value, so that starting time is shortest on your motor. Drive signal frequency during startup can be calculated as follows: Optimum value depends on motor, while 0.1 - 0.2 μ F is recommended.

$$\frac{\text{DETECT terminal charging and discharging current}}{(\text{DETECT terminal H voltage} - \text{DETECT terminal L voltage}) \times C_{\text{DETECT}} \times 6} \quad (\text{Hz})$$

DETECT terminal H voltage	: 1.3V (Typ. value)
DETECT terminal L	: 0.65V (Typ. value)
DETECT terminal charging and discharging current	: 5μA (Typ. value)

6) PCI/PCV terminal connecting capacitor (capstan/cylinder)

Capacitor connected to PCI and PCV terminal is used to compensate the phase of upper and lower saturation prevention circuit and current feedback loop. When it is too large, the entire loop (including servo system), becomes unstable. When it is too small, the output waveform oscillates. Recommended are 100pF for PCI terminal, 0.1 μ F for PCV terminal of cylinder, 0.1 μ F for PCI terminal and 0.1 μ F for PCV terminal of capstan.

7) DC/DC (capstan/cylinder)

When the output of VS terminal of capstan/cylinder is connected to the DC/DC converter, the motor voltage can be controlled according to the output voltage waveform of the motor. When the DC/DC converter gain is low, the maximum VM voltage cannot be output. The output current waveform is distorted, therefore adjust to an optimum value.

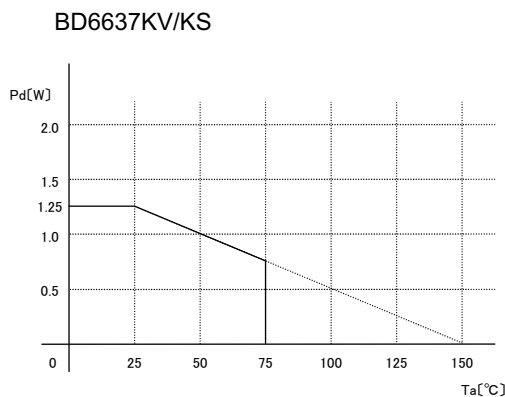
8) RNF terminal

Connect a small resistor (0.33 Ω to 0.5 Ω) between RNF terminal and GND for detecting output current. Because High current flows in this resistor, take precautions against high resistor wattage. The value of the torque command gain versus this resistor (0.33 Ω), is described in the electrical characteristics. Note that this value also changes when resistance changes.

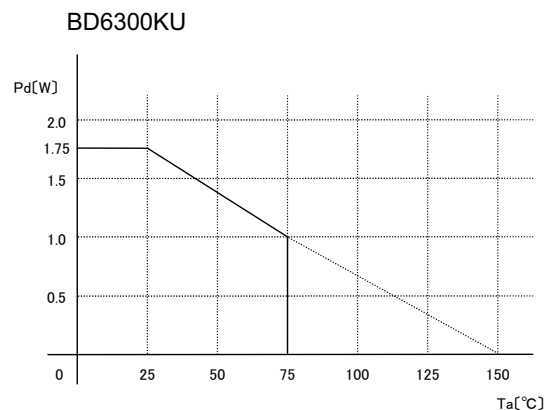
9) Voltage rising circuit

This IC applies Nch DMOS on output stage, and incorporates a voltage boost current for the corresponding gate voltage. When the capacitance value between CP1 terminal and CP2 terminal is low, the current capability of VG terminal voltage is low. When the capacitance value between VG terminal and GND terminal is low, the ripple of VG voltage becomes high. Recommended capacitance value between terminal CP1 and CP2 is 0.1 to 0.22 μ F and that between terminal VG and GND is 1 to 10 μ F.

● Thermal derating characteristics



* 70 mm x 70 mm x 1.6 mm glass epoxy board mounted
Reduce by 10m W/°C when Ta = 25 °C



* 70 mm x 70 mm x 1.6 mm glass epoxy board mounted
Reduce by 14m W/°C when Ta = 25 °C

● Operation Notes

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

3) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage less than or equal to the GND pin, including during actual transient phenomena. The voltage of the motor output pin may, however, drop below the GND potential due to the BEMF voltage of the motor. Malfunctions or other failures may result, depending on the operating conditions, environment, and individual characteristics of the motor. Check that the IC has no operational problems.

4) Thermal Design

Use a proper thermal design that allows for a sufficient margin of the power dissipation (P_d) at actual operating conditions.

5) Pin short and mistake fitting

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

6) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong magnetic field, as doing so may cause the IC to malfunction.

7) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

8) Thermal shutdown circuit

If the junction temperature (T_j) reaches 175°C (Typ.), the TSD circuit will operate, and the coil output circuit of the motor will open. There is a temperature hysteresis of approximately 25°C (Typ.). The TSD circuit is designed only to shut off the IC in order to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. The performance of the IC's characteristics is not guaranteed and it is recommended that the device is replaced after the TSD is activated.

9) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

10) Ground wiring patterns

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

11) Capacitors connected between output and ground pins

If a large capacitance value is connected between the output and ground pins, and if the VCC falls to 0 V or becomes shorted with the ground pin, the current stored in the capacitor may flow to the output pin. This can cause damage to the IC. The capacitance value between the output and GND must be $100\mu\text{F}$ or lower.

12) Regarding input pin of the IC

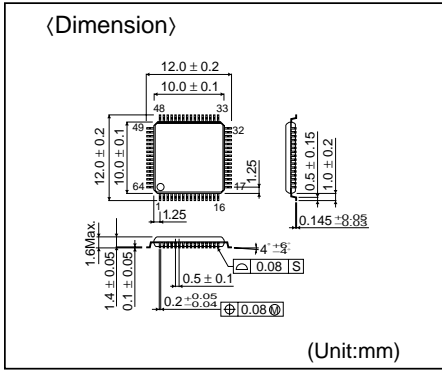
If no VCC voltage is applied to the IC do not apply any voltage to the input pins. If a voltage higher, or as high as the VCC, or a voltage lower than, or as low as, the GND is applied, parasitic elements may result due to the structure of the IC. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. Use caution so that the IC is not used in a manner that will trigger the operation of parasitic elements.

13) Operating Precautions

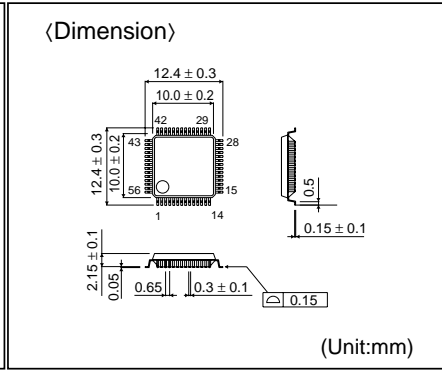
Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.

● Physical Dimension

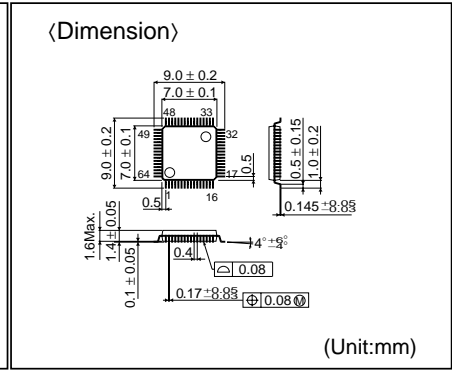
VQFP64



SQFP56

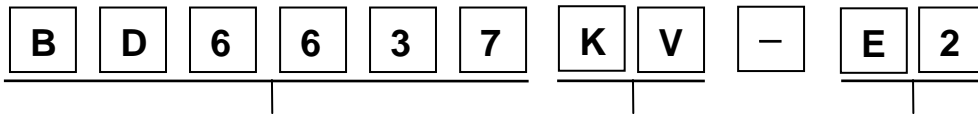


UQFP64



● Ordering part number

• Please order by ordering part number. • Please confirm the combination of each items. • Please write the letter close to left when column is blank



Part Number

- BD6637KV
- BD6637KS
- BD6300KU

Package Type

- KV : VQFP64
- KS : SQFP56
- KU : UQFP64

- E1 Emboss tape reel Pin 1 on draw-out side
- E2 Emboss tape reel Pin 1 opposite draw-out side

<Packing information>

Container	Tray(with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.

※When you order , please order in times the amount of package quantity.

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