Micro Linear

ML6310

3V/5V Read Channel Front-end Processor

GENERAL DESCRIPTION

The ML6310 is a BiCMOS Read Channel Front-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of small form factor (1.8" & 1.3") disk drives, operating on 3V and/or 5V supplies. It works in conjunction with the ML6311 Read Channel Back-end Processor to form a complete solution for the low-voltage/ low-power disk read/write channel. It incorporates a full function pulse detector, four channel servo demodulator, and a filter/equalizer with switchable response characteristics between data and servo.

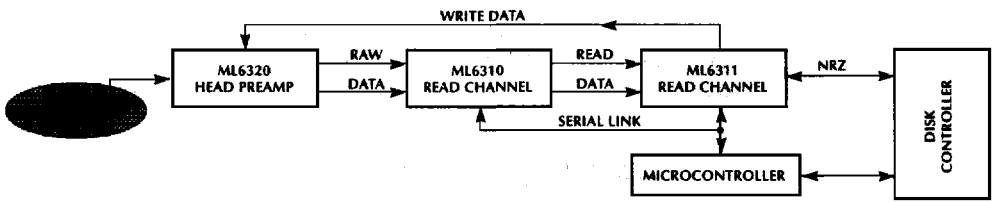
The filter architecture consists of a 6-pole, 2-zero, 0.05° Equiripple type, continuous time filter, with asymmetric equalization, realizing a family of frequency response curves optimized for the disk drive read channel. The cutoff frequency and boost (asymmetric equalization) are programmable through the serial interface using internal 5- & 4-bit DACs. The pulse detector is implemented with a high bandwidth AGC whose attack and decay rates are programmable through the serial interface using 2-bit DACs respectively. The Hysteresis level for the pulse detector Gate channel is also programmable through the serial interface using a 4-bit DAC. A four channel servo demodulator is onboard which offers buffered outputs for head positioning with a programmable option to bring out either A, B, C, D or A+B, A–B, C–D, C+D outputs.

The ML6310 supports four power down modes for implementation of real-time power management in an optimal manner. The operating power dissipation is targeted to be less than 300mW at 3V, while the part will dissipate less than 15µW in the sleep mode. The ML6310 requires only three external components.

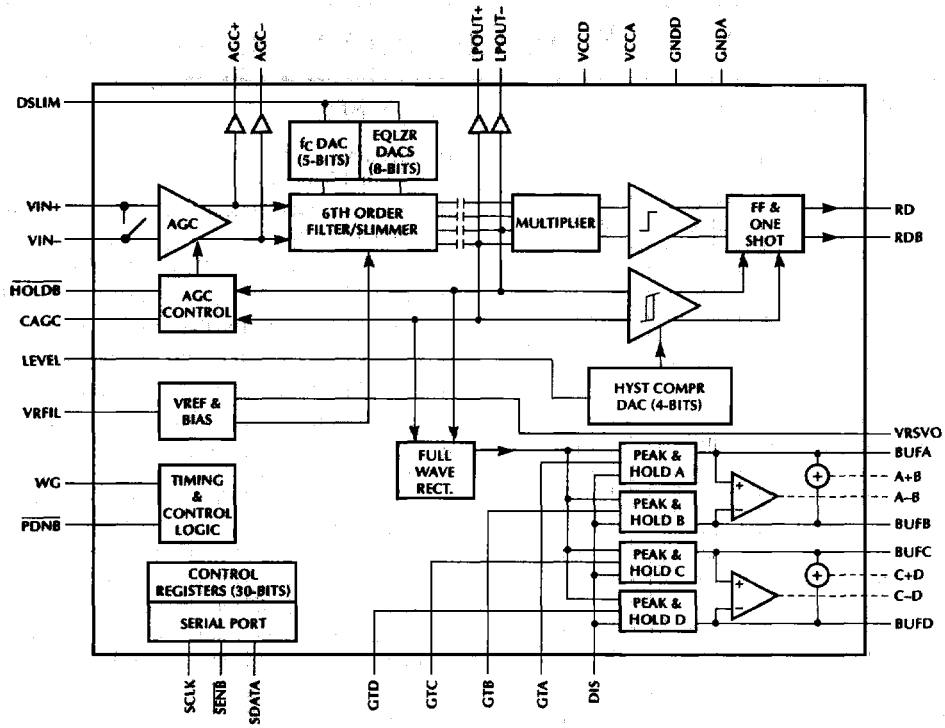
FEATURES

- Operating supply ranges are 2.7V to 3.3V or 3.0V to 3.6V or 4.5 to 5.5V.
- Very Low Power dissipation at 3V P_{SLEEP} < 15µW, P_{OPR} < 300 mili-watts
- Low profile, 32-pin TQFP package, (7 x 7 x 1) mm^3
- NRZ Disk data rates up to 32 Mbits/s, for 1,7 RLL
- Pulse detector with less than ±500ps pulse pairing
- Wide bandwidth (> 60MHz) AGC amplifier
- Internal stable reference voltage level for AGC
- Programmable hysteresis level in Gate channel (static)
- Four channel servo demodulator with internal capacitors for track & hold capability. Selectable A, B, C, D or A–B, C–D, A+B, C+D demod outputs.
- Onboard coupling capacitors and DC offset cancellation circuitry to minimize internal offsets
- 6-pole, 2-zero continuous time, 0.05° equiripple filter with less than 40dB harmonic distortion
- Programmable filter cutoff frequency (3 :1 range in 32 steps) (f_C = 6.0 to 18 MHz). Also allows a 10% range shift under external resistor control
- Programmable Asymmetric Equalization in 256 steps (256 combinations of Group Delay and Boost), providing 0 to 11.6 dB slimming boost at f_C.
- High speed (20MHz clock) three wire serial microprocessor interface with double buffered data latch for synchronous or asynchronous data loading.
- Four Power-down modes selectable, plus hardware pin
- CMOS / TTL compatible I/O to minimize power

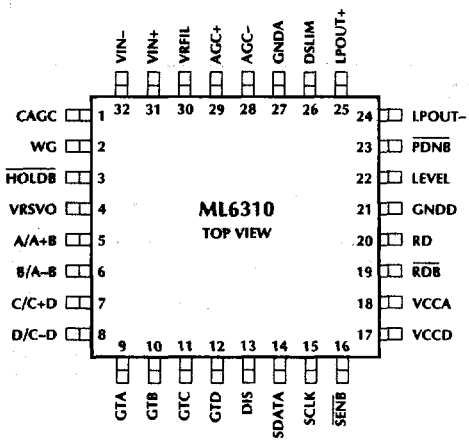
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

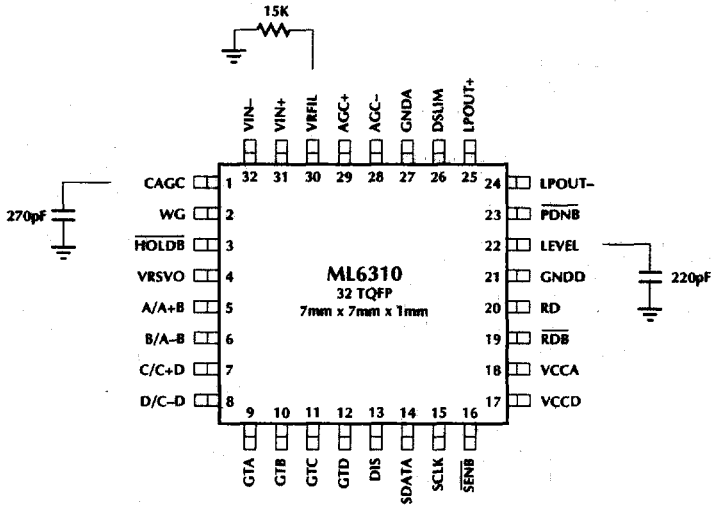
PIN	NAME	FUNCTION
Pulse Detector		
31 32	VIN+ VIN–	AGC amplifier differential input. This input is AC coupled from the Read/ Write amplifier output. It is recommended that the differential input signal be in the range of $15mV_{P-P}$ to $150mV_{P-P}$.
1	CAGC	The AGC loop capacitor is connected from this pin to GNDA. Lead-Lag network may be used for a differential loop filter characteristic, if desired. The Attack and Decay currents of the AGC can be adjusted through the bits in the control register.
3	$\overline{HOLDB}$	This is an active low CMOS input pin. When this pin is forced to a logic low, all the charging and discharging paths on the CAGC pin are disabled. The AGC amplifier now acts as a fixed gain amplifier with the gain being determined by the voltage on the CAGC pin.
22	LEVEL	Rectified signal level output and input to the programmable hysteresis comparator. An external capacitor between this pin and GNDA, in conjunction with an internal resistor (8 Kohms typical), sets up the discharge time constant.
20 19	RD $\overline{RDB}$	These pins provide the differential pulse detector encoded read data output (ECL). These signals form the input to the ML6311 — read channel back-end processor chip which does the data synchronization and clock recovery. (Low voltage ECL O/P's)
29 28	AGC+ AGC–	Buffered AGC outputs used for test and prototyping purposes. These are differential open emitter outputs and hence should be left open in normal operation to minimize power dissipation.
Filter / Equalizer		
30	VRFIL	A resistor between this pin and GNDA sets up the center frequency of the filter.
26	DSLIM	When this pin is high, the slimming function is disabled and the filter cutoff frequency is switched to the servo filter cutoff frequency. When this pin is low the filter data path cutoff frequency is used, with the slimming being programmable.

PIN	NAME	FUNCTION
Filter / Equalizer (continued)		
25 24	LPOUT+ LPOUT–	Buffered lowpass filter outputs used for test and prototyping purposes. These are differential open emitter outputs and hence should be left open in normal operation to minimize power dissipation.
Timing and Control		
23	$\overline{PDNB}$	Active low CMOS input. In conjunction with the power management bits in the Control Register, this helps setup the ML6310 in one of the four power down modes.
2	WG	Active high CMOS input. This input is used to activate the input clamp for a period of 1µs, to generate the write to read transition delay.
Servo Demodulator		
4	VRSVO	This reference voltage derived from the internal bandgap is used by the A/D converter handling the servo bursts, to define the middle point of the dynamic range. A typical value for this is 1.0V.
9 10 11 12	GTA GTB GTC GTD	Gate control for the four channel servo burst detectors. Active high CMOS inputs. Internal holding capacitors hold the charge corresponding to the peaks of the servo bursts.
13	DIS	Active high CMOS input. When this pin is asserted high, the four servo peak detector capacitors are discharged.
5 6 7 8	A/A+B B/A–B C/C+D D/C–D	Buffered four channel servo demodulator outputs. The four outputs can be optionally selected to be either A, B, C, D or A+B, A–B, C+D, C–D through a bit (SMODE), in the Control Register #6
Serial Interface		
15	SCLK	This is a CMOS input which clocks the Control Register (negative edge trigger). Internally this pin is gated with the $\overline{SENB}$ signal.
14	SDATA	Control Register Data, CMOS input, clocked by SCLK.
16	$\overline{SENB}$	Active low CMOS input — Control Register enable. A logic low input on this pin pin allows the SCLK input to clock the SDATA into the control register and a logic high latches the control register contents.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
Power Supply and Ground		
18	VCCA	This is the analog VCC input, used for the pulse detector, filter/equalizer and servo demodulator. In the case of a 5V supply operation this pin needs to be left open, while in the case of a 3V supply operation this pin is tied to VCCD.
17	VCCD	Digital VCC input for serial microprocessor interface and related logic. This can handle the 2.7V to 5.5V supply range.
27	GNDA	Analog ground
21	GNDD	Digital ground

TYPICAL EXTERNAL COMPONENTS



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCCA & VCCD) ..... –0.3 to +7V
Analog & Digital Inputs/Outputs ..... –0.3 to VCCA + 0.3V
Input Current per Pin ..... –25 to +25mA
Storage Temperature ..... –65 to +150°C
Maximum Junction Temperature ..... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range .... 2.7V to 3.6V or 4.5V to 5.5V
For 5V Operation ..... VCCA is left open, VCCD is at 5V
For 3V Operation ..... VCCA and VCCD are tied to 3V
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 2.7 to 3.6 Volts or 4.5 to 5.5 Volts and T_A = 0 to 70°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
Analog V_{CC} (VCCA)	Left open for 5V operation	2.7		3.6	V
Digital V_{CC} (VCCD)	Connected for both 3V & 5V	2.7		5.5	V
Supply Current (Analog)	@ VCCA = 3.0V @ Sleep mode (PDNB pin = 0)			80 8	mA µA
Supply Current (Digital)	@ VCCA = 3.0V or 5.0V @ Sleep mode (PDNB pin = 0)			10 2	mA µA
Supply Current (Total)	VCCA = VCCD = 3.0V VCCD = 5.0V, VCCA = *open* @ sleep mode (PDNB pin = 0)			90 110 10	mA mA µA
Power Down Current (Normal mode)	PDNB pin = 1 Control Reg bits PM1=PM0=0			90	mA
Power Down Current (Servo mode)	Serial Interface + AGC + Filter + Servo demodulator enabled PDNB = 1, PM1= 0, PM0 = 1			65	mA
Power Down Current (Pulse mode)	Serial Interface + AGC + Filter + Pulse Detector enabled PDNB = 1, PM1= 1, PM0 = 0			68	mA
Power Down Current (Idle mode)	Only Serial Interface enabled PDNB = 1, PM1= 1, PM0 = 1				
	VCC = 2.7 to 3.6V		0.45	30	µA
	VCC = 4.5 to 5.5V		0.8	1.5	mA
Power Down Current (Sleep mode)	Control register retains data PDNB = 0, PM1= X, PM0 = X		0.15	5	µA
Digital I/O Specifications					
High level input voltage		VCCD-0.5		VCCD	V
Low level input voltage		GNDD		GNDD+0.5	V
High level input current	@ VCC and GND			1	µA
Low level input current	@ VCC and GND			1	µA
AGC Amplifier and Input Clamp					
Differential Input signal range	Note 2	15		150	mV_{P-P}
Maximum AGC gain	VCAGC = 1.2V @ AGC ± pins	15	22	28	V/V
Minimum AGC gain	VCAGC = 2.2V @ AGC ± pins		0.6	3	V/V
Differential input resistance	Read mode (WG is low)	3.75	5	6.25	Kohms
	Write mode (WG is high)	200	500	700	Ohms

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AGC Amplifier and Input Clamp (continued)					
CMRR	$V_{IN+} = V_{IN-}$ = 100 mV @ 5MHz & VCAGC = 1.2 V	40			dB
PSRR	VCCA = 100 mV @ 5 MHz & VCAGC = 1.2 V		40		dB
CAGC voltage range	@ VCCD = 2.7V Note 1	1		2.2	V
Input Clamp Off time	From WG active to input clamp release	0.7	1	1.3	µs
Clamp propagation delay	From WG inactive to input Z clamped		20	100	ns
AGC Control — Rectifier and Comparator					
CAGC clamp voltage		1.2	1.8	2.5	V
CAGC Output voltage	Maximum possible	1.8	VCCA/0.5	3.0	V
CAGC Attack current	Min — Control register bits = 00 Max — Control register bits = 11	20 70	30 120	45 170	µA µA
CAGC Decay current	Min — Control register bits = 00 Max — Control register bits = 11	1 6	3 9	6 12	µA µA
CAGC leak current	$\overline{HOLDB}$ pin is low			±0.1	µA
HOLD on / off	$\overline{HOLDB}$ pin, ON time and OFF time		0.5		µs
Hysteresis Comparator					
Input signal range	Differential input, Note 1				
Hysteresis range	percent of input signal amplitude	0		93.8	%
Hysteresis resolution	controlled by internal DAC, Note 1		6.25		%
Max output current	LEVEL pin short to gnd (I_{SHORT} > 1 mA)	1			mA
Output resistance	LEVEL pin		400		ohms
Pulse Qualification Section					
Read Data pulse width		20		30	ns
Pulse Pairing	0.2 MHz sinewave @ 15 mV_{P-P} diff, f_C = 9MHz (1 sigma)		±0.5	±1	ns
Jitter on RD (falling edge)	0.2 MHz sinewave @ 15 mV_{P-P} diff, f_C = 9MHz (1 sigma)		±0.1	±1	ns
RD/RDB raw data output	Differential, Psuedo ECL $\lvert V_{RD} - V_{RDB} \rvert$	0.6	0.7	0.8	V
$V_{RD/RDB}$ common mode	Note 1		VCCA – V_{BE}		V
Filter / Equalizer Section					
Differential Group delay	0.3f_C to f_C, f_C0–f_C4 = 1			±5	%
Cutoff Frequency Accuracy		–10		+10	%
Slimming Level Accuracy		–1		+1	dB
Phase shift (LP & BP)	f_C0–f_C4 = 1, Note 2		90 ±2		degree
Response settling time	Due to change in f_C, Note 2		1		µs

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Servo Demodulator Section (All tests @ f = 5 MHz)					
Servo Amplifier voltage gain	@ Input = 50 mV and 150 mV. AGC set to a gain of 1.	3	5	7	V/V
Channel offset matching			±2	±10	mV
Output leakage current			5		nA
Discharge time	Input = 150 mV, discharge to 50% output			5	µs
Droop rate	Input = 150 mV, GATE on to GATE off		0.01	0.1	mV/µs
Acquisition time	Gate enable to 90% of peak detector output		1	1.5	µs
Difference error	Input = 150 mV		±2	±10	mV
VRSVO output voltage		0.9	1.05	1.3	V
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		0.01		20	MHz
SCLK pulse width	t_{PW}	20			ns
SCLK to SDATA hold time	t_{HSD}	5			ns
SDATA to SCLK setup time	t_{SSD}	5			ns
$\overline{SENB}$ to SCLK setup time	t_{SSEN}	10			ns
SCLK to $\overline{SENB}$ hold time	t_{SSEN}			10	ns

Note 1: *These specifications are design goals and are not tested. They are provided for informational purposes only.*

Note 2: These parameters are guaranteed by design and verified by characterization only and are not part of the production test program, hence only the typical values are indicated for system designer's reference.

TIMING DIAGRAM

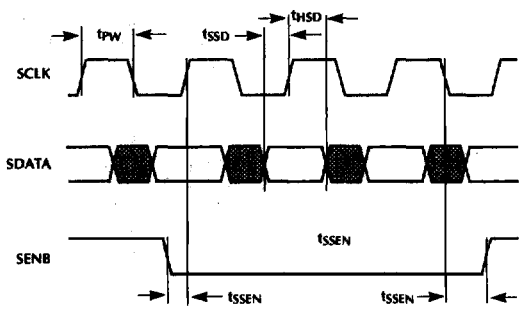


Figure 1. 3-Wire Serial Interface.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ML6310 is a Read Channel Front-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of small form factor (1.8" & 1.3") disk drives, operating on 3V and/or 5V supplies. Fabricated in Micro Linear's BiCMOS process (1.5µ CMOS, 4GHz f_t bipolar), it works in conjunction with the ML6311 Read Channel Back-end Processor to form a complete solution for the low voltage/low power disk read/write channel. It incorporates a full function pulse detector, four channel servo demodulator, and a filter/equalizer with switchable response characteristics between data and servo. The ML6310 supports four power down modes for implementation of real-time power management in an optimal manner. The maximum power dissipation is targeted to be less than 350mW, while the part will dissipate less than 1 mW in the sleep mode. In this mode all sections are powered down except the serial microprocessor interface. A high level of digital programmability through this interface and onboard registers contributes to reducing the external component count significantly.

The pulse detector is implemented with a high bandwidth AGC whose attack and decay rates are programmable through the serial interface using 2-bit DACs respectively. The Hysteresis level for the pulse detector Gate channel is also programmable through the serial interface using a 4-bit DAC. Pulse qualification is achieved by using both level and polarity.

A four channel servo demodulator is onboard which offers buffered outputs for head positioning with a programmable option to bring out either A, B, C, D or A+B, A–B, C–D, C+D outputs. The four hold capacitors for the servo peak detectors are implemented on board.

The programmable filter architecture consists of a 6-pole, 2-zero. 0.05° Equiripple type, continuous time filter, with asymmetric equalization, realizing a family of frequency response curves optimized for the disk drive read channel. For embedded servo handling, the servo and the data path filter cutoff frequencies are programmed separately. Using the external DSLIM pin, the filter characteristics can be switched to the servo cutoff frequency with no slimming boost. The switching of the filter frequency response is very fast, thus allowing for real-time embedded servo handling The cutoff frequency and boost (asymmetric equalization) are programmable through the serial interface using internal 5-bit and 4-bit DACs.

The three wire serial interface is also used to program a number of parameters controlling the various sections of the chip. On physical power-up, the control registers will come up in an undetermined state and hence these registers must be initialized to their default values first, so that the chip is put in a defined state. The contents of the control registers are retained in all power down modes, except when the power is physically turned off to the chip.

The ML6310 is designed to offer the lowest power dissipation, a high level of integration and offer a high level of programmability to minimize the number of external components, thus resulting in an optimized read channel front-end. It outputs raw data in an ECL format whose level is compatible with the input to the companion chip ML6311, used for data separation and clock synchronization. Please refer to the block diagram of the ML6310 for the details.

PULSE DETECTOR

The pulse detector consists of the AGC amplifier with a full AGC control loop, on the front-end, which works in conjunction with the programmable filter/equalizer circuitry. The pulse detector consists of the conventional time channel and gate channel to help in pulse qualification, for generating the raw data output which represents the time position of the peaks corresponding to the flux reversals on the disk.

AGC

The AGC amplifier is a two stage differential amplifier design with high bandwidth, typically greater than 100MHz. The first stage of the AGC is a Variable Gain Amplifier (VGA) whose gain is controlled by the voltage on the CAGC pin. The gain of the amplifier decreases as the voltage on the CAGC pin increases. The second stage is essentially a fixed gain amplifier.

The AGC usually gets its differential input from the output of the head preamp circuit. The input signal range is 15mV to 150mV peak-to-peak differential. The AGC's input has a switchable input impedance clamp to enhance the write to read transient recovery. This is indirectly controlled by the Write Gate signal from the disk controller. When Write Gate is active-high (write mode), the input impedance is reduced or clamped to a low impedance state and when Write Gate goes inactive-low, the input impedance switches back to the normal (high impedance state), after a 1µs delay, typically.

The output of the AGC amplifier feeds into the filter/equalizer directly. The lowpass output from the filter/equalizer serves as the input to the AGC control front-end which is a full wave rectifier. The AGCSET comparator compares the full wave rectifier output with an internal settled voltage reference and generates an output to the AGC control circuitry. The AGC control circuitry compares this voltage with the voltage from the CAGC pin, before providing the feedback into the control nodes of the Variable Gain Amplifier. The capacitor on the CAGC pin then gets charged or discharged depending on whether the full wave rectifier output is greater than or less than the preset internal reference voltage. The charging and discharging current, also referred to as the attack and decay rates, are programmable through the bits in control register #5, as shown below. Refer to the section on Control Register for programming details.

1	0	1	REG	DKY1	DKY0	ATK1	ATK0

During the servo capture period, the AGC amplifier functions as a fixed gain amplifier, under control of the $\overline{HOLDB}$ pin. When the $\overline{HOLDB}$ pin is forced to a logic low, the AGC control loop is disabled and the charging and discharging of the capacitor on the CAGC pin is stopped. The AGC loop maintains the gain setting prior to the $\overline{HOLDB}$ pin going low. The impedance and gain of the AGC amplifier are not affected.

Time Channel

The time channel of the pulse detector consists of a multiplier and a zero crossing comparator, the output of which generates the clocking signal to the pulse qualification flip-flop. The input of the multiplier is the differential lowpass and bandpass outputs of the filter/equalizer. The capacitative coupling ensures the removal of any DC offsets in the differentiated outputs of the filter/equalizer. This technique contributes significantly to better pulse pairing by eliminating the need for a matching bidirectional one-shot as used in conventional approaches.

The output of the multiplier goes to the zero-crossing comparator which produces a logic output whose edges correspond to the zero crossing points of the input signal. A positive transient of state at the zero crossing output indicates that a minima and maxima has been detected at the filter/equalizer's differentiated output.

Gate Channel

The Gate Channel consists of a hysteresis comparator which prevents false triggering of the output one-shot due to baseline noise. The lowpass output of the filter/equalizer forms the input of the hysteresis comparator. Only when a data pulse is of sufficient amplitude will the hysteresis comparator allow the output one shot to be triggered. The hysteresis comparator also ensures that the output one-shot is triggered once for each data pulse polarity. The hysteresis level (as a percentage of the hysteresis comparator input signal peak), is programmable through the bits in control register #4, as shown below. Refer to the section on Control Register for programming details.

1	0	0	NC	HYS3	HYS2	HYS1	HYS0

Pulse Qualification

The pulse qualification circuitry consists of a D flip-flop whose data input is the hysteresis comparator output and it is clocked by the zero-crossing comparator output in the time channel. The output of this D flip-flop triggers a one-shot whose pulse width is programmed through an internal RC constant. In order to allow the zero-crossing comparator output to fire the one-shot, every positive transient in the zero-crossing comparator shall correspond to the opposite polarity of the hysteresis comparator output. The output of the one-shot then constitutes the raw data output which represents the time position of the peaks corresponding to the flux transitions on the disk media.

PROGRAMMABLE FILTER/EQUALIZER

The programmable filter/equalizer circuit approximately realizes a sixth-order, 0.05° Equiripple function thus achieving a flat group delay up to twice the cutoff frequency ($2f_C$). The filter processes signals in a differential mode for greater noise immunity. This filter architecture is capable of handling fast transients and provides smaller excess phase and power dissipation. It is made up of three biquads which generate a lowpass and bandpass (differentiated) output. The cutoff (corner) frequency of the filter is controlled by 5 bits in control register which provide 32 combinations in the range of 6MHz to 18MHz. Control register #0 is used to program the data channel corner frequency while the servo channel corner frequency is programmed in control register #1, as shown below. Refer to the section on Control Register for programming details.

DATA PATH CUTOFF FREQUENCY

0	0	0	Df_C4	Df_C3	Df_C2	Df_C1	Df_C0

SERVO PATH CUTOFF FREQUENCY

0	0	1	Sf_C4	Sf_C3	Sf_C2	Sf_C1	Sf_C0

These five bits are used to control a DAC to generate a current which is used to control the frequency of the filter. The cutoff (corner) frequency of the filter is given by the following equation :

$$f_C = 6 + (0.387 \times 16 f_C4 + 8 f_C3 + 4 f_C2 + 2 f_C1 + f_C0)$$

Table 1 lists the corner frequencies and the corresponding control register bit configurations.

Two real zeroes are introduced by two equalizers (slimmers) inserted between the first/second and the second/third biquads. The zeroes can be adjusted independently so that it is possible to realize asymmetric equalization, if desired. The transfer function of the equalizer (slimmer) is given by :

$$H_S = \left[1 - \left(k_1 \times \frac{S}{\omega_{O1}}\right)\right]\left[1 + \left(k_2 \times \frac{S}{\omega_{O2}}\right)\right]$$

Where ω_{O1}, ω_{O2} are the corner frequencies of the first and second biquads and $S = j\omega$ is the complex frequency. The normalized corner frequencies of the first and second biquads are 0.981 and 2.074. The group delay variation at the corner frequency is given by :

$$\Delta G_{\omega C} = \frac{1}{\omega_C}\left[\frac{\left(\frac{k_1}{0.981}\right)^3}{1+\left(\frac{k_1}{0.981}\right)^2} - \frac{\left(\frac{k_2}{2.074}\right)^3}{1+\left(\frac{k_2}{2.074}\right)^2}\right]$$

k_1 and k_2 can be controlled by adjusting the bias currents in the slimmers. They are adjusted by changing the slimming control bits — zeroA (N_A) in control register #2 and zeroB (N_B) in control register #3 as shown below. Refer to Table 2 and the section on Control Register, for details.

MSB

0	1	0	RSVD	EA3	EA2	EA1	EA0

MSB

0	1	1	RSVD	EB3	EB2	EB1	EB0

k_1 & k_2 are expressed by the equations below :

$$k_1 = \frac{k_{1MAX} N_A}{15} \qquad k_{1MAX} = 1.578$$

$$k_2 = \frac{k_{2MAX} N_B}{15} \qquad k_{2MAX} = 3.327$$

N_A and N_B are the decimal expression of the slimming bits EA3 – EA0 and EB3 – EB0, respectively. Hence the group delay and corner frequency product (refer table 2), is given by :

$$\Delta G_{\omega C} f_C = \frac{1}{2\pi}\left[\frac{(0.1078N_A)^3}{1+(0.1078N_A)^2} - \frac{(0.1078N_B)^3}{1+(0.1078N_B)^2}\right]$$

The equalization (slimming) level is given by :

$$SL(dB) = 10\log\left[1+\left(\frac{k_1 \times \omega}{\omega_{O1}}\right)^2\right] + 10\log\left[1+\left(\frac{k_2 \times \omega}{\omega_{O2}}\right)^2\right]$$

At the corner frequency of the filter (18 MHz), the equation is reduced to :

$$SL(dB) = 10\log\left[1+(0.1078N_A)^2\right] + 10\log\left[1+(0.1078N_B)^2\right]$$

TABLE 1: Corner frequency programming values

f_C4	f_C3	f_C2	f_C1	f_C0	f_C (MHz)
0	0	0	0	0	6.000
0	0	0	0	1	6.387
0	0	0	1	0	6.774
0	0	0	1	1	7.161
0	0	1	0	0	7.548
0	0	1	0	1	7.935
0	0	1	1	0	8.323
0	0	1	1	1	8.710
0	1	0	0	0	9.097
0	1	0	0	1	9.484
0	1	0	1	0	9.871
0	1	0	1	1	10.258
0	1	1	0	0	10.645
0	1	1	0	1	11.032
0	1	1	1	0	11.419
0	1	1	1	1	11.806
1	0	0	0	0	12.194
1	0	0	0	1	12.581
1	0	0	1	0	12.968
1	0	0	1	1	13.355
1	0	1	0	0	13.742
1	0	1	0	1	14.129
1	0	1	1	0	14.516
1	0	1	1	1	14.903
1	1	0	0	0	15.290
1	1	0	0	1	15.677
1	1	0	1	0	16.065
1	1	0	1	1	16.452
1	1	1	0	0	16.839
1	1	1	0	1	17.226
1	1	1	1	0	17.613
1	1	1	1	1	18.000

Table 2 shows the Product of Delta Group Delay & f_C , slimming level, zeroA and zeroB programming values with control register bit configurations. The values, Binary (EA3 – EA0) = Decimal N_A and Binary (EB3 – EB0) = Decimal N_B.

FILTER TRANSFER FUNCTION

$$= \left[\frac{\omega_{01}^2}{s^2 + \frac{s \times \omega_{01}}{Q_1} + \omega_{01}^2}\right]\left[\frac{\omega_{02}^2}{s^2 + \frac{s \times \omega_{02}}{Q_2} + \omega_{02}^2}\right]\left[\frac{\omega_{03}^2}{s^2 + \frac{s \times \omega_{03}}{Q_3} + \omega_{03}^2}\right]$$

Where: $\omega_{01} = 0.981\ \omega_C$
$\omega_{02} = 2.074\ \omega_C$
$\omega_{03} = 1.470\ \omega_C$
$Q_1 = 0.551$
$Q_2 = 1.686$
$Q_3 = 0.893$

TABLE 2

N_A	N_B	ΔGf_C(sHz)	SL(dB)
0	0	0	0
0	1	0.0002	0.0502
0	2	0.0015	0.1973
0	3	0.0049	0.432
0	4	0.0108	0.7406
0	5	0.0193	1.1077
0	6	0.0304	1.5178
0	7	0.0436	1.9574
0	8	0.0585	2.4148
0	9	0.0749	2.8809
0	10	0.0922	3.3487
0	11	0.1103	3.8132
0	12	0.1289	4.2706
0	13	0.1478	4.7187
0	14	0.1669	5.1557
0	15	0.1862	5.5807
1	0	–0.0002	0.0502
1	1	0	0.1004
1	2	0.0013	0.2475
1	3	0.0047	0.4822
1	4	0.0106	0.7908
1	5	0.0191	1.1578
1	6	0.0302	1.568
1	7	0.0434	2.0076
1	8	0.0583	2.465
1	9	0.0747	2.9311
1	10	0.092	3.3989
1	11	0.1101	3.8634
1	12	0.1287	4.3208
1	13	0.1476	4.7688
1	14	0.1667	5.2058
1	15	0.186	5.6309
2	0	–0.0015	0.1973
2	1	–0.0013	0.2475
2	2	0	0.3946
2	3	0.0033	0.6293
2	4	0.0092	0.9379
2	5	0.0178	1.305
2	6	0.0288	1.7152
2	7	0.0421	2.1547
2	8	0.057	2.6121
2	9	0.0733	3.0782
2	10	0.0907	3.546
2	11	0.1088	4.0105
2	12	0.1273	4.468
2	13	0.1463	4.916
2	14	0.1654	5.353
2	15	0.1846	5.778
3	0	–0.0049	0.432
3	1	–0.0047	0.4822
3	2	–0.0033	0.6293
3	3	0	0.864
3	4	0.0059	1.1726
3	5	0.0144	1.5397
3	6	0.0255	1.9498
3	7	0.0387	2.3894
3	8	0.0537	2.8468
3	9	0.07	3.3129
3	10	0.0873	3.7807
3	11	0.1054	4.2452
3	12	0.124	4.7026
3	13	0.1429	5.1507
3	14	0.162	5.5877
3	15	0.1813	6.0127

N_A	N_B	ΔGf_C(sHz)	SL(dB)
4	0	–0.0108	0.7406
4	1	–0.0106	0.7908
4	2	–0.0092	0.9379
4	3	–0.0059	1.1726
4	4	0	1.4812
4	5	0.0086	1.8483
4	6	0.0196	2.2584
4	7	0.0328	2.698
4	8	0.0478	3.1554
4	9	0.0641	3.6215
4	10	0.0815	4.0893
4	11	0.0995	4.5538
4	12	0.1181	5.0112
4	13	0.137	5.4593
4	14	0.1562	5.8963
4	15	0.1754	6.3213
5	0	–0.0193	1.1077
5	1	–0.0191	1.1578
5	2	–0.0178	1.305
5	3	–0.0144	1.5397
5	4	–0.0086	1.8483
5	5	0	2.2153
5	6	0.0111	2.6255
5	7	0.0243	3.065
5	8	0.0392	3.5225
5	9	0.0556	3.9886
5	10	0.0729	4.4564
5	11	0.091	4.9208
5	12	0.1096	5.3783
5	13	0.1285	5.8263
5	14	0.1476	6.2633
5	15	0.1668	6.6884
6	0	–0.0304	1.5178
6	1	–0.0302	1.568
6	2	–0.0288	1.7152
6	3	–0.0255	1.9498
6	4	–0.0196	2.2584
6	5	–0.0111	2.6255
6	6	0	3.0357
6	7	0.0132	3.4752
6	8	0.0282	3.9326
6	9	0.0445	4.3987
6	10	0.0619	4.8666
6	11	0.0799	5.331
6	12	0.0985	5.7885
6	13	0.1174	6.2365
6	14	0.1366	6.6735
6	15	0.1558	7.0985
7	0	–0.0436	1.9574
7	1	–0.0434	2.0076
7	2	–0.0421	2.1547
7	3	–0.0387	2.3894
7	4	–0.0328	2.698
7	5	–0.0243	3.065
7	6	–0.0132	3.4752
7	7	0	3.9148
7	8	0.015	4.3722
7	9	0.0313	4.8383
7	10	0.0486	5.3061
7	11	0.0667	5.7706
7	12	0.0853	6.228
7	13	0.1042	6.6761
7	14	0.1233	7.1131
7	15	0.1426	7.5381

TABLE 2 (continued)

N_A	N_B	ΔGf_C(sHz)	SL(dB)
8	0	–0.0585	2.4148
8	1	–0.0583	2.465
8	2	–0.057	2.6121
8	3	–0.0537	2.8468
8	4	–0.0478	3.1554
8	5	–0.0392	3.5225
8	6	–0.0282	3.9326
8	7	–0.015	4.3722
8	8	0	4.8296
8	9	0.0163	5.2957
8	10	0.0337	5.7635
8	11	0.0517	6.228
8	12	0.0703	6.6854
8	13	0.0892	7.1335
8	14	0.1084	7.5705
8	15	0.1276	7.9955
9	0	–0.0749	2.8809
9	1	–0.0747	2.9311
9	2	–0.0733	3.0782
9	3	–0.07	3.3129
9	4	–0.0641	3.6215
9	5	–0.0556	3.9886
9	6	–0.0445	4.3987
9	7	–0.0313	4.8383
9	8	–0.0163	5.2957
9	9	0	5.7618
9	10	0.0173	6.2296
9	11	0.0354	6.6941
9	12	0.054	7.1515
9	13	0.0729	7.5996
9	14	0.092	8.0366
9	15	0.1113	8.4616
10	0	–0.0922	3.3487
10	1	–0.092	3.3989
10	2	–0.0907	3.546
10	3	–0.0873	3.7807
10	4	–0.0815	4.0893
10	5	–0.0729	4.4564
10	6	–0.0619	4.8666
10	7	–0.0486	5.3061
10	8	–0.0337	5.7635
10	9	–0.0173	6.2296
10	10	0	6.6975
10	11	0.0181	7.1619
10	12	0.0367	7.6194
10	13	0.0556	8.0674
10	14	0.0747	8.5044
10	15	0.0939	8.9294
11	0	–0.1103	3.8132
11	1	–0.1101	3.8634
11	2	–0.1088	4.0105
11	3	–0.1054	4.2452
11	4	–0.0995	4.5538
11	5	–0.091	4.9208
11	6	–0.0799	5.331
11	7	–0.0667	5.7706
11	8	–0.0517	6.228
11	9	–0.0354	6.6941
11	10	–0.0181	7.1619
11	11	0	7.6264
11	12	0.0186	8.0838
11	13	0.0375	8.5318
11	14	0.0566	8.9688
11	15	0.0759	9.3939

N_A	N_B	ΔGf_C(sHz)	SL(dB)
12	0	–0.1289	4.2706
12	1	–0.1287	4.3208
12	2	–0.1273	4.468
12	3	–0.124	4.7026
12	4	–0.1181	5.0112
12	5	–0.1096	5.3783
12	6	–0.0985	5.7885
12	7	–0.0853	6.228
12	8	–0.0703	6.6854
12	9	–0.054	7.1515
12	10	–0.0367	7.6194
12	11	–0.0186	8.0838
12	12	0	8.5413
12	13	0.0729	7.5996
12	14	0.092	8.0366
12	15	0.1113	8.4616
13	0	–0.1478	4.7187
13	1	–0.1476	4.7688
13	2	–0.1463	4.916
13	3	–0.1429	5.1507
13	4	–0.137	5.4593
13	5	–0.1285	5.8263
13	6	–0.1174	6.2365
13	7	–0.1042	6.6761
13	8	–0.0892	7.1335
13	9	–0.0729	7.5996
13	10	–0.0556	8.0674
13	11	–0.0375	8.5318
13	12	–0.0189	8.9893
13	13	0	9.4373
13	14	0.0191	9.8743
13	15	0.0384	10.299
14	0	–0.1669	5.1557
14	1	–0.1667	5.2058
14	2	–0.1654	5.353
14	3	–0.162	5.5877
14	4	–0.1562	5.8963
14	5	–0.1476	6.2633
14	6	–0.1366	6.6735
14	7	–0.1233	7.1131
14	8	–0.1084	7.5705
14	9	–0.092	8.0366
14	10	–0.0747	8.5044
14	11	–0.0566	8.9688
14	12	–0.038	9.4263
14	13	–0.0191	9.8743
14	14	0	10.311
14	15	0.0192	10.736
15	0	–0.1862	5.5807
15	1	–0.186	5.6309
15	2	–0.1846	5.778
15	3	–0.1813	6.0127
15	4	–0.1754	6.3213
15	5	–0.1668	6.884
15	6	–0.1558	7.0985
15	7	–0.1426	7.5381
15	8	–0.1276	7.9955
15	9	–0.1113	8.4616
15	10	–0.0939	8.9294
15	11	–0.0759	9.3939
15	12	–0.0573	9.8514
15	13	–0.0384	10.299
15	14	–0.0192	10.736
15	15	0	11.162

SERVO DEMODULATOR

Four gated peak detectors are incorporated for recovery of embedded servo information. The ML6310 provides four buffered low impedance outputs (A, B, C, D), which represent the peak detected level of each servo burst. The voltages on these pins are suitable for digitizing by an external A/D converter and processed by the controlling microprocessor for head positioning. With the help of the SMODE bit in control register #6, these four outputs can be configured to be (A+B, A–B, C+D, C–D) using internal summation and difference amplifiers. The summation outputs (A+B, C+D) are equal to the sum of the peak detected levels divided by 2. The difference outputs (A–B, C–D) are equal to the difference of the peak detected levels divided by 2. The zero-level for the difference outputs (A–B, C–D) is given at the VRSVO pin. The typical value for this reference signal is 1V. There is also a VSET bit in control register #6 which controls the direction of the VRSVO pin. If VSET = 0, the difference zero-level is generated internally (1V). If VSET = 1, an external reference voltage is used to set the difference zero-level.

The zero-level for the buffered servo outputs (A, B, C, D) or the summation outputs (A+B, C+D) is internally generated and has a value of 0.5V.

1	1	0	RSVD	SMODE	VSET	PM1	PM0

The servo peak detectors in the demodulator section receive the servo burst signal from the lowpass output of the filter/equalizer, which are then amplified to the proper amplitude and sent through a full wave rectifier before the sample and hold operation. There are four identical peak and hold circuits, with internal holding capacitors which perform the sample and hold operation. This optimized architecture thus provides for higher integration by not only eliminating the four external holding capacitors but also the pins required for them, thus contributing towards minimizing the external component count and hence cost.

POWER MANAGEMENT

The ML6310 provides a hardware pin ($\overline{PDNB}$) and two bits in the control register #6 for five levels of micro power management control.

1	1	0	RSVD	SMODE	VSET	PM1	PM0

The major circuit blocks in the ML6310 comprise of the regulator, the serial interface, the AGC, the filter/equalizer, the pulse detector, the servo demodulator and the bias circuits. The $\overline{PDNB}$ pin in conjunction with the two bits in the control register #6 can be used to selectively turn of a combination of these blocks depending on the mode of operation viz, read mode, write mode, servo mode, etc. This allows the system designer to turn off the sections of the chip that are not in use during the operation and thus minimize power dissipation at a micro management level. Table 3 below shows these five different power management modes and the circuits that are active in these individual modes.

TABLE 3: Power Management Modes

PIN	PM1	PM0	POWER MANAGEMENT MODE
1	0	0	Normal mode
1	0	1	Servo mode
1	1	0	Data mode
1	1	1	Idle mode
0	X	X	Sleep mode

Normal Mode — All circuits are enabled. Typical Power dissipation @ 2.7V is 175mW.

Servo Mode — Pulse Detector is disabled. Typical Power dissipation @ 2.7V is 150mW.

Data Mode — Servo demodulator is disabled. Typical Power dissipation @ 2.7V is 160mW.

Idle Mode — Only serial interface circuit and regulator are enabled. In 3V mode of operation the regulator is not used and could be powered off using the 'reg' bit in control register #5. Typical Power dissipation @ 4.75V is 4mW. Typical Power dissipation @ 2.7V is 1.2µW.

Sleep Mode — All circuits disabled, however control registers will hold latest programmed data and can be accessed through the serial interface. Typical Power dissipation @ 2.7V is 0.5µW.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is shifted serially into the ML6310 on the SDATA line on the falling edges of the serial shift clock, SCLK, provided the $\overline{SENB}$ pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme thus allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset bit configuration so that the behavior of the chip is predictable. The control registers retain their programmed information in any of the power-down modes, until the chip is physically powered-down. When the $\overline{SENB}$ pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the $\overline{SENB}$, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. Control register #7 is not used and some of the bits in control register 0 through 6 are reserved. Outlined below are the detailed bit by bit definitions of the control registers 0 through 6.

CONTROL REGISTER #0

Data Channel filter cutoff frequency control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	$Dfc4$	$Dfc3$	$Dfc2$	$Dfc1$	$Dfc0$

CONTROL REGISTER #1

Servo Channel filter cutoff frequency control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	$Sfc4$	$Sfc3$	$Sfc2$	$Sfc1$	$Sfc0$

f_C4	f_C3	f_C2	f_C1	f_C0	f_C (MHz)
0	0	0	0	0	6.000
0	0	0	0	1	6.387
0	0	0	1	0	6.774
0	0	0	1	1	7.161
0	0	1	0	0	7.548
0	0	1	0	1	7.935
0	0	1	1	0	8.323
0	0	1	1	1	8.710
0	1	0	0	0	9.097
0	1	0	0	1	9.484
0	1	0	1	0	9.871
0	1	0	1	1	10.258
0	1	1	0	0	10.645
0	1	1	0	1	11.032
0	1	1	1	0	11.419
0	1	1	1	1	11.806
1	0	0	0	0	12.194
1	0	0	0	1	12.581
1	0	0	1	0	12.968
1	0	0	1	1	13.355
1	0	1	0	0	13.742
1	0	1	0	1	14.129
1	0	1	1	0	14.516
1	0	1	1	1	14.903
1	1	0	0	0	15.290
1	1	0	0	1	15.677
1	1	0	1	0	16.065
1	1	0	1	1	16.452
1	1	1	0	0	16.839
1	1	1	0	1	17.226
1	1	1	1	0	17.613
1	1	1	1	1	18.000

CONTROL REGISTER #2

Asymmetric equalization (slimming) — zero A (N_A)

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	RSVD	EA3	EA2	EA1	EA0

Refer to Table 2 for programming configurations

CONTROL REGISTER #3

Asymmetric equalization (slimming) — zero B (N_B)

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	RSVD	EB3	EB2	EB1	EB0

Refer to Table 2 for programming configurations

CONTROL REGISTER #4

Hysteresis Comparator qualification level

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	RSVD	HYS3	HYS2	HYS1	HYS0

HYS3	HYS2	HYS1	HYS0	% OF SIGNAL PEAK
0	0	0	0	0.00 %
0	0	0	1	6.25 %
0	0	1	0	12.50 %
0	0	1	1	18.75 %
0	1	0	0	25.00 %
0	1	0	1	31.25 %
0	1	1	0	37.50 %
0	1	1	1	43.75 %
1	0	0	0	50.00 %
1	0	0	1	56.25 %
1	0	1	0	62.50 %
1	0	1	1	68.75 %
1	1	0	0	75.00 %
1	1	0	1	81.25 %
1	1	1	0	87.50 %
1	1	1	1	93.75 %

CONTROL REGISTER #5

AGC Attack & Decay rate control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	REG	DKY1	DKY0	AKY1	AKY0

REG bit = 1 implies regulator is ON

REG bit = 0 implies regulator is OFF

This bit applies only in the 3V operating mode where the regulator could be switched OFF, to minimize power dissipation, as it is not needed. This bit must be set to a "1" in the 5V operating mode.

ATK1	ATK0	AGC ATTACK CURRENT
0	0	30µA
0	1	60µA
1	0	90µA
1	1	120µA

DKY1	DKY0	AGC DECAY CURRENT
0	0	3.0µA
0	1	5.0µA
1	0	7.0µA
1	1	9.0µA

CONTROL REGISTER #6

Miscellaneous functions register

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	RSVD	SMODE	VSET	PM1	PM0

RSVD implies bit reserved for future use. Can be zero or one.

PM1, PM0 power management mode bits

$\overline{\text{PDNB}}$ PIN	PM1	PM0	POWER MANAGEMENT MODE
1	0	0	Normal mode
1	0	1	Servo mode
1	1	0	Data mode
1	1	1	Idle mode
0	x	x	Sleep mode

SMODE = 1 implies servo demodulator outputs are configured as A+B, A–B, C+D, C–D

SMODE = 0 implies servo demodulator outputs are configured as A, B, C, D

VSET = 1 VRSVO servo reference pin configured as **input**. This allows the use of an external reference to calibrate the servo demodulator outputs for data conversion.

VSET = 0 VRSVO servo reference pin configured as **output**. This implies that the internal reference is used to calibrate the servo demodulator outputs for data conversion purposes.

ORDERING INFORMATION

PART NUMBER	VCC RANGE	TEMPERATURE RANGE	PACKAGE
ML6310 CH2	2.7V to 3.3V	0°C to 70°C	32-pin TQFP (H32)
ML6310 CH3	3.0V to 3.6	0°C to 70°C	32-pin TQFP (H32)
ML6310 CH5	4.5V to 5.5V	0°C to 70°C	32-pin TQFP (H32)