14-BIT 1:2 REGISTERED BUFFER WITH PARITY

IDT74SSTU32D869

FEATURES:

- **1.8V Operation**
- **Designed to drive low impedance nets**
- **SSTL_18 style clock and data inputs**
- **Differential CLK input**
- **Control inputs compatible with LVCMOS levels**
- **Center input architecture for optimum PCB design**
- **Latch-up performance exceeds 100mA**
- **ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)**
- **Available in 150-pin CTBGA package**

APPLICATIONS:

- **Along with CSPU877/A/D DDR2 PLL, provides complete solution for DDR2 DIMMs**
- **Optimized for DDR2-400/533 [PC2-3200/4300] Raw card L**

DESCRIPTION:

The SSTU32D869 is a 14-bit 1:2 configurable registered buffer designed for 1.7V to 1.9V V_{DD} operation. All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32D869 operates from a differential clock (CLK and $\overline{CLK}$). Data are registered at the crossing of CLK going high and $\overline{CLK}$ going low.

The SSTU32D869 includes a parity checking function. The SSTU32D869 accepts parity bits from the memory controller at its input pins PARIN[1:2], compares it with the data received on the D-inputs, and indicates whether a parity error has occured on its open-drain $\overline{PTYERR[1:2]}$ pins (active low). When used as a single device, the C1 inputs are tied low. In this configuration, the partial-parity-out (PPO[1:2]) and $\overline{PTYERR[1:2]}$ signals are produced two clock cycles after the corresponding data output. When used in pairs, the C1 inputs of the first register are tied low and the C1 inputs of the second register are tied high. The $\overline{PTYERR[1:2]}$ outputs of the first SSTU32D869 is left floating and the valid error information is latched on the $\overline{PTYERR[1:2]}$ outputs of the second SSTU32D869 .

This device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{RESET}$ and Cx inputs must always be held at a valid logic high or low level.

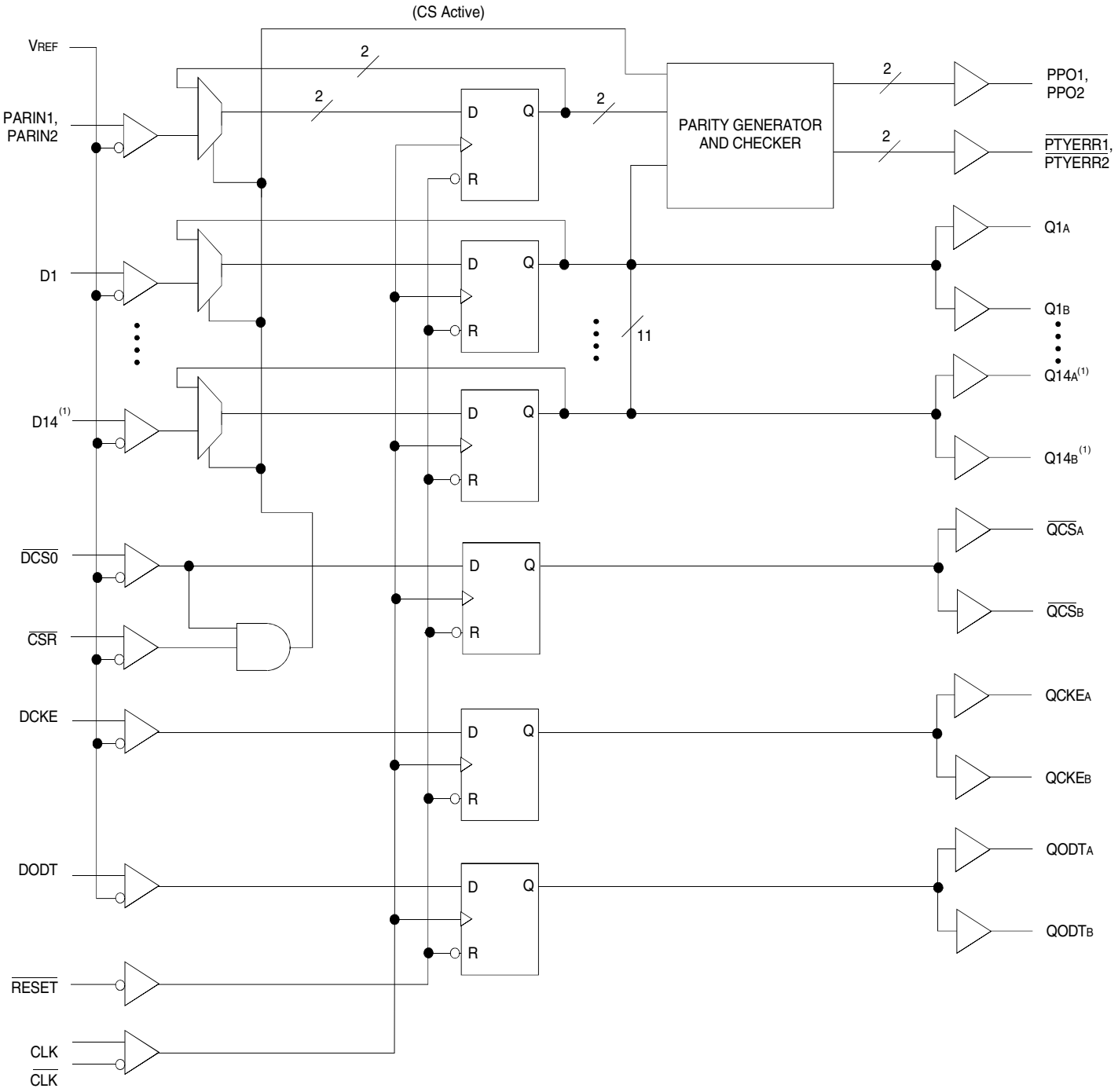
To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 DIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CLK and $\overline{CLK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of a reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RESET}$ until the input receivers are fully enabled, the design of the SSTU32D869 must ensure that the outputs will remain low, thus ensuring no glitches on the outputs.

The device monitors the $\overline{DCS}$ input and will gate the Qn outputs from changing states when $\overline{DCS}$ is high. If the $\overline{DCS}$ input is low, the Qn outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ control and will force the Qn outputs low and the $\overline{PTYERR[1:2]}$ outputs high. The EF[0:3] inputs control the driver strength and slew rate for both the A and B outputs independently.

This device also supports low-power active operation by monitoring both system chip select ($\overline{DCS}$ and $\overline{CSR}$) inputs and will fate the Qn and PPO outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are high. If either $\overline{DCS}$ and $\overline{CSR}$ input is low, the Qn and PPO outputs will function normally. Also, if the $\overline{DCS}$ and $\overline{CSR}$ are high, the device will gate the $\overline{PTYERR[1:2]}$ outputs from changing states. If the $\overline{DCS}$ and $\overline{CSR}$ are low, the $\overline{PTYERR[1:2]}$ will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control. When driven low, they will force the Qn and PPO outputs low and the $\overline{PTYERR[1:2]}$ outputs high. If the $\overline{DCS}$ control functionality is not desired, then the $\overline{CSR}$ input can be hard-wired to ground, in which case the setup-time requirement for the $\overline{DCS}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{DCS}$ only, then the $\overline{CSR}$ input should be pulled up to V_{DD} through a pullup resistor.

FUNCTIONAL BLOCK DIAGRAM (1:2)



NOTE:
1. This range does not include D1, D4, and D7, and their corresponding outputs.

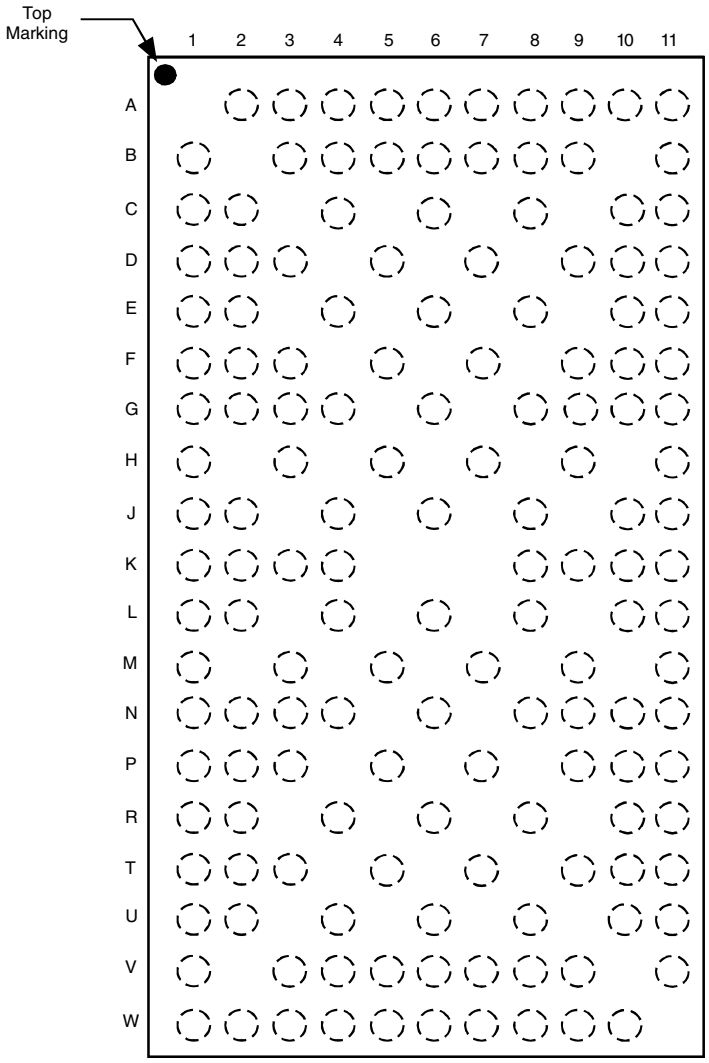
PIN CONFIGURATION[1]

	1	2	3	4	5	6	7	8	9	10	11
A	NB	VDD	EF0	PPO2	GND	VREF	GND	PARIN2	EF1	VDD	$\overline{\text{PYTERR2}}$
B	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
C	QCKEA	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	QCKEB
D	Q2A	VDD	GND	NB	DCKE	NB	D2	NB	GND	VDD	Q2B
E	Q3A	VDD	NB	D3	NB	NC	NB	DODT	NB	C1	Q3B
F	QODTA	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	QODTB
G	Q5A	VDD	GND	D5	NB	CLK	NB	D6	GND	VDD	Q5B
H	Q6A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q6B
J	$\overline{\text{QCSA}}$	VDD	NB	NC	NB	$\overline{\text{RST}}$	NB	$\overline{\text{CSR}}$	NB	VDD	$\overline{\text{QCSB}}$
K	VDD	VDD	GND	GND	NB	NB	NB	GND	VDD	VDD	VDD
L	Q8A	VDD	NB	$\overline{\text{DCS}}$	NB	$\overline{\text{CLK}}$	NB	D8	NB	VDD	Q8B
M	Q9A	NB	GND	NB	NC	NB	NC	NB	GND	NB	Q9B
N	Q10A	VDD	GND	D9	NB	NC	NB	D10	GND	VDD	Q10B
P	Q11A	VDD	GND	NB	NC	NB	NC	NB	GND	VDD	Q11B
R	Q12A	C1	NB	D11	NB	NC	NB	D12	NB	VDD	Q12B
T	Q13A	VDD	GND	NB	D13	NB	D14	NB	GND	VDD	Q13B
U	Q14A	VDD	NB	GND	NB	GND	NB	GND	NB	VDD	Q14B
V	VDD	NB	VDD	GND	GND	GND	GND	GND	VDD	NB	VDD
W	$\overline{\text{PYTERR1}}$	VDD	EF2	PARIN1	GND	VREF	GND	PPO1	EF3	VDD	NB

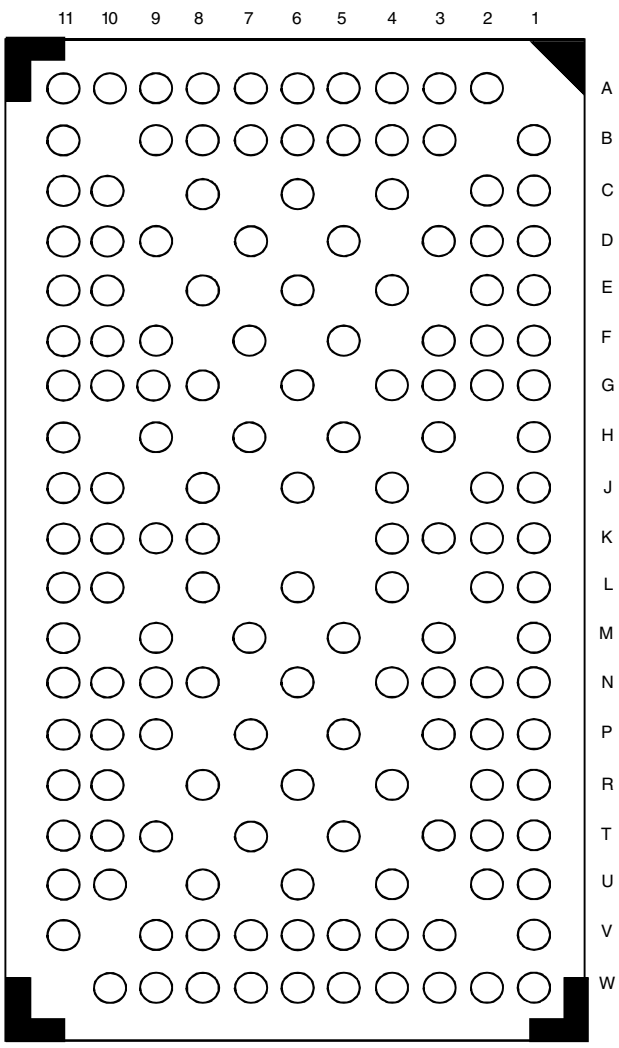
150-BALL CTBGA
TOP VIEW

NOTE:
1. The symmetrical center input design allows the front and back register of a pair to share the same pinout. This keeps the component library simple.

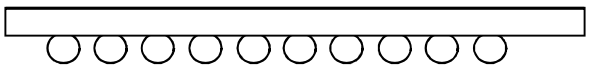
150 BALL CTBGA PACKAGE ATTRIBUTES



TOP VIEW



BOTTOM VIEW



SIDE VIEW

FUNCTION TABLE (EACH FLIP-FLOP) (1)

Inputs						Qx	$\overline{QCS}$x	QODTx, QCKEx
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Dx, DODT, DCKE	Outputs	Output	Outputs
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
H	H	H	↑	↓	L	Q_0(2)	H	L
H	H	H	↑	↓	H	Q_0(2)	H	H
H	H	H	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

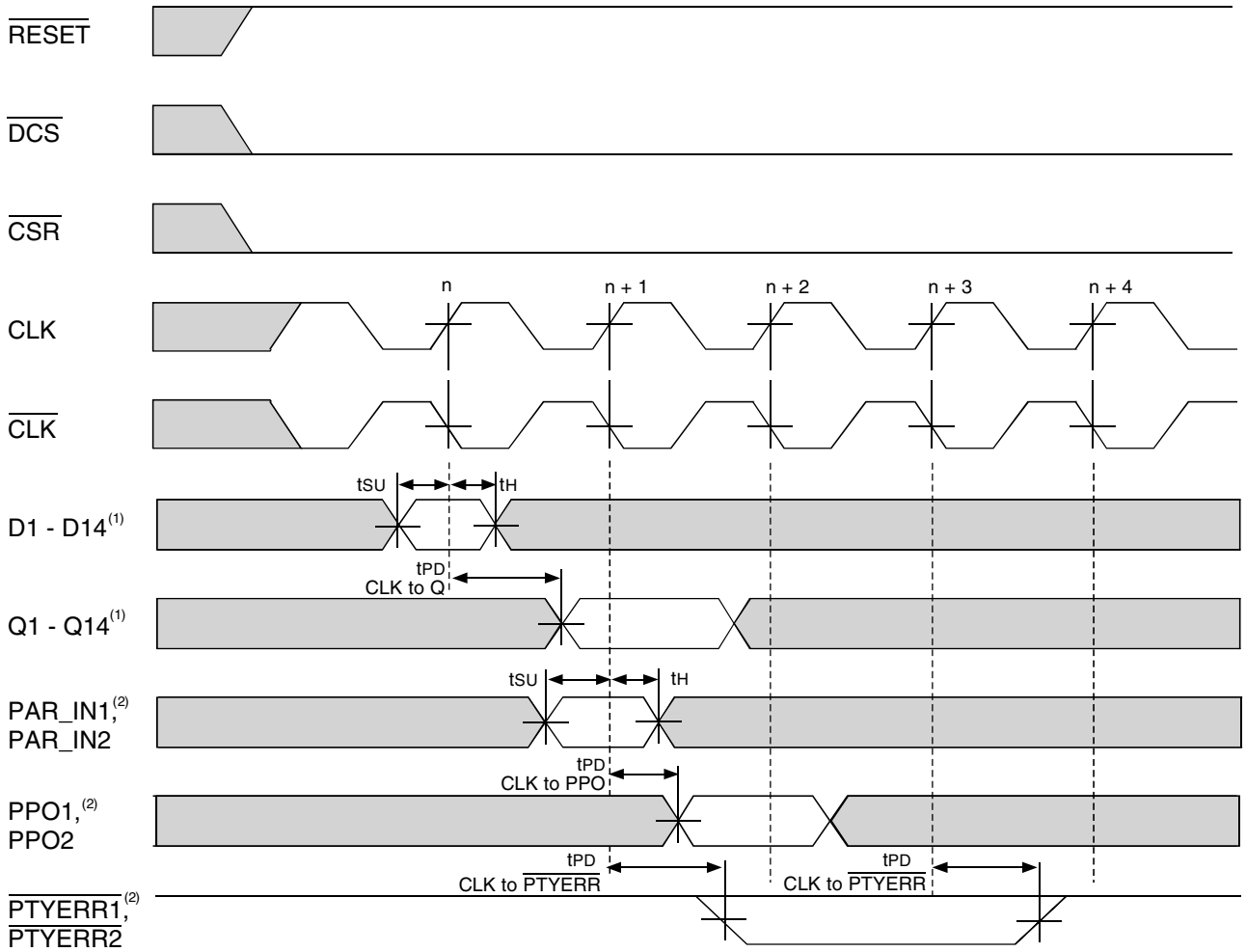
NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. Output level before the indicated steady-state conditions were established.

PARITY AND STANDBY FUNCTION TABLE(1)

Inputs							Outputs	
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Σ of Inputs = H (D1 - D14)(2)	PAR_IN(3)	PPO(3,4)	$\overline{PTYERR}$(3,5)
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	X	L	↑	↓	Even	L	L	H
H	X	L	↑	↓	Odd	L	H	L
H	X	L	↑	↓	Even	H	H	L
H	X	L	↑	↓	Odd	H	L	H
H	H	H	↑	↓	X	X	PPO_0	$\overline{PTYERR}_0$
H	X	X	L or H	L or H	X	X	PPO_0	$\overline{PTYERR}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	H

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. This range does not include D1, D4, and D7.
3. PARIN1 is used to generate PPO1 and $\overline{PTYERR1}$. PARIN2 is used to generate PPO2 and $\overline{PTYERR2}$.
4. PAR_IN arrives one clock cycle (C1 = 0), or two clock cycles (C1 = 1), after the data to which it applies.
5. This transition assumes $\overline{PTYERR[1:2]}$ is HIGH at the crossing of CLK going HIGH and $\overline{CLK}$ going LOW. If $\overline{PTYERR[1:2]}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{RESET}$ is driven LOW.

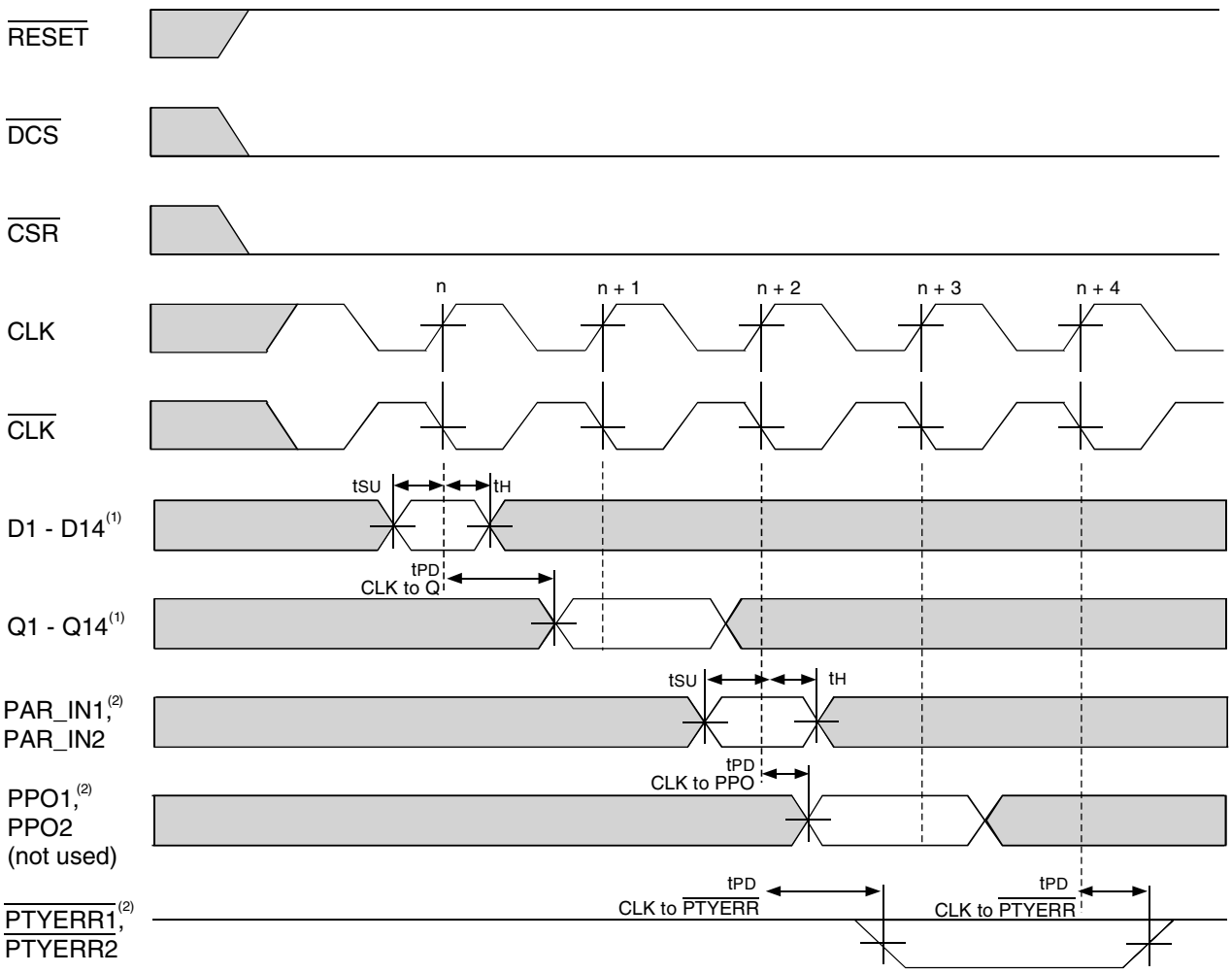
REGISTER TIMING



Timing Diagram for the First SSTU32D869 Device, C1 = 0

NOTES:
1. This range does not include D1, D4, and D7, and their corresponding outputs.
2. PAR_IN1 is used to generate PPO1 and $\overline{\text{PTYERR1}}$. PAR_IN2 is used to generate PPO2 and $\overline{\text{PTYERR2}}$.

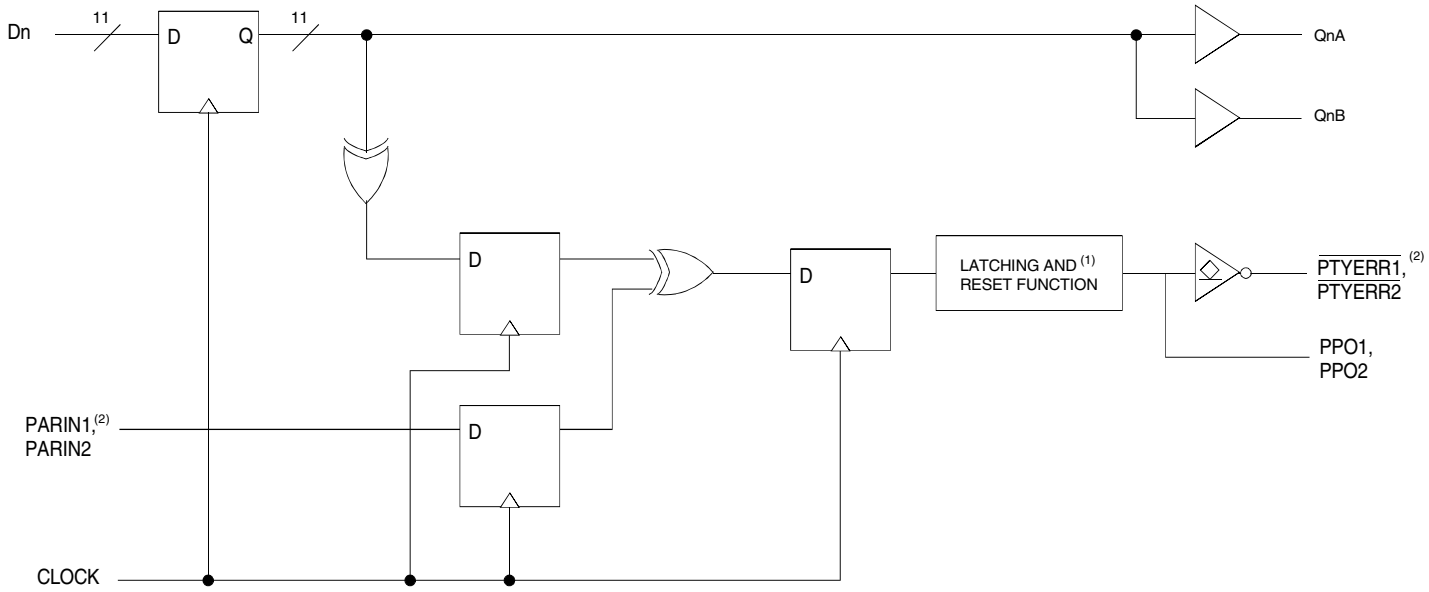
REGISTER TIMING



Timing Diagram for the Second SSTU32D869 Device Used in a Pair; C1 = 1

NOTES:
1. This range does not include D1, D4, and D7, and their corresponding outputs.
2. PAR_IN1 is used to generate PPO1 and $\overline{\text{PTYERR1}}$. PAR_IN2 is used to generate PPO2 and $\overline{\text{PTYERR2}}$.

PARITY LOGIC DIAGRAM



NOTES:
1. This function holds the error for two cycles. See REGISTER TIMING diagram.
2. PAR_IN1 is used to generate $\overline{\text{PTYERR1}}$. PAR_IN2 is used to generate $\overline{\text{PTYERR2}}$.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description		Max.	Unit
V_{DD}	Supply Voltage Range		–0.5 to 2.5	V
V_I(2,3)	Input Voltage Range		–0.5 to 2.5	V
V_O(2,3)	Output Voltage Range		–0.5 to V_{DD} +0.5	V
I_{IK}	Input Clamp Current	V_I < 0	±50	mA
		V_I > V_{DD}		
I_{OK}	Output Clamp Current	V_O < 0	±50	mA
		V_O > V_{DD}		
I_O	Continuous Output Current, V_O = 0 to V_{DD}		±50	mA
V_{DD}	Continuous Current through each V_{DD} or GND		±100	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
3. This value is limited to 2.5V maximum.

MODE SELECT

C_1	Device Mode
0	Single Device, Front
1	Second Device in Pair, Back

OUTPUT CONTROL

EF0,(1) EF3	EF1,(1) EF2	Output
0	0	Standard Drive, Higher Slew
0	1	Standard Drive, Standard Slew
1	0	Higher Drive, Higher Slew
1	1	Higher Drive, Standard Slew

NOTE:
1. EF0 and EF2 control QA outputs; EF1 and EF3 control QB outputs.

TERMINAL FUNCTIONS

Signal Group	Terminal Name	Type	Description
Ungated Inputs	DCKE, DODT	SSTL_18	DRAM function pins not associated with Chip Select
Chip Select Gated Inputs	D1:D14[1]	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW
Chip Select Inputs	$\overline{DCS}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be LOW when a valid address/command is present. The register can be programmed to re-drive all D-inputs only ($\overline{CSR}$ HIGH) when at least one Chip Select input is LOW.
Re-Driven Outputs	Q1A:Q14A[1] Q1B:Q14B[1] $\overline{QCS}$A, B QCKEA, B QODTA, B	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock
Parity Input	PARIN1, PARIN2	SSTL_18	Input parity is received on pin PARIN, and should maintain odd parity across the D1:D14 inputs, at the rising edge of the clock
Partial Parity Output	PPO1, PPO2	SSTL_18	PPO1 of the front register is connected to PAR_IN1 of the back register, and PPO2 to PAR_IN2, respectively.
Parity Error Output	$\overline{PTYERR1}$, $\overline{PTYERR2}$	Open Drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{PTYERR}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program Inputs	$\overline{CSR}$	SSTL_18	Chip Select Gate Enable. When HIGH, the D1:D14 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D1:D14 inputs will be latched and redriven on every rising edge of the clock.
Clock Inputs	CLK, $\overline{CLK}$	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CLK).
Miscellaneous Inputs	C1	1.8V LVCMOS	Configuration Pins. When C1 is LOW, the register is used as a single register, or as the first register when used in pairs. When C1 is HIGH, the register is used as the second register in a pair.
	EF0:EF3	1.8V LVCMOS	Output Control
	$\overline{RESET}$	1.8V LVCMOS	Asynchronous Reset Input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{RESET}$ also resets the $\overline{PTYERR}$ signal.
	V_{REF}	0.9V nominal	Input reference voltage for SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.

NOTE:
1. This range does not include D1, D4, and D7, and their corresponding outputs.

OPERATING CHARACTERISTICS, T_A = 25ºC (1,2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.7	—	1.9	V
V_{REF}	Reference Voltage		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
V_{TT}	Termination Voltage		V_{REF}– 40mV	V_{REF}	V_{REF}+ 40mV	V
V_I	Input Voltage		0	—	V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Data Inputs	V_{REF}+ 250mV	—	—	V
V_{IL}	AC Low-Level Input Voltage	Data Inputs	—	—	V_{REF}– 250mV	V
V_{IH}	DC High-Level Input Voltage	Data Inputs	V_{REF}+ 125mV	—	—	V
V_{IL}	DC Low-Level Input Voltage	Data Inputs	—	—	V_{REF}– 125mV	V
V_{IH}	High-Level Input Voltage	$\overline{RESET}$, Cx	0.65 * V_{DD}	—	—	V
V_{IL}	Low-Level Input Voltage	$\overline{RESET}$, Cx	—	—	0.35 * V_{DD}	V
V_{ICR}	Common Mode Input Voltage	CLK, $\overline{CLK}$	0.675	—	1.125	V
V_{ID}	Differential Input Voltage	CLK, $\overline{CLK}$	600	—	—	mV
I_{OH}	High-Level Output Current		—	—	-8	mA
I_{OL}	Low-Level Output Current		—	—	+8	mA
T_A	Operating Free-Air Temperature		0	—	70	°C

NOTES:
1. The $\overline{RESET}$ and Cx inputs of the device must be held at valid levels (not floating) to ensure proper device operation.
2. The differential inputs must not be floating unless $\overline{RESET}$ is LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, V_{DD} = 1.8V ±0.1V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}		V_{DD} = 1.7V to 1.9V, I_{OH} = – 6 mA	1.2	—	—	V
V_{OL}		V_{DD} = 1.7V to 1.9V, I_{OL} = +6 mA	—	—	0.5	V
I_I	All Inputs	V_I = V_{DD} or GND	—	—	±5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = GND	—	—	200	µA
	Static Operating	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$	—	—	80	mA
I_{DDD}	Dynamic Operating (Clock Only)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle.	—	—	—	µA/Clock MHz
	Dynamic Operating (Per Each Data Input)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, 1:2 Mode, CLK and $\overline{CLK}$ Switching at 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	—	—	—	µA/Clock MHz/Data Input
C_I	Data Inputs	V_I = V_{REF} ± 250mV	2.5	—	4	pF
	$\overline{DCSn}$ / $\overline{CSR}$	V_I = V_{REF} ± 250mV	4	—	6	
	CLK and $\overline{CLK}$	V_{ICR} = 0.9V, V_{ID} = 600mV	4	—	6	
	$\overline{RESET}$	V_I = V_{DD} or GND	2	—	6	
	Parity Inputs	V_I = V_{REF} ± 250mV	2	—	3	

SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED) (1)

Symbol	Parameter	V_{DD} = 1.8V ± 0.1V		Unit
		Min	Max.	
f_{MAX}	Max Input Clock Frequency	340	—	MHz
t_{PDM}(2)	CLK and $\overline{CLK}$ to Q	1.41	2.15	ns
t_{LH}	LOW to HIGH Delay, CLK and $\overline{CLK}$ to $\overline{PTYERR}$	1.2	3	ns
t_{HL}	HIGH to LOW Delay, CLK and $\overline{CLK}$ to $\overline{PTYERR}$	1	3	ns
t_{PLH}	LOW to HIGH Propagation Delay, $\overline{RESET}$ to $\overline{PTYERR}$	—	3	ns
t_{PDMSS}(2,3)	CLK and $\overline{CLK}$ to Q (simultaneous switching)	—	2.25	ns
t_{RPHL}	$\overline{RESET}$ to Q	—	3	ns
dV/dt_r	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt_f	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt_Δ(4)	Output slew rate from 20% to 80%	—	1	V/ns

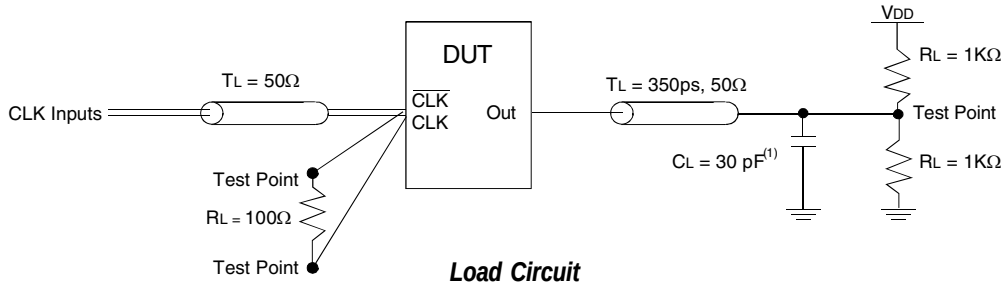
NOTES:
1. See TEST CIRCUITS AND WAVEFORMS.
2. Includes 350ps of test load transmission line delay.
3. This parameter is not production tested.
4. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

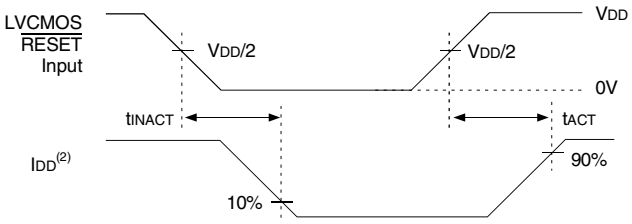
Symbol	Parameter		V_{DD} = 1.8V ± 0.1V		Unit
			Min.	Max.	
f_{CLOCK}	Clock Frequency		—	340	MHz
t_W	Pulse Duration, CLK, $\overline{CLK}$ HIGH or LOW		1	—	ns
t_{ACT}(1,2)	Differential Inputs Active Time		—	10	ns
t_{INACT}(1,3)	Differential Inputs Inactive Time		—	15	ns
t_{SU}	Setup Time	$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ HIGH	0.5	—	ns
		$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ LOW	0.3	—	
		DODT, $\overline{CSR}$, Data, and DCKE before CLK↑, $\overline{CLK}$↓	0.3	—	
t_H	Hold Time	Data, $\overline{DCS}$, $\overline{CSR}$, DCKE, and DODT after CLK↑, $\overline{CLK}$↓	0.3	—	ns

NOTES:
1. This parameter is not production tested.
2. Data and V_{REF} inputs must be low a minimum time of t_{ACT} max, after $\overline{RESET}$ is taken HIGH.
3. Data, V_{REF}, and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max, after $\overline{RESET}$ is taken LOW.

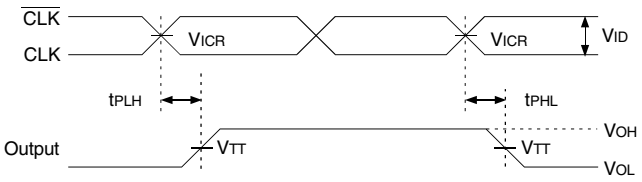
TEST CIRCUITS AND WAVEFORMS (V_{DD} = 1.8V ± 0.1V)



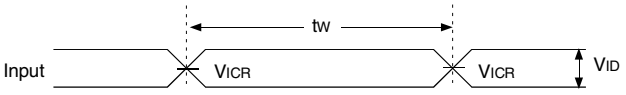
Load Circuit



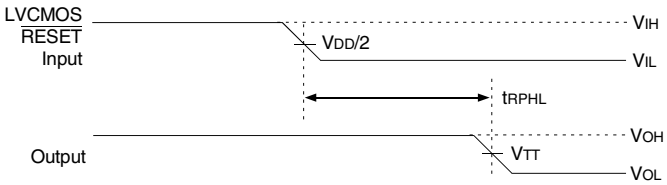
Voltage and Current Waveforms
Inputs Active and Inactive Times



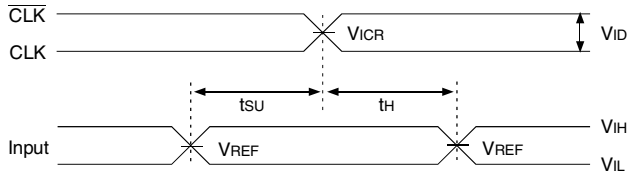
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



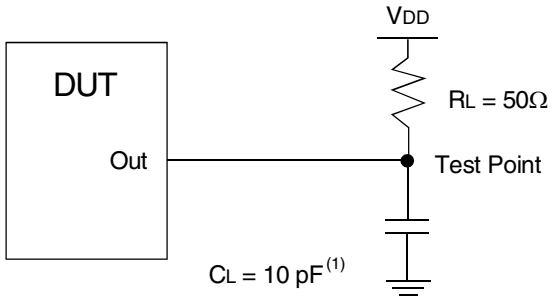
Voltage Waveforms - Propagation Delay Times



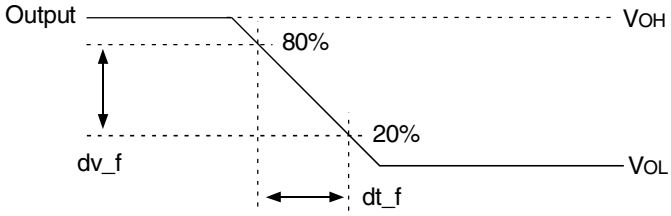
Voltage Waveforms - Setup and Hold Times

NOTES:
1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF}$ + 250mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ - 250mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600mV.
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.

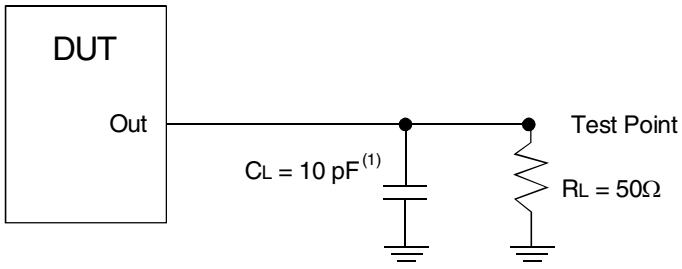
TEST CIRCUITS AND WAVEFORMS (V_{DD} = 1.8V ± 0.1V)



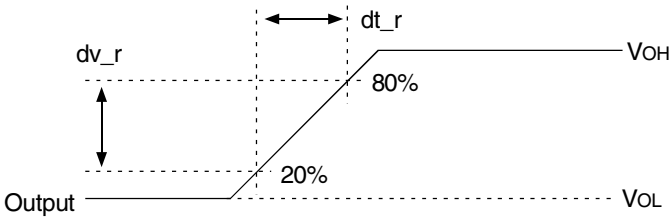
Load Circuit: High-to-Low Slew-Rate



Voltage Waveforms: High-to-Low Slew-Rate



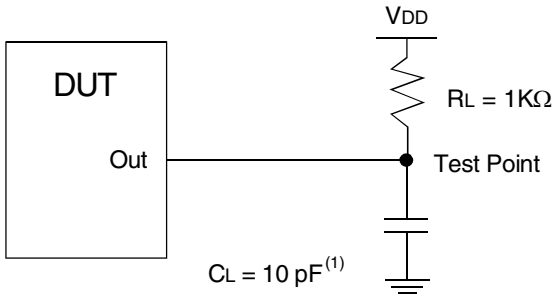
Load Circuit: Low-to-High Slew-Rate



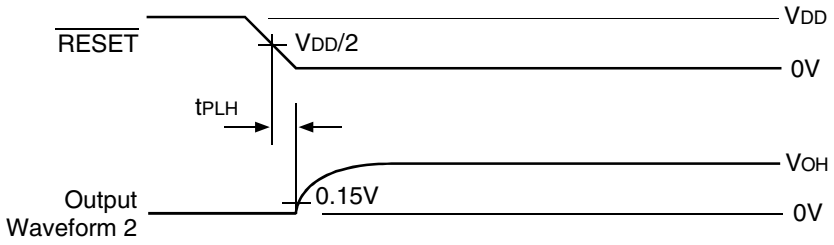
Voltage Waveforms: Low-to-High Slew-Rate

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

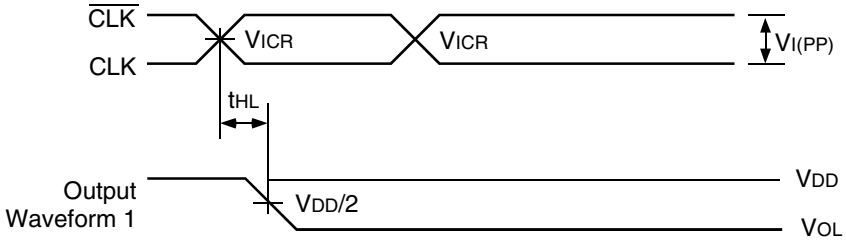
TEST CIRCUITS AND WAVEFORMS (V_{DD} = 1.8V ± 0.1V)



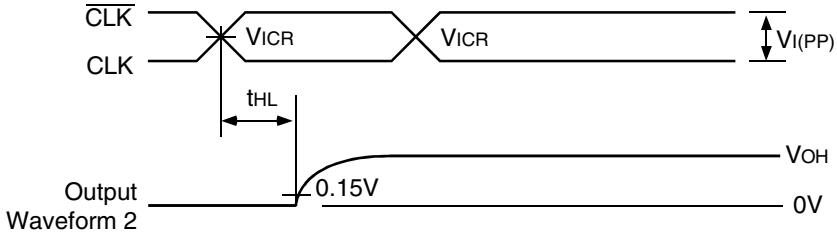
Load Circuit: $\overline{PTYERR}$ Output



Voltage Waveforms: Open Drain Output Low-to-High Transition Time



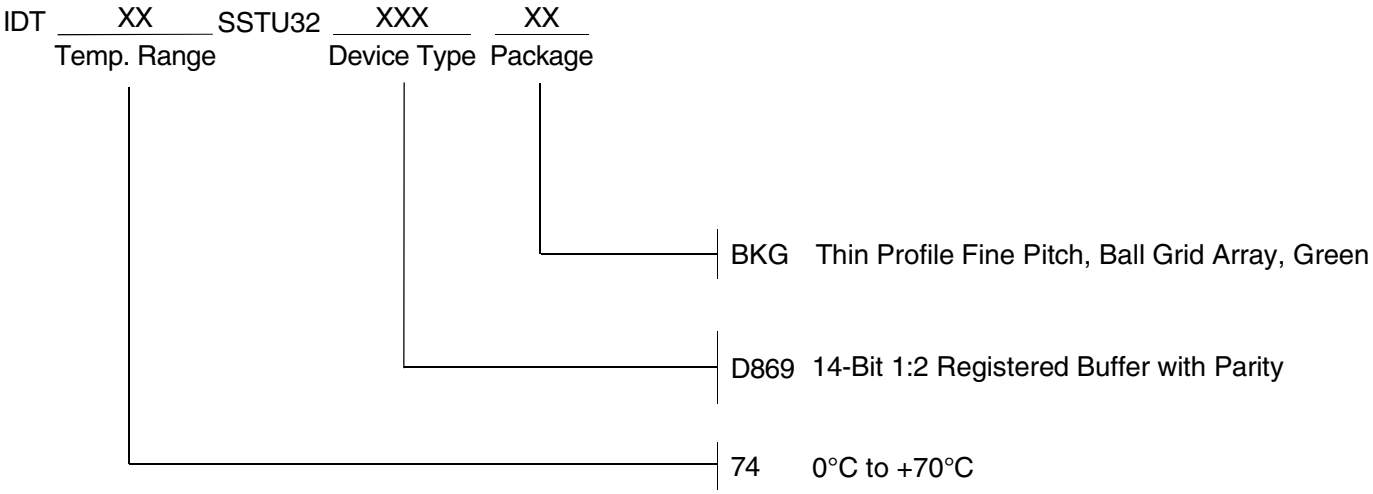
Voltage Waveforms: Open Drain Output High-to-Low Transition Time



Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with Respect to Clock Inputs)

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

ORDERING INFORMATION



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