Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

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SP9548

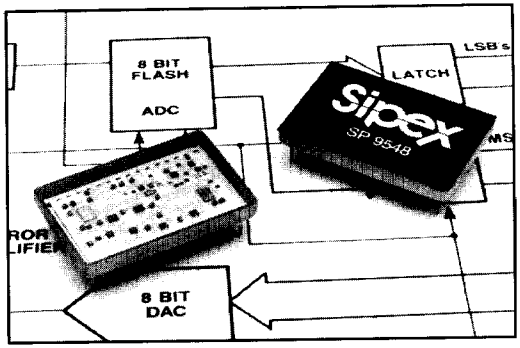
2 MHz, MULTIPASS™ 12-BIT A/D CONVERTER

DESCRIPTION

The SP9548 is a 12-bit, 500 nanosecond, analog-to-digital converter employing the SIPEX state-of-the-art Multipass™ subranging Flash technology while consuming much less than 2 Watts. The subranging Multipass process is optimized for low power operation by multiplexing a single 8-bit Flashe for each of the two ranges to yield a final resolution of 12 bits

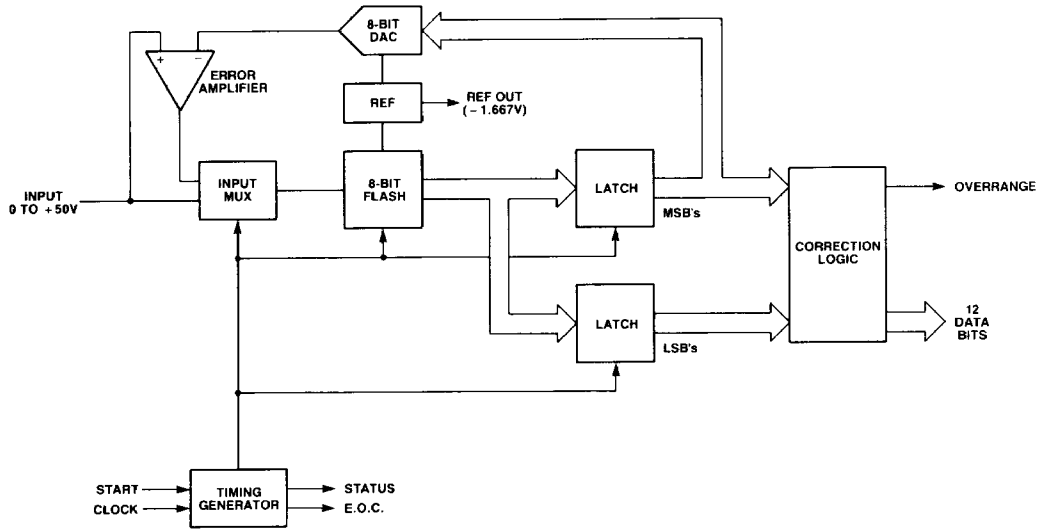
The SP9548 can be used in either a single or continuous mode. In the single mode, a START command initiates the conversion on the next CLOCK cycle. Total conversion can is completed in 500 nanoseconds...in synch with the clock.

In the continuous mode, the SP9548 can operate at a 2 MHz sampling rate and can be interfaced with the HS9720 Sample/Hold Amplifier. The SP9548 provides a control signal to the HS9720 permitting the S/H to begin tracking as soon as the Flash has latched the subrange data. This results in no conversion time degradation for the SP9548/HS9720 pair...the sampling time remains 2 MHz.



The SP9548 input range, 0 to +5V, has been optimized for high speed applications such as radar, sonar and video digitization, and high speed data acquisition systems. The SP9548 is ideal in all applications that require 12-bit performance at high speed with low power consumption.

FUNCTIONAL DIAGRAM



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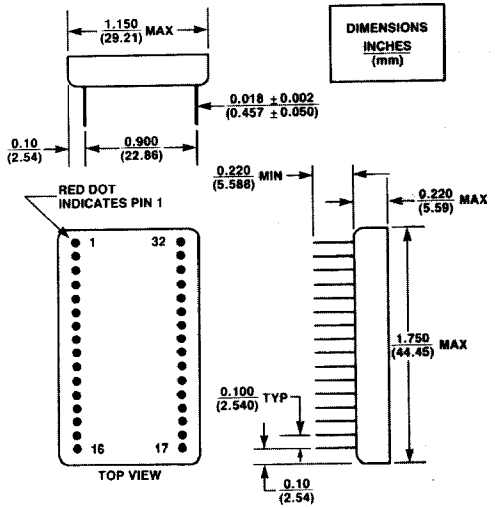
SPECIFICATIONS

(Typical @25°C and nominal supply voltages unless otherwise specified.)

MODEL	SP 9548
RESOLUTION	12-Bits
ANALOG INPUTS	
Input Voltage Range	0 to +5V
Input Impedance	1kΩ
DIGITAL INPUTS	
Logic Levels Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Loading	1 TTL Load
ACCURACY	
Integral Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
Differential Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
No Missing Codes	Guaranteed
Offset Error	0.1% of FSR typ, 0.3% max
Gain Error	0.2% of FSR typ, 0.5% max
DYNAMIC PERFORMANCE	
Conversion Time	500nsec
STABILITY	
Integral Linearity Tempco	10 ppm/°C
Differential Linearity Tempco	2 ppm/°C
Unipolar Offset Error Drift	5 ppm/°C
Gain Error Drift	40 ppm/°C
DIGITAL OUTPUTS	
Output Coding (Straight Binary)	See Table
Output Drive Capability	4 TTL Loads
REFERENCE	
Voltage	-1.67V nom
External Current	5mA
POWER SUPPLY REQUIREMENTS	
Current @nominal Voltage	
+15V (±10%)	20mA
-15V (±10%)	20mA
+5V Digital (±10%)	100mA
+5V Analog (±1%)	50mA
-5V (±1%)	50mA
Dissipation	1.6W typ, 2.0W max
PACKAGE	
Triple DIP — Metal	32-Pin

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK	32	START
2	STATUS	31	+5V DIGITAL
3	EOC	30	DIGITAL GND
4	BIT 12 (LSB)	29	+5V ANALOG
5	BIT 11	28	-5V
6	BIT 10	27	ANALOG GND
7	BIT 9	26	ANALOG GND
8	BIT 8	25	-15V
9	BIT 7	24	+15V
10	BIT 6	23	REF OUT
11	BIT 5	22	TEST POINT
12	BIT 4	21	NC
13	BIT 3	20	TEST POINT
14	BIT 2	19	NC
15	BIT 1 (MSB)	18	TRIM
16	OVERRANGE	17	ANALOG INPUT

THEORY OF OPERATION

INTERFACE INFORMATION

The SP 9548 is designed primarily for high speed applications that require a sampling rate of up to 2 MHz. It should be noted that the SP 9548 will also operate at slower rates than 2 MHz with no degradation in performance. The rate of conversion is set by the CLOCK signal that is applied to it. For ideal operation the CLOCK signal should be a square wave at twice the desired sampling rate...it takes two clock cycles for a total conversion.

The input stage has been designed for fast settling so as to function in a data acquisition environment with S/H amplifiers and multiplexers. As such, the input signal should be driven by a low impedance source sufficient to drive the 1K ohm input impedance at 12-bit accuracy. Most S/H amplifiers and fast operational amplifiers are adequate.

CONVERSION PROCESS

As shown in the block diagram, the input analog signal is attenuated and switched, via the input multiplexer (INPUT MUX) to the input of the 8-BIT FLASH ADC. The FLASH converter also receives a reference voltage (REF) of 1.667 volts. The input signal is compared to this reference in the conversion process by the FLASH converter and the resulting digital 8-bit word, which represents the most significant bits (MSB), is internally latched for further processing by both the 8-bit DAC and the CORRECTION LOGIC.

The above sequence is refered to as the "first pass" or "input" conversion. The resulting 8-bit word is sent to an 8-bit DAC which is trimmed to better than 12-bit accuracy. The DAC output is then directly subtracted from the input signal to determine the "error" or "second pass" input signal to be converted by the Flash.

The "second pass" occurs when the INPUT MUX switches the ERROR AMPLIFIER output to the input of the FLASH converter. The result of this conversion process is a digital word which represents the least significant bits (LSB). This digital output is also latched for processing by the CORRECTION LOGIC.

INPUT VOLTAGE	BINARY BITS OR	1	2	3	4	5	6	7	8	9	10	11	12	HEX CODE
0.00000		0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0.00122		0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
2.49878		0	1	1	1	1	1	1	1	1	1	1	1	0 7 F F
2.50000		1	0	0	0	0	0	0	0	0	0	0	0	0 8 0 0
2.50122		1	0	0	0	0	0	0	0	0	0	0	1	0 8 0 1
4.99878		1	1	1	1	1	1	1	1	1	1	1	1	0 F F F
5.00000	1	0	0	0	0	0	0	0	0	0	0	0	0	1 0 0 0
5.00122	1	0	0	0	0	0	0	0	0	0	0	0	1	1 0 0 1
5.29175	1	0	0	0	0	1	1	1	0	1	1	1	1	1 0 E F
5.83%	Overrange													

SP 9548 Coding Table @5 Volt Full Scale

The CORRECTION LOGIC accepts the 8 MSB's and the 8 LSB's and combines them by an improved, unique algorithm using digital addition. The result is a 12-bit digital word which accurately represents the analog input. The CORRECTION LOGIC also provides an overrange (O.R.) bit to indicate that the input has exceeded full scale. The output coding is straight binary. Refer to Coding Table.

The entire conversion process is controlled by the TIMING GENERATOR which requires requires a square wave CLOCK at twice the sampling speed i.e., the clock should be 4 MHz for 2 MHz operation. This is not to be confused with the Nyquist Criterion...2 MHz sampling can only convert input signals up to 1 MHz. The SP 9548 requires two such clock cycles (4 MHz) for a complete (2 MHz) sampling cycle or (500nsec) conversion.

SINGLE CONVERSION MODE

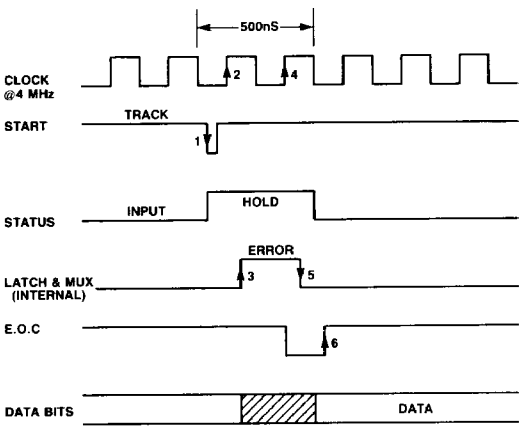
The single conversion mode is shown on the TIMING GENERATOR timing diagram. The timing sequence shown reflects the nominal minimum conversion time required...the START pulse is applied just before the rising edge of the clock. If the START pulse is applied immediately after the rising edge of the clock, the process will not begin until the next clock cycle.

If the START pulse is applied asynchronously then the conversion time will vary with the relationship of the START pulse to the clock...in any case the resulting data will still be accurate even though the conversion time may be varying from 350nsec to 850nsec.

Referring to the timing diagram, the process is as follows:

1. Negative going START pulse (50nsec min) is applied to the SP 9548 initiating conversion. In this mode the STATUS signal can be used to control a S/H amplifier as shown.
2. The rising edge of the next CLOCK cycle causes the FLASH to perform a conversion to determine the MSB's.
3. The FLASH data is latched for the DAC and accordingly the INPUT MUX is switched to the ERROR AMPLIFIER connecting it to the FLASH converter.
4. On the next CLOCK cycle, positive edge, the FLASH converts the error to determine the LSB's.
5. The FLASH data is latched for the CORRECTION LOGIC.
6. The positive edge of the E.O.C. (end of conversion) signal can be used to externally latch the valid data to the outside world. Note, that the data is not valid during the conversion process as indicated by the STATUS signal.

Note, that if the START pulse stays negative for more than two clock pulses a second conversion process will commence. If this happens the STATUS signal will stay high until that conversion is completed. In fact, if the START pulse is kept low...the SP 9548 will be in the continuous mode of operation.



SP 9548 Timing Diagram: Single Conversion Mode

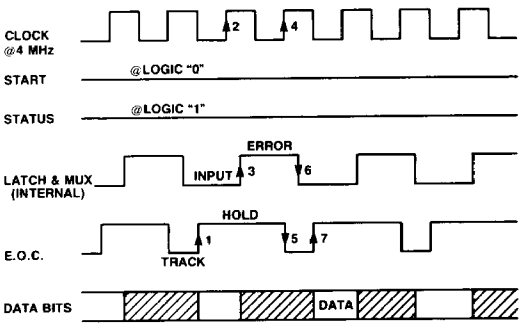
CONTINUOUS CONVERSION MODE

The SP 9548 will be in the continuous conversion mode as long as the START signal is kept low. This mode is used to follow high speed input signals and is capable of up to a 1 MHz (Nyquist Limit) input signal at a 2 MHz sampling rate by simply applying a 4 MHz CLOCK to the SP 9548. Since the STATUS signal will remain high during this mode, the E.O.C. signal should be used to control an input S/H amplifier. Also, by using the E.O.C. signal the maximum conversion rate will not be affected by the addition of the S/H process. Of course, the S/H amplifier should be of the high speed variety such as the HS 9720.

Referring to the timing diagram, the process is as follows:

1. The positive edge of the E.O.C. signal causes the external S/H, HS 9720 or equivalent, to hold the input signal.
2. The rising edge of the next CLOCK cycle causes the FLASH to perform a conversion to determine the MSB's.
3. The FLASH data is latched for the DAC and accordingly the INPUT MUX is switched to the ERROR AMPLIFIER connecting it to the FLASH converter.
4. On the next CLOCK cycle, positive edge, the FLASH converts the error to determine the LSB's.
5. The negative edge of the E.O.C. causes the S/H amplifier to track the input signal in preparation for the next conversion cycle.
6. The FLASH data is latched for the CORRECTION LOGIC.
7. The positive edge of the E.O.C. (end of conversion) signal can be used to externally latch the valid data to the outside world. Note, that the data is not valid during the conversion process as indicated by the STATUS signal.

The process is repeated continuously as shown in the timing diagram. The STATUS signal remains high as long as the START pulse remains low and the SP 9548 is in the continuous conversion mode.

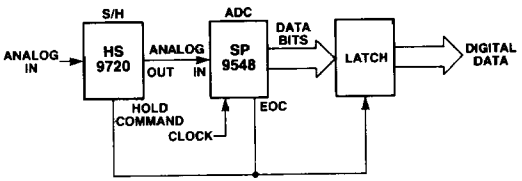


SP 9548 Timing Diagram: Continuous Conversion Mode

TYPICAL APPLICATIONS

The application block diagram illustrates a typical system using the SP 9548 with an external S/H amplifier such as the HS 9720 and an external latch for the data bits. Note that the E.O.C. signal from the SP 9548 can be used for both the hold command and the latch strobe.

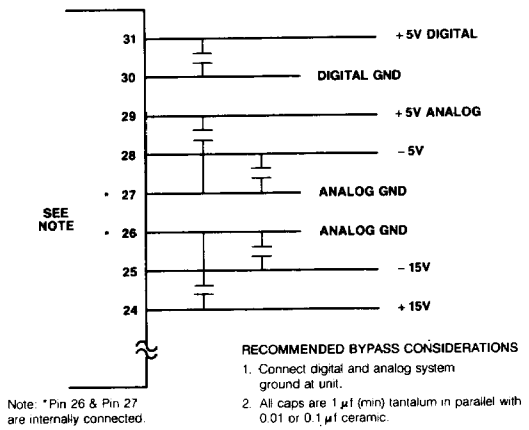
The SP 9548 can be used directly without a S/H amplifier to take a quick snapshot of a slow moving input signal. The maximum input frequency that can be followed without a S/H amplifier is approximately 20 kHz which allows for the conversion of audio band signals.



Typical Application: SP 9548 Continuous Mode With External S/H Amplifier & External Latch

POWER SUPPLY CONNECTIONS

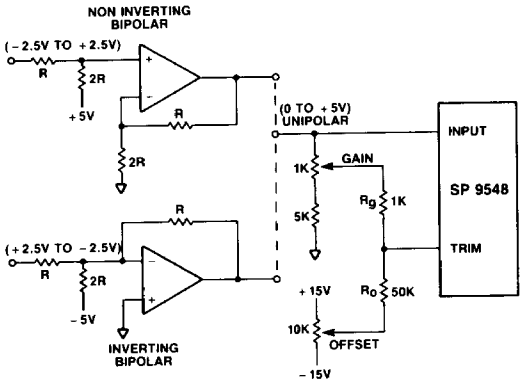
As shown in the Power Supply Connection diagram, 5 pairs of capacitors are recommended for bypassing the power supplies at the SP 9548. Also note that it is recommended to externally connect the analog and digital grounds at the SP 9548. Also, the analog and digital +5V supplies should be separate for optimum performance.



SP 9548 Power Supply Connections

TRIM ADJUSTMENTS

The SP 9548 can be externally trimmed for gain and offset as shown in the block diagram. To change the sensitivity of the gain trim, increase or decrease the value of R_g (1K ohm). To change the sensitivity of the offset trim, increase or decrease the value of R_o (50k ohm). The interaction of the gain and offset trim is minimal; some readjustment may have to be made if one or the other trim is extreme.



To change sensitivity of GAIN Trim increase/decrease R_g
To change sensitivity of OFFSET Trim increase/decrease R_o

SP 9548 Fine Trim Adjustments

BIPOLAR OPERATION

Since the SP 9548 is a unipolar A/D converter, bipolar operation can only be obtained by level shifting the input signal. The FINE TRIM block diagram illustrates this process for either inverting or non-inverting operation using a suitable Operational Amplifier. The value of R should be carefully selected for speed and accuracy. The GAIN and OFFSET adjustments can be used to trim the final input range as previously described.

SUMMARY

The SP 9548 has been designed to simplify high speed conversion and operate at reasonably low power levels. The subranging technique and correction logic have been optimized to provide the accuracy. With this in mind, the SP 9548 is a reasonable solution to most high speed data conversion problems.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	SCREENING
SP 9548C	0 to +70°C	—

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