AT84CS001
10-bit 2.2 Gsps 1:4 DMUX

Datasheet

Features

- **High-speed ADC Family Companion Chip**
- **Selectable 1:2 or 1:4 DMUX Ratio**
- **Power Consumption: 2.7W**
- **LVDS Compatible Differential Data and Clock Inputs (100Ω Terminated)**
- **LVDS Compatible Differential Data and Data Ready Outputs**
- **Staggered or Simultaneous Data Outputs**
  - **11^{th} Bit = Ports A, B, C and D Clock in Staggered Mode**
- **Selectable Active Edge for Input and Output Clocks:**
  - **Only Rising: CLK and DR Mode**
  - **Rising and Falling: CLK/2 and DR/2 Mode**
- **Fine Tuning of Input Clock Path Delay**
  - **Compensation of External Data and Clock Path Misalignment and Skews**
  - **Once Tuned, Setting is Valid over Full Operating Frequency and Over Full Specified Temperature Range**
- **Additional 11^{th} Bit (Example: for Out-of-range Bit)**
- **Built-in Self Test (BIST)**
- **Stand-alone Tunable Delay Cell**
- **Power Supplies: V_{CCD} = 3.3V (Digital), V_{PLUSD} = 2.5V (Outputs)**
- **Power Consumption Reduction Mode: 1.15W**
- **EBGA240 Package**

Screening

- **Temperature Range:**
  - **- 40 °C < T_C; T_J < 110 °C (Industrial Grade)**

Applications

This DMUX enables users to process high-speed output data streams from fast analog-to-digital converters down to standard FPGA processor speed.

Description

The AT84CS001 is a monolithic high-speed demultiplexer, used to lower a 10-bit data stream of up to 2.2 Gsps guaranteed rate by a selectable 4 or 2 ratio (a 1:8 ratio might be achieved by interleaving two DMUXes).

The DMUX is a companion chip designed to fit perfectly with all of e2v's high-speed ADCs and is capable of tracking the ADC's output sampling rate over all operating frequency and temperature ranges.

Thanks to its LVDS buffers, this DMUX can easily be interfaced with standard high-speed FPGAs (100Ω differentially terminated).

The AT84CS001 has the same footprint as e2v's TS81102G0 DMUX, with a very similar pinout. Minimum re-design efforts are required to use this low-power DMUX. An application note "Migration from AT84AS008 to AT84AS008B " reference 5413, is available to assist in migrating from the TS81102G0 to the AT84CS001.

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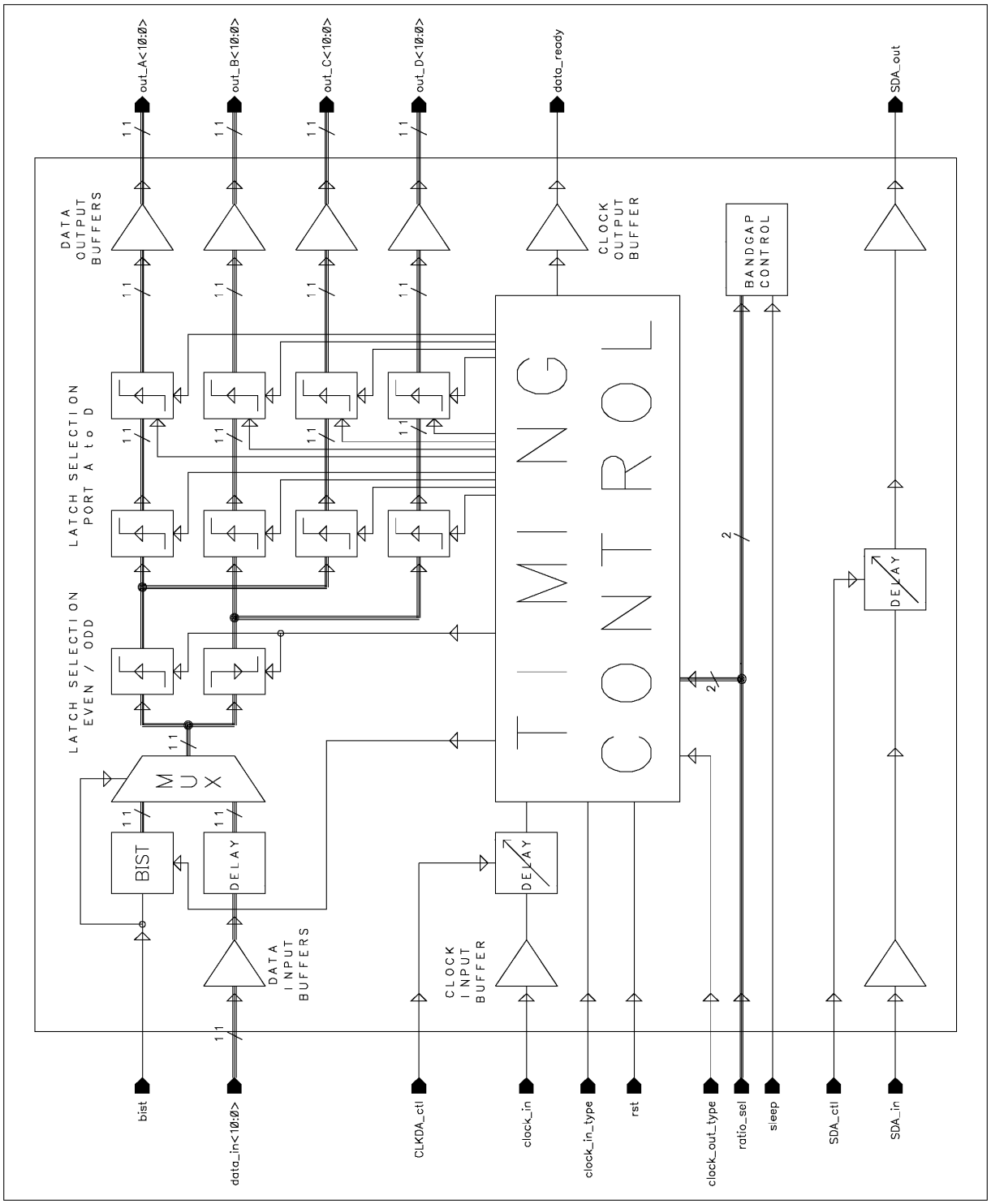
1. Block Diagram

Figure 1-1. Block Diagram



2. Overview

The AT84CS001 is a monolithic high-speed demultiplexer (DMUX) using high-speed e2v technology.

It enables the user to lower a 10-bit stream of 2.2 Gsps maximum by a factor of two or four. One can obtain a 1:8 ratio by using two interleaved AT84CS001 devices. The maximum input data rate is 2.2 Gsps in 1:4 ratio and 1.8 Gsps in 1:2 ratio.

The AT84CS001 DMUX is capable of processing an 11-bit data flow. The additional 11^{th} bit (IOR, IORN) might be connected for example to the out-of-range bit of a 10-bit ADC.

The input and output clocks as well as the input and output data are LVDS compatible. Digital inputs are 100Ω differentially terminated on chip. Digital output buffers shall be terminated by a 100Ω differential ASIC load.

The improved architecture of the DMUX facilitates interfacing with high-speed ADCs operating at up to 2.2 Gsps. A tunable delay cell is integrated in serial with the clock input: it can be used to tune the delay between the data and clock paths namely for high speed rates and in the case of misalignment or skews between the external clock path and the data path. The delay is controlled by means of the CLKDACTRL analog control input. The tunable delay ranges from - 250 ps to 250 ps for CLKDACTRL varying from $V_{CCD}/2$ to $(2 \times V_{CCD})/3$.

Two modes can be selected for the clock input (CLK and CLK/2) and the clock output (DR and DR/2):

- CLK and DR mode: Only the rising edges of the input (CLK,CLKN) and output (DR, DRN) clocks are active. The input (or output) clock rate remains the same as the input or output data rate.
- CLK/2 and DR/2 mode: Both the rising and falling edges of the input (CLK,CLKN) and output (DR, DRN) clocks are active. The input (or output) clock rate is half the input or output data rate.

The data outputs can be received at the DMUX output in two different modes:

- Staggered: even and odd bits are output with half a data period delay
- Simultaneous: even and odd bits are output at the same time

The AT84CS001 DMUX is started by the ASYNCRST control input that acts as a master asynchronous reset for the device. Once reset, there is no loss of synchronization over an indefinite time period, therefore no additional incoming synchronous reset signal is required.

The power consumption of the AT84CS001 is 2.7W and can be reduced by approximately 60% of its nominal value by means of the SLEEP control input.

A standalone delay cell is provided. It features a typical 550 ps tuning range (± 275 ps around the center value of DACTRL analog control input).

A Built-in Self Test (BIST) is implemented for rapid debugging of the DMUX.

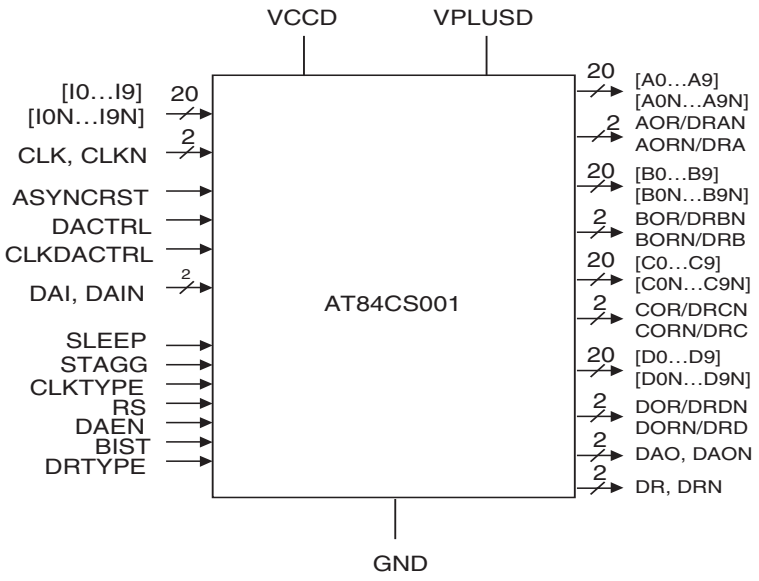
The AT84CS001 DMUX is a companion chip designed to fit perfectly with all of e2v's high-speed ADCs.

3. Description of Main Functions

Table 3-1. Description of Main Functions

Name	Function	Name	Function
V_{CCD}	Digital 3.3V power supply	D0, D0N...D9, D9N	Output data port D
V_{PLUSD}	Output 2.5V power supply		
GND	Ground	DOR/DRDN, DORN/DRD	Additional output bit port D or port D output clock in staggered mode
CLK, CLKN	Input clock signals	DAO, DAON	Output signals for stand-alone delay cell
I0, I0N…I9, I9N	Input data	DAI, DAIN	Input signals for stand-alone delay cell
		DACTRL	Control signal for standalone delay cell
IOR, IORN	Additional input bit	CLKDACTRL	Control signal for clock delay cell
DR/DRN	Output clock signals	DAEN	Enable signal for standalone delay cell
A0, A0N…A9, A9N	Output data port A	ASYNCRST	Asynchronous reset signal
		SLEEP	Sleep mode selection signal
AOR/DRAN, AORN/DRA	Additional output bit port A or port A output clock in staggered mode	RS	DMUX ratio selection signal
B0, B0N…B9, B9N	Output data port B	CLKTYPE	Input clock type selection signal
		DRTYPE	Output clock type selection signal
BOR/DRBN, BORN/DRB	Additional output bit port B or port B output clock in staggered mode	STAGG	Staggered mode selection for data outputs
C0, C0N…C9, C9N	Output data port C	BIST	Built-in Self Test enable
COR/DRCN, CORN/DRC	Additional output bit port C or port C output clock in staggered mode		

Figure 3-1. Device Pinout



3.1 Control Signal Settings

The ASYNCRST, SLEEP, DAEN, STAGG, BIST, RS, CLKTYPE and DRTYPE control signals use the same static input buffer.

ASYNCRST is activated on logic HIGH (tied/switched to V_{CCD} = 3.3V, or 10 kΩ to ground, or left floating), and deactivated on logic LOW (grounded).

SLEEP, DAEN, STAGG, BIST are activated on logic LOW (10Ω grounded), and deactivated on logic HIGH (10 kΩ to ground, or tied to V_{CCD} = 3.3V, or left floating).

Figure 3-2. Control Signal Settings

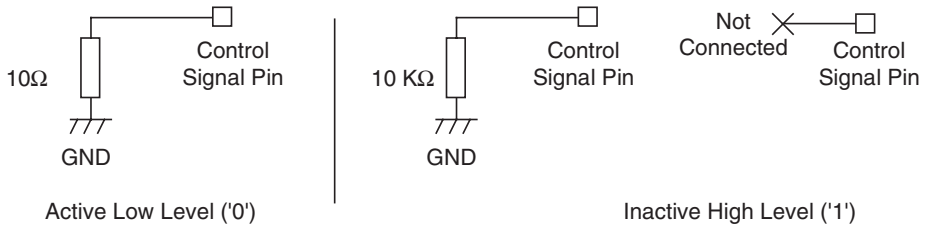


Table 3-2. Summary of DMUX Mode Settings

Function	Logic Level	Electrical Level	Description
BIST	0	10Ω to ground	BIST
	1	10 kΩ to ground	Normal conversion
		N/C	
SLEEP	0	10Ω to ground	Power reduction mode (the outputs are fixed at an arbitrary LVDS level)
	1	10 kΩ to ground	Normal conversion
		N/C	
STAGG	0	10Ω to ground	Staggered mode
	1	10 kΩ to ground	Simultaneous mode
		N/C	
DAEN	0	10Ω to ground	Standalone delay adjust activated
	1	10 kΩ to ground	Standalone delay adjust disabled
		N/C	
RS	0	10Ω to ground	1:2 ratio
	1	10 kΩ to ground	1:4 ratio
		N/C	
CLKTYPE	0	10Ω to ground	CLK mode
	1	10 kΩ to ground	CLK/2 mode
		N/C	
DRTYPE	0	10Ω to ground	DR/2 mode
	1	10 kΩ to ground	DR mode
		N/C	

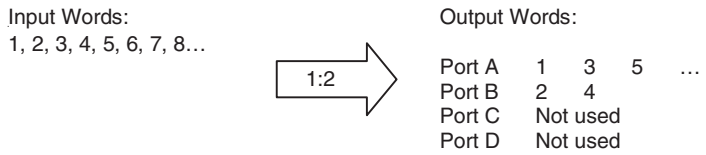
3.2 Programmable DMUX Ratio

The demultiplexer ratio is programmable through the RS ratio selection signal:

Table 3-3. DMUX Ratio Selection Settings

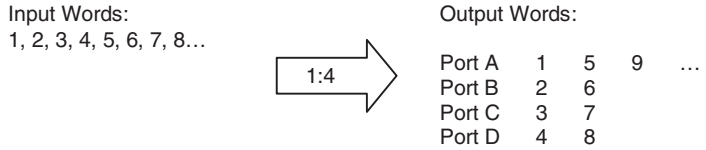
RS	DMUX Ratio
0	1:2
1	1:4

Figure 3-3. DMUX in 1:2 Ratio



Note: Ports C & D data have undetermined level. They can be left unconnected.

Figure 3-4. DMUX in 1:4 Ratio



3.3 Additional Bit (IOR,IORN)

When a signal is applied on IOR and IORN, the *additional bit* is activated. It can be used to process the out-of-range bit from the ADC, in which case the DMUX features an 11-bit input/output data stream.

IOR, IORN is demultiplexed by the selected DMUX ratio:

- In 1:4 ratio, AOR/DRAN, AORN/DRA, BOR/DRBN, BORN/DRB, COR/DRCN, CORN/DRC and DOR/DRDN, DORN/DRD output this signal at a quarter of its initial speed.
- In 1:2 ratio, AOR/DRAN, AORN/DRA and BOR/DRBN, BORN/DRB output this signal at half its initial speed.

Note: In staggered output mode:
(AORN/DRA, AOR/DRAN), (BORN/DRB, BOR/DRBN), (CORN/DRC, COR/DRCN) and (DORN/DRD, DOR/DRDN) are used as the Data Ready signal (output clock) for each port. In this mode the additional bit is disabled.

3.4 Clock Type Selection CLKTYPE and DRTYPE

Two modes for the input and output clock type can be selected by way of the CLKTYPE and DRTYPE single-ended digital inputs.

For correct logic 1 or 0 settings, please refer to “Control Signal Settings” on page 5.

- When CLKTYPE is at logic *0* and DRTYPE is at logic *1*, the DMUX is set to CLK and DR modes for both the input and output clocks – only the rising edges of the input and output clocks are active and the input and output clock rates are the same as the input and output data rate.
- When CLKTYPE is at logic *1* and DRTYPE is at logic *0*, the CLK/2 and DR/2 modes are activated for both the input and output clocks, both the rising and falling edges of the input and output clocks are active and the input and output clock rates are half the input and output data rate.

When CLKTYPE is left floating, the default (recommended) mode is selected (CLK/2).

Notes: 1. CLK or CLK/2 and DR or DR/2 modes can be indifferently combined together (example: CLK/2 for the input and DR for the output).
2. The preferred (and recommended) mode is CLK/2 together with DR/2.

Figure 3-5. CLK and DR Mode (CLKTYPE = 0, DRTYPE = 1)

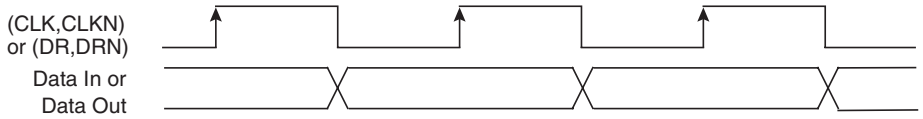
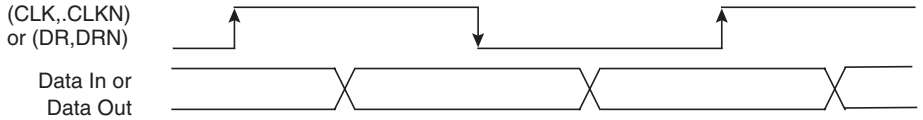


Figure 3-6. CLK/2 and DR/2 Mode (CLKTYPE = 1, DRTYPE = 0)



Note: In Figure 3-5 and Figure 3-6 above, the CLK and DR signals are not on the same time scale. In 1:4 DMUX ratio, the DR and data-out frequencies are equal to one quarter of the CLK and data-in frequencies.

Table 3-4. Logical Settings of the DMUX Input Clock Type Selection

CLKTYPE	DMUX Input Clock Type
0	CLK
1	CLK/2

Table 3-5. Logical Settings of the DMUX Output Clock Type Selection

DRTYPE	DMUX Output Clock Type
1	DR
0	DR/2

3.5 Output Mode (STAGG)

Two output modes are provided:

- Staggered: the data packets are output one after the other
- Simultaneous: all the data packets are output at the same time

In staggered mode, the output clock for each port is provided by the DRA, DRAN, DRB, DRBN, DRC, DRCN and DRD, DRDN signals, which correspond to AORN, AOR, BRON, BOR, CORN, COR, DORN and DOR respectively.

The Simultaneous mode is the default mode (STAGG left floating or at logic *1*). The Staggered mode is activated through the STAGG input (active low level).

Figure 3-7. Simultaneous Mode in 1:4 Ratio (STAGG = 1)

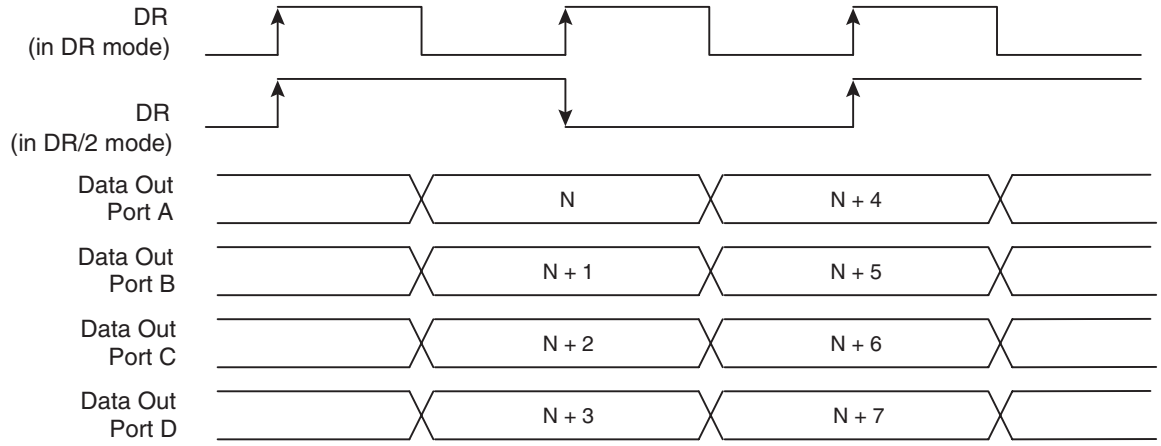


Figure 3-8. Staggered Mode in 1:2 Ratio (STAGG = 0)

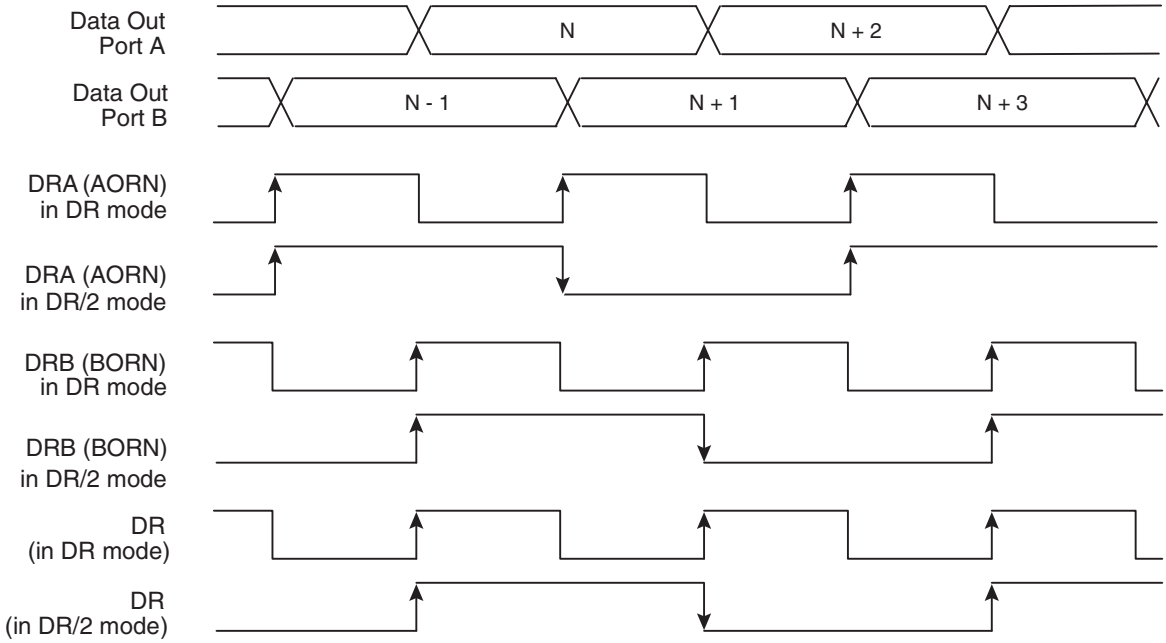
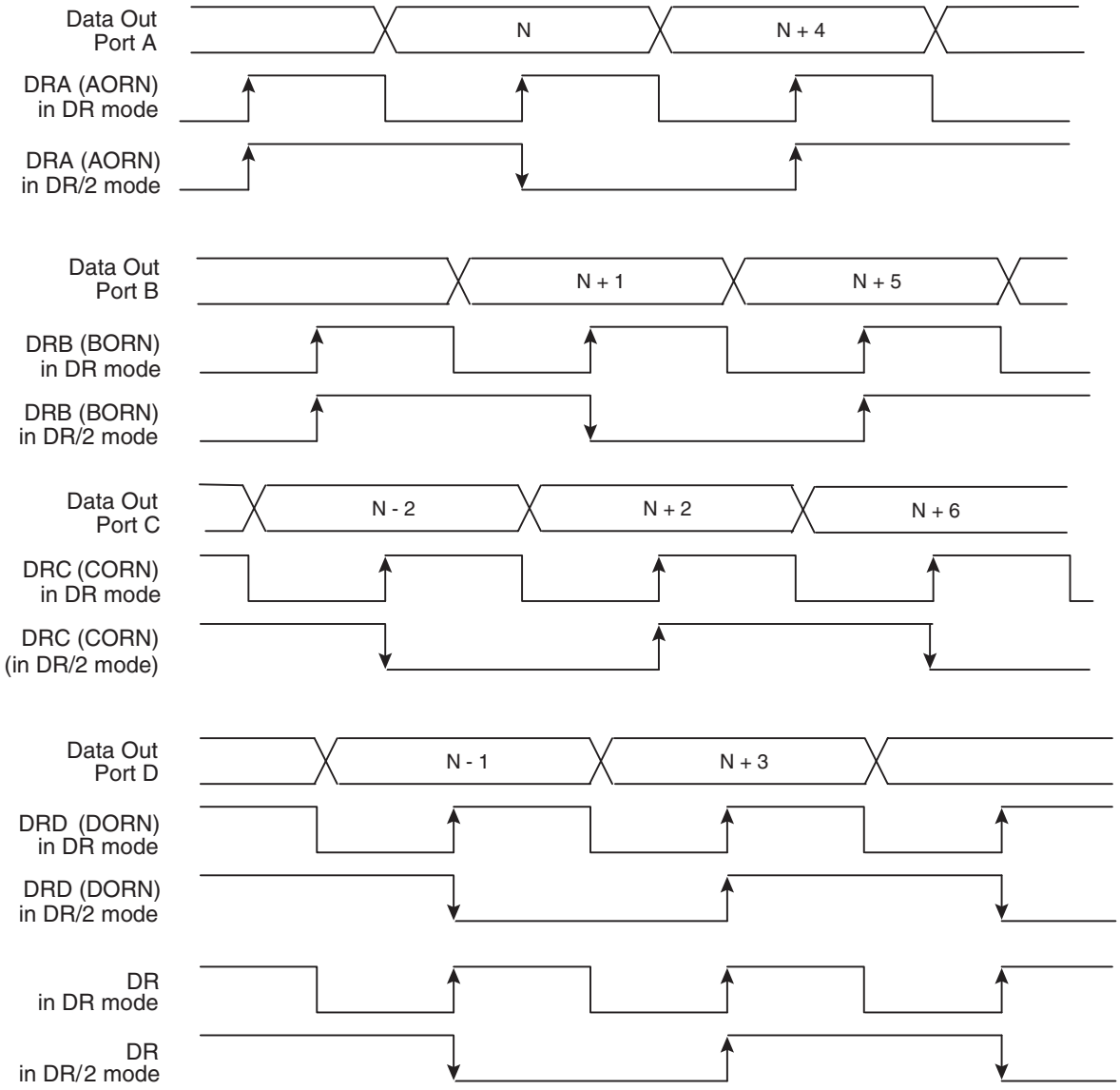


Figure 3-9. Staggered Mode in 1:4 Ratio (STAGG = 0)



3.6 Asynchronous Reset (ASYNCRST)

The ASYNCRST asynchronous reset input is required to start/initialize the device, and acts as master reset of the DMUX.

ASYNCRST is activated on logic HIGH (tied/switched to V_{CCD} = 3.3V, or 10 KΩ to ground, or left floating), and deactivated on logic LOW (grounded).

During the asynchronous reset, the DMUX' differential clock input (CLK, CLKN) should be stopped at low level (state in which e2v's single ADC Data Ready signals are when the ADC is in reset mode).

The ASYNCRST maximum signal frequency should not exceed 200 MHz. The ASYNCRST pulse should last at least 1 ns. For ASYNCRST to CLK timing see Figure 4-1 on page 20.

3.7 Power Reduction Mode (SLEEP)

The power reduction mode saves up to 60% of power consumption. In this mode, the DMUX delivers an arbitrary digital output pattern with LVDS logic states (no toggling).

The power reduction mode is enabled by the SLEEP input. SLEEP is activated on logic LOW (grounded), and deactivated on logic HIGH (10 KΩ to Ground, or tied to V_{CCD} = 3.3V, or left floating).

3.8 Standalone Delay Cell (DAI, DAIN) (DAO, DAON)

A standalone tunable delay cell is provided. The delay line is controlled via the DACTRL analog control input. The tuning range is about 550 ps for DACTRL varying from V_{CCD} / 3 to $(2 \times V_{CCD})/ 3$.

The (DAI, DAIN) and (DAO, DAON) are LVDS compatible input and output respectively. The Standalone Delay Cell is enabled by the DAEN input.

DAEN is activated on Logic Low (Grounded), and deactivated on Logic High (10 KΩ to ground, or tied to V_{CCD} = 3.3V, or left floating).

Figure 3-10. Block Diagram of the Standalone Delay Cell

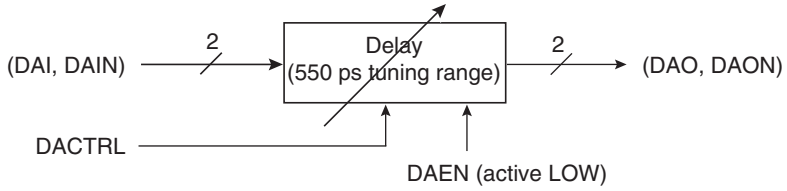
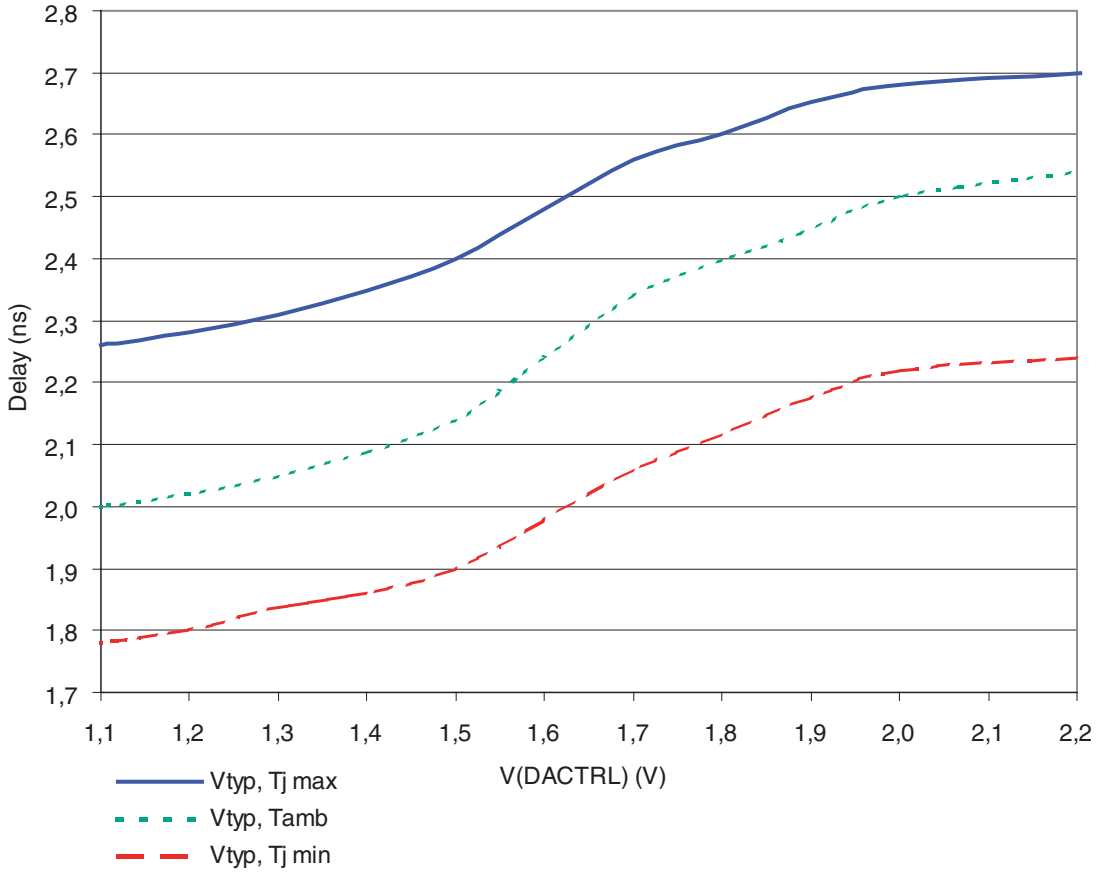
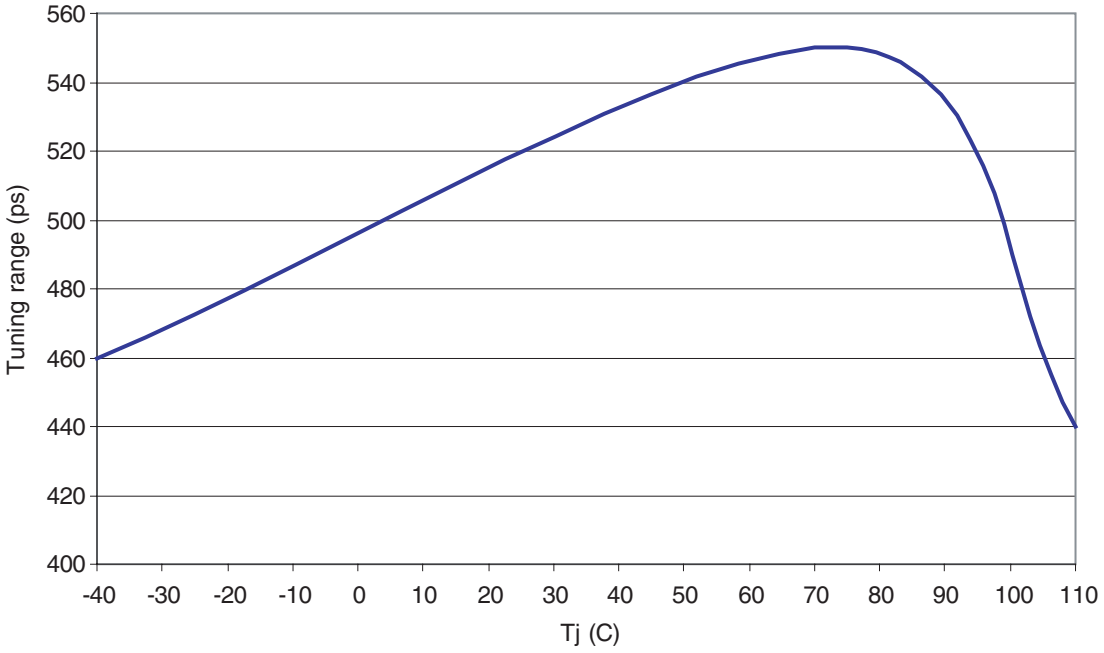


Figure 3-11. Transfer Characteristics of the Standalone Delay Cell



The tuning range is not constant over the specified temperature range. The longest tuning range is obtained in typical conditions (typical power supplies and ambient temperature) and it slightly decreases when temperature is rising or decreasing.

Figure 3-12. Standalone Delay Cell Tuning Range Versus Tj



3.9 Clock Input Delay Cell (CLKDACTRL)

A fine tune delay cell is provided to fine-tune the delay between the clock path and the data path the DMUX input. This adjustment may be necessary depending on the sampling rate and/or if there are misalignments or skews on the different input data. However, data path skews should be maintained below 50 ps.

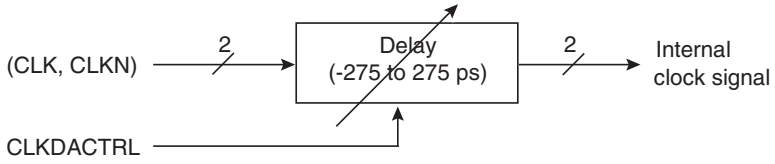
For more information on CLKDACTRL values to be applied, depending on the sampling rate, please refer to the application note reference 5444.

The delay is controlled by the CLKDACTRL analog control input. It ranges from -275 to 275 ps for CLKDACTRL varying from $V_{CCD}/3$ to $(2 \times V_{CCD})/3$. The transfer characteristics of the delay cell is identical to the one used in standalone delay cell.

This embedded delay line has characteristics similar to those of the standalone delay cell described in “Standalone Delay Cell (DAI, DAIN) (DAO, DAON)” above.

This delay depends on the center position of the (CLK, CLKN) clock path in relation to the digital input data in the DMUX input data paths (I0, I0N) …(I9, I9N) and (IOR, IORN).

Figure 3-13. Block Diagram of the Clock Input Delay Cell



3.10 Built-in Self Test (BIST)

A pattern generator might be activated by means of the BIST input. The BIST is activated on logic LOW (grounded), and deactivated on logic HIGH (10 KΩ to ground, or tied to V_{CCD} = 3.3V, or left floating).

When activated, the digital outputs correspond to a sequence of *0* and *1*. Each bit is toggled at the clock rate.

For proper operation of pattern Built-In Test, the minimum V_{CCD} voltage should be 3.3V.

3.11 Data Rate Versus Modes

The following table describes the frequency of the Data Ready output signal according to the 8 modes, assuming a 500 MHz DEMUX input clock.

Table 3-6. Data Ready Output Frequency (MHz)

	Data Ready Output Frequency (MHz)			
	1:2		1:4	
DEMUX Ratio	**DR**	**DR/2**	**DR**	**DR/2**
CLK TYPE				
CLK	250	125	125	62,5
CLK/2	500	250	250	125

The following table describes the maximum input data rate guaranteed depending on CLK TYPE, DR TYPE and RatioSel settings.

Table 3-7. Maximum Input Data Rate

CLK TYPE	DR TYPE	RatioSel	Maximum Input Data Rate Guaranteed (Gsps)
CLK/2	DR/2	1:2	1.8
		1:4	2.2
	DR	1:2	1.0
		1:4	2.0
CLK	DR/2	1:2	1.2
		1:4	1.2
	DR	1:2	1.0
		1:4	1.2

4. Electrical Specifications

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Digital power supply	V_{CCD}	3.6	V
Output power supply	V_{PLUSD}	3.6	V
Data input	I0, I0N…I9, I9N, IOR, IORN, DAI, DAIN	- 0.3 to V_{CCD} + 0.3	V
Clock input	VCLK, VCLKN	- 0.3 to V_{CCD} + 0.3	V
Control inputs	SLEEP, STAGG, ASYNCRST, BIST, RS, DAEN, CLKTYPE, DRTYPE	- 0.3 to V_{CCD} + 0.3	V
Control inputs	CLKDACTRL, DACTRL	- 0.3 to V_{CCD} + 0.3	V
Maximum junction temperature	T_J	125	°C
Storage temperature	T_{stg}	- 65 to 150	°C

Notes: 1. Absolute maximum ratings are limiting values (referenced to GND = 0V) and are to be applied individually, while other parameters are within the specified operating conditions. Long exposure to maximum ratings might affect device reliability.

2. All integrated circuits must be handled with appropriate care to avoid damage caused by ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure of the device.

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Table 4-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Digital power supply	V_{CCD}		3.15	3.3	3.45	V
Output power supply	V_{PLUSD}		2.375	2.5	2.625	V
Operating temperature range	T_C, T_J	Industrial grade	- 40 ° < T_C, T_J < 110°			°C

Table 4-3. Electrical Characteristics

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Resolution		4	10 bit with additional 11th bit			Bit
ESD protection		4	1000			V
Power Requirements						
Digital power supply voltage[1]	V_{CCD}	1	3.15	3.3	3.45	V
Output power supply voltage	V_{PLUSD}	1	2.375	2.5	2.625	V
Digital power supply current 1:2 mode 1:4 mode SLEEP mode Additional current with SDA enabled Additional current with BIST enabled	I_{VCCD}	1		 540 600 170 22 27	 610[5] 680[5] 200[5] 30 35	mA
Output power supply current 1:2 mode 1:4 mode SLEEP mode	I_{VPLUSD}	1		 260 280 230	 340[5] 360[5] 290[5]	mA
Power dissipation 1:2 mode 1:4 mode SLEEP mode (1:4) All active (1:4, BIST & SDA enabled)	P_D	1		 2.45 2.7 1.15 2.85	 3.0[5] 3.3[5] 1.4[5] 3.4[5]	W
LVDS Data/Clock inputs and Outputs (including DAI, DAIN and DAO, DAON)						
Logic compatibility			LVDS			
Input common mode[2]	V_{ICM}	1	1	1.25	1.6	V
Output common mode[3]	V_{OCM}	1	1.125	1.25	1.375	V
Differential input[2]	V_{IDIFF}	1	100	350	–	mV
Differential output	V_{ODIFF}	1	250	350	500	mV
Output level *High*[4]	V_{OH}	1	1.25	1.425	–	V
Output level *Low*[4]	V_{OL}	1	–	1.075	1.25	V
Static Inputs (SLEEP, STAGG, BIST, RS, DAEN, CLKTYPE, DRTYPE)						
Control input voltages: - Logic low Resistor to ground Voltage level - Logic high Resistor to ground Voltage level	 R_{IL} V_{IL} R_{IH} V_{IH}	 1	 0 10k 2.0		 10 0.5 Infinite	 Ω V Ω V
Static Inputs (CLKDACTRL, DACTRL)						
Control input voltages		4	$V_{CCD}/3$		$2 \times V_{CCD}/3$	V

Table 4-3. Electrical Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Reset Input (ASYNCRST)						
Logic compatibility			LVCMOS/CMOS			
Control input voltages: resistor to Ground - Logic low - Logic high	 V_{IL} V_{IH}	 1	 0 1.6		 1.0 3.3	 V

Notes:
1. For proper operation of BIST mode, V_{CCD} min = 3.3V.
2. Given for a differential input.
3. Assuming 100Ω termination ASIC load
4. V_{OH} min and V_{OL} max can never be at 1.25V at the same time when V_{ODIFF} min = 250 mV.
5. Worst case value obtained with maximum supply voltages over full temperature range.

Table 4-4. Switching Performances and Characteristics

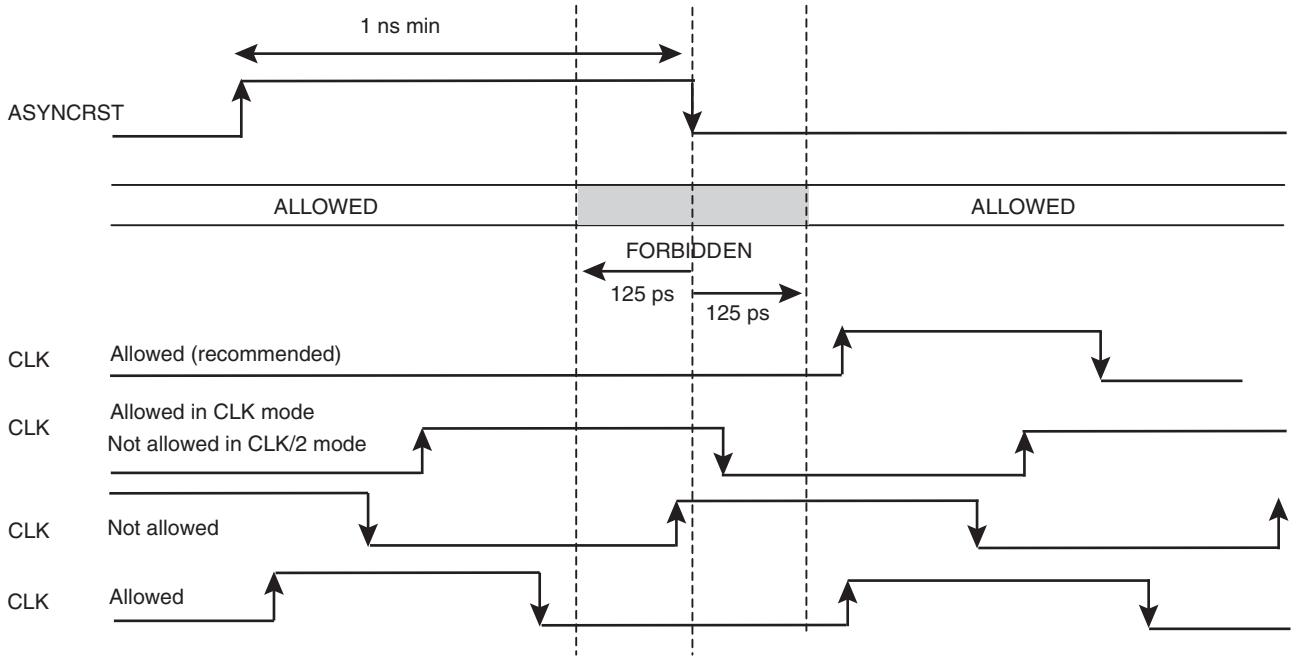
Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Input Clock						
Input Clock duty cycle	**DCYC**	**4**	40	50	60	%
Maximum Input Data Rate						
CLK TYPE = CLK/2, DR TYPE = DR/2, RS = 1:2			0.9			
CLK TYPE = CLK/2, DR TYPE = DR/2, RS = 1:4			1.1			
CLK TYPE = CLK/2, DR TYPE = DR, RS = 1:2			0.5			
CLK TYPE = CLK/2, DR TYPE = DR, RS = 1:4	Fclk	4	1.0			GHz
CLK TYPE = CLK, DR TYPE = DR/2, RS = 1:2			1.2			
CLK TYPE = CLK, DR TYPE = DR/2, RS = 1:4			1.2			
CLK TYPE = CLK, DR TYPE = DR, RS = 1:2			1.0			
CLK TYPE = CLK, DR TYPE = DR, RS = 1:4			1.2			
Input Data						
Data to Input Clock setup & hold time[1]	TSetup/ THold	4				ps
Maximum Input Data Rate						
CLK TYPE = CLK/2, DR TYPE = DR/2, RS = 1:2			1.8			
CLK TYPE = CLK/2, DR TYPE = DR/2, RS = 1:4			2.2			
CLK TYPE = CLK/2, DR TYPE = DR, RS = 1:2			1.0			
CLK TYPE = CLK/2, DR TYPE = DR, RS = 1:4	Fs	4	2.0			Gsps
CLK TYPE = CLK, DR TYPE = DR/2, RS = 1:2			1.2			
CLK TYPE = CLK, DR TYPE = DR/2, RS = 1:4			1.2			
CLK TYPE = CLK, DR TYPE = DR, RS = 1:2			1.0			
CLK TYPE = CLK, DR TYPE = DR, RS = 1:4			1.2			
Output Data						
Maximum Output Data Rate						
CLK TYPE = CLK/2, DR TYPE = DR/2, RS = 1:2			900			
CLK TYPE = CLK/2, DR TYPE = DR/2, RS = 1:4			550			
CLK TYPE = CLK/2, DR TYPE = DR, RS = 1:2			500			
CLK TYPE = CLK/2, DR TYPE = DR, RS = 1:4		4	500			Msps
CLK TYPE = CLK, DR TYPE = DR/2, RS = 1:2			600			
CLK TYPE = CLK, DR TYPE = DR/2, RS = 1:4			300			
CLK TYPE = CLK, DR TYPE = DR, RS = 1:2			500			
CLK TYPE = CLK, DR TYPE = DR, RS = 1:4			300			
Output Rise/Fall time for Data (20% – 80%)	TR/TF	4		460/630	550/750	ps
Output Rise/Fall time for Data Ready (20% – 80%)	TR/TF	4		460/630	550/750	ps
CLK to Data Output delay	TOD	4	5.0	5.9	7.1	ns
CLK to Data Ready Output delay	TDR	4	4.5	5.5	6.7	ns
Data Ready to Data delay	|TOD–TDR|	4	200	500	600	ps

Table 4-4. Switching Performances and Characteristics (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Output Data Pipeline delay Synchronized 1:2 mode Synchronized 1:4 mode Staggered 1:2 mode Staggered 1:4 mode	TPD	4		 0.5 1.5 0/0.5 0/0.5 /1/1.5		Clock Cycles
Asynchronous Reset						
ASYNCRST maximum input frequency	FRST	5		200		MHz
ASYNCRST minimum pulse width	RSTPW	5		1		ns
CLK to ASYNCRST timing[2] Forbidden area width Minimum delay between falling edge of ASYNCRST and rising edge of CLK		 4 4			 250 ± 125	 ps ps
Standalone Delay Cell[3]						
Maximum Input Frequency	FMSDA	4	600			MHz
Input duty cycle	DCYCSDA	4	40	50	60	%
(DAI, DAIN) to (DAO, DAON) propagation delay[3] with DACTRL = $V_{CCD}/3$	TSDAMIN	4	1.70	2.00	2.30	ns
(DAI, DAIN) to (DAO, DAON) propagation delay[3] with DACTRL = $2*V_{CCD}/3$	TSDAMAX	4	2.20	2.50	2.80	ns
SDA tuning range[4]	SDARANGE	4	400	550	600	ps

Notes:
1. Input data to input clock setup and hold time are not defined, because they are dependent of CLKDACTRL adjustment. It is recommended to center the clock edge in the middle of the data (with ± 100 ps) and to adjust CLKDACTRL depending on clock sampling rate.
2. See Figure 4-1 on page 20, CLK to ASYNCRST timing is given assuming V (CLKDACLTRL) = $V_{CC}/2$
3. See Transfer characteristic on Figure 3-11 on page 12.
4. The delay cell used in both standalone delay cell and Input clock path, has a characteristics that is not linear with Junction temperature. The largest tuning range is obtained near ambient temperature. See Figure 3-12 on page 13.

Figure 4-1. CLK to ASYNCRST timing with V(CLKDACTRL) = V_{CC}/2g



It is highly recommended to stop the clock at the Low level when ASYNCRST is active (high level). Note that when Amel's ADCs are in reset, the ADC Data Ready output (input clock of the DMUX) is stopped at the low level. In the case where the clock can not be stopped during the reset (not recommended), it is not allowed to have an active edge (rising edge in CLK mode but both rising and falling edge in CLK/2 mode) of the CLK clock within a ±125 ps area around the falling edge of ASYNCRST.

The end of the reset occurs at the falling edge of ASYNCRST, and the active edge of the Clock has to occur at the minimum 125 ps after the falling edge of ASYNCRST to ensure a proper timing.

The figure represented above is given for V(CLKDACTRL) = V_{CC}/2 = 1.65V. If V(CLKDACTRL) has a different value, the forbidden area has to be shifted accordingly to V(CLKDACTRL) value. Please refer to Figure 3-11 on page 12 for delay calculation.

For example, assuming ambient temperature and typical supplies, if V(CLKDACTRL) is set to 2.2V, the additional delay compared to 1.65V is 2.55 ns - 2.25 ns = 300 ps. This means that it is forbidden to have an active edge of the clock within - 425 ps/- 175 ps (the forbidden area is shifted on the left on the above figure).

4.1 Timing Diagrams

Figure 4-2. Simultaneous 1:2 Mode – CLKTYPE = DR/2 – DRTYPE = DR

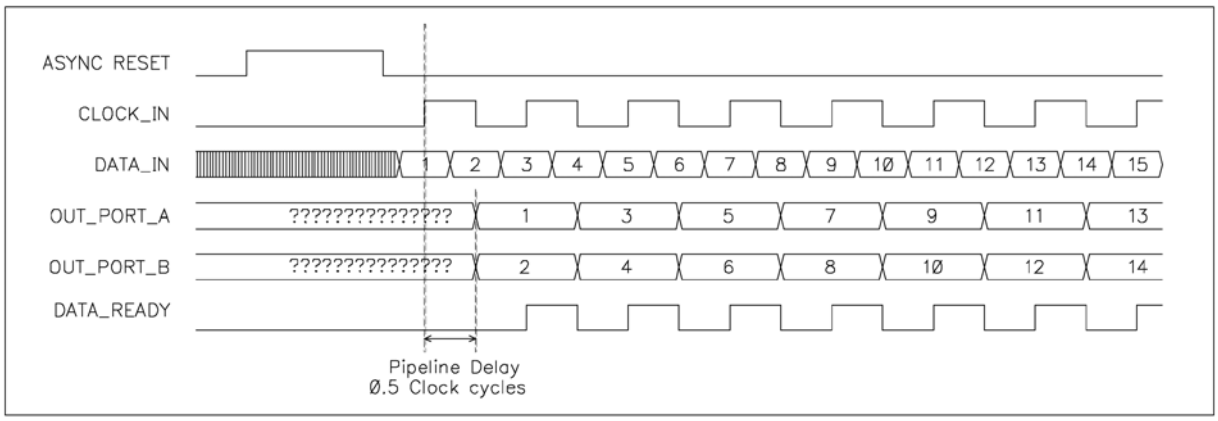


Figure 4-3. Simultaneous 1:4 Mode – CLKTYPE = DR/2 – DRTYPE = DR

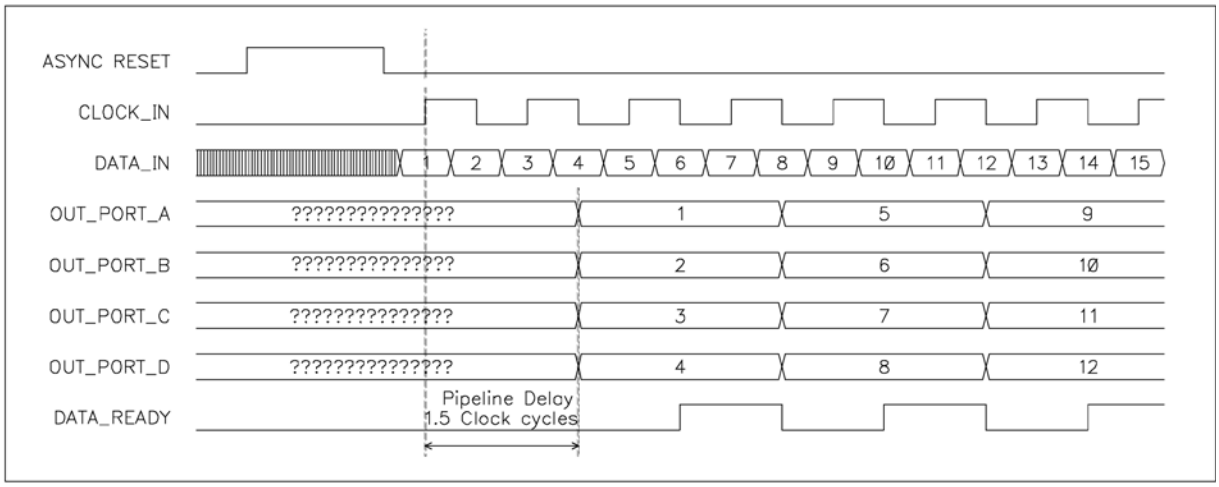
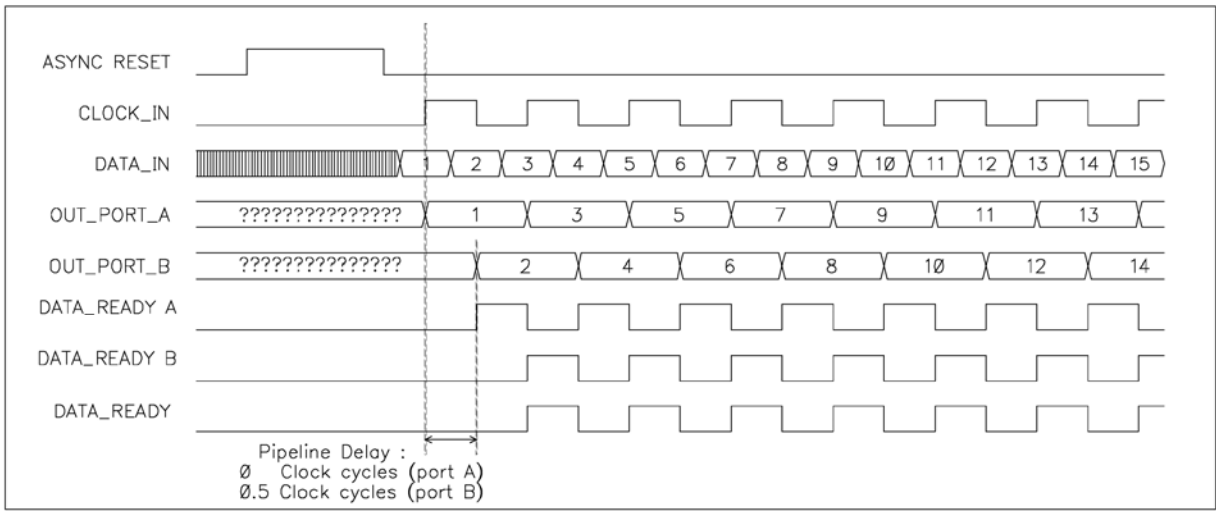
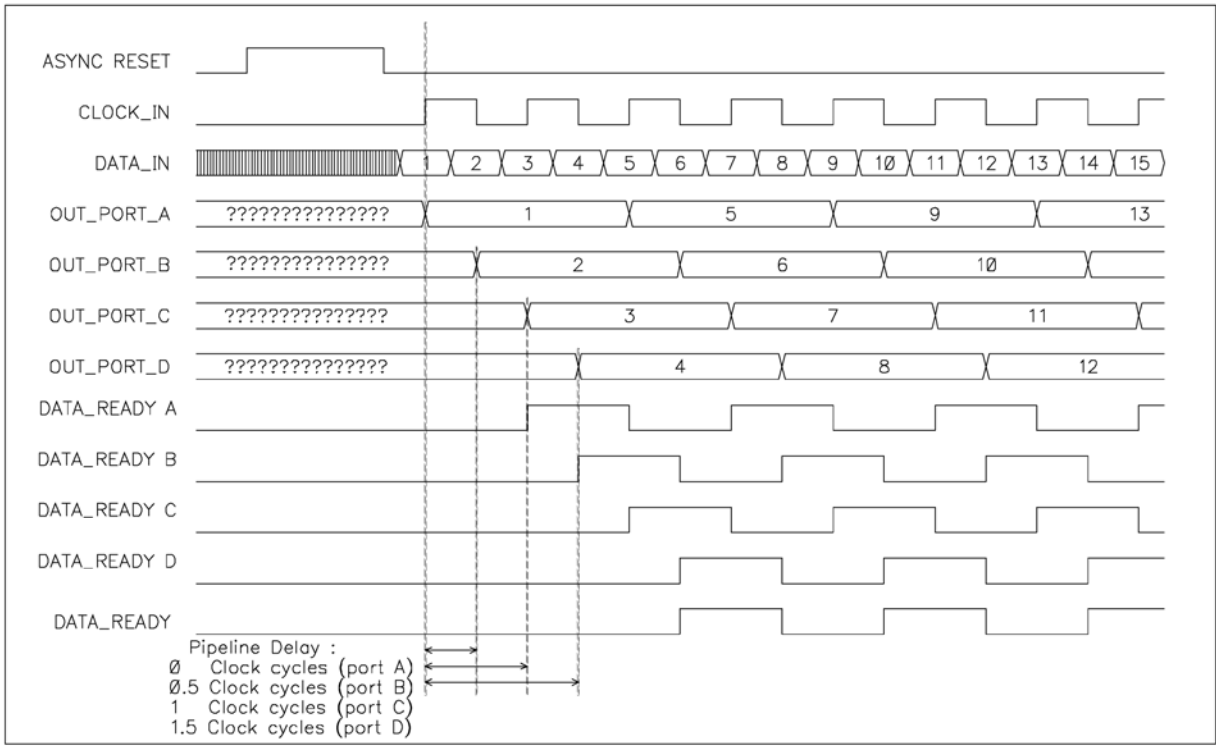


Figure 4-4. Staggered 1:2 Mode – CLKTYPE = DR/2 – DRTYPE = DR



Note: DATA_READY A = DRA (pin A6)
DATA_READY B = DRB (pin H1)

Figure 4-5. Staggered 1:4 Mode – CLKTYPE = DR/2 – DRTYPE = DR



Note: DATA_READY A = DRA (pin A6)
DATA_READY B = DRB (pin H1)
DATA_READY C = DRC (pin W5)
DATA_READY D = DRD (pin W16)

4.2 Explanation of Test Levels

Table 4-5.

1	100% production tested at + 25 °C
2	100% production tested at + 25 °C , and sample tested at specified temperature.
3	Sample tested only at specified temperature.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only.

Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

The level 1 and 2 tests are performed at 10 MHz.

5. Pin Description

Table 5-1. Pin Description

Symbol	Pin Number	Function
Power Supplies		
V_{CCD}	C12, C10, C8, C3, D12, D10, D8, D5, D4, D3, E4, E17, E16, G17, G16, G4, G3, J17, J16, K16, K4, K3, L17, L16, N17, N16, R16, T17, T16, T12, T10, T8, T5, T4, T3, U12, U10, U8, U3	Digital 3.3V supply
V_{PLUSD}	C15, C14, C13, C11, C9, C7, C6, C5, C4, D13, D11, D9, D7, D6, E3, J4, J3, L4, L3, N4, N3, R4, R3, T14, T13, T11, T9, T7, T6, U15, U14, U13, U11, U9, U7, U6, U5, U4	Output 2.5V supply
DGND	C18, C17, C16, D17, D14, F17, F16, F4, F3, H17, H16, H4, H3, K17, M17, M16, M4, M3, P17, P16, P4, P3, R17, T15, U19, U18, U17, U16	Ground
Digital Inputs		
I0, I1, I2, I3, I4, I5, I6, I7, I8, I9	D19, E19, F19, G19, J19, K19, L19, M19, N19, P19	In-phase (+) digital input signal
I0N, I1N, I2N, I3N, I4N, I5N, I6N, I7N, I8N, I9N	D18, E18, F18, G18, J18, K18, L18, M18, N18, P18	Inverted phase (-) digital input signal
IORN	B18	In-phase (+) digital input signal additional bit
IOR	B19	Inverted phase (-) digital input signal for additional bit
DAI	T18	In-phase (+) input signal for standalone delay cell
DAIN	T19	Inverted phase (-) input signal for standalone delay cell
Clock Inputs		
CLK	H19	In-phase (+) clock input
CLKN	H18	Inverted phase (-) clock input
Digital Outputs		
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9	B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	In-phase (+) digital outputs for port A A0 is the LSB, A9 is the MSB
A0N, A1N, A2N, A3N, A4N, A5N, A6N, A7N, A8N, A9N	A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	Inverted phase (-) digital outputs for port A
AOR/DRAN	B6	In-phase (+) additional bit output for port A or inverted phase (-) output clock in staggered mode for port A
AORN/DRA	A6	Inverted phase (-) additional bit output for port A or in-phase (+) output clock in staggered mode for port A

Table 5-1. Pin Description (Continued)

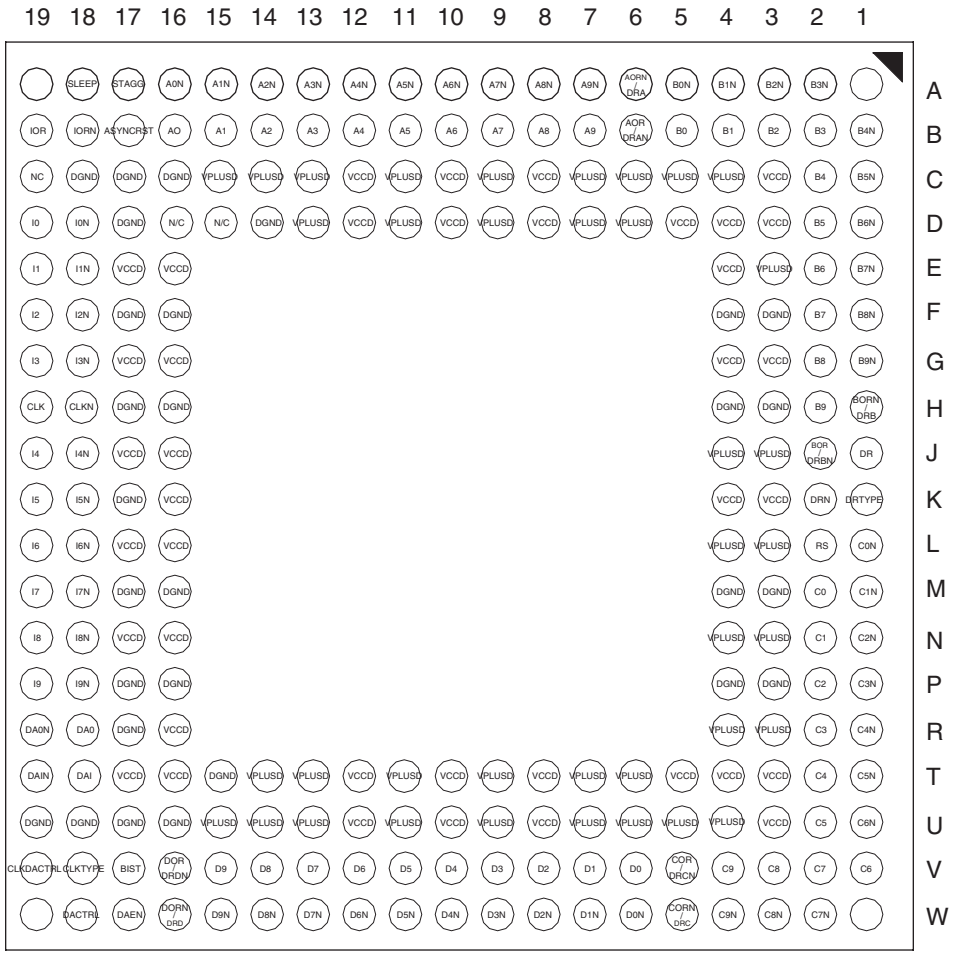
Symbol	Pin Number	Function
B0, B1, B2, B3, B4, B5, B6, B7, B8, B9	B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	In-phase (+) digital outputs for port B B0 is the LSB, B9 is the MSB
B0N, B1N, B2N, B3N, B4N, B5N, B6N, B7N, B8N, B9N	A5, A4, A3, A2, B1, C1, D1, E1, F1, G1	Inverted phase (-) digital outputs for port B
BOR/DRBN	J2	In-phase (+) additional bit output for port B or inverted phase (-) output clock in staggered mode for port B
BORN/DRB	H1	Inverted phase (-) additional bit output for port B or in-phase (+) output clock in staggered mode for port B
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9	M2, N2, P2, R2, T2, U2, V1, V2, V3, V4	In-phase (+) digital outputs for port C C0 is the LSB, C9 is the MSB
C0N, C1N, C2N, C3N, C4N, C5N, C6N, C7N, C8N, C9N	L1, M1, N1, P1, R1, T1, U1, W2, W3, W4	Inverted phase (-) digital outputs for port C
COR/DRCN	V5	In-phase (+) additional bit output for port C or inverted phase (-) output clock in staggered mode for port C
CORN/DRC	W5	Inverted phase (-) additional bit output for port C or in-phase (+) output clock in staggered mode for port C
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	In-phase (+) digital outputs for port D D0 is the LSB, D9 is the MSB
D0N, D1N, D2N, D3N, D4N, D5N, D6N, D7N, D8N, D9N	W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	Inverted phase (-) digital outputs for port D
DOR/DRDN	V16	In-phase (+) additional bit output for port D or inverted phase (-) output clock in staggered mode for port D
DORN/DRD	W16	Inverted phase (-) additional bit output for port D or in-phase (+) output clock in staggered mode for port D
DR	J1	In-phase (+) data ready signal output
DRN	K2	Inverted phase (-) data ready signal output
DAO	R18	In-phase (+) output signal for standalone delay cell
DAON	R19	Inverted phase (-) output signal for standalone delay cell
Additional Functions		
ASYNCRST	B17	Asynchronous reset signal
CLKTYPE	V18	Input clock type selection signal
DRTYPE	K1	Output clock type selection signal
CLKDACTRL	V19	Clock delay cell control signal
DACTRL	W18	Standalone delay cell control signal
DAEN	W17	Standalone delay cell enable signal
RS	L2	Ratio selection signal
SLEEP	A18	Sleep mode enable

Table 5-1. Pin Description (Continued)

Symbol	Pin Number	Function
STAGG	A17	Staggered output mode selection signal
BIST	V17	Built-in Self Test enable
NC	C19, D15, D16	Leave floating

5.1 AT84CS001 Pinout

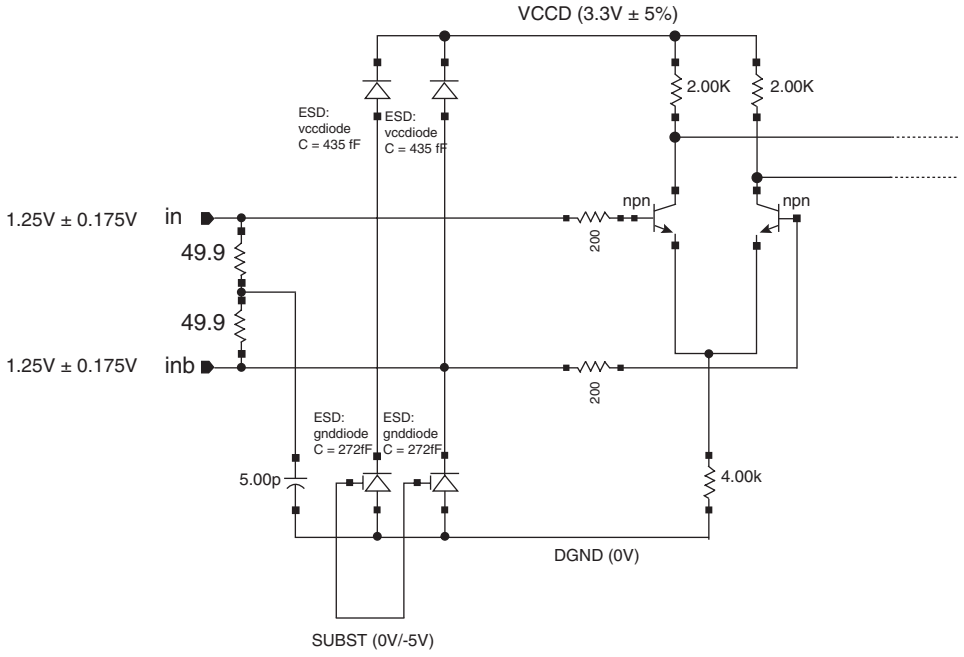
Figure 5-1. EBGA 240 (Bottom View)



6. Input/Output Equivalent Schematics

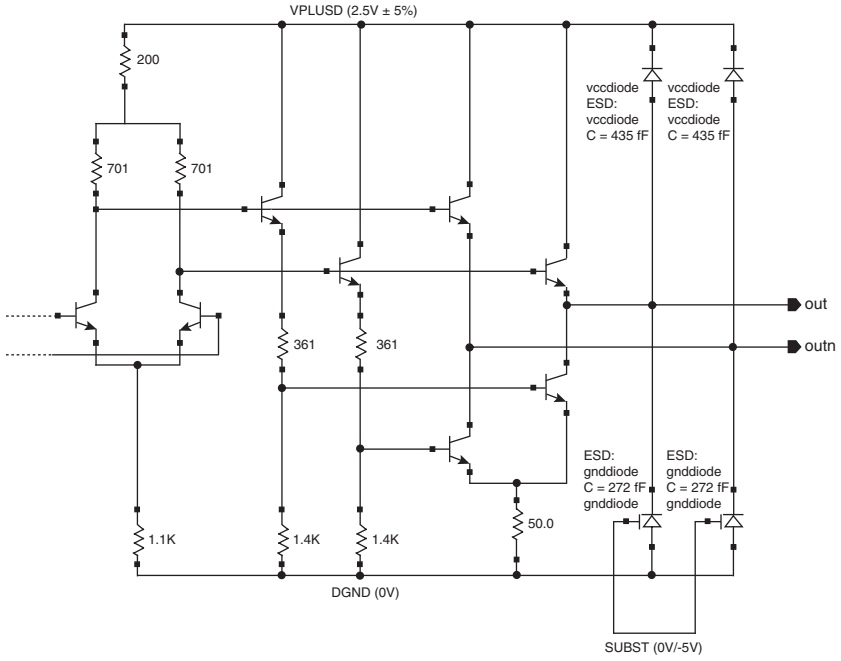
6.1 Data and Clock Differential Input Buffer

Figure 6-1. LVDS Data and LVDS Clock Input Buffer and Standalone Delay Line Input (DAI, DAIN)



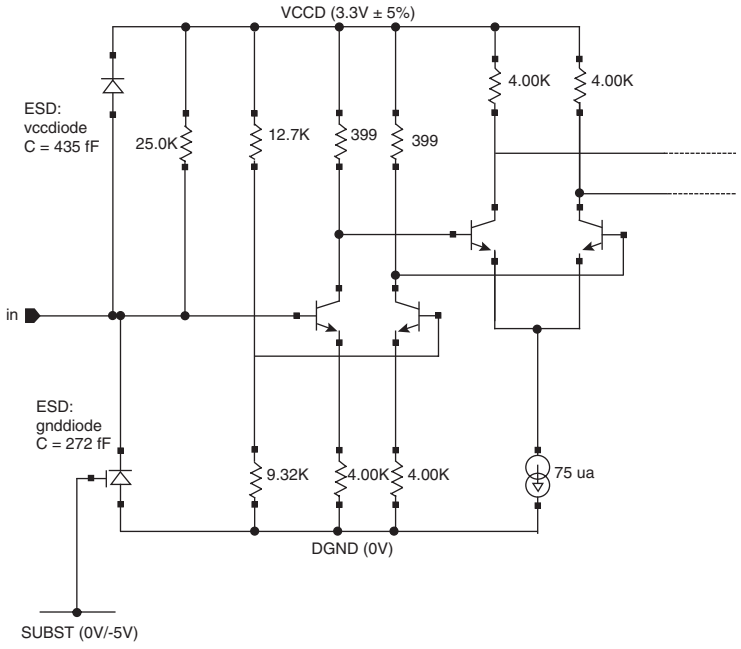
6.2 Data and Clock Output Buffer

Figure 6-2. LVDS Data and Clock Output Buffer and (DAO, DAON) Standalone Line Output



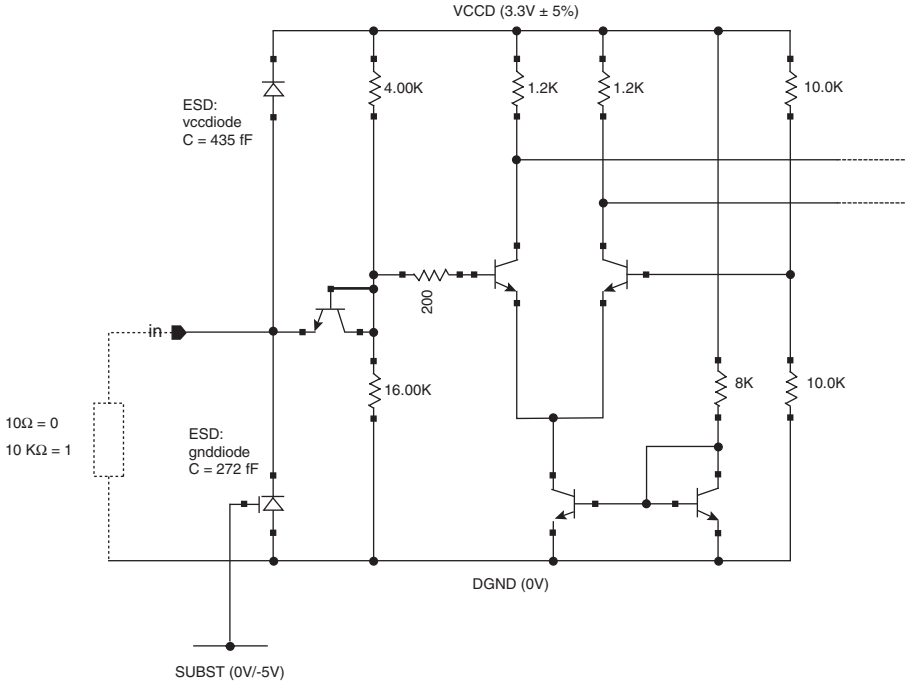
6.3 Asynchronous Reset Buffer

Figure 6-3. Asynchronous Reset Input Buffer



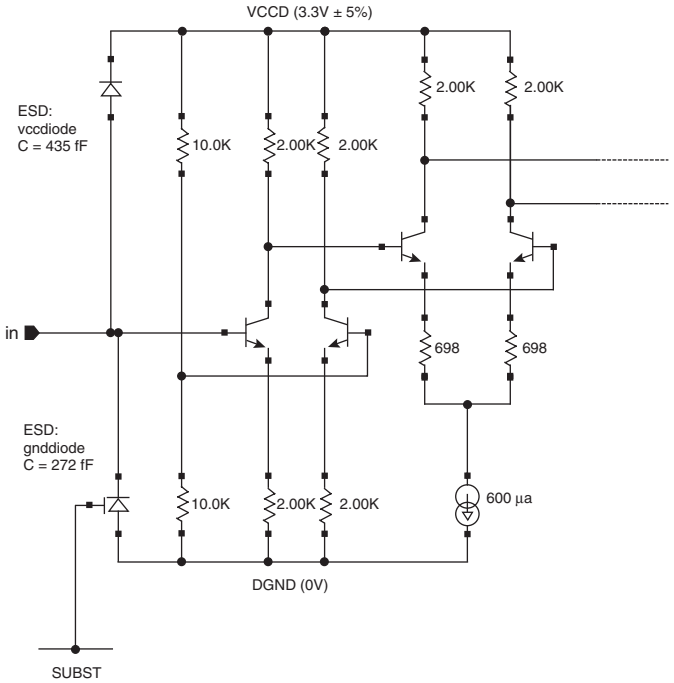
6.4 Control Signals Input Buffers

Figure 6-4. Control Signals Input Buffers: BIST, STAGG, SLEEP, RS, CLKTYPE, DRTYPE, DAEN



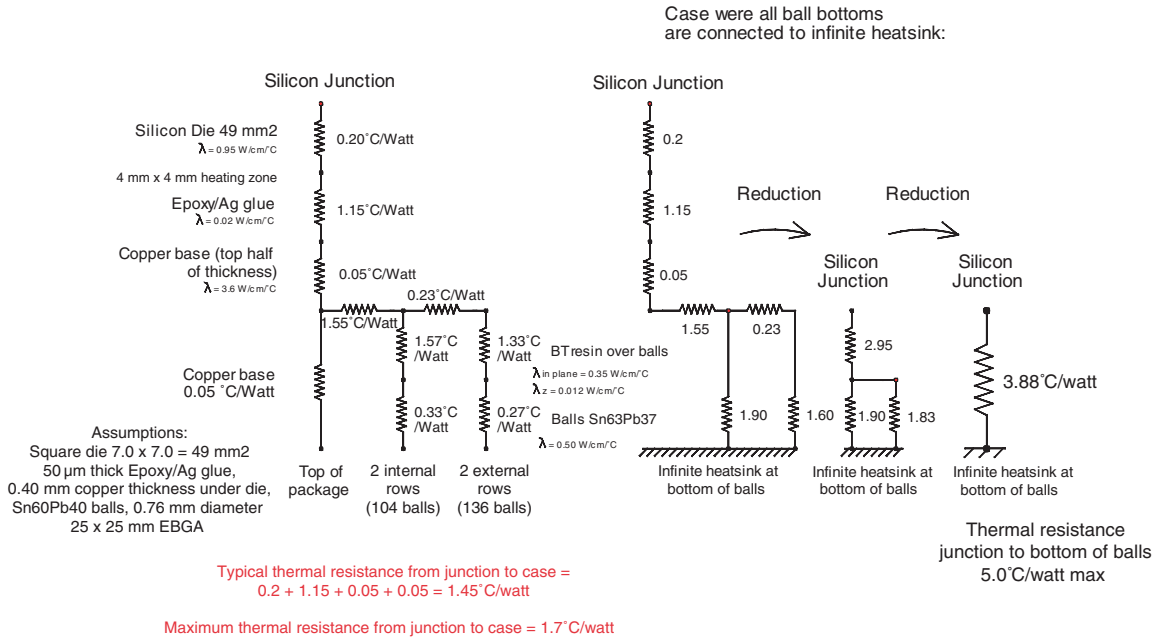
6.5 Standalone Delay Cell Control Input Buffer

Figure 6-5. Standalone Delay Cell Control Input Buffer (DACTRL, CLKDACTRL)



7. Thermal and Moisture Characteristics

Figure 7-1. DMUX Thermal Model for 240 EBGA (Typical Values) Derived from ANSYS Thermal Simulation



7.1 Moisture Characteristics

This device is sensitive to moisture (MSL3 according to JEDEC standard). Its shelf life in sealed bag is 12 months at < 40 °C and < 90% relative humidity (RH).

Once the bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220 °C) must be:

- Mounted within 168 hours in factory conditions of ≤ 30 °C/60% RH, or
- Stored at ≤ 20% RH

Before mounting, devices will require baking if the humidity indicator is > 20% when read at 23 °C ± 5 °C.

If baking is indeed required, the devices might be baked for:

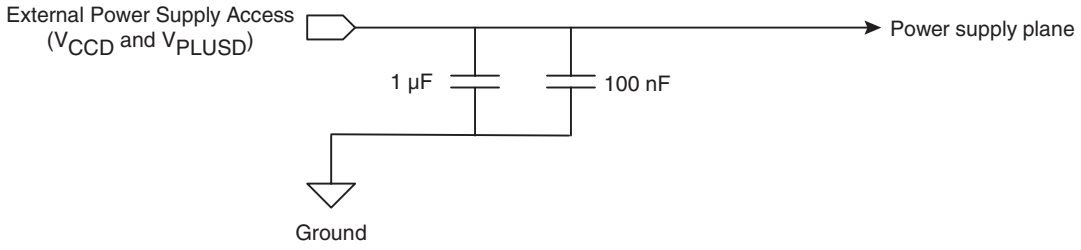
- 192 hours at 40 °C + 5 °C/-0 °C and < 5% RH for low-temperature device containers, or
- 24 hours at 125 °C ± 5 °C for high-temperature device containers

8. Applying the AT84CS001

8.1 Bypassing, Decoupling and Grounding

All power supplies must be decoupled to Ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Figure 8-1. AT84CS001 Power Supplies Decoupling and Grounding Scheme

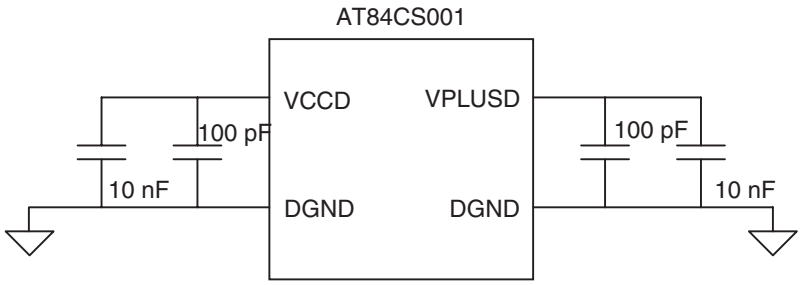


Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF capacitors in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required pairs of capacitors by power supply type is:

- 15 for V_{CCD}
- 14 for V_{PLUSD}

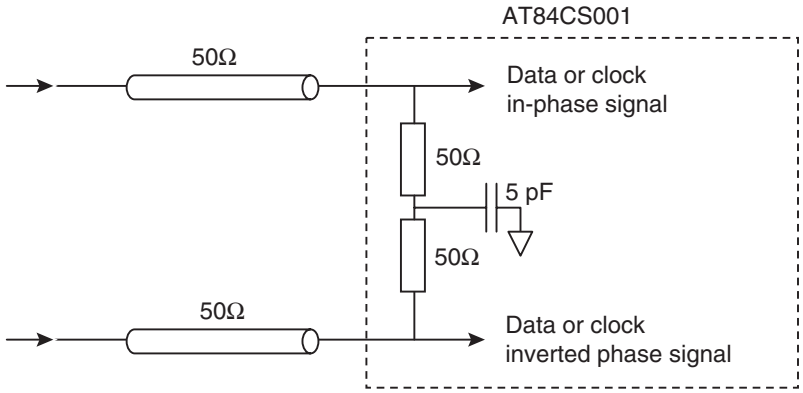
Figure 8-2. AT84CS001 Power Supplies Bypassing Scheme



8.2 LVDS Input Implementation

The input data (I0, I0N...I9, I9N and IOR, IORN) and clock (CLK, CLKN) as well as the (DAI, DAIN) input data of the standalone delay cell are LVDS-compatible. They are 2 × 50Ω differentially terminated as shown in Figure 8-3.

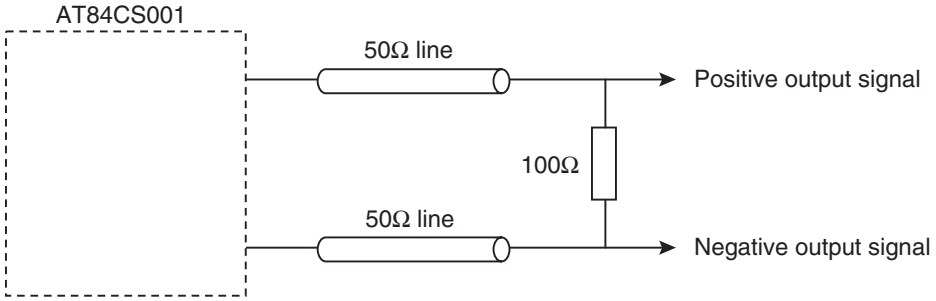
Figure 8-3. AT84CS001 LVDS Input Data and Clock Termination Scheme



8.3 LVDS Output Implementation

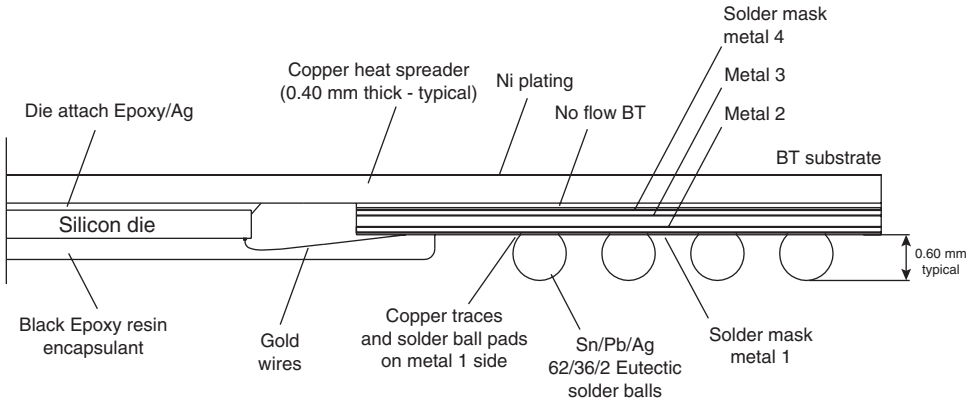
The data (AI, AIN…DI, DIN, AOR/DRAN, AORN/DRA…DOR/DRDN, DORN/DRD and DAO/DAON) and clock outputs (DR, DRN) are LVDS compatible. They must be 100Ω differentially terminated as shown in Figure 8-4.

Figure 8-4. AT84CS001 LVDS Output Termination Scheme



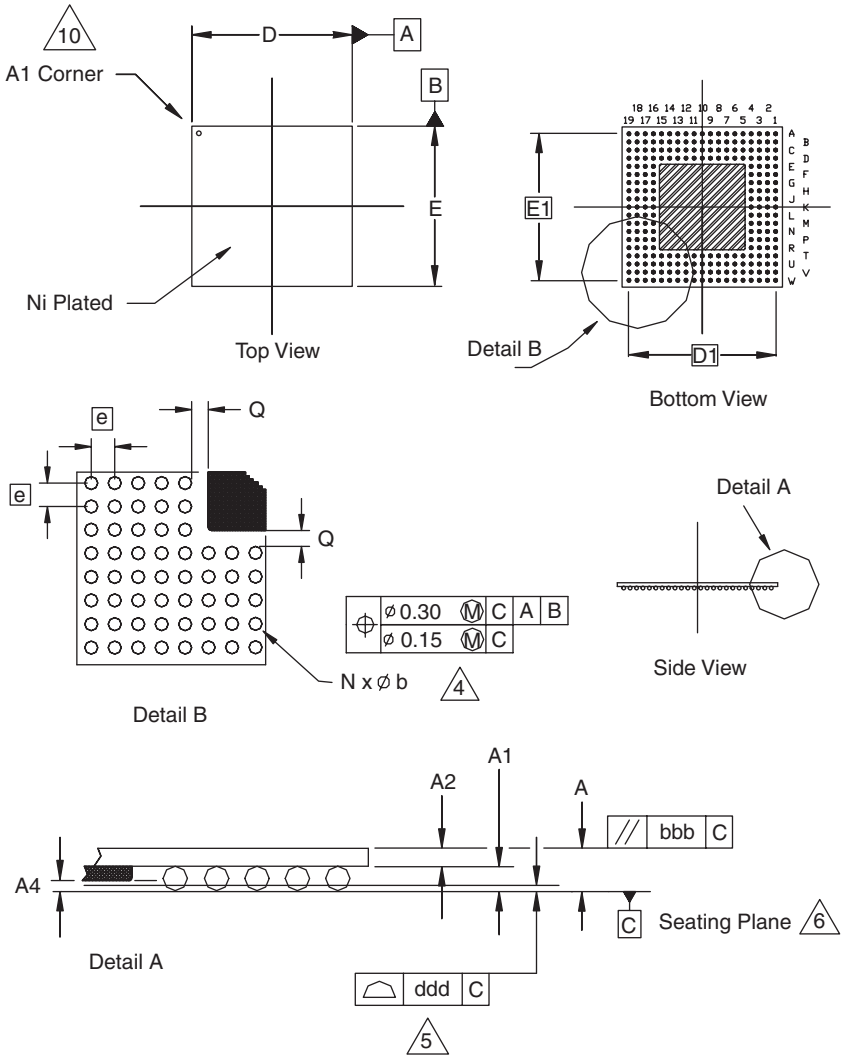
9. Package Information

Figure 9-1. Detailed Cross Section of the EBGA 240 Package



Note: In the DMUX package above, the die's underside is attached to the copper heat spreader so the copper heat spreader is at GND (0V). We recommend electrically isolating the copper heat spreader from the heat sink if a heat sink is used, in which case adequate low Rth electrical isolation should be used.

Figure 9-2. EBGA 240 Outline Dimensions



Dimensional References			
Ref	Min	Nom	Max
A	1.25	1.45	1.60
A1	0.50	0.60	0.70
D	24.80	25.00	25.20
D1		22.86 (BSC)	
E	24.80	25.00	25.20
E1		22.86 (BSC)	
b	0.70	0.80	0.90
A2	0.75	0.85	0.95
M		19	
N		240	
bbb			0.25
ddd			0.20
e		1.27 TYP	
A4	0.15		
Q	0.35		
Ref: JEDEC MS-034B Variation BAK-1			

Notes:
1. All dimensions are in millimeters
2. "e" represents the BASIC solder ball grid pitch.
3. "M" represents the BASIC solder ball matrix size, and symbol "N" is the maximum allowable number of balls after depolulating.
4. Dimension "b" is measured at the maximum solder ball diameter parallel to primary Datum C.
5. Dimension "ddd" is measured parallel to primary Datum C.
6. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be Ni plated.
8. Encapsulant size may vary with die size.
9. Black spot for pin 1 identification.
10. "A4" is measured at the Edge of encapsulant to the inner Edge of ball pad.
11. Dimensioning and tolerancing per ASME Y14.5 1994.
12. This drawing is for qualification purpose only.

10. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84CS001VTP	EBGA 240	Industrial grade -40 °C < T_C; T_J < 110 °C	Standard	
AT84CS001VTPY	EBGA 240 RoHS	Industrial grade -40 °C < T_C; T_J < 110 °C	Standard	
AT84CS001TP-EB	EBGA 240	Ambient	Prototype	Evaluation kit

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