



Dear customers,

About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", "Oki Electric", and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008
OKI Semiconductor Co., Ltd.

OKI SEMICONDUCTOR CO., LTD.

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MSM511666C/CL**65,536-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO (BYTE WRITE)****DESCRIPTION**

The MSM511666C/CL is a 65,536-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM511666C/CL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM511666C/CL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP. The MSM511666CL (the low-power version) is specially designed for lower-power applications.

FEATURES

- 65,536-word × 16-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 256 cycles/4 ms, 256 cycles/32 ms (L-version)
- Byte write and fast page mode with EDO, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Package options:

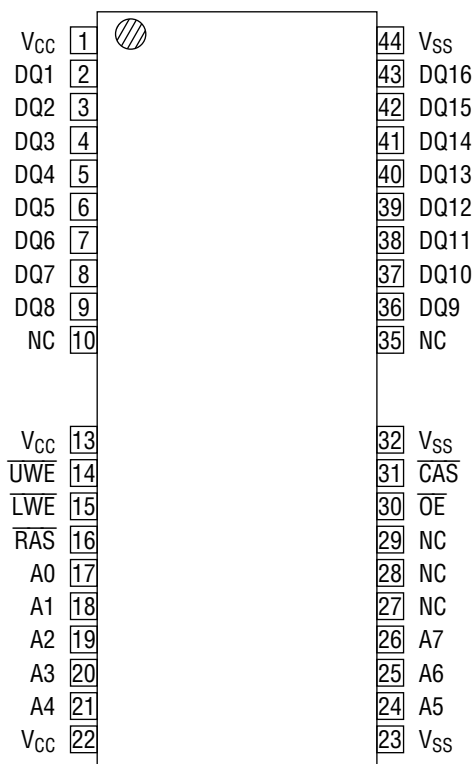
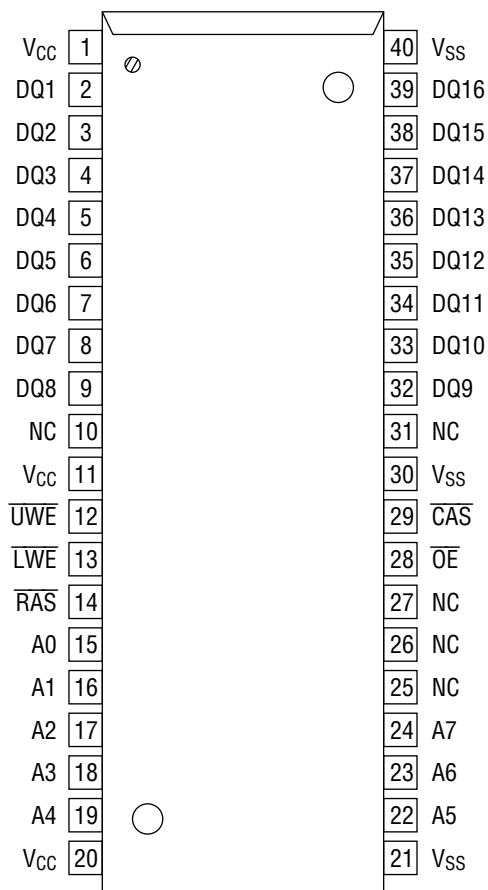
40-pin 400 mil plastic SOJ	(SOJ40-P-400-1.27)	(Product : MSM511666C/CL-xxJS)
44/40-pin 400 mil plastic TSOP	(TSOPII44/40-P-400-0.80-K)	(Product : MSM511666C/CL-xxTS-K)

xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM511666C/CL-60	60 ns	30 ns	20 ns	20 ns	110 ns	550 mW	5.5 mW/
MSM511666C/CL-70	70 ns	35 ns	20 ns	20 ns	120 ns	495 mW	1.1 mW (L-version)

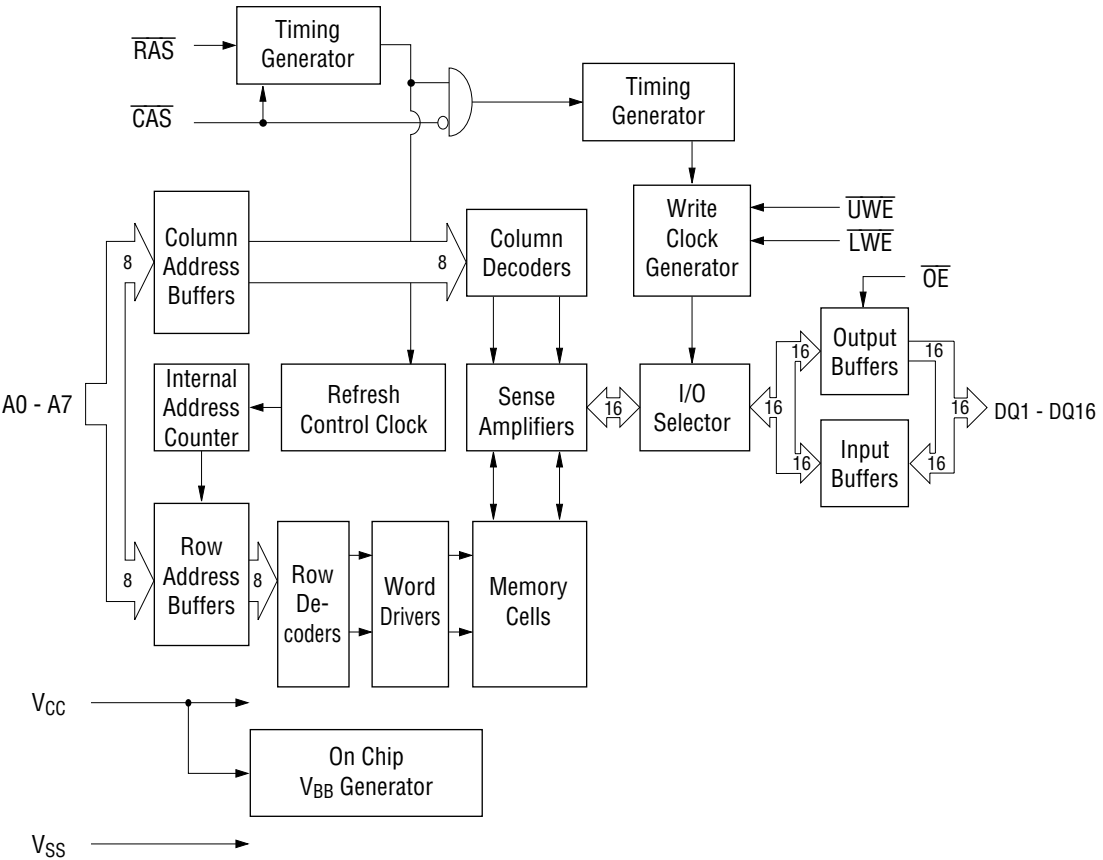
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A7	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{LWE}}$	Lower Byte Write Enable
$\overline{\text{UWE}}$	Upper Byte Write Enable
V_{CC}	Power Supply (5 V)
V_{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{LWE}}$	$\overline{\text{UWE}}$	$\overline{\text{OE}}$	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	*	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	D _{OUT}	Word Read
L	L	L	H	H	D _{IN}	Don't Care	Lower Byte Write
L	L	H	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	L	H	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D^*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$

Recommended Operating Conditions

($T_a = 0^{\circ}\text{C}$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

Capacitance

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{UWE}}$, $\overline{\text{LWE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Condition	MSM511666 C/CL-60		MSM511666 C/CL-70		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -2.5\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{ mA}$	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0\text{ V} \leq V_I \leq 6.5\text{ V}$; All other pins not under test = 0 V	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	100	—	90	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$	—	1	—	1		
		$\geq V_{CC} - 0.2\text{ V}$	—	200	—	200	μA	1, 5
Average Power Supply Current (RAS-only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = \text{Min.}$	—	100	—	90	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, DQ = enable	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	100	—	90	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, $t_{HPC} = \text{Min.}$	—	95	—	85	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	$t_{RC} = 125\text{ }\mu\text{s}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, $t_{RAS} \leq 1\text{ }\mu\text{s}$	—	300	—	300	μA	1, 4, 5

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. The address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
 4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$, $-1.0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.
 5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM511666 C/CL-60		MSM511666 C/CL-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	120	—	ns	
Read Modify Write Cycle Time	t _{RWC}	155	—	170	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{HPRWC}	65	—	70	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	15	0	15	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	15	0	15	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	15	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	15	0	15	ns	7
Transition Time	t _T	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	4	—	4	ms	
Refresh Period (L-version)	t _{REF}	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	40	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	15	—	15	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t _{CP}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10,000	10	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	50	—	55	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	ns	
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	ns	6
$\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time	t _{RSCD}	60	—	70	—	ns	
Row Address Set-up Time	t _{ASR}	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	10	—	10	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	45	—	55	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	ns	

AC Characteristics (2/2)

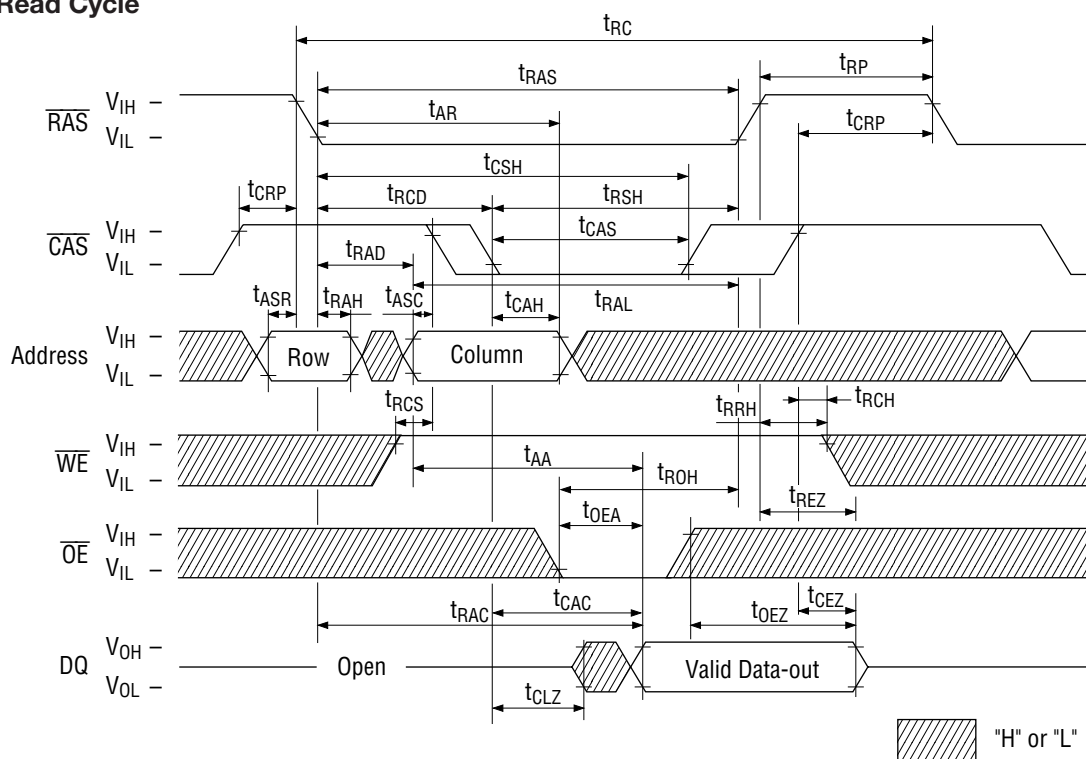
(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM511666 C/CL-60		MSM511666 C/CL-70		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	10	—	10	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	40	—	45	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t _{WPE}	7	—	7	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	10	—	10	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OCH}	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	20	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	ns	11
Data-in Hold Time	t _{DH}	10	—	10	—	ns	11
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	40	—	45	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	15	—	15	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40	—	45	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	50	—	60	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80	—	95	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	—	65	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	0	—	0	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	ns	

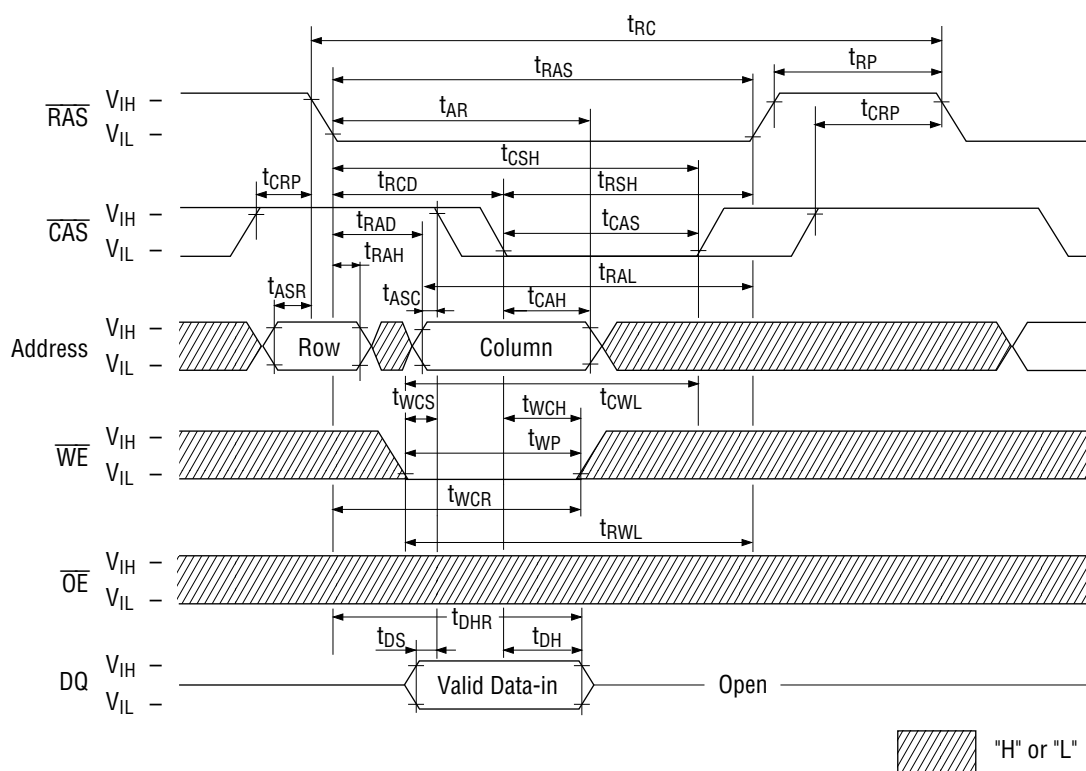
- Notes:
1. A start-up delay of 100 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1 TTL load and 50 pF. The output timing reference levels are $V_{OH} = 2.0$ V ($I_{OH} = -2$ mA) and $V_{OL} = 0.8$ V ($I_{OL} = 2$ mA).
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.

TIMING WAVEFORM

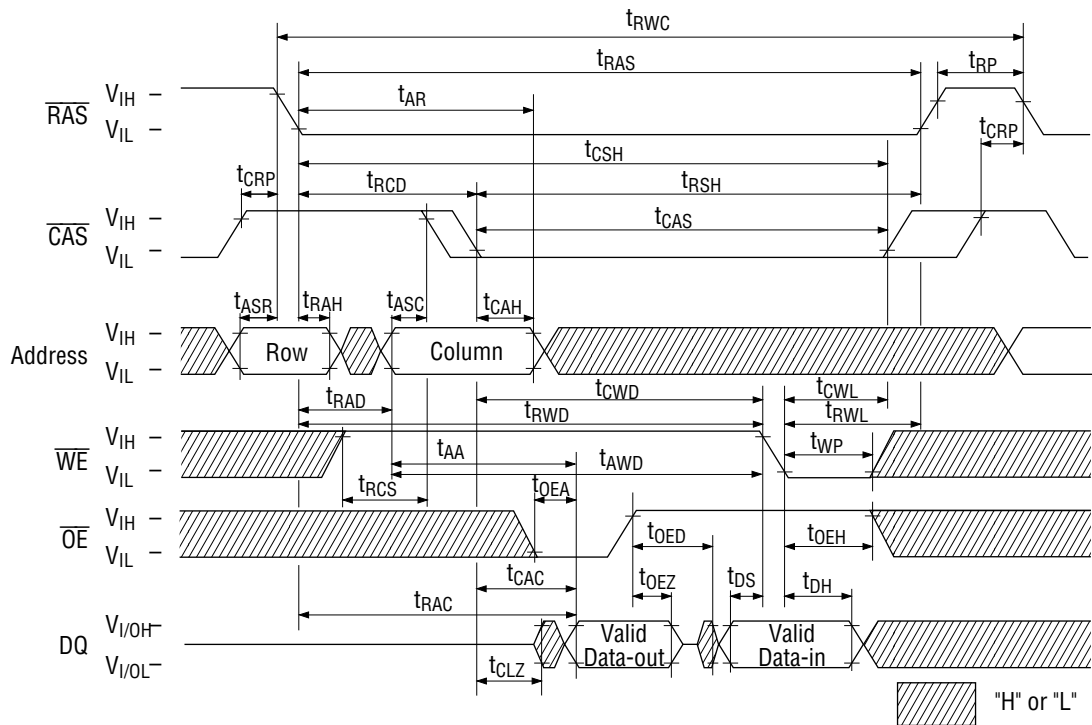
Read Cycle



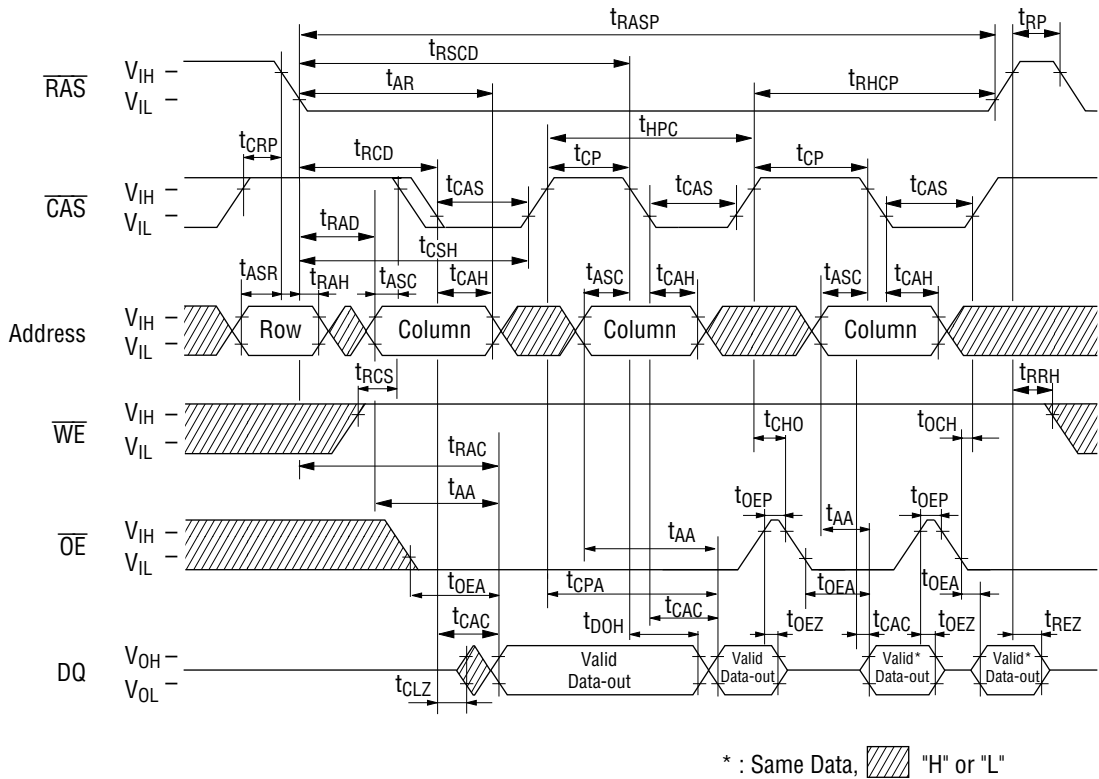
Write Cycle (Early Write)



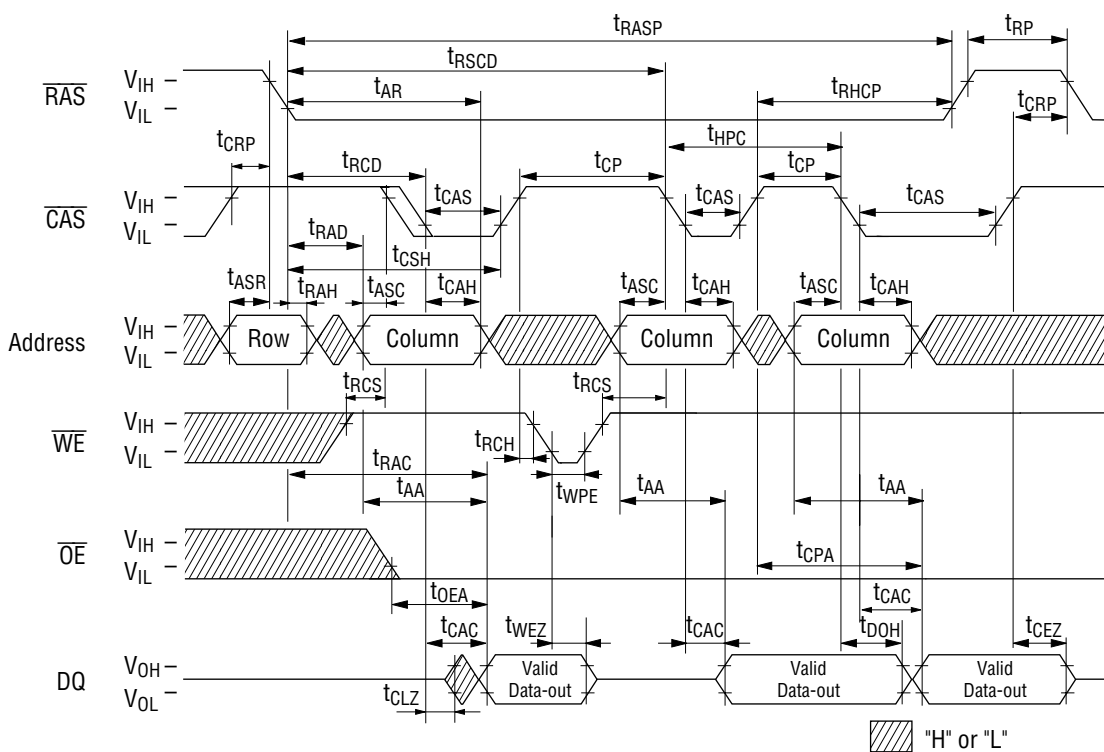
Read Modify Write Cycle



Fast Page Mode Read Cycle (Part-1)



Fast Page Mode Read Cycle (Part-2)



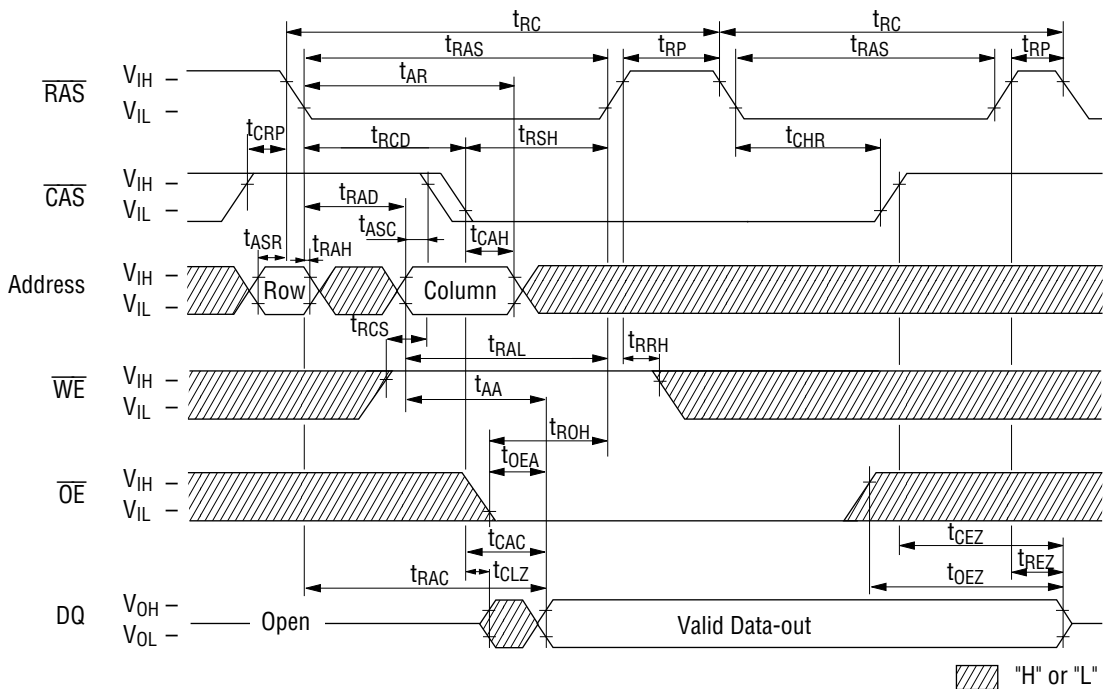
The diagram illustrates the timing relationships for a memory device. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, and DQ. The timing parameters are defined as follows:

- t_{RAS} : RAS pulse width
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{RSH} : RAS to SH (Sense Amplifier) delay
- t_{ASR} : Address to RAS delay
- t_{RAH} : Address to RAS hold time
- t_{ASC} : Address to CAS delay
- t_{CAH} : Address to CAS hold time
- t_{WCS} : Write Command to Data Strobe delay
- t_{WCH} : Write Command to Data Strobe hold time
- t_{DHR} : Data Strobe to Data Hold time
- t_{DS} : Data Strobe to Data Setup time
- t_{DH} : Data Strobe to Data Hold time

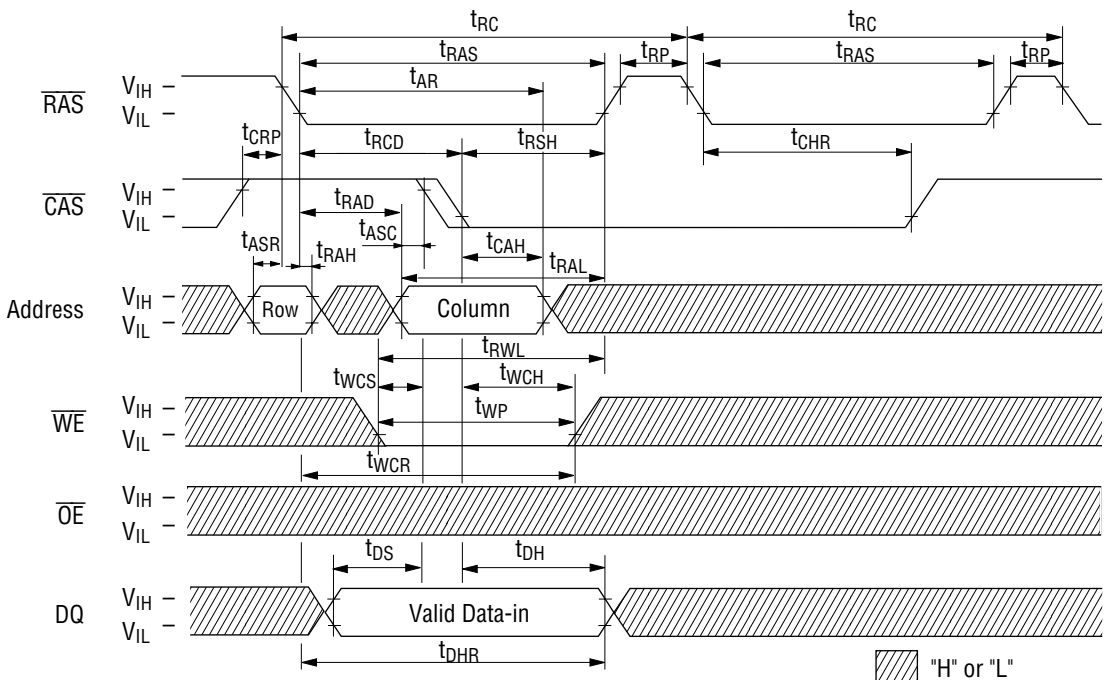
The diagram shows three memory access cycles: Row, Column, and Column. The Address signal is shown as a sequence of pulses, with the first pulse being shaded. The $\overline{\text{WE}}$ signal is shown as a sequence of pulses, with the first pulse being shaded. The $\overline{\text{OE}}$ signal is shown as a shaded area, indicating it is active low. The DQ signal is shown as a sequence of pulses, with the first pulse being shaded. The timing parameters are indicated by arrows and labels on the diagram.

[illegible]

Hidden Refresh Read Cycle

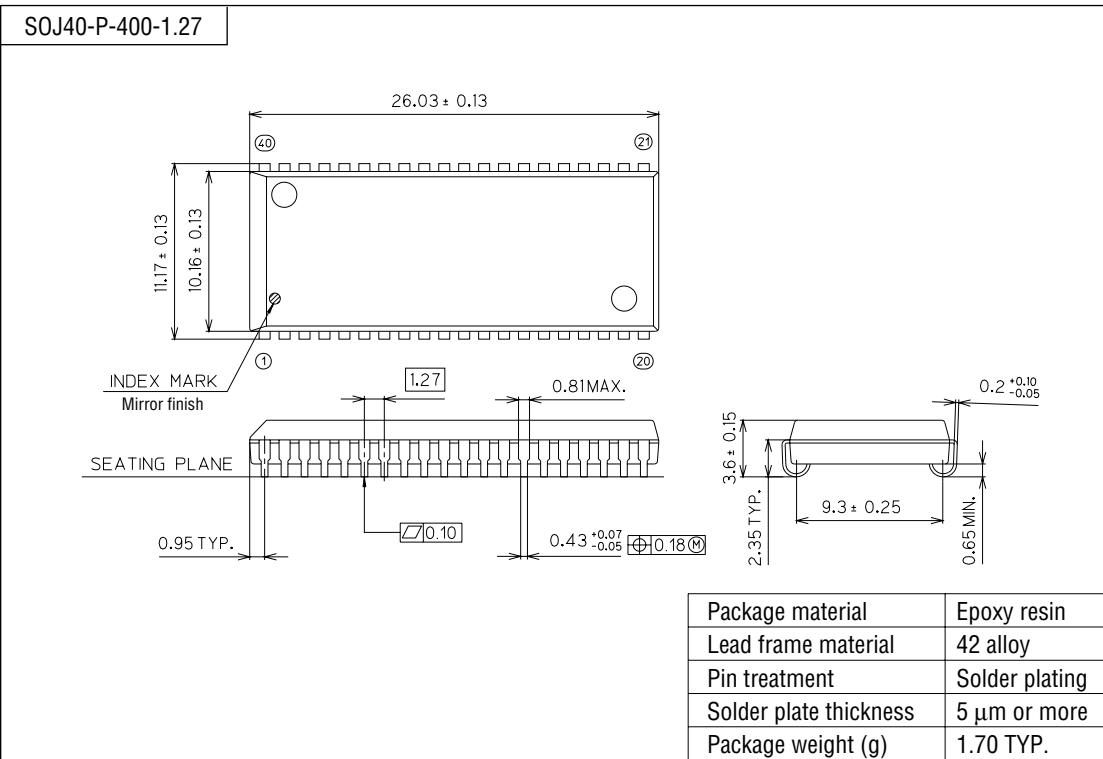


Hidden Refresh Write Cycle



PACKAGE DIMENSIONS

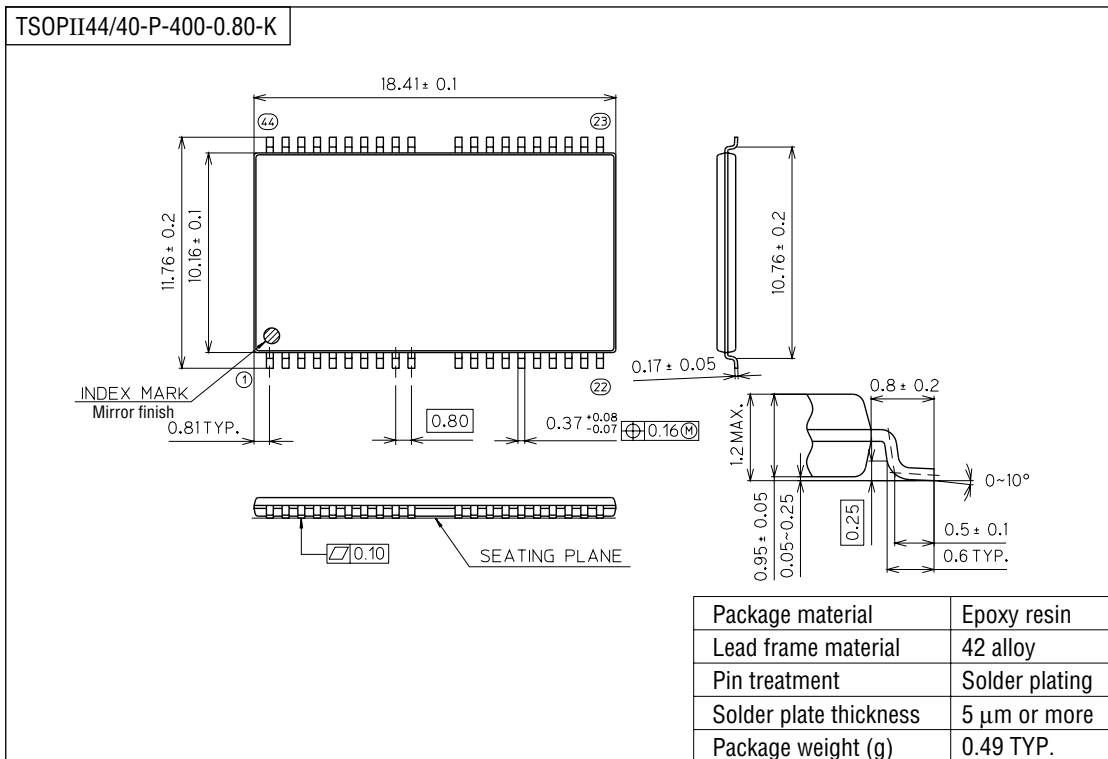
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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