

SILICON STACKED GATE CMOS

131,072 WORD x 8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY

Description

The TC541000AP/AF and the TC541001AP/AF are 131,072 word x 8 bit CMOS one time programmable read only memories molded in 32-pin plastic packages.

The TC541000AP/AF and TC541001AP/AF access times are 120ns/150ns. They have a low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as for the TC571000AD/TC571001AD UV EPROMs. Once programmed, the TC541000AP/AF and TC541001AP/AF cannot be erased because of the use of a plastic package without a transparent window.

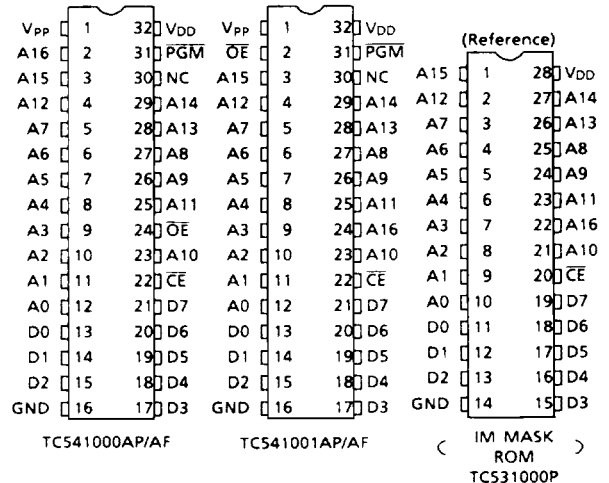
Features

- Peripheral circuit : CMOS
- Memory cell : NMOS
- Access time

	-12	-15
t_{ACC}	120ns	150ns
Temp	0 ~ 70°C	

- Low power dissipation
 - Active : 30mA/8.3MHz
 - Standby : 100µA
- Single 5V power supply
- Fully static operation
- High speed programming mode : $t_{PW} = 0.1ms$
- Inputs and outputs TTL compatible
- JEDEC standard 32-pin : TC541000AP/AF
- 1M MROM compatible : TC541001AP/AF
- Package
 - TC541000AP/TC541001AP : DIP32-P-600
 - TC541000AF/TC541001AF : SOP32-P-525

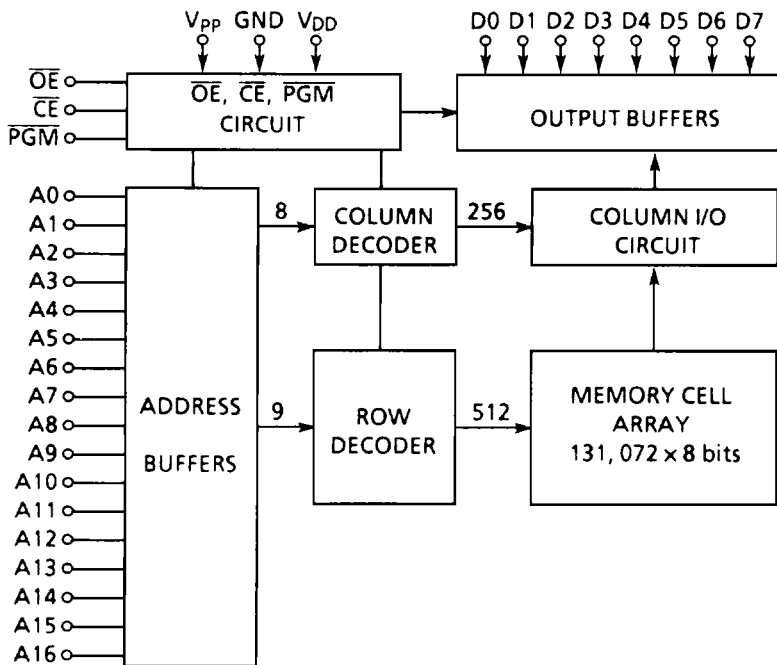
Pin Connection (Top View)



Pin Names

A0 ~ A16	Address Inputs
D0 ~ D7	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
V _{DD}	Power Supply Voltage (+5V)
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

Block Diagram



Operating Mode

MODE \ PIN	PGM	CE	OE	V _{PP}	V _{DD}	D0 ~ D7	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V _{IN}	Input Voltage	-0.6 ~ 7.0	
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{DD} + 0.5	
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 125	°C
T _{OPR}	Operating Temperature	0 ~ 70	

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	–	0.8	
V _{DD}	Power Supply Voltage	4.75	5.00	5.25	
V _{PP}	Program Supply Voltage	V _{DD} - 0.6	V _{DD}	V _{DD} + 0.6	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	–	–	±10	μA
I _{DDO1}	Operating Current	CE = 0V I _{OUT} = 0mA	f = 8.3MHz	–	–	30
I _{DDO2}						
I _{DDS1}	Standby Current	CE = V _{IH}	–	–	1	μA
I _{DDS2}		CE = V _{DD} - 0.2V	–	–	100	
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	–	–	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	–	–	0.4	
I _{PP1}	V _{PP} Current	V _{PP} = V _{DD} ±0.6V	–	–	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V ~ V _{DD}	–	–	±10	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±5%, V_{PP} = V_{DD}±0.6V)

SYMBOL	PARAMETER	TC541000AP-12/TC541001AP-12 TC541000AF-12/TC541001AF-12		TC541000AP-15/TC541001AP-15 TC541000AF-15/TC541001AF-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	–	120	–	150	ns
t _{CE}	CE to Output Valid	–	120	–	150	
t _{OE}	OE to Output Valid	–	60	–	70	
t _{PGM}	PGM to Output Valid	–	60	–	70	
t _{DF1}	CE to Output in High-Z	0	50	0	60	
t _{DF2}	OE to Output in High-Z	0	50	0	60	
t _{DF3}	PGM to Output in High-Z	0	50	0	60	
t _{OH}	Output Data Hold Time	0	–	0	–	

AC Test Conditions

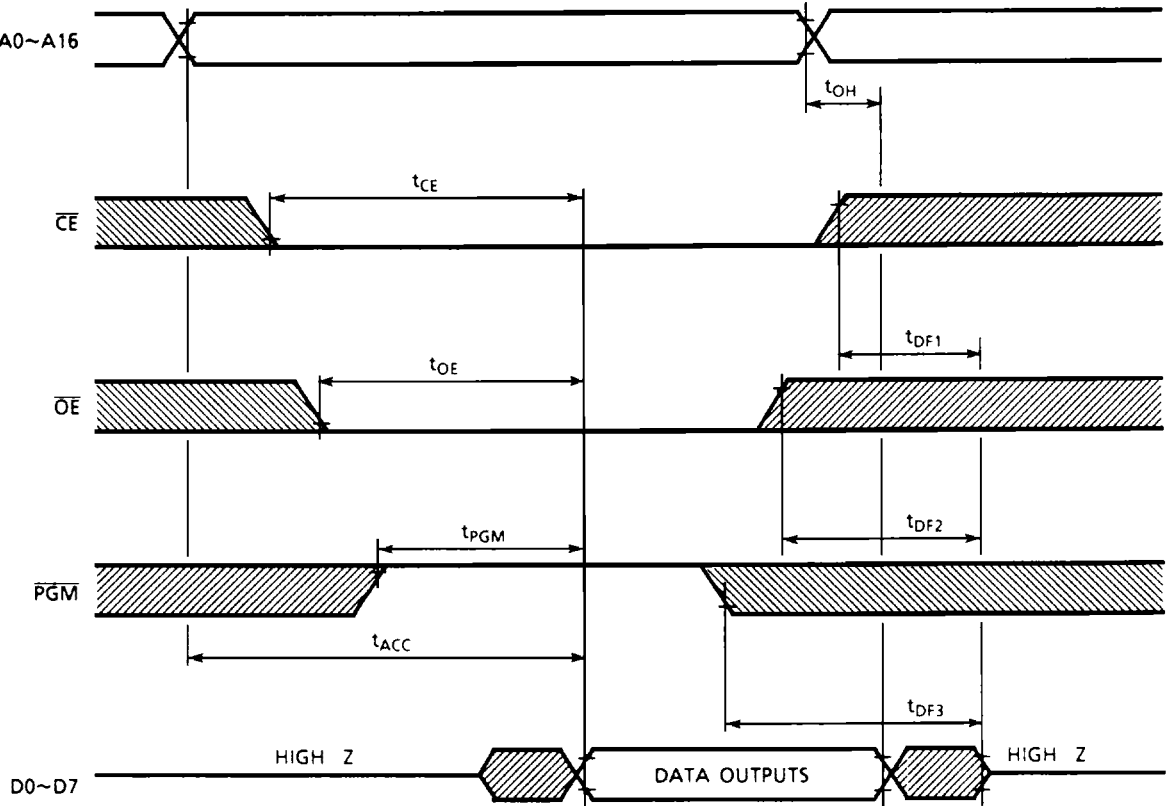
Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C _L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	–	16	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	–	16	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms (Read)



High Speed Programming Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 1.0	V
V _{IL}	Input Low Voltage	-0.3	–	0.8	
V _{DD}	Power Supply Voltage	6.00	6.25	6.50	
V _{PP}	Program Supply Voltage	12.50	12.75	13.00	

DC Characteristics (T_a = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	–	–	±10	μA
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	–	–	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	–	–	0.4	
I _{DD}	V _{DD} Supply Current	–	–	–	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V	–	–	50	

AC Programming Characteristics (T_a = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

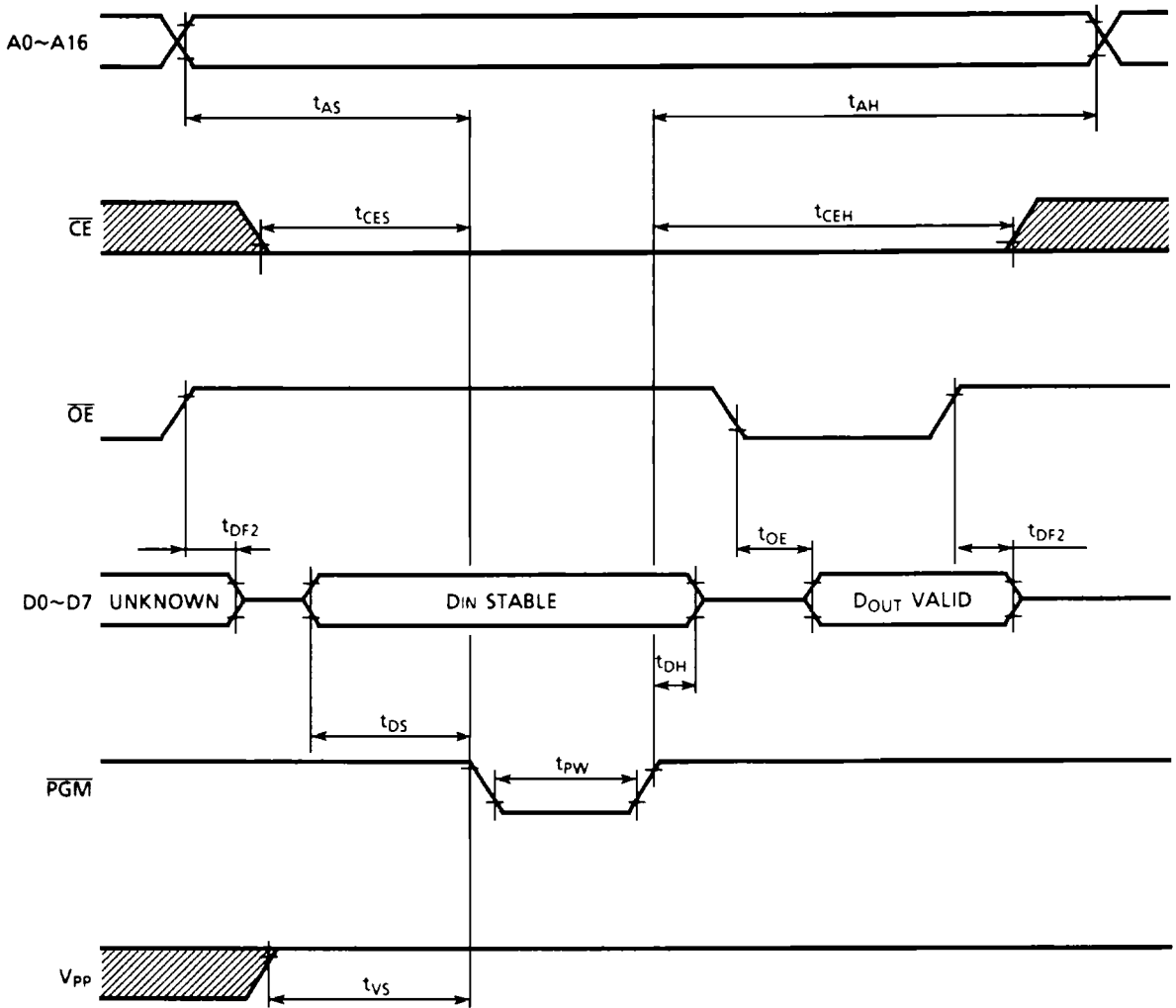
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	–	2	–	–	μs
t _{AH}	Address Hold Time	–	2	–	–	
t _{CES}	CE Setup Time	–	2	–	–	
t _{CEH}	CE Hold Time	–	2	–	–	
t _{DS}	Data Setup Time	–	2	–	–	
t _{DH}	Data Hold Time	–	2	–	–	
t _{VS}	V _{PP} Setup Time	–	2	–	–	ms
t _{PW}	Program Pulse Width	–	0.095	0.1	0.105	
t _{OE}	OE to Output Valid	–	–	–	100	
t _{DF2}	OE to Output in High-Z	CE = V _{IL}	–	–	90	

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C _L = 100 pF

Timing Waveforms (Program)

High Speed Programming Mode



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}
2. Removing the device from a programming socket and replacing the device in the socket while $V_{PP} = 12.75V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Operation Information

The TC541000AP/AF/TC541001AP/AF's six operating modes are listed in the following table. Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE	PIN	PGM	CE	OE	V _{PP}	V _{DD}	D0 - D7	POWER
Read Operation (Ta = 0 ~ 70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta = 25±5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Read Mode

The TC541000AP/AF/TC541001AP/AF has three control inputs. The chip enable (CE) input controls the operating power and should be used for device selection.

The output enable (OE) and program control (PGM) inputs control the output buffers.

Assuming that CE = OE = V_{IL} and PGM = V_{IH}, once the address has stabilized, output data will be valid after the address access time has elapsed.

The CE to output valid time (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that CE = V_{IL}, PGM = V_{IH} and that the address has been stable for at least t_{ACC}, then output data will be valid after t_{CE} from the falling edge of OE.

And assuming that CE = OE = V_{IL} and that all address lines have been stable, then output data is valid after t_{PGM} from the rising edge of PGM.

Output Deselect Mode

If CE = V_{IH} or OE = V_{IH}, the outputs will be in a high impedance state.

Therefore, two or more devices can be connected together on a common bus if the output of only one device is enabled.

When CE is used for device selection, all deselected devices are in the low power standby mode.

Standby Mode

The TC541000AP/AF/TC541001AP/AF has a low power standby mode controlled by the CE signal.

By applying a MOS high level voltage (V_{DD}) to the CE input, the TC541000AP/AF/TC541001AP/AF is placed in the standby mode which reduces the operating current to 100µA and puts the outputs in a high impedance state, independent of the OE input.

Program Mode

When the TC541000AP/AF/TC541001AP/AF is initially received by customers, all bits of the device are in the "1" state, which is the erased state. Therefore, the object of the program operation is to introduce "0" data into the desired bit locations.

The TC541000AP/AF/TC541001AP/AF is in the programming mode when V_{PP} = 12.75V, PGM = CE = V_{IL}, and OE = V_{IH}.

The TC541000AP/AF/TC541001AP/AF can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when OE = CE = V_{IL} and PGM = V_{IH}.

Program Inhibit Mode

When the programming voltage (+12.75V) is applied to the V_{PP} terminal, a high level CE or PGM input inhibits the TC541000AP/AF/TC541001AP/AF from being programmed.

The programming of two or more EPROMs in parallel with different data is easily accomplished. All inputs except for CE and PGM may be commonly connected, then a TTL low level program pulse is applied to CE and PGM of the desired device only while a TTL high level signal is applied to the CE of the other devices.

High Speed Programming Mode

The device is set up in high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{DD} = 6.25V$ and $\overline{PGM} = V_{IH}$.

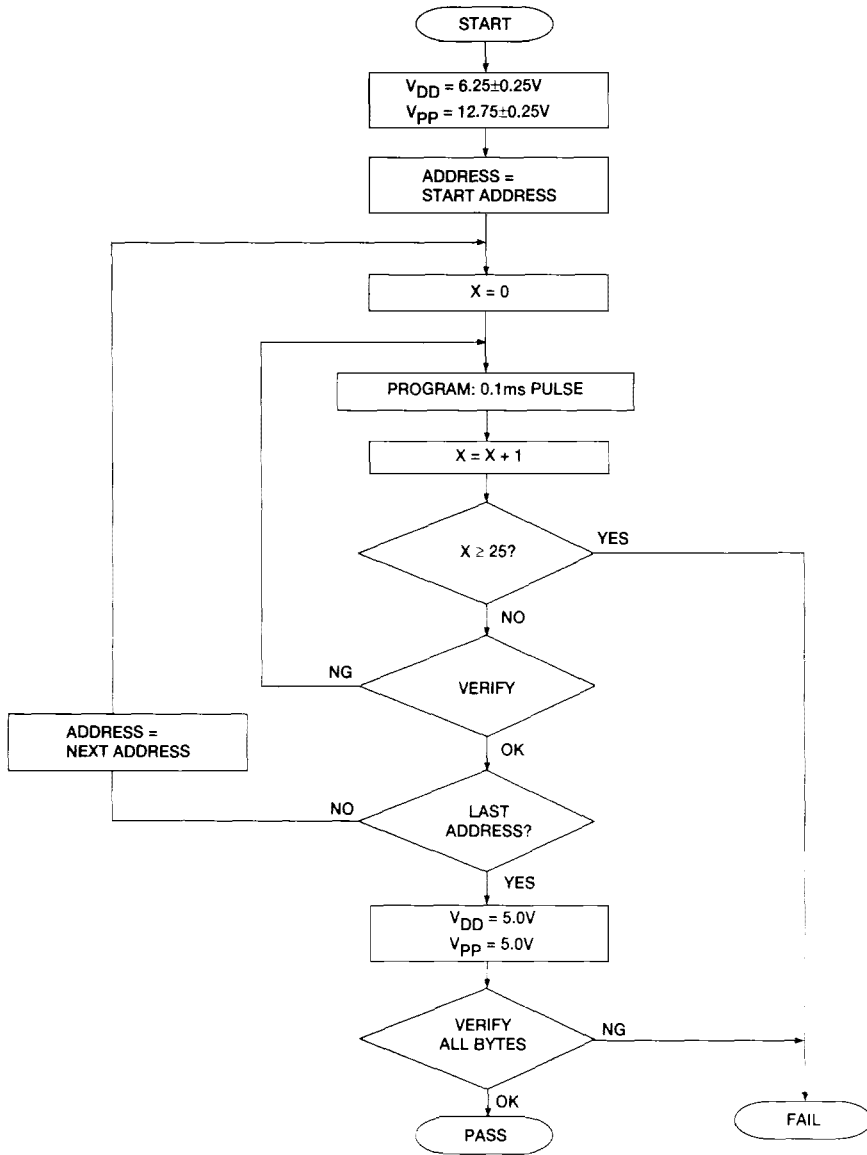
Programming is achieved by applying a single 0.1ms TTL low level pulse to the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using the program verify mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{DD} = V_{PP} = 5V$.

High Speed Programming Mode

Flow Chart



Electric Signature Mode

The electric signature mode allows one to read out a code from the TC541000AP/AF/TC541001AP/AF which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC541000AP/AF/TC541001AP/AF by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit being the MSB (D7). The following table shows the electric signature of the TC541000AP/AF/TC541001AP/AF.

SIGNATURE		PINS									HEX. DATA
		A0	D7	D6	D5	D4	D3	D2	D1	D0	
Manufacturer Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC541000AP/AF	V_{IH}	1	0	0	0	0	1	1	0	86
	TC541001AP/AF		0	0	0	0	0	1	1	1	07

Notes: A9 = 12V±0.5V

A1 - A8, A10 - A16, CE, OE = V_{L}

PGM = V_{L}