FAIRCHILD SEMICONDUCTOR™

March 1998

100360
Low Power Dual Parity Checker/Generator

General Description

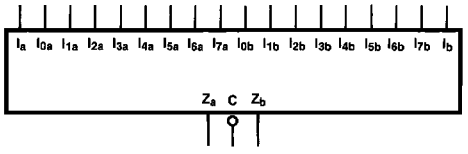
The 100360 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The 100360 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words. The $\overline{C}$ output is LOW when the two words match, bit for bit. All inputs have 50 kΩ pull-down resistors.

Features

- Lower power than 100160
- 2000V ESD protection
- Pin/function compatible with 100160
- Voltage compensated operating range = –4.2V to –5.7V
- Min to Max propagation delay 35% tighter than 100160
- Available to industrial grade temperature range

Ordering Code:

Logic Symbol

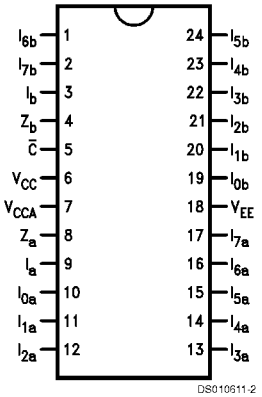


DS010611-1

Pin Names	Description
I_a, I_b, I_{na}, I_{nb}	Data Inputs
Z_a, Z_b	Parity Odd Outputs
$\overline{C}$	Compare Output

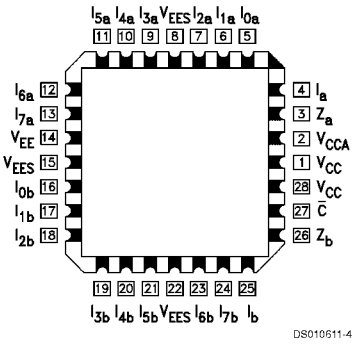
Connection Diagrams

24-Pin DIP



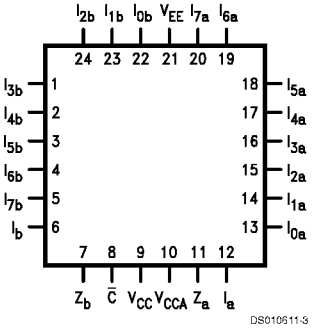
DS010611-2

28-Pin PCC



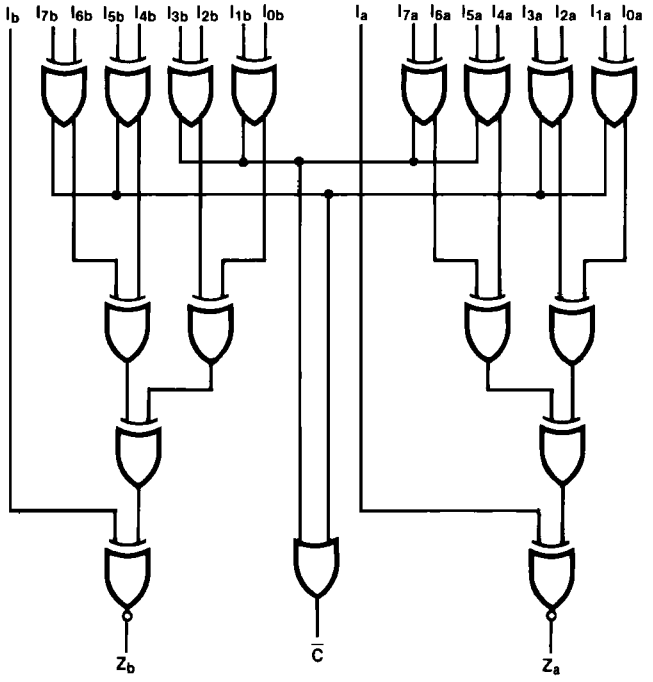
DS010611-4

24-Pin Quad Cerpak



DS010611-3

Logic Diagram



DS010611-5

Truth Table

(Each Half)

Sum of HIGH Inputs	Output Z
Even	HIGH
Odd	LOW

Comparator Function

$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or $V_{IL\ (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or $V_{IL\ (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current						
	I_a, I_b			340	µA	V_{IN} = V_{IH} (Max)	
	I_{na}, I_{nb}			240			
I_{EE}	Power Supply Current	−100		−50	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.10	2.75	1.10	2.75	1.10	2.75	ns	
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.10	2.80	1.10	2.80	1.10	2.80	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	1.30	0.60	1.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.10	2.75	1.10	2.75	1.10	2.75	ns	

PCC and Cerpak AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.10	2.80	1.10	2.80	1.10	2.80	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	1.30	0.60	1.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Industrial Version
PCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C (Note 4)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} =V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	or V_{IL} (Max)	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current							
	Ia, Ib		340		340	µA	V_{IN} = V_{IH} (Max)	
	Ina, Inb		240		240			
I_{EE}	Power Supply Current	−100	−50	−100	−50	mA	Inputs Open	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.00	2.75	1.10	2.75	1.10	2.75	ns	
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.00	2.80	1.10	2.80	1.10	2.80	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	1.30	0.60	1.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	

Military Version — Preliminary
DC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = –55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	–1025	–870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to –2.0V	(Notes 5, 6, 7)
		–1085	–870	mV	–55°C			
V_{OL}	Output LOW Voltage	–1830	–1620	mV	0°C to +125°C			
		–1830	–1555	mV	–55°C			
V_{OHC}	Output HIGH Voltage	–1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to –2.0V	(Notes 5, 6, 7)
		–1085		mV	–55°C			
V_{OLC}	Output LOW Voltage		–1610	mV	0°C to +125°C			
			–1555	mV	–55°C			
V_{IH}	Input HIGH Voltage	–1165	–870	mV	–55°C to +125°C	Guaranteed HIGH Signal for All Inputs		(Notes 5, 6, 7, 8)
V_{IL}	Input LOW Voltage	–1830	–1475	mV	–55°C to +125°C	Guaranteed LOW Signal for All Inputs		(Notes 5, 6, 7, 8)
I_{IL}	Input LOW Current	0.50		µA	–55°C to +125°C	V_{EE} = –4.2V V_{IN} = V_{IL} (Min)		(Notes 5, 6, 7)
I_{IH}	Input HIGH Current							
	I_a, I_b		340	µA	0°C to +125°C	V_{EE} = –5.7V V_{IN} = V_{IH} (Max)		(Notes 5, 6, 7)
	I_{na}, I_{nb}		240					
	I_a, I_b		490	µA	–55°C			
	I_{na}, I_{nb}		340					
I_{EE}	Power Supply Current	–110	–50	mA	–55°C to +125°C	Inputs Open		(Notes 5, 6, 7)

Note 5: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 6: Screen tested 100% on each device at –55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 7: Sample tested (Method 5005, Table I) on each manufactured lot at –55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 8: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = –55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.00	2.95	1.00	2.95	1.00	2.95	ns	*Figures 1, 2*	(Notes 9, 10, 11)
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.00	3.00	1.00	3.00	1.00	3.00	ns		
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.40	1.40	0.50	1.50	0.50	1.50	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns		(Note 12)

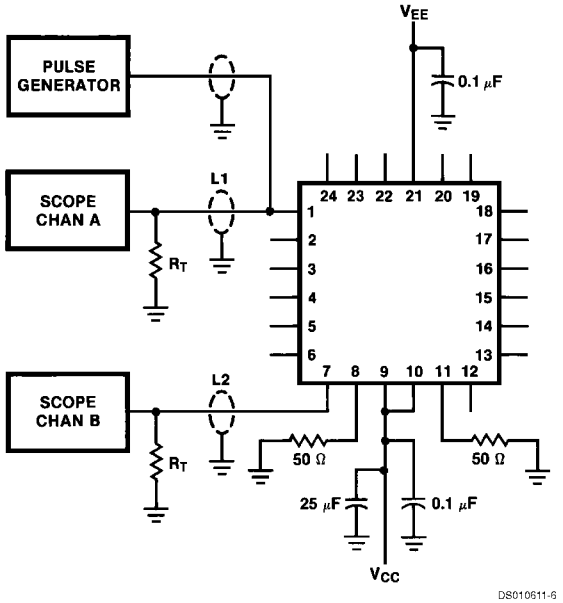
Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 11: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and –55°C temperatures, Subgroups A10 and A11.

Note 12: Not tested at +25°C, +125°C, and –55°C temperature (design characterization data).

Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Switching Waveforms

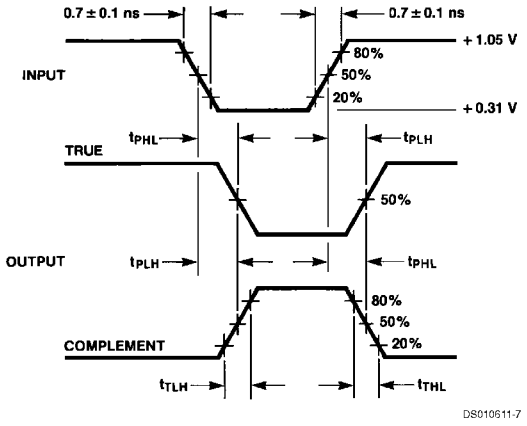
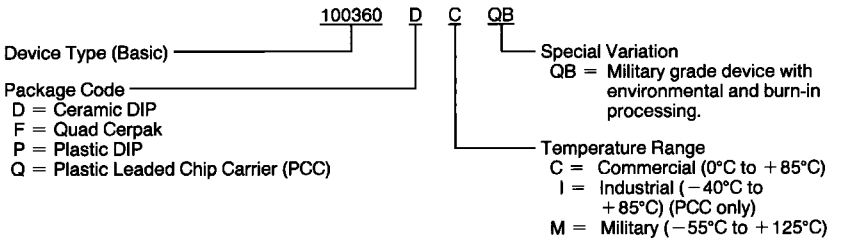


FIGURE 2. Propagation Delay and Transition Times

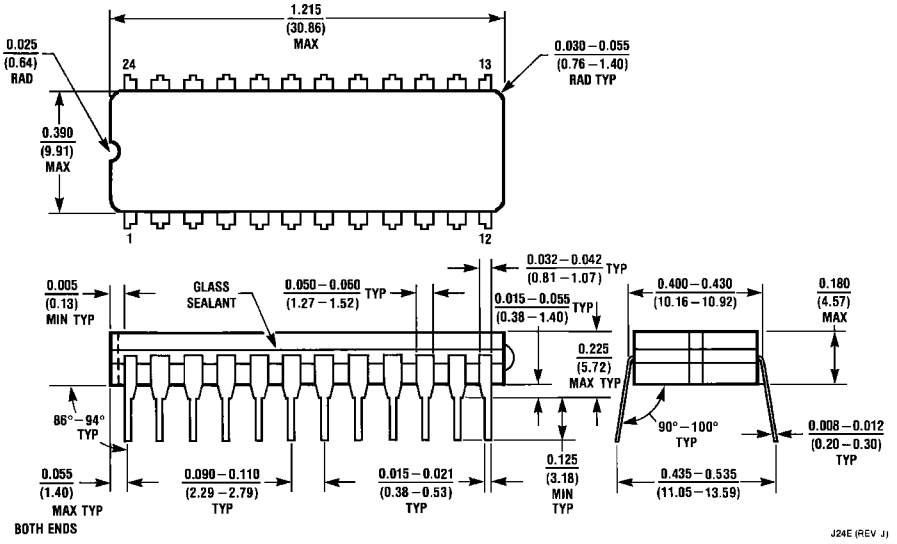
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



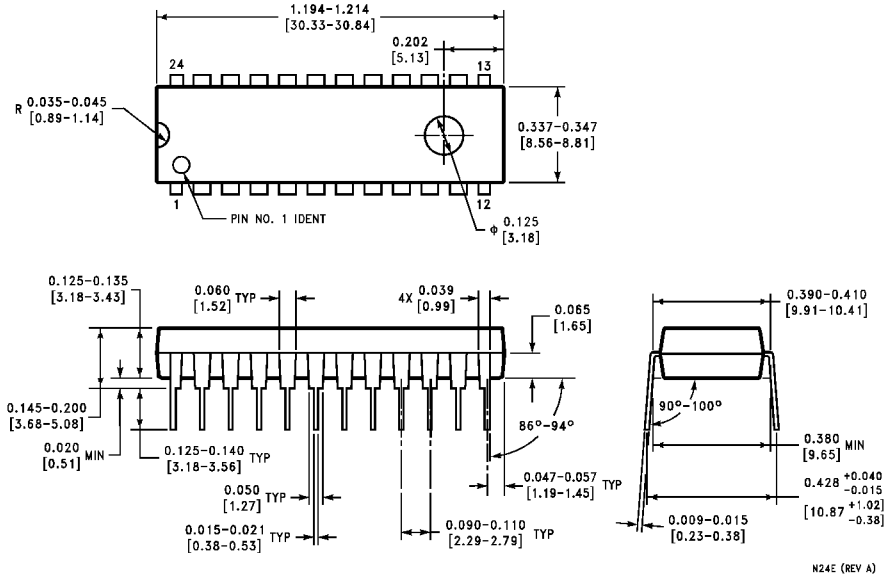
DS010611-8

Physical Dimensions inches (millimeters) unless otherwise noted



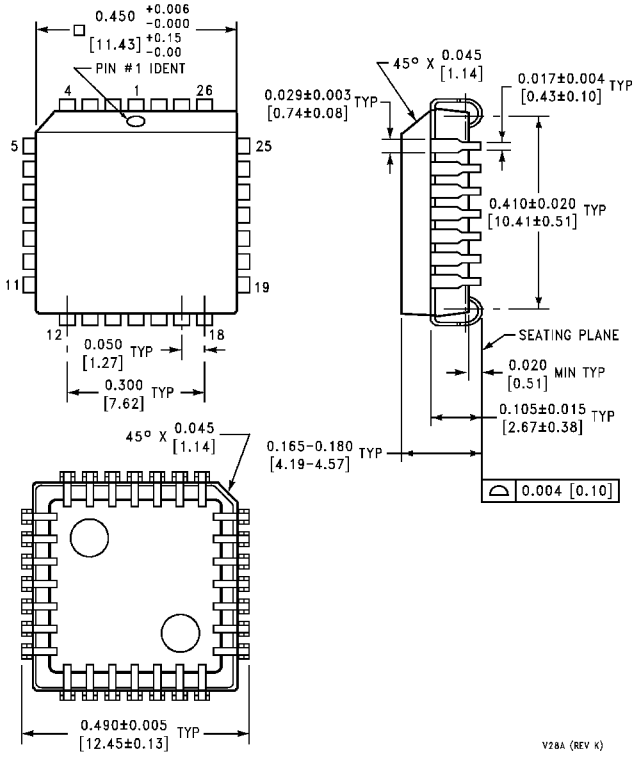
24-Lead Ceramic Dual-In-Line Package (D)
Package Number J24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



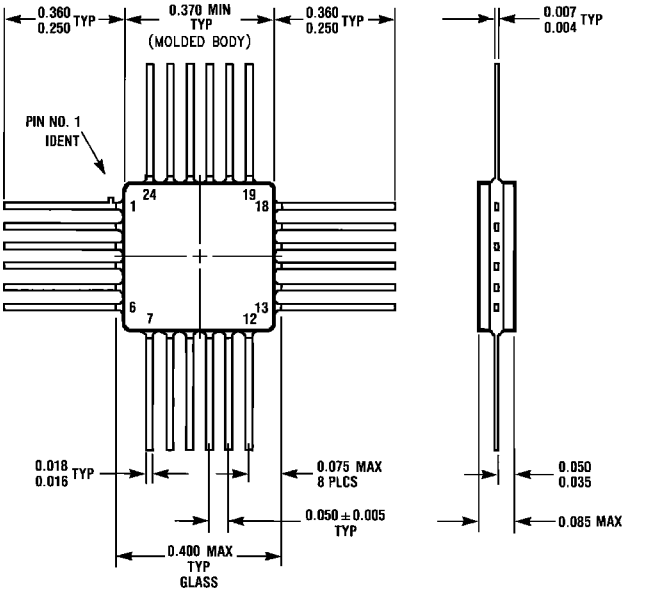
24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Chip Carrier (Q)
Package Number V28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Ceramic Flatpak (F)
Package Number W24B

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com