HARRIS

HC-5512D

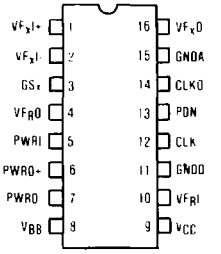
PCM or CVSD Monolithic Filter

Features

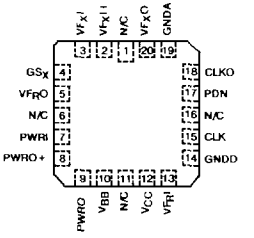
- +5V, -5V Power Supplies
- Low Power Consumption:
  45mW (600Ω 0dBm Load)
  30mW (Power Amps Disabled)
- Power Down Mode: 0.5mW
- No External Anti-Aliasing Components
- Sin x/x Correction in Receive Filter
- 50/60Hz Rejection in Transmit Filter
- TTL and CMOS Compatible Logic
- All Inputs Protected Against Static Discharge Due to Handling
- HC-5512D-2/-8
  Temperature Range..... -55°C to +125°C

Pinouts

HC-5512D (CERAMIC)
TOP VIEW



HC4-5512D (LCC)
TOP VIEW



Description

The HC-5512D filter is a monolithic circuit containing both transmit and receive filters originally designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter lends itself well as a cost effective replacement of a discrete audio input/output filter for CVSD/PCM/ADPCM/PAM speech filtering. Other applications include telephone line cards, modems and multiplexers.

The HC-5512D is a wider specification version of the HC-5512 that meets high-rel requirements and most D3/D4 and CCITT specifications. To meet the Harris high-rel Dash -8 program (-55°C to+125°C), the HC-5512D undergoes a manufacturing process which requires more test, burn-in and inspection than the HC-5512.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

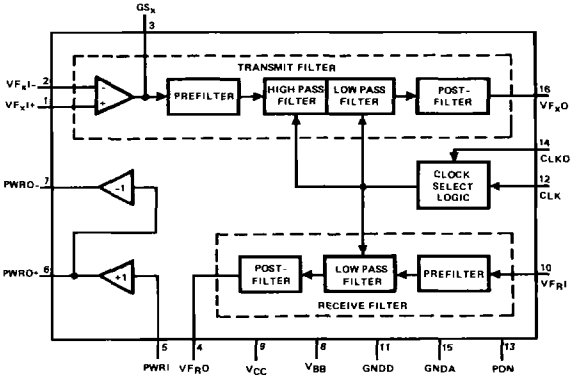
Transmit Filter Stage

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

Receive Filter Stage

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stairstep signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Functional Diagram



CAUTION These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings

Supply Voltages ..... ±7V
Input Voltage ..... ±7V
Output Short-Circuit Duration ..... Continuous
Junction Temperature ..... 175°C

Operating Temperature Range
HC-5512D-2, -8 ..... -55°C to +125°C
HC-5512D -9 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

DC Electrical Specifications Unless Otherwise Noted, T_A = Operating temperature range for min-max parameters, V_{CC} = 5.0V ±5%, Clock Frequency is 1.544MHz. Typical parameters are specified at T_A = +25°C, V_{CC} = +5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	200	µA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode	-200	-50		µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	7.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive	-7.0	-3.0		mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	9.0	mA
I_{BB2}	V_{BB} Operating Current	Note 1	-9.0	-4.6		mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \leq V_{IN} \leq V_{CC}$	-10		10	µA
I_{INP}	Input Current, PDN	$V_{BB} \leq V_{IN} \leq V_{CC}$	-100		100	µA
I_{IN0}	Input Current CLK0	$V_{BB} \leq V_{IN} \leq V_{CC}$ - 0.5V	-10		0	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB} +0.5	V
V_{I10}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC} -0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_XI	Input Leakage Current, VF_XI	$V_{BB} \leq VF_XI \leq V_{CC}$	-100		100	nA
RI_XI	Input Resistance, VF_XI	$V_{BB} \leq VF_XI \leq V_{CC}$	10			MΩ
VOS_XI	Input Offset Voltage, VF_XI	-2.5V $\leq V_{IN} \leq$ +2.5V	-20		20	mV
V_{CM}	Common Mode Range, VF_XI		-2.5		2.5	V
CMRR	Common Mode Rejection Ratio	-2.5V $\leq V_{IN} \leq$ +2.5V	60			dB
PSRR+	Power Supply Rejection of V_{CC}		60			dB
PSRR-	Power Supply Rejection of VBB		60			dB
R_{OL}	Open Loop Output Resistance, GS_X			1		kΩ
R_L	Minimum Load Resistance, GS_X		10			kΩ
C_L	Maximum Load Capacitance, GS_X				100	pF
VO_XI	Output Voltage Swing, GS_X	$R_L \geq$ 10k	-2.5		2.5	V
A_{VOL}	Open Loop Voltage Gain, GS_X	$R_L \geq$ 10k	3000			V/V
F_C	Open Loop Unity Gain Bandwidth, GS_X			2		MHz

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT FILTER (Transmit filter input op amp set to the noninverting unity gain mode, with $VFxI^+$ = 1.09Vrms unless otherwise noted)						
RL_X	Minimum Load Resistance	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_X	Load Capacitance, VF_XO				100	pF
RO_X	Output Resistance, VF_XO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_XO	f = 1kHz, VF_XI^+ = 0Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_XO	Same as above	35			dB
GA_X	Absolute Gain	f = 1kHz	2.8	3.0	3.2	dB
GR_X	Gain Relative to GA_X	Below 50Hz			-35	dB
		50Hz		-41	-35	dB
		60Hz		-35	-30	dB
		200Hz	-1.5		0.15	dB
		300Hz to 3kHz	-0.15		0.15	dB
		3.3kHz	-0.35		0.15	dB
		3.4kHz	-1.0		0.0	dB
		4.0kHz		-15	-10	dB
		4.6kHz and Above			-30	dB
DA_X	Absolute Delay at 1kHz				230	μs
DD_X	Differential Envelope Delay from 1kHz to 2.6kHz				60	μs
DP_X1	Single Frequency Distortion Products				-40	dB
DP_X2	Distortion at Maximum Signal Level	0.16Vrms, 1kHz Signal Applied to VF_XI^+, Gain = 20dB, R_L = 10k			-40	dB
	Level					
NC_X1	Total C Message Noise at VF_XO with V_{IN} = 0				10	dBrnC0
NC_X2	Total C Message Noise at VF_XO with V_{IN} = 0	Gain Setting Op Amp at 20dB, Non-Inverting			10	dBrnC0
GA_XT	Temperature Coefficient of 1kHz Gain			0.0004		dB/°C
GA_XS	Supply Voltage Coefficient of 1kHz Gain			0.01		dB/V
CTR_X	Crosstalk, Receive to Transmit $20 \log \frac{VF_XO}{VF_RO}$	Receive Filter Output = 2.2Vrms, VF_XI^+ = 0Vrms, f = 0.2kHz to 3.4kHz, Measure VF_XO			-60	dB
GR_XL	Gaintracking Relative to GA_X	Output Level = +3dBm0 to -45dBm0	-0.1		0.1	dB
		-50dBm0	-0.15		0.15	dB
		-55dBm0	-0.25		0.25	dB

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x / x filter with an input signal level of 1.54Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-2.5V \leq V_{IN} \leq 2.5V$	-100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	-200		200	mV
GA_R	Absolute Gain	f = 1kHz	-0.2	0	0.2	dB
GR_R	Gain Relative to Gain at 1kHz	Below 300Hz			0.125	dB
		300Hz to 3.0kHz	-0.15		0.15	dB
		3.3kHz	-0.5		0.15	dB
		3.4kHz	-1.0		0.0	dB
		4.0kHz			-10	dB
		4.6kHz and Above			-30	dB
DA_R	Absolute Delay at 1kHz				100	μs
DD_R	Differential Envelope Delay 1kHz to 2.6kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1kHz			-40	dB
DP_R2	Distortion at Maximum Signal Level	2.2Vrms Input to Sin x / x Filter, f = 1kHz, R_L = 10k			-40	dB
NC_R	Total C-Message Noise at VF_RO				10	dBrnC0
GA_RT	Temperature Coefficient of 1kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2Vrms VF_RI = 0Vrms, f = 0.3kHz to 3.4kHz Measure VF_RO			-60	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3dBm0 to -45dBm0	-0.1		0.1	dB
		-50 dBm0	-0.15		0.15	dB
		-55 dBm0 Note 3	-0.25		0.25	dB

8 TELECOM-MUNICATIONS

A.C. Electrical Specifications Unless otherwise specified, typical parameters @ 25°C. Min-Max parameters are over operating temperature range. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-2.5V \leq V_{IN} \leq 2.5V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO + PWRO-	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO + PWRO-				500	pF
GAP+	Gain, PWRI to PWRO+	R_L = 600Ω Connected Between		1		V/V
GAP-	Gain, PWRI to PWRO-	PWRO+ and PWRO-		-1		V/V
		Input Level = 0dBm0 (Note 2)				
GRPL	Gaintracking Relative to 0dBm0	V = 2.05Vrms, R_L = 600Ω	-0.1		0.1	dB
	Output Level	V = 1.75Vrms, R_L = 300Ω (Notes 2,3)	-0.1		0.1	dB
S/DP	Signal/Distortion	V = 2.05Vrms, R_L = 600Ω			-45	dB
		V = 1.75Vrms, R_L = 300Ω (Notes 2,3)			-45	dB
VOSP	Output DC Offset, PWRO + PWRO-	PWRI Connected to GNDA	-50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

NOTES:
1. Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0dBm is delivered to 600Ω connected from PWRO+ to PWRO-.
2. The 0dBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA the 0dBm0 level is 1.43Vrms measured at the amplifier output. For R_L = 300Ω the 0dBm0 level is 1.22Vrms.
3. VF_RO connected to PWRI, input signal applied to VF_RI.

Typical Performance Specifications

TRANSMIT FILTER STAGE

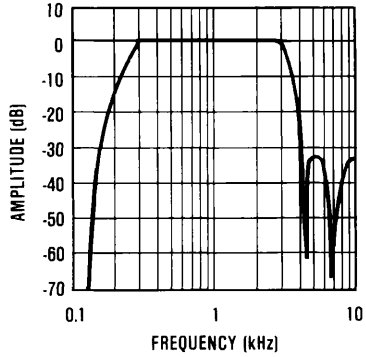


FIGURE 2.

RECEIVE FILTER STAGE

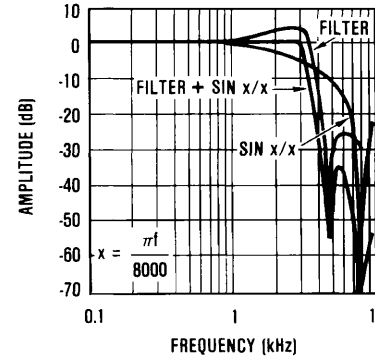


FIGURE 3.

Pin Assignments

PIN # 16-PIN DIP	PIN # 20-PIN LCC	SYMBOL	DESCRIPTION
1	2	VF_XI+	The non-inverting input to the transmit filter stage
2	3	VF_XI-	The inverting input to the transmit filter stage
3	4	GS_X	The output used for gain adjustments of the transmit filter.
4	5	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	7	PWRI	The input to the receive filter differential power amplifier.
6	8	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids
7	9	PWRO-	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	10	V_{BB}	The negative power supply pin. Recommended input is -5V.
9	12	V_{CC}	The positive power supply pin. Recommended input is 5V.
10	13	VF_RI	The input pin for the receive filter stage.
11	14	GNDD	Digital ground input pin. All digital signals are referenced to this pin
12	15	CLK	Master input clock. Input frequency can be selected as 2.048MHz, 1.544MHz or 1.536MHz
13	17	PDN	The input pin used to power down the HC-5512D during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	18	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** — **Connect CLK0 to:** 2048kHz — VCC 1544kHz — GNDD 1536kHz — VBB An internal pull-up is provided.
15	19	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD
16	20	VFxO	The output of the transmit filter stage
	1, 6, 11, 16	NC	No internal connection is made to these pins.

Die Characteristics

Transistor Count 815
Die Dimensions ..... 180 x 129
Substrate Potential ..... +V
Process ..... SAJI CMOS

Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

8 TELECOMMUNICATIONS

Functional Description

The HC-5512D monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (Figure 1). A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ, a voltage gain of greater than 3,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 100pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±2.5V peak to peak signal into a 10kΩ load in parallel with up to 100pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits in PCM applications. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3 and R4 (Figure 4). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

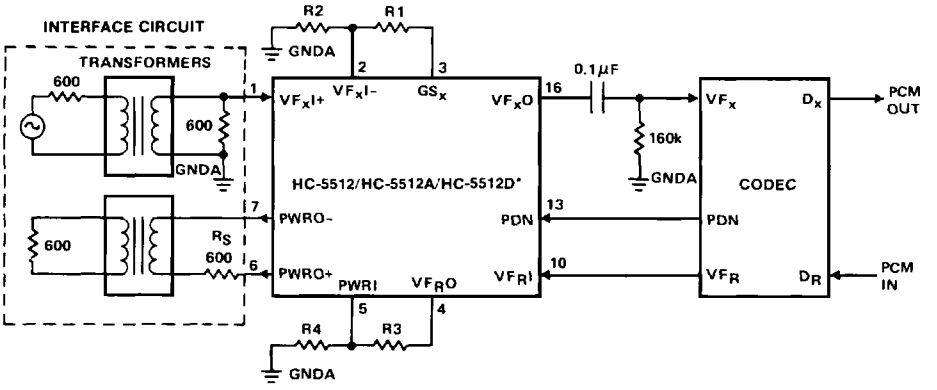
Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to VBB, the power amplifier output will enter a high impedance (three-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to VCC, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and VBB selects 1.536MHz.

Interface Circuit



Note 1 Transmit voltage gain $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 + R2 ≥ 10k)

Note 2 Receive gain $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10k)

Note 3. In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

*Note 4 The HC-5512D may be used in some PCM telephone applications, it does meet most CCITT and D3, D4 specifications for PCM telephone transmission systems.

FIGURE 4.

Interface Circuit for HC-55564 CVSD

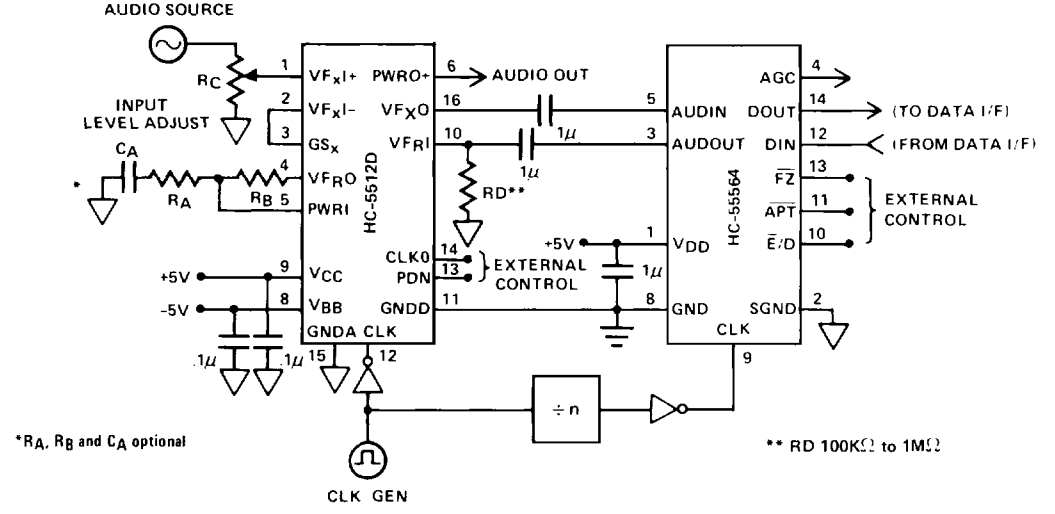


FIGURE 5.

Applications Information

Gain Adjust

Figure 4 shows the signal path interconnections between the HC-5512D and a single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Figure 5 shows the signal path interconnections between the HC-5512D and the HC-55564 CVSD. For the circuit shown, the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. R_A, R_B and C_A form a simple lead/lag filter at the output of the HC-5512D receive filter which introduces a pole and a zero at 3.3kHz to help compensate against the filters' inherent sin x/x characteristic. (See Figure 3). Note that the transmit side of the filter provides an inherent +3dB voltage gain, and the resistor RD, at VFRI causes a voltage loss from audio out to VFRI, owing to the 100kΩ output impedance of the CVSD at audio out. Generally, the higher the RD value used, the more thermal noise introduced to the circuit.

Optimum noise and distortion performance will be obtained for the HC-5512D filter when operated with system peak overload voltages of ±2.5V to ±3.2 at VF_XO and VF_RO. When interfacing to a PCM CODEC or CVSD with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512/12A/12D filter can be used with the CODEC which has a 5.5V peak overload voltage, or with the HC-55564 CVSD which has a 4.0V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC or CVSD output are required in this case.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground of each filter and each CVSD should be connected to digital ground at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC, and each filter and CVSD is recommended. Ground loops should be avoided between GNDA and GNDD, between the GNDA traces of adjacent filters and CODECs, and between the analog ground traces of adjacent filters and CVSDs.