# LOW POWER LCD/CRT VGA CONTROLLER

## ■ DESCRIPTION

The SPC8100FOA is a single chip multi-function Low Power LCD & CRT VGA Controller with an integrated RAMDAC and Liquid Crystal Display interface. The controller's unique architecture allows a fully VGA compatible display on CRT monitors or single- or dual-panel, monochrome or color, passive or active matrix LCD displays without special software drivers or external hardware circuitry.

The target markets for this device are price and space sensitive portable computers or other specialized LCD products where low cost, low power, low component count and a high quality 16 or 64 grey shade VGA image on a 640x480 LCD panel display are the major design considerations.

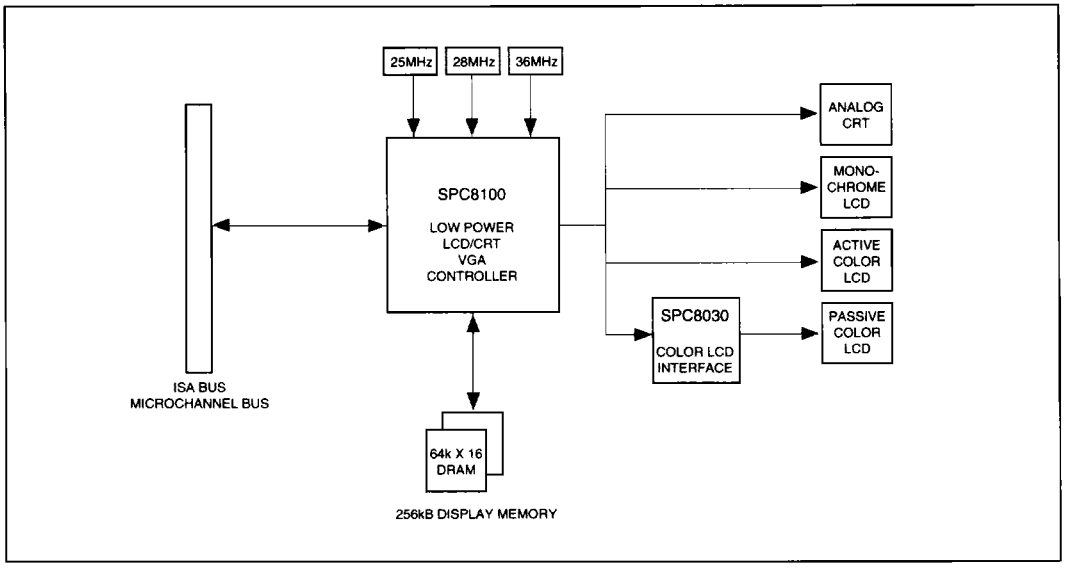
## ■ FEATURES

- Hardware VGA and EGA compatible
- Software CGA, MDA, and Hercules compatible
- 16 bit ISA or Microchannel Bus interface
- Two 64kx16 DRAMs for 256kB display memory
- 16 bit display memory interface
- Two-terminal crystals support
- Four power down modes
- 5.0V low power CMOS
- 144 pin QFP package
- Video BIOS, software drivers, and utilities support
- Internal 256x18bit RAMDAC
- Direct analog CRT monitor drive
- 16 & 64 gray scale LCD panel interface
- 512 color active matrix LCD panel interface
- EL & plasma panel support
- Vertical centering
- Panel power sequencing

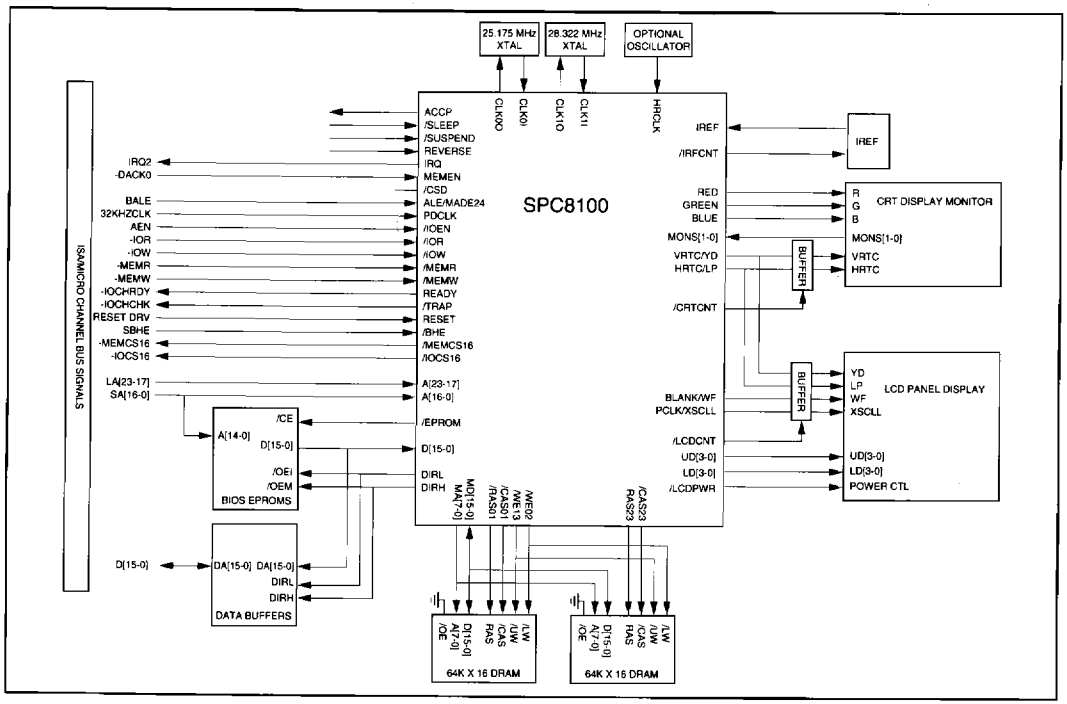
**With Additional SPC8030**

- 512 color passive matrix LCD panel interface
- 44 pin QFP

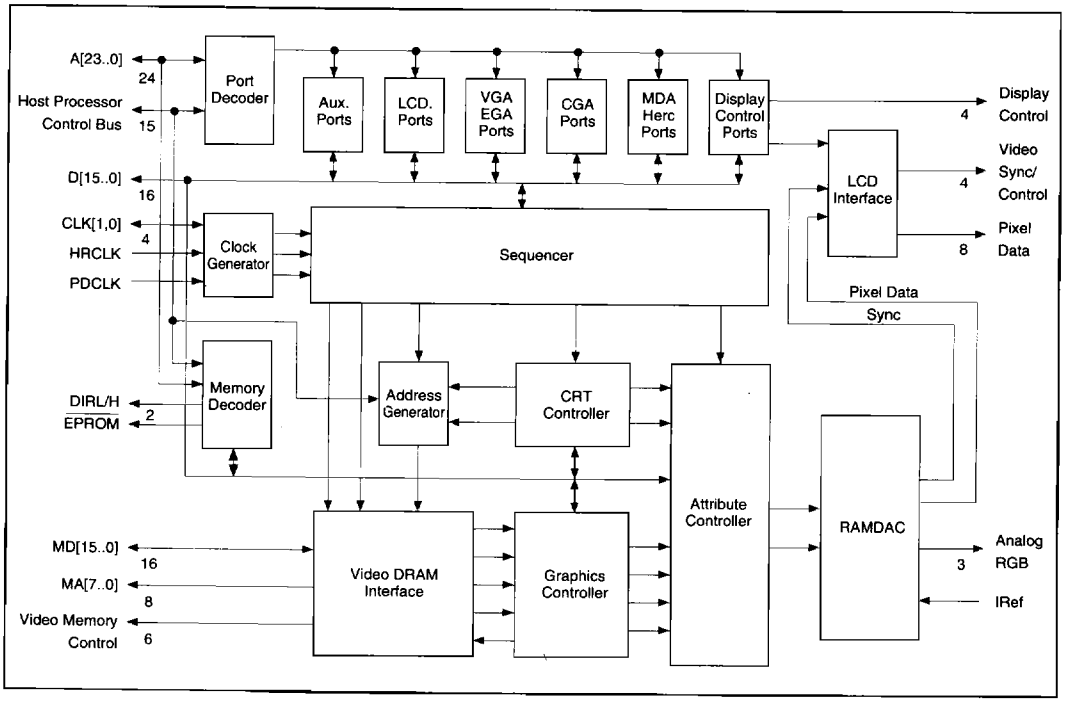
## ■ SYSTEM BLOCK DIAGRAM



## ■ BLOCK DIAGRAM




## ■ FUNCTIONAL BLOCK DESCRIPTION



## ■ FUNCTIONAL BLOCK DESCRIPTION

- **Sequencer**
  The Sequencer generates internal signals to synchronize the operation of the chip. It also generates signals to control the timing of the display memory DRAM. The Sequencer arbitrates between CPU and Video Display (CRT) accesses to the video display memory. The Sequencer contains registers that allow selection of the character font set, control the organization of video memory, and allow write masking of individual planes of memory. CAS-before-RAS DRAM refresh cycles are also controlled by the Sequencer.

- **CRT Controller**
  The CRT Controller generates the horizontal and vertical sync signals for the video display. It also generates character and/or pixel addresses for the display data. It contains registers that allow all the video timing to be programmed. Logic to automatically support Dual Panel LCD displays is also contained in the CRT controller block.

- **Address Generator**
  The Address Generator takes the display addresses from the CRT controller block and converts them into RAS and CAS addresses for the display DRAM, and multiplexes these display accesses with CPU memory accesses.

- **Attributes Controller**
  The Attributes Controller takes in pixel and attribute information from the graphics controller and display memory and formats the data into pixel information which is clocked out from the chip. This block controls display character attributes such as Blink, Underline, and Horizontal Scrolling.

- **Graphics Controller**
  The Graphics Controller supplies display memory data to the Attributes Controller during display time, and provides data translation between the CPU bus and the display memory during CPU read or write access cycles. As well, the graphics controller can do logical operations to the display data as it passes through to the attributes controller.

- **Memory Decoder**
  The Memory Decoder block monitors the CPU bus activity and decodes cycles for the display DRAM, and the external BIOS EPROM chip. It supplies memory access control signals to the Sequencer.

- **Port Decoder**
  The Port Decoder decodes CPU I/O cycles to provide enable and write strobes for the on-chip I/O registers.

- **Auxiliary Ports**
  The Auxiliary Ports are a block of I/O registers used to control all functions of the chip beyond the basic VGA register set. Registers are included for controlling Traps (interrupts), LCD interface circuits, Emulation Modes, extended CRT resolutions, Extended Addressing modes for the chip. Power save control registers and logic are also provided to control the various power down and power save modes of operation.

- **CGA Ports**
  The CGA Ports are a block of I/O registers only used in CGA emulation.

- **VGA/EGA Ports**
  This block contains I/O registers used in VGA and EGA modes, such as the Miscellaneous Output Register, Input status register, etc.

- **Hercules/MDA Ports**
  The Hercules/MDA ports are a block of I/O registers used in Hercules/MDA emulation.

- **Display Control Ports**
  Several control bits are provided to control external logic to enable/disable CRT and LCD display devices.

- **Clock Generation**
  This block contains on-chip circuitry support of 25MHz and 28MHz crystals for standard VGA mode operation, and also allows selection of external clock oscillator sources and optional clocks for high resolution modes and power-down refresh generation.

- **LCD Interface Logic**
  The LCD Interface block converts the CRT display video data from the VGA core logic into LCD display data of up to 64 gray shades using Frame Rate Modulation and dithering. Additionally, this block generates control signals necessary to drive dual-panel or single-panel LCD displays.

- **RAMDAC**
  This block is a VGA-compatible color lookup table-D/A converter. The color lookup table (VGA palette) consists of a memory array of 256 locations of 18 bits each, allowing selection of 256 colors from a possible 256K. The D/A converter consists of 3 six-bit digital to analog converters (one 6 bit D/A for each of R, G, and B) used to drive an analog CRT display monitor.

## ■ FUNCTIONAL DESCRIPTION (cont.)

### ● Power Down Modes

There are four power down modes supported by the SPC8100. Modes 1, 3, and 4 can be initiated by software. Modes 1, 2, and 4 can be initiated by hardware.

1. **Power down mode 1.**
   - Only the 28MHz clock is used to clock internal chip logic. 25MHz oscillator cell itself can be disabled.
   - No CRT display accesses to display memory.
   - Sequencer is dedicated to CPU accesses to/from display memory.
   - Display memory refresh is maintained.
   - I/O read/write allowed.
   - Horizontal and Vertical Retrace output signals maintained.

2. **Power down mode 2.**
   - Only the 28MHz clock is used to clock internal chip logic. 25MHz oscillator cell itself can be disabled.
   - Sequencer is driven by a divided down clock (28/N MHz, where N = 112, 224, 448, and 896)
   - No CRT display accesses to display memory.
   - Sequencer is dedicated to display memory refresh only.
   - No CPU Accesses to/from display memory.
   - I/O read/write allowed.
   - Horizontal and Vertical Retrace output signals maintained.

3. **Power down mode 3.**
   - Both 25MHz and 28MHz clocks are not used; additionally, oscillator cells themselves can be disabled.
   - No CRT display accesses to display memory.
   - No CPU accesses to/from display memory.
   - No display memory refresh.
   - I/O read allowed.
   - I/O write to Auxiliary Registers only (for wake up).
   - Horizontal and Vertical Retrace output signals may be optionally maintained or disabled. If retrace signals are maintained, then the 28MHz oscillator cell must be enabled as it is used in this case by the power-save logic.

4. **Power down mode 4.**
   - Only PDCLK input used to clock essential circuitry (refresh, retrace). Both 25MHz and 28MHz clocks can be disabled.
   - No CRT display accesses to display memory.
   - No CPU accesses to/from display memory.
   - Display memory refresh controlled by clock input pin PDCLK.
   - I/O read allowed.
   - I/O write to Auxiliary Registers only (for wake up).
   - Horizontal and Vertical Retrace output signals maintained (generated from PDCLK input).
   - In Micro Channel configuration, MEMEN is available as an alternate clock source for DRAM refresh, horizontal retrace and vertical retrace.

## ■ VIDEO MODES

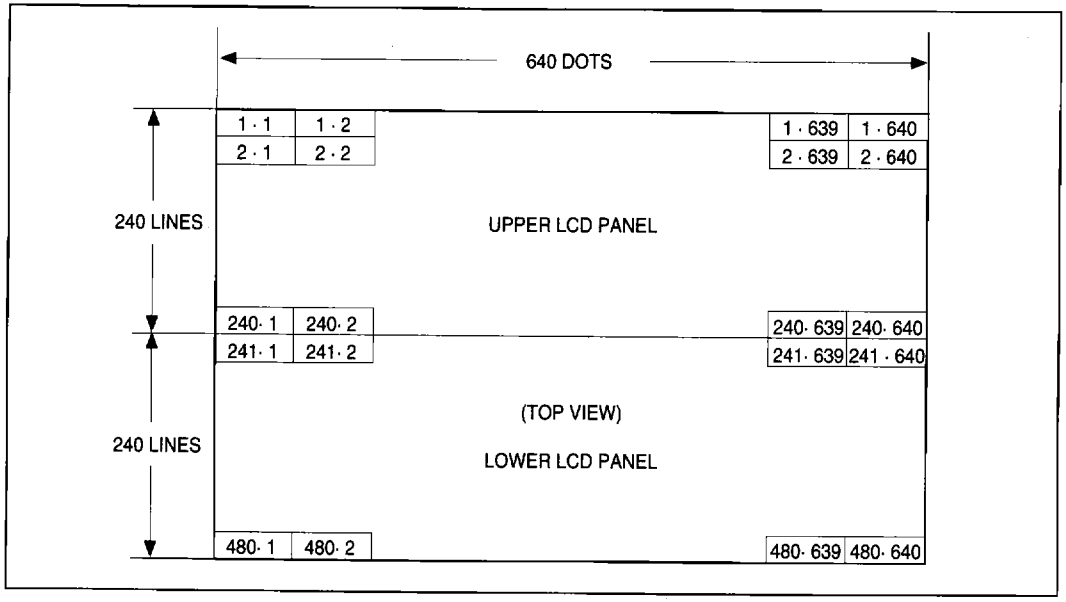
| Mode Number | CRT Font Size | CRT Resolution | Character Resolution | Panel Font Size | Panel Resolution | Analog CRT | Monochrome Passive LCD | Color Active Matrix LCD | Color Passive LCD with SPC8030 |
|---|---|---|---|---|---|---|---|---|---|
| (Hex) | (Pixels) | (Pixels) | (Character) | (Pixels) | (Pixels) | (Colors) | (Grey Shades) | (Colors) | (Colors) |
| 0 | 8x8 | 320x200 | 40x25 | 8x8 | 320x200 | 16 | 16 | 16 | 16 |
| 0+ | 8x14 | 320x350 | 40x25 | 8x14 | 320x350 | 16 | 16 | 16 | 16 |
| 0++ | 9x16 | 360x400 | 40x25 | 8x16 | 320x400 | 16 | 16 | 16 | 16 |
| 1 | 8x8 | 320x200 | 40x25 | 8x8 | 320x200 | 16 | 16 | 16 | 16 |
| 1+ | 8x14 | 320x350 | 40x25 | 8x14 | 320x350 | 16 | 16 | 16 | 16 |
| 1++ | 9x16 | 360x400 | 40x25 | 8x16 | 320x400 | 16 | 16 | 16 | 16 |
| 2 | 8x8 | 640x200 | 80x25 | 8x8 | 640x200 | 16 | 16 | 16 | 16 |
| 2+ | 8x14 | 640x350 | 80x25 | 8x14 | 640x350 | 16 | 16 | 16 | 16 |
| 2++ | 9x16 | 720x400 | 80x25 | 8x16 | 640x400 | 16 | 16 | 16 | 16 |
| 3 | 8x8 | 640x200 | 80x25 | 8x8 | 640x200 | 16 | 16 | 16 | 16 |
| 3+ | 8x14 | 640x350 | 80x25 | 8x14 | 640x350 | 16 | 16 | 16 | 16 |
| 3++ | 9x16 | 720x400 | 80x25 | 8x16 | 640x400 | 16 | 16 | 16 | 16 |
| 4 | — | 320x200 | — | — | 320x200 | 4 | 4 | 4 | 4 |
| 5 | — | 320x200 | — | — | 320x200 | 4 | 4 | 4 | 4 |
| 6 | — | 640x200 | — | — | 640x200 | 2 | 2 | 2 | 2 |
| 7 | 9x14 | 720x350 | 80x25 | 8x14 | 640x350 | 2 | 2 | 2 | 2 |
| 7+ | 9x16 | 720x400 | 80x25 | 8x16 | 640x400 | 2 | 2 | 2 | 2 |
| 0D | — | 320x200 | — | — | 320x200 | 16 | 16 | 16 | 16 |
| 0E | — | 640x200 | — | — | 640x200 | 16 | 16 | 16 | 16 |
| 0F | — | 640x350 | — | — | 640x350 | 2 | 2 | 2 | 2 |
| 10 | — | 640x350 | — | — | 640x350 | 16 | 16 | 16 | 16 |
| 11 | — | 640x480 | — | — | 640x480 | 2 | 2 | 2 | 2 |
| 12 | — | 640x480 | — | — | 640x480 | 16 | 16 | 16 | 16 |
| 13 | — | 320x200 | — | — | 320x200 | 256 | 64 | 256 | 256 |
| 6A | — | 800x600 | — | — | — | 16* | — | — | — |
| 100 | — | 640x400 | — | — | — | — | — | — | — |
| 101 | — | 640x480 | — | — | — | — | — | — | — |
| 102 | — | 800x600 | — | — | — | 16* | — | — | — |
| 109 | 8x16 | 1056x400 | 132x25 | — | — | 16 | — | — | — |
| 10B | 8x8 | 1056x400 | 132x50 | — | — | 16 | — | — | — |
| 10C | 8x8 | 1056x480 | 132x60 | — | — | 16 | — | — | — |
| Hercules | — | 720x348 | — | — | 640x348 | 2 | 2 | 2 | 2 |

*** 36.0 MHz oscillator required**

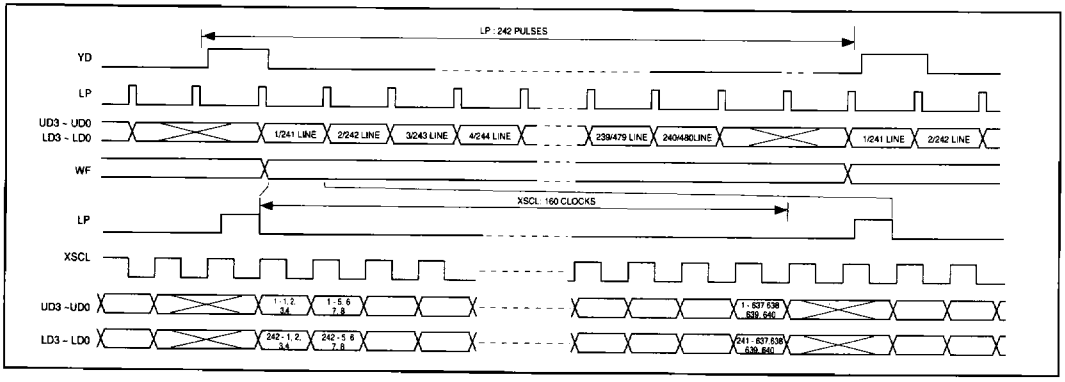
**— Not available or not applicable**

## ● Monochrome LCD Panels

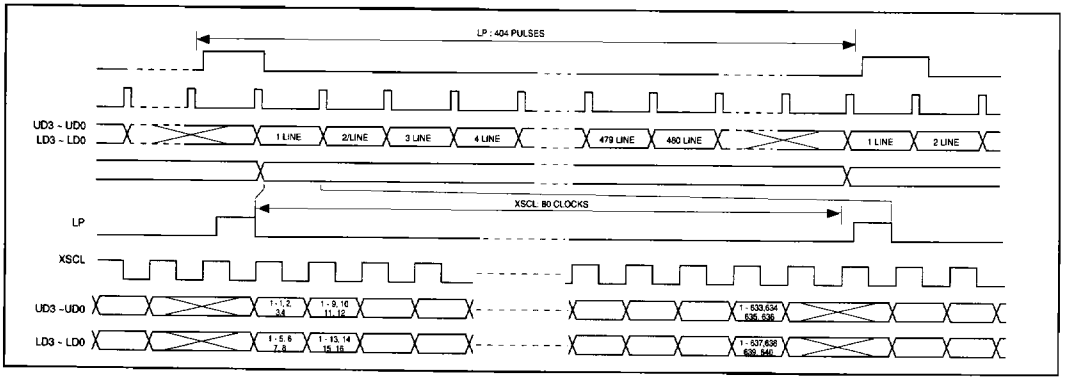
The SPC8100 supports both dual and single panel monochrome passive matrix LCD panels.



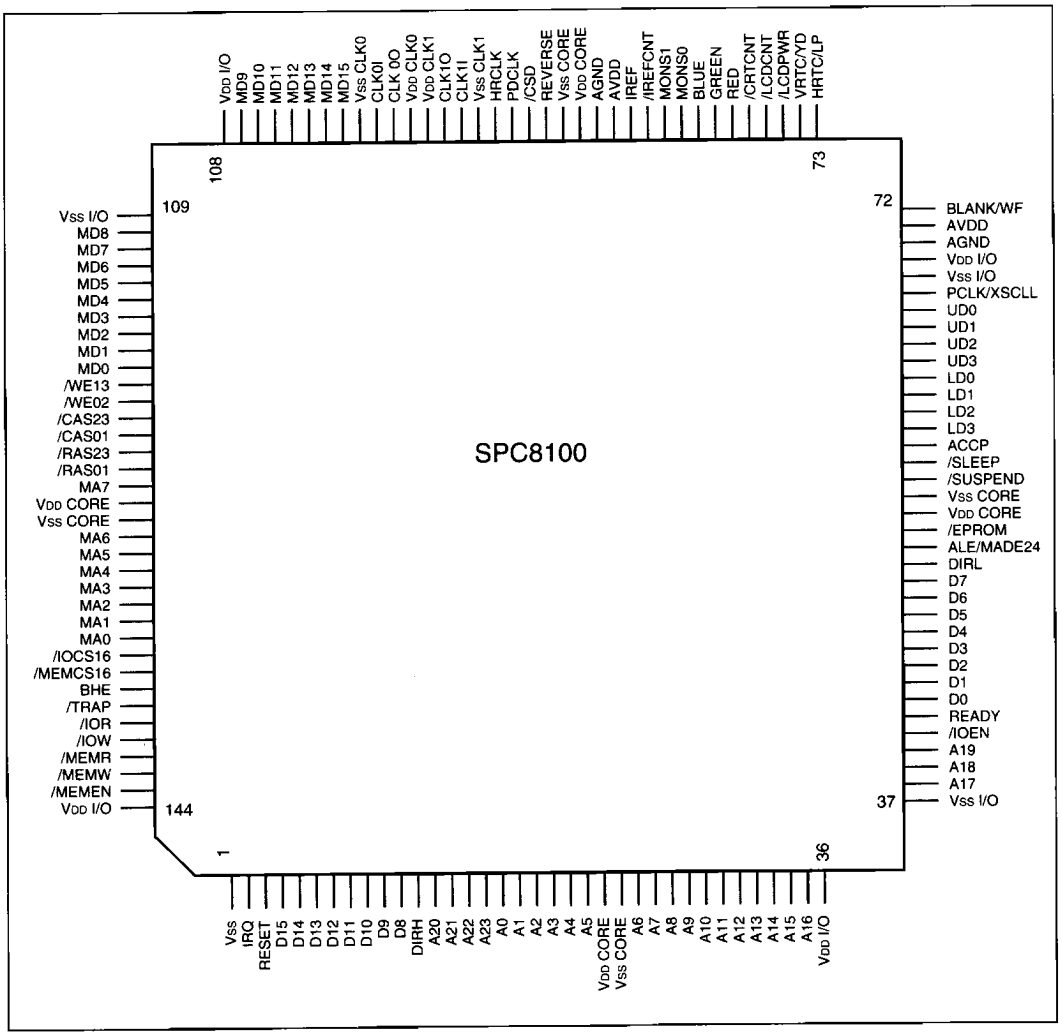

1) Dual-panel Dual-drive



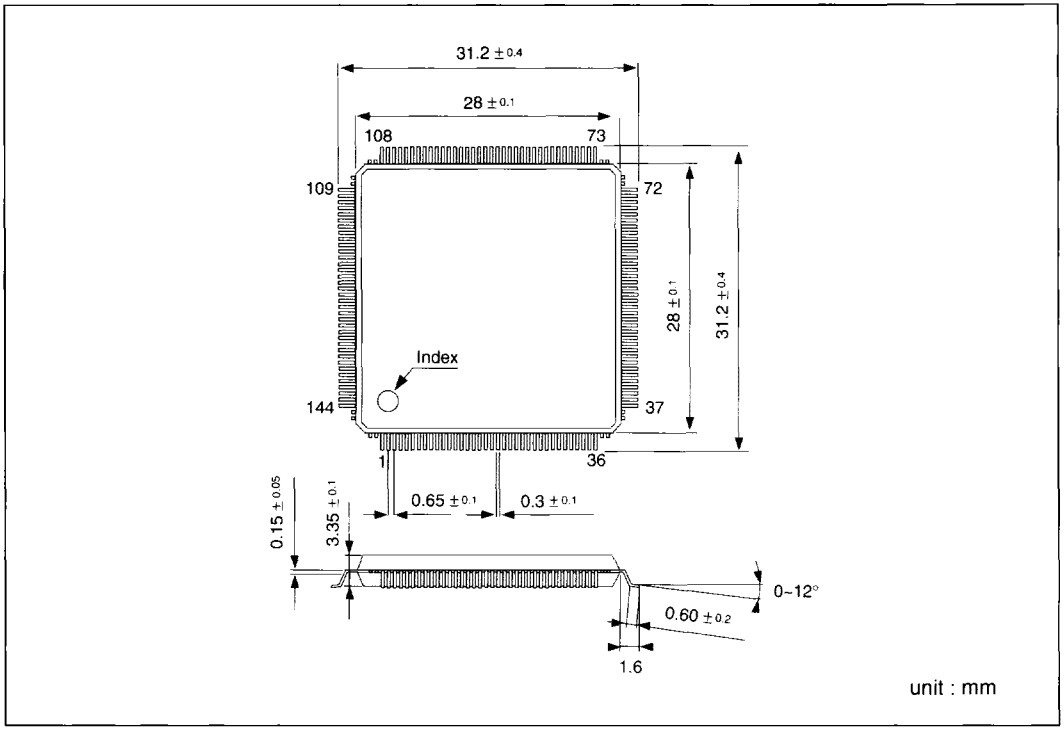

2) Single-panel Single-drive



## ■ PIN CONFIGURATION



## ■ PACKAGE DIMENSIONS
**144 PIN QFP**




**Comprehensive Support Tools:**

S-MOS Systems provides to the system designer and computer OEM manufacturer a complete set of resources and tools for the development of VGA Graphics Systems.

**Evaluation/Demonstration Board:**

- Assembled and fully tested Graphics Evaluation board
- Schematic of Evaluation/Demo board
- Parts List
- Installation Guide
- Multiple Flat-Panel Adaptor Board
- Cabling and power supply terminals

**VGA Chip Set Documentation:**

- Pamphlets
- Device Data Sheets
- Technical Manuals
- Application notes
- Programmer's Manual

**Software:**

- Demonstration disk
- Video BIOS on EPROM or Floppy
- OEM Utilities
- User Utilities
- Evaluation Software

**Application Engineering Support:**

In order to help customers implement the Dragon Chip Set in their design, S-MOS offers training, technical support and the following services.

- Sales Technical Support
- Customer Training
- Design Assistance
- OEM and Application Support
- Technical Bulletins
- BIOS Software Documentation
- Application Program Driver Software
- Text or Drawing Support
- Consultant Referral