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**DATA SHEET**

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**HC 3052/HC 3053  
HC 3054/HC 3057**

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**MONOLITHIC CMOS SERIAL INTERFACE  
COFIDEC FAMILY**

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**FEATURES**

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**COMPLETE CODEC/FILTER (COFIDEC) FAMILY**

- HC 3052 -  $\mu$ -LAW WITH SHORT FRAME SIGNALING (18 PIN)
- HC 3053 -  $\mu$ -LAW WITH BOTH SHORT AND LONG FRAME SIGNALING (20 PIN)
- HC 3054 -  $\mu$ -LAW WITHOUT SIGNALING (16 PIN)
- HC 3057 - A-LAW (16 PIN)
- LOW OPERATION POWER (60 mW typical)

- LOW STANDBY POWER (1 mW typical)
- $\pm 5$  V POWER SUPPLIES
- MEETS OR EXCEED ALL D3/D4 AND CCITT SPECIFICATIONS
- TTL COMPATIBLE DIGITAL INTERFACES
- PCM DATA SERIAL INPUT/OUTPUT
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION

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**DESCRIPTION**

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The MHS CODEC/FILTER (COFIDEC) family includes A-Law and  $\mu$ -Law monolithic CODEC/FILTERS implemented with double-poly CMOS technology.

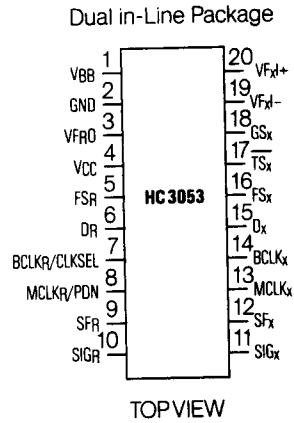
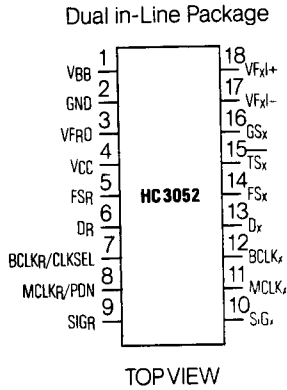
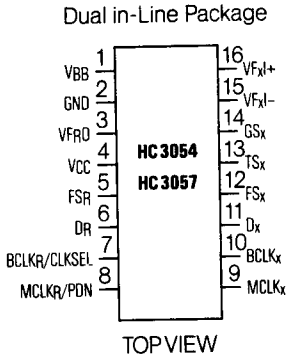
**The transmit side of the device consists of:**

- an amplifier with external gain adjustment
- an RC active prefilter to eliminate high frequency noise
- a switched capacitor band-pass filter including a notch filter at 55 Hz to reject signals below 200 Hz and above 3400 Hz
- a charge redistribution coder which samples and encodes filtered signal in the companded  $\mu$ -Law or A-Law PCM format
- a precision voltage reference
- an internal auto-zero network to cancel the transmit offset.

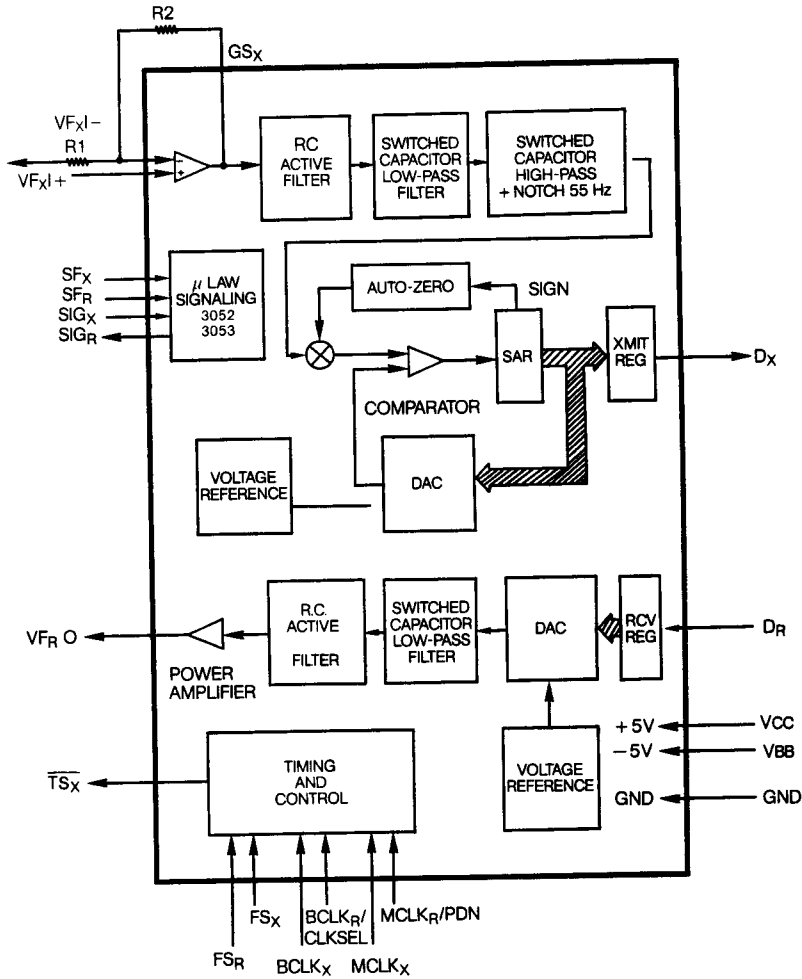
**The receive side of the device consists of:**

- an expanding decoder (A-Law or  $\mu$ -Law) to reconstruct the analog signal
  - a switched-capacitor low-pass filter which corrects for the  $\sin x/x$  response of the decoder output and rejects signals above 3400 Hz
  - an RC active filter followed by a single ended power amplifier able to drive a 600 ohms load
  - a precision voltage reference.
- The PCM word is transmitted/received in a serial format compatible with industry standard.
- The device is operated with two (transmit and receive) master clocks (1.536 MHz, 1.544 MHz or 2.048 MHz) which may be asynchronous.
- Also required are transmit and receive bit clocks which may vary from 64 KHz to 2.048 MHz and transmit and receive frame sync pulses.

**PINOUTS**



**FUNCTIONAL DIAGRAM**



**PIN DESCRIPTION**

HC 3052 PIN NO	HC 3053 PIN NO	HC 3054 HC 3057 PIN NO	NAME	FUNCTION
1	1	1	V <sub>BB</sub>	Negative power supply V <sub>BB</sub> = -5 V.
2	2	2	GND	Ground.
3	3	3	V <sub>FRO</sub>	Analog output of the receive filter.
4	4	4	V <sub>CC</sub>	Positive power supply V <sub>CC</sub> = +5 V.
5	5	5	F <sub>SR</sub>	Receive frame sync pulse. An 8 KHz pulse train which enables the PCM word to be shifted into the receive register.
6	6	6	D <sub>R</sub>	Receive data input. The receive register clocks in D <sub>R</sub> input with bit clock falling edge following an F <sub>SR</sub> rising edge.
7	7	7	BCLK <sub>R</sub> & CLKSEL	Bit clock which shifts D <sub>R</sub> input into the receive register. May vary from 64 KHz to 2.048 MHz. Alternatively may be a clock selection in synchronous mode. See table in functional description for synchronous operation.
8	8	8	MCLK <sub>R</sub> & PDN	Receive master clock must be 1.536 or 1.544 MHz. May be asynchronous with MCLK <sub>X</sub> and BCLK <sub>R</sub> . If MCLK <sub>R</sub> is low, the COFIDEC operates in synchronous mode. If MCLK <sub>R</sub> is tied high, the COFIDEC is powered down.
	9		S <sub>FR</sub>	When high during F <sub>SR</sub> , S <sub>FR</sub> indicates a receive signaling frame in long frame mode.
9	10		SIG <sub>R</sub>	The signaling bit appears at this output after each receive signaling frame.
10	11		SIG <sub>X</sub>	Signaling data input. This input is inserted in place of LSB of PCM word during signaling frame.
	12		S <sub>FX</sub>	When high during F <sub>SX</sub> , S <sub>FX</sub> indicates a transmit signaling frame in long frame mode.
11	13	9	MCLK <sub>X</sub>	Transmit master clock. Must be 1.536, 1.544 or 2.048 MHz. May be asynchronous with MCLK <sub>R</sub> . See table in functional description for synchronous operation.
12	14	10	BCLK <sub>X</sub>	Bit clock. May vary from 64 KHz to 2.048 MHz, but must be synchronous with MCLK <sub>X</sub> .
13	15	11	D <sub>X</sub>	Three-state PCM data output enabled by F <sub>SX</sub> .
14	16	12	F <sub>SX</sub>	Transmit frame sync pulse. An 8 KHz pulse train which enables the PCM word to be shifted out through D <sub>X</sub> with BCLK <sub>X</sub> .
15	17	13	T <sub>SX</sub>	Open drain output. Pulled down during time slot.
16	18	14	G <sub>SX</sub>	Analog output of transmit amplifier used to set the gain.
17	19	15	V <sub>FX</sub> I-	Inverting input of transmit amplifier.
18	20	16	V <sub>FX</sub> I+	Non inverting input of transmit amplifier.



**FUNCTIONAL DESCRIPTION**

**POWER-UP**

When power is first applied, power-on reset circuitry initializes the COFIDEC and places it into a power-down state. All non-essential circuits are deactivated and the  $D_x$  and  $V_{FRO}$  outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the  $MCLK_R$ /PDN pin and  $FS_x$  and/or  $FS_R$  pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the  $MCLK_R$ /PDN pin high ; the alternative is to hold both  $FS_x$  and  $FS_R$  inputs continuously low - the device will power-down approximately 2 ms after the last  $FS_x$  or  $FS_R$  pulse. Power-up will occur on the first  $FS_x$  or  $FS_R$  pulse. The three state PCM data output,  $D_x$ , will remain in the high impedance state until the second  $FS_x$  pulse.

**SYNCHRONOUS OPERATION**

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to  $MCLK_x$  and the  $MCLK_R$ /PDN pin can be used as a power-down control. A low level on  $MCLK_R$ /PDN powers up the device and a high level powers down the device. In either case,  $MCLK_x$  will be selected as the master clock for both the transmit and receive circuits.

A bit clock must also be applied to  $BCLK_x$  and the  $BCLK_R$ /CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.554 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the  $BCLK_R$ /CLKSEL pin,  $BCLK_x$  will be selected as the bit clock for both the transmit and receive directions. *Table 1* indicates the frequencies of operation which can be selected, depending on the state of  $BCLK_R$ /CLKSEL. In this synchronous mode, the bit clock,  $BCLK_x$ , may be from 64 KHz to 2.048 MHz, but must be synchronous with  $MCLK_x$ .

Each  $FS_x$  pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled  $D_x$  output on the positive edge of  $BCLK_x$ . After 8 bit clock periods, the three state  $D_x$  output is returned to a high impedance state. With an  $FS_R$  pulse, PCM data is latched via the  $D_R$  input on the negative edge of  $BCLK_x$  (or  $BCLK_R$  if running) :  $FS_x$  and  $FS_R$  must be synchronous with  $MCLK_x/R$ .

**ASYNCHRONOUS OPERATION**

Two asynchronous modes are allowed with excellent transmission performance :

- 1)  $MCLK_R$  is fully independent of  $MCLK_x$  and must be 2.048 MHz for HC 3057 (A law) and 1.544 or 1.536 MHz for HC 3052/3053/3054 ( $\mu$  law) (freq  $MCLK_x$  = freq  $MCLK_R \pm 50$  ppm).
- 2) If required,  $MCLK_x$  can be used as a master clock for both transmit and receive sections by applying static logic levels to the  $MCLK_R$ /PDN pin. In both modes,  $BCLK_x$  and  $BCLK_R$  may operate from 64 KHz to 2.048 MHz.  $BCLK_x$  must be synchronous

**Table 1 - Selection of Master Clock Frequencies**

BCLK <sub>R</sub> / CLKSEL	Master Clock Frequency Selected	
	HC 3057	HC 3052 HC 3053 HC 3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz 2.048 MHz
0	1.536MHz or 1.544 MHz	1.536 MHz or 1.544 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

with  $MCLK_x$ , but  $BCLK_R$  may be asynchronous with  $MCLK_R$  (freq  $BCLK_R$  = freq  $MCLK_R \pm 50$  ppm). The degradation of the total signal to distortion ratio under all permitted asynchronous conditions does not exceed 0.5 dB as compared to the same measurement made with fully synchronous clocks.

**SHORT FRAME SYNC OPERATION**

The COFIDEC can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses,  $FS_x$  and  $FS_R$ , must be one bit clock period long, with timing relationships specified in *Figure 2*. With  $FS_x$  high during a falling edge of  $BCLK_x$ , the next rising edge of  $BCLK_x$  enables the  $D_x$  three state output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the  $D_x$  output. With  $FS_R$  high during a falling edge of  $BCLK_R$  ( $BCLK_x$  in synchronous mode), the next falling edge of  $BCLK_R$  latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

**LONG FRAME SYNC OPERATION**

To use the long frame mode, both the frame sync pulses,  $FS_x$  and  $FS_R$ , must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync,  $FS_x$ , the COFIDEC will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The  $D_x$  three state output buffer is enabled with the rising edge of  $FS_x$  or the rising edge of  $BCLK_x$ , whichever comes later, and the first bit clocked out is the sign bit. The following seven  $BCLK_x$  rising edges clock out the remaining seven bits. The  $D_x$  output is disabled by the falling  $BCLK_x$  edge following the eighth rising edge, or by  $FS_x$  going low, whichever comes later. A rising edge on the receive frame sync pulse,  $FS_R$ , will cause the PCM data at  $D_R$  to be latched in on the next eight falling edges of  $BCLK_R$  ( $BCLK_x$  in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

**SIGNALING**

The HC 3052 and HC 3053  $\mu$ -law COFIDECs contain circuitry to insert and extract signaling information in the PCM data stream. The HC 3052 is intended for short frame sync applications, and the HC 3053 for long frame sync applications, although the HC 3053 may also be used in short frame sync applications. The HC 3054 and HC 3057 have no provision for signaling. Signaling for the HC 3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in Figure 2. With  $SIG_X$  two bit clock periods long, the data present at  $SIG_X$  input will be inserted as the LSB in the PCM data transmitted during that frame. With  $SF_R$  two bit clock periods long, the LSB of the PCM data read into the  $D_R$  input will be latched and appear on the  $SIG_R$  output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "1/2" to minimize noise and distortion. This short frame signaling may also be implemented using the HC 3053, providing  $SF_R$  and  $SF_X$  are left open circuit or tied low. The HC 3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the HC 3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the HC 3052. For long frame signaling, two additional frame sync pulses are required,  $SF_X$  and  $SF_R$ , which indicate transmit and receive signaling frames, respectively. With an  $SF_X$  signaling frame sync, the data present at the  $SIG_X$  input will be inserted as the LSB in the PCM data transmitted during that frame. With an  $SF_R$  signaling frame sync, the LSB of the PCM data at  $D_R$  will be latched and appear on the  $SIG_R$  output pin until the

next signaling frame. The decoder will also do the "1/2" step interpretation to compensate for the loss of the LSB.

**TRANSMIT SECTION**

The input of the transmit section is an operational amplifier whose gain can be externally adjusted. This amplifier exhibits low noise, wide bandwidth and low offset voltage (1mV typical). The input amplifier drives an antialiasing RC active filter. The switched capacitor bandpass filter is split into a 5th order elliptic low-pass filter and a 3rd order elliptic high-pass filter which includes a 55 Hz notch filter to guarantee excellent line (50 or 60 Hz) rejection. The structure of each filter is fully differential so that their performance is not affected by parasitic elements. The A/D converter is of a companding type according to A (HC 3057) or  $\mu$  (HC 3052/3053/3054) coding laws.

**RECEIVE SECTION**

The receive section includes an expanding D/A converter according to A (HC 3057) or  $\mu$  (HC 3052/3053/3054) coding laws. The decoder is followed by a 5th order switched capacitor low-pass filter and an RC active filter.

As for the transmit part, the filters are fully differential. The output amplifier has a unity gain and can drive a 600  $\Omega$ /500 pF load.

Separately trimmed voltage references are provided for transmit and receive sections respectively. Clocking circuits and internal power supplies are also fully independent. This arrangement greatly reduces crosstalk between the transmit and receive blocks and improves performance.



**ELECTRICAL SPECIFICATIONS**

Operating Temperature Range -25 °C to 80 °C  
 Storage Temperature Range -65 °C to 150 °C  
 Lead Temperature (Soldering 10 seconds) 300 °C

**ABSOLUTE MAXIMUM RATINGS**

V<sub>CC</sub> to GND -0.3V to 7V  
 V<sub>BB</sub> to GND +0.3V to -7V  
 Voltage at any Digital Input or Output V<sub>CC</sub> + 0.3V to GND - 0.3V  
 Voltage at any Analog Input or Output V<sub>CC</sub> + 0.3V to V<sub>BB</sub> - 0.3V

**ELECTRICAL CHARACTERISTICS**

Unless otherwise noted: V<sub>CC</sub> = 5.0V ± 5% V<sub>BB</sub> = 5V ± 5% GND = 0V  
 T<sub>A</sub> = 0 °C to 70 °C: typical characteristics specified at V<sub>CC</sub> = 5.0V, V<sub>BB</sub> = -5.0V, T<sub>A</sub> = 25 °C: all signals are referenced to GND

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INTERFACE</b>						
V <sub>IL</sub>	Input Low Voltage				0.6	V
V <sub>IH</sub>	Input High Voltage		2.2			V
V <sub>OL</sub>	Output Low Voltage	D <sub>X</sub> , I <sub>L</sub> = 5.0mA S <sub>IGR</sub> , I <sub>L</sub> = 1.0mA T <sub>SX</sub> , I <sub>L</sub> = 3.2mA, Open Drain			0.4 0.4 0.4	V V V
V <sub>OH</sub>	Output High Voltage	D <sub>X</sub> , I <sub>L</sub> = -5.0mA S <sub>IGR</sub> , I <sub>L</sub> = -1.0mA	2.4 2.4			V V
I <sub>IL</sub>	Input Low Current (Note 1)	GND ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> . All Digital Inputs	-10		10	μA
I <sub>IH</sub>	Input High Current (Note 1)	V <sub>IH</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10		10	μA
I <sub>OZ</sub>	Output Current in High Impedance State	D <sub>X</sub> , GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10		10	μA
<b>ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)</b>						
I <sub>LXA</sub>	Input Leakage Current	-2.5V ≤ V <sub>s</sub> ≤ +2.5V, V <sub>FxI</sub> + or V <sub>FxI</sub> -	-200		200	nA
R <sub>IXA</sub>	Input Resistance	-2.5V ≤ V <sub>s</sub> ≤ +2.5V, V <sub>FxI</sub> + or V <sub>FxI</sub> -	10			MΩ
R <sub>OXA</sub>	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R <sub>LXA</sub>	Load Resistance	G <sub>SX</sub>	10			kΩ
C <sub>LXA</sub>	Load Capacitance	G <sub>SX</sub>			50	pF
V <sub>OXA</sub>	Output Level	G <sub>SX</sub> R <sub>L</sub> = 10k Ω	±2.8	±4.2		V
A <sub>VXA</sub>	Voltage Gain	V <sub>FxI</sub> + to G <sub>SX</sub>	5000			VV
F <sub>UXA</sub>	Unity Gain Bandwidth		1	2		MHz
V <sub>OSXA</sub>	Offset Voltage		-20	1	20	mV
V <sub>CMXA</sub>	Common-Mode Voltage		-2.5		+2.5	V
CMRR <sub>XA</sub>	Common-Mode-Rejection Ratio		60	80		dB
PSRR <sub>XA</sub>	Power Supply Rejection Ratio		60	70		dB
<b>ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)</b>						
R <sub>O<sub>RF</sub></sub>	Output Resistance	Pin V <sub>FRO</sub>		1	3	Ω
R <sub>L<sub>RF</sub></sub>	Load Resistance	V <sub>FRO</sub> = ± 2.5V	600			Ω
C <sub>L<sub>RF</sub></sub>	Load Capacitance				500	pF
V <sub>OS<sub>RO</sub></sub>	Output DC Offset Voltage		-100		100	mV
<b>POWER DISSIPATION (ALL DEVICES)</b>						
I <sub>CCO</sub>	Power-Down Current			0.15	0.5	mA
I <sub>BBO</sub>	Power-Down Current			0.05	0.3	mA
I <sub>CC1</sub>	Active Current			6	9	mA
I <sub>BB1</sub>	Active Current			6	9	mA

**Note 1:** SF<sub>x</sub>, SF<sub>R</sub>: Internal pull down (2μ A typical) - BCLK<sub>R</sub>: Internal pull up (2μ A typical)

**TRANSMISSION CHARACTERISTICS (ALL DEVICES)**

Unless otherwise specified:  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = OV$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm0}$ , transmit input amplifier connected for unity-gain non-inverting.

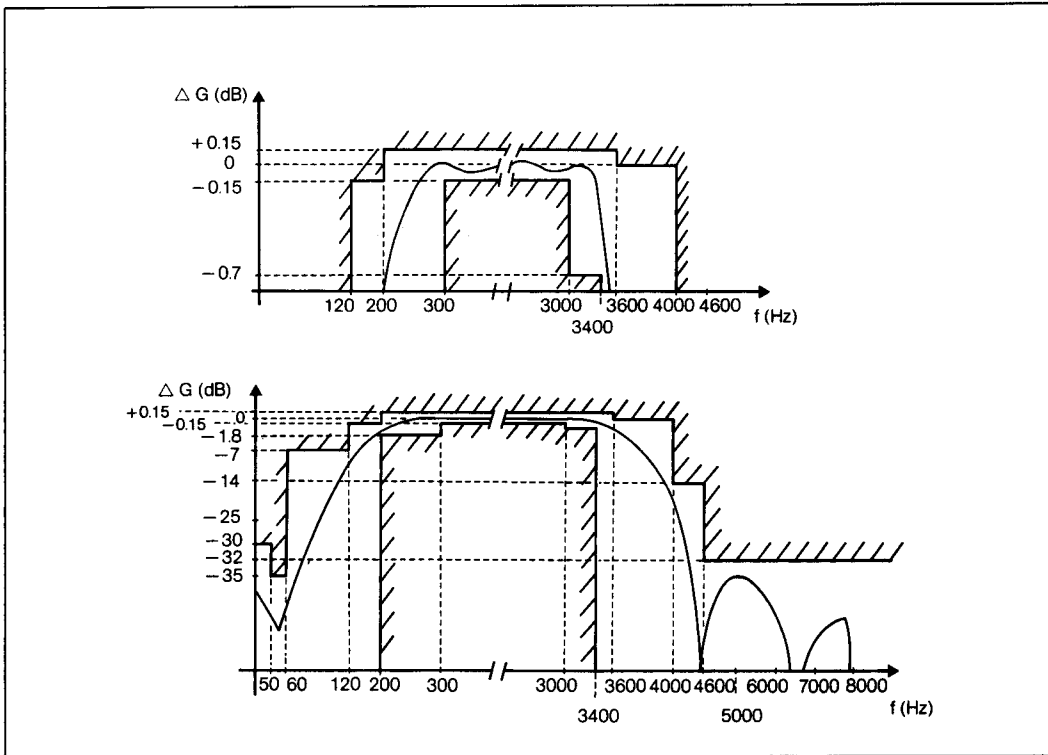
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AMPLITUDE RESPONSE</b>						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600 $\Omega$ ). 0 dBm0 (all devices)		1.2277		Vrms
	Max Overload Levels	HC 3052, HC 3053, HC 3054 (3.17 dBm0) HC 3057 (3.14 dBm0)		2.501 2.492		V <sub>DC</sub> V <sub>DC</sub>
GXA	Transmit Gain, Absolute	$T_A = 25\text{ }^\circ\text{C}$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input at $GS_X = 0\text{ dBm0}$ at 1020 Hz	-0.15		0.15	dB
GXATV	Absolute Transmit Gain Variation with Temperature and Supply Voltage	$T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ $V_{CC} = 5V \pm 5\%$ , $V_{BB} = -5V \pm 5\%$			$\pm 0.15$	dB
GXRL	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level 10 dBm0 $V_{FX}   + 40\text{ dBm0}$ to $+ 3\text{ dBm0}$ $V_{FX}   + 50\text{ dBm0}$ to $40\text{ dBm0}$ $V_{FX}   + 55\text{ dBm0}$ to $50\text{ dBm0}$	0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
GRA	Receive Gain, Absolute	$T_A = 25\text{ }^\circ\text{C}$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	-0.15		0.15	dB
GRATV	Absolute receive Gain Variation with Temperature and Supply Voltage	$T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ $V_{CC} = 5V \pm 5\%$ $V_{BB} \pm 5V \pm 5\%$			$\pm 0.15$	dB
GRRL	Receive Gain Variations with Level	Sinusoidal Test Method : Reference Input PCM Code Corresponds to an ideally Encoded -10 dBm0 Signal PCM Level = -40 dBm0 to $+ 3\text{ dBm0}$ PCM Level = -50 dBm0 to $- 40\text{ dBm0}$ PCM Level = -55 dBm0 to $= 50\text{ dBm0}$	-0.2 -0.4 -1.2		+0.2 +0.4 +1.2	dB dB dB
VRO	Receive Output Drive Level	$R_L = 600\ \Omega$	2.5		2.5	V
<b>ENVELOPE DELAY DISTORTION WITH FREQUENCY</b>						
DXA	Transmit Delay, Absolute	$f = 1600\text{ Hz}$		290	315	$\mu\text{s}$
DXR	Transmit Delay, Relative to DXA	$f = 500\text{ Hz} - 600\text{ Hz}$		140	220	$\mu\text{s}$
		$f = 600\text{ Hz} - 800\text{ Hz}$		100	145	$\mu\text{s}$
		$f = 800\text{ Hz} - 1000\text{ Hz}$		50	75	$\mu\text{s}$
		$f = 1000\text{ Hz} - 1600\text{ Hz}$		20	50	$\mu\text{s}$
		$f = 1600\text{ Hz} - 2600\text{ Hz}$		60	100	$\mu\text{s}$
		$f = 2600\text{ Hz} - 2800\text{ Hz}$		80	110	$\mu\text{s}$
		$f = 2800\text{ Hz} - 3000\text{ Hz}$		140	200	$\mu\text{s}$
DRA	Receive Delay, Absolute	$f = 750\text{ Hz}$		160	180	$\mu\text{s}$
DRR	Receive Delay, Relative to DRA	$f = 500\text{ Hz} - 1600\text{ Hz}$		40	60	$\mu\text{s}$
		$f = 1600\text{ Hz} - 2600\text{ Hz}$		90	120	$\mu\text{s}$
		$f = 2600\text{ Hz} - 2800\text{ Hz}$		120	140	$\mu\text{s}$
		$f = 2800\text{ Hz} - 3000\text{ Hz}$		140	175	$\mu\text{s}$

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**TRANSMISSION CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5\text{V} \pm 5\%$ ,  $V_{BB}=-5\text{V} \pm 5\%$ ,  $GND=0\text{V}$ ,  $f=1.02\text{ kHz}$ ,  $V_{IN}=0\text{ dBm}$ , transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>TRANSMIT SECTION TRANSFER CHARACTERISTICS</b>						
GXR	Transmit Gain Relative to Gain at 820 Hz (0dBm0)	f = 50 Hz - 60 Hz			-35	dB
		f = 60 Hz - 120 Hz			-7	dB
		f = 120 Hz - 200 Hz			-0.15	dB
		f = 200 Hz - 300 Hz		-1.8	+0.15	dB
		f = 300 Hz - 3000 Hz		-0.15	+0.15	dB
		f = 3000 Hz - 3400 Hz		-0.7	+0.15	dB
		f = 3400 Hz - 3600 Hz			+0.15	dB
		f = 3600 Hz - 4000 Hz			0	dB
		f = 4000 Hz - 4600 Hz			-14	dB
f = 4600 Hz and Up			-32	dB		

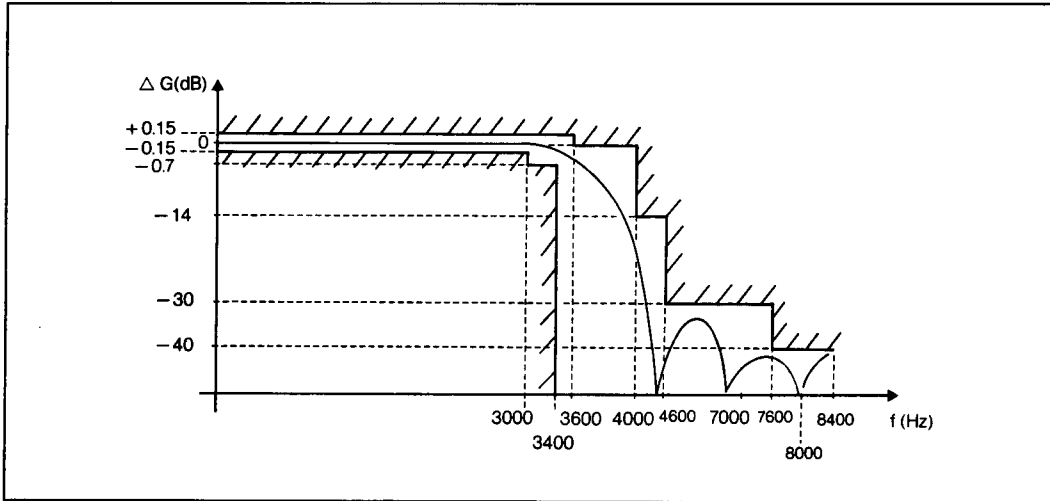


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**TRANSMISSION CHARACTERISTICS (continued)**

Unless otherwise specified :  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5\text{V}\pm 5\%$ ,  $V_{BB}=-5\text{V}\pm 5\%$ ,  $GND=0\text{V}$ ,  $f=1.02\text{ kHz}$ ,  $V_{IN}=0\text{ dBm}$ , transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RECEIVE SECTION TRANSFER CHARACTERISTICS</b>						
GRR	Receive Gain Relative to Gain at 820 Hz (0dBm0)	$f=0\text{ Hz} - 3000\text{ Hz}$	-0.15		+0.15	dB
		$f=3000\text{ Hz} - 3400\text{ Hz}$	-0.7		+0.15	dB
		$f=3400\text{ Hz} - 3600\text{ Hz}$			+0.15	dB
		$f=3600\text{ Hz} - 4000\text{ Hz}$			0	dB
		$f=4000\text{ Hz} - 4600\text{ Hz}$			-14	dB
SOS	Spurious Out-of-Band Signals at the channel Output	Image Signals at VFO :				dB
		$f=4600\text{ Hz} - 7600\text{ Hz}$			-30	dB
		$f=7600\text{ Hz} - 8400\text{ Hz}$			-40	dB



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**TRANSMISSION CHARACTERISTICS (continued)**

Unless otherwise specified :  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = 0V$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm0}$ , transmit input amplifier connected for unity-gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>NOISE</b>						
NXC	Transmit Idle Channel Noise, C Message Weighted	HC 3052, HC 3053, HC 3054 $V_{FXI}^- = 0V$		12	15	dBmC0
NXP	Transmit Noise, P Message Weighted	HC 3057 $V_{FXI}^- = 0V$		Note 1 -74 Note 2 -70	-69 -67	dBm0p dBm0p
NRC	Receive Idle Channel Noise C Message Weighted	HC 3052, HC 3053, HC 3054 PCM Code equals alternating Positive and Negative Zero		8	11	dBmC0
NRP	Receive Idle Channel Noise P Message Weighted	HC 3057 PCM Code equals Positive Zero		-82	-79	dBm0p
NRS	Noise, Single Frequency	$f = 0\text{ KHz}$ to $100\text{ KHz}$ , Loop Around Measurement, $V_{FXI}^- = 0\text{ Vrms}$			-53	dBm0
<b>POWER SUPPLY REJECTION</b>						
PPSRX	Positive Power Supply Rejection Transmit	$V_{FXI}^- = 0\text{ Vrms}$ $V_{CC} = 5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0 - 50\text{ KHz}$	40			dB
NPSRX	Negative Power Supply Rejection Transmit	$V_{FXI}^+ = 0\text{ Vrms}$ $V_{BB} = -5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0 - 50\text{ KHz}$	40			dB
PPSRr	Positive Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{CC} = 5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0.4000\text{ Hz}$ $f = 0 - 50\text{ KHz}$	40 25			dB dB
NPSRr	Negative Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{BB} = -5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0 - 4000\text{ Hz}$ $f = 0 - 50\text{ KHz}$	40 25			dB dB
<b>DISTORTION</b>						
STD <sub>X/R</sub>	Signal to Total Distortion Transmit or Receive Channel	Sinusoidal Test Method Level = $3.0\text{ dBm0}$ = $0\text{ dBm0}$ to $-30\text{ dBm0}$ = $-40\text{ dBm0}$ XMT RCV = $-55\text{ dBm0}$ XMT RCV	33 36 29 30 14 15			dB dB dB dB dB dB
SFD <sub>X</sub>	Single Frequency Distortion Transmit				-46	dB
SFD <sub>R</sub>	Single Frequency Distortion Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement. $V_{FXI}^- = -4\text{ dBm0}$ to $-21\text{ dBm0}$ , two frequencies in the range $300\text{ Hz}$ to $3400\text{ Hz}$			-41	dB
<b>CROSSTALK</b>						
CT <sub>X-R</sub>	Transmit to Receive Crosstalk $0\text{ dBm0}$ Transmit Level	$f = 300\text{ Hz} - 3400\text{ Hz}$ $D_R = \text{Steady PCM Code}$		-90	-75	dB
CT <sub>R-X</sub>	Receive to Transmit Crosstalk $0\text{ dBm0}$ Receive Level	$f = 300\text{ Hz} - 3400\text{ Hz}$ $V_{FXI}^- = 0V$		-90	-70	dB

**Note 1 :** Quantization Noise, measured by extrapolation from the distortion result.

**Note 2 :** Idle Channel Noise, due to alternating sign bit of a perfectly zeroed encoder.

**TIMING SPECIFICATIONS**

Unless otherwise specified  $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = 0V$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1/fPM	Frequency of Master Clocks	Depends on the Device Used and the BCLK <sub>R</sub> /CLKSEL Pin MCLK <sub>X</sub> and MCLK <sub>R</sub>		1.536 1.544 2.048		MHz MHz MHz
t <sub>WMH</sub>	Width of Master Clock High	MCLK <sub>X</sub> and MCLK <sub>R</sub>	160			ns
t <sub>WML</sub>	Width of Master Clock Low	MCLK <sub>X</sub> and MCLK <sub>R</sub>	160			ns
t <sub>SBFM</sub>	Set-Up Time from BCLK <sub>X</sub> High (and FS <sub>X</sub> in Long Frame Sync Mode) to MCLK <sub>X</sub> Falling Edge	First Bit Clock after the Leading Edge of FS <sub>X</sub>	100			ns
t <sub>WBH</sub>	Width of Bit Clock High	V <sub>IH</sub> = 2.2V	160			ns
t <sub>WBL</sub>	Width of Bit Clock Low	V <sub>IL</sub> = 0.6V	160			ns
t <sub>HBF</sub>	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t <sub>HOLD</sub>	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t <sub>SBF</sub>	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t <sub>DBD</sub>	Delay Time from BCLK <sub>X</sub> High to Data Valid	Load = 150 pF plus 2 LSTTL loads	0		140	ns
t <sub>XDP</sub>	Delay Time to $\overline{TSX}$ Low	Load = 150 pF plus 2 LSTTL loads			140	ns
t <sub>DZC</sub>	Delay Time from BCLK <sub>X</sub> Low to Data Output Disabled	C <sub>L</sub> = 0 pF to 150 pF	50		165	ns
t <sub>DZF</sub>	Delay Time to Valid Data from FS <sub>X</sub> or BCLK <sub>X</sub> , Whichever Comes later	C <sub>L</sub> = 0 pF to 150 pF	20		165	ns
t <sub>SSFF</sub>	Set-Up Time from SF <sub>X/R</sub> High to FS <sub>X/R</sub>	HC 3053 Only	60			ns
t <sub>SSFB</sub>	Set-Up Time from Signal Frame Sync High to BCLK <sub>X/R</sub> Clock	HC 3053 Only	60			ns
t <sub>SSGB</sub>	Set-Up Time from SIG <sub>X</sub> to BCLK <sub>X</sub>	HC 3052 and HC 3053	100			ns
t <sub>HBSG</sub>	Hold Time from BCLK <sub>X</sub> High to SIG <sub>X</sub>	HC 3052 and HC 3053	50			ns
t <sub>SDB</sub>	Set-Up Time from D <sub>R</sub> Valid to BCLK <sub>R/X</sub> Low		50			ns
t <sub>HBD</sub>	Hold Time from BCLK <sub>R/X</sub> Low to D <sub>R</sub> Invalid		50			ns
t <sub>HBSF</sub>	Hold Time from BCLK <sub>X/R</sub> Low to Signaling Frame Sync	HC 3053 Only	100			ns
t <sub>SF</sub>	Set-Up Time from FS <sub>X/R</sub> to BCLK <sub>X/R</sub> Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
t <sub>HF</sub>	Hold Time from BCLK <sub>X/R</sub> Low to FS <sub>X/R</sub> Low	Short frame Sync Pulse (1 Bit Clock Period Long)	100			ns
t <sub>HBF1</sub>	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS <sub>X</sub> or FSR)	Long Fram Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t <sub>WFL</sub>	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns

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**ELECTRICAL SPECIFICATIONS**

**ABSOLUTE MAXIMUM RATINGS**

V<sub>CC</sub> to GND -0.3V to 7V  
 V<sub>BB</sub> to GND +0.3V to -7V  
 Voltage at any Digital Input or Output V<sub>CC</sub> + 0.3V to GND - 0.3V  
 Voltage at any Analog Input or Output V<sub>CC</sub> + 0.3V to V<sub>RR</sub> - 0.3V

Operating Temperature Range -40 °C to 85 °C  
 Storage Temperature Range -65 °C to 150 °C  
 Lead Temperature (Soldering 10 seconds) 300 °C

**ELECTRICAL CHARACTERISTICS**

Unless otherwise noted: V<sub>CC</sub> = 5.0V ± 5% V<sub>BB</sub> = 5V ± 5% GND = 0V  
 T<sub>A</sub> = -40 °C to 85 °C : typical characteristics specified at V<sub>CC</sub> = 5.0V, V<sub>BB</sub> = -5.0V, T<sub>A</sub> = 25 °C : all signals are referenced to GND

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INTERFACE</b>						
V <sub>IL</sub>	Input Low Voltage				0.6	V
V <sub>IH</sub>	Input High Voltage		2.2			V
V <sub>OL</sub>	Output Low Voltage	D <sub>X</sub> , I <sub>L</sub> = 5.0mA S <sub>IGR</sub> , I <sub>L</sub> = 1.0mA T <sub>SX</sub> , I <sub>L</sub> = 3.2mA, Open Drain			0.4 0.4 0.4	V V V
V <sub>OH</sub>	Output High Voltage	D <sub>X</sub> , I <sub>L</sub> = -5.0mA S <sub>IGR</sub> , I <sub>L</sub> = -1.0mA	2.4 2.4			V V
I <sub>IL</sub>	Input Low Current (Note 1)	GND ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> . All Digital Inputs	-10		10	µA
I <sub>IH</sub>	Input High Current (Note 1)	V <sub>IH</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10		10	µA
I <sub>OZ</sub>	Output Current in High Impedance State	D <sub>X</sub> , GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10		10	µA
<b>ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)</b>						
I <sub>IAX</sub>	Input Leakage Current	-2.5V ≤ V ≤ +2.5V, V <sub>F<sub>X</sub>I</sub> + or V <sub>F<sub>X</sub>I</sub> -	-200		200	nA
R <sub>IXA</sub>	Input Resistance	-2.5V ≤ V ≤ +2.5V, V <sub>F<sub>X</sub>I</sub> + or V <sub>F<sub>X</sub>I</sub> -	10			MΩ
R <sub>OXA</sub>	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R <sub>LXA</sub>	Load Resistance	G <sub>SX</sub>	10			kΩ
C <sub>LXA</sub>	Load Capacitance	G <sub>SX</sub>			50	pF
V <sub>OXA</sub>	Output Level	G <sub>SX</sub> R <sub>L</sub> = 10k Ω	±2.8	±4.2		V
A <sub>VXA</sub>	Voltage Gain	V <sub>F<sub>X</sub>I</sub> + to G <sub>SX</sub>	5000			VV
F <sub>UXA</sub>	Unity Gain Bandwidth		1	2		MHz
V <sub>O<sub>SX</sub>A</sub>	Offset Voltage		-20	1	20	mV
V <sub>CMXA</sub>	Common-Mode Voltage		-2.5		+2.5	V
CMRR <sub>XA</sub>	Common-Mode-Rejection Ratio		60	80		dB
PSRR <sub>XA</sub>	Power Supply Rejection Ratio		60	70		dB
<b>ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)</b>						
R <sub>ORF</sub>	Output Resistance	Pin V <sub>F<sub>R</sub>O</sub>		1	3	Ω
R <sub>LRF</sub>	Load Resistance	V <sub>F<sub>R</sub>O</sub> = ± 2.5V	600			Ω
C <sub>LRF</sub>	Load Capacitance				500	pF
V <sub>O<sub>S</sub>R<sub>O</sub></sub>	Output DC Offset Voltage		-100		100	mV
<b>POWER DISSIPATION (ALL DEVICES)</b>						
I <sub>CCO</sub>	Power-Down Current			0.15	0.5	mA
I <sub>BBO</sub>	Power-Down Current			0.05	0.3	mA
I <sub>CC1</sub>	Active Current			6	9	mA
I <sub>BB1</sub>	Active Current			6	9	mA

**Note 1:** S<sub>F<sub>x</sub></sub>, S<sub>F<sub>r</sub></sub>: Internal pull down (2µ A typical) - B<sub>CLK<sub>R</sub></sub>: Internal pull up (2µ A typical)

**TRANSMISSION CHARACTERISTICS (ALL DEVICES)**

Unless otherwise specified:  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = 0V$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm}$ , transmit input amplifier connected for unity-gain non-inverting.

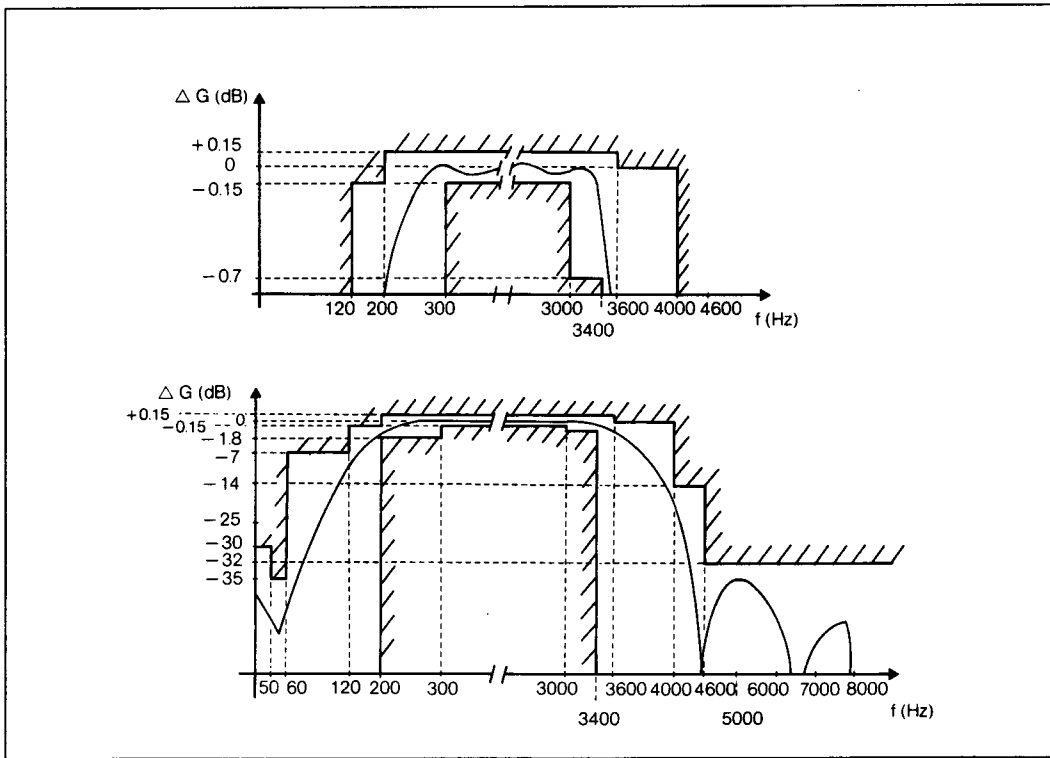
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AMPLITUDE RESPONSE</b>						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600 $\Omega$ ). 0 dBm0 (all devices)		1.2277		Vrms
	Max Overload Levels	HC 5552, HC 5553, HC 5554 (3.17 dBm0) HC 5557 (3.14 dBm0)		2.501 2.492		V <sub>DC</sub> V <sub>DC</sub>
GXA	Transmit Gain, Absolute	$T_A = 25^\circ\text{C}$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input at $GS_X = 0\text{ dBm0}$ at 1020 Hz	-0.15		0.15	dB
GXATV	Absolute Transmit Gain Variation with Temperature and Supply Voltage	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5V \pm 5\%$ , $V_{BB} = -5V \pm 5\%$			$\pm 0.15$	dB
GXRL	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level 10 dBm0 $V_{FX} _{+-40\text{ dBm0}}$ to $+3\text{ dBm0}$ $V_{FX} _{+-50\text{ dBm0}}$ to $40\text{ dBm0}$ $V_{FX} _{+-55\text{ dBm0}}$ to $50\text{ dBm0}$	0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
GRA	Receive Gain, Absolute	$T_A = 25^\circ\text{C}$ , $V_{CC} = 5V$ , $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	-0.15		0.15	dB
GRATV	Absolute receive Gain Variation with Temperature and Supply Voltage	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5V \pm 5\%$ $V_{BB} \pm 5V \pm 5\%$			$\pm 0.15$	dB
GRRL	Receive Gain Variations with Level	Sinusoidal Test Method : Reference Input PCM Code Corresponds to an ideally Encoded -10 dBm0 Signal PCM Level = -40 dBm0 to $+3\text{ dBm0}$ PCM Level = -50 dBm0 to $-40\text{ dBm0}$ PCM Level = -55 dBm0 to $50\text{ dBm0}$	0.2 -0.4 -1.2		0.2 +0.4 +1.2	dB dB dB
VRO	Receive Output Drive Level	$R_L = 600\ \Omega$	2.5		2.5	V
<b>ENVELOPE DELAY DISTORTION WITH FREQUENCY</b>						
DXA	Transmit Delay, Absolute	$f = 1600\text{ Hz}$		290	315	$\mu\text{s}$
DXR	Transmit Delay, Relative to DXA	$f = 500\text{ Hz} - 600\text{ Hz}$		140	220	$\mu\text{s}$
		$f = 600\text{ Hz} - 800\text{ Hz}$		100	145	$\mu\text{s}$
		$f = 800\text{ Hz} - 1000\text{ Hz}$		50	75	$\mu\text{s}$
		$f = 1000\text{ Hz} - 1600\text{ Hz}$		20	50	$\mu\text{s}$
		$f = 1600\text{ Hz} - 2600\text{ Hz}$		60	100	$\mu\text{s}$
		$f = 2600\text{ Hz} - 3000\text{ Hz}$		80	110	$\mu\text{s}$
DRA	Receive Delay, Absolute	$f = 750\text{ Hz}$		160	180	$\mu\text{s}$
DRR	Receive Delay, Relative to DRA	$f = 500\text{ Hz} - 1600\text{ Hz}$		40	60	$\mu\text{s}$
		$f = 1600\text{ Hz} - 2600\text{ Hz}$		90	120	$\mu\text{s}$
		$f = 2600\text{ Hz} - 2800\text{ Hz}$		120	140	$\mu\text{s}$
		$f = 2800\text{ Hz} - 3000\text{ Hz}$		140	175	$\mu\text{s}$

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**TRANSMISSION CHARACTERISTICS (continued)**

Unless otherwise specified:  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = 0V$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm}_0$ , transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>TRANSMIT SECTION TRANSFER CHARACTERISTICS</b>						
GXR	Transmit Gain Relative to Gain at 1020 Hz (0dBm0)	f = 50 Hz - 60 Hz			-35	dB
		f = 60 Hz - 120 Hz			-7	dB
		f = 120 Hz - 200 Hz			-0.15	dB
		f = 200 Hz - 300 Hz			+0.15	dB
		f = 300 Hz - 3000 Hz	-1.8		+0.15	dB
		f = 3000 Hz - 3400 Hz	-0.7		+0.15	dB
		f = 3400 Hz - 3600 Hz			+0.15	dB
		f = 3600 Hz - 4000 Hz			0	dB
		f = 4000 Hz - 4600 Hz			-14	dB
f = 4600 Hz and Up			-32	dB		

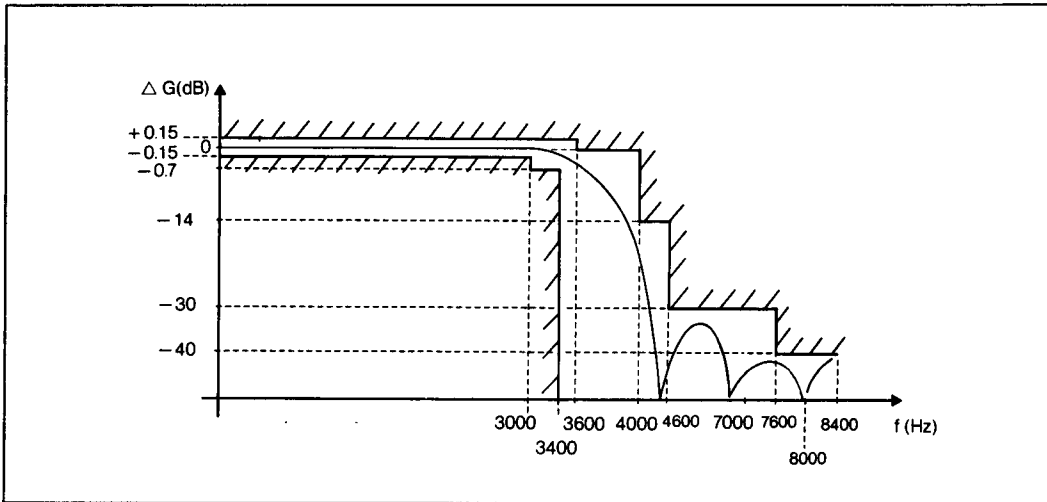


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**TRANSMISSION CHARACTERISTICS (continued)**

Unless otherwise specified :  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ ,  $V_{BB} = -5\text{V} \pm 5\%$ ,  $GND = 0\text{V}$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm}$ , transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RECEIVE SECTION TRANSFER CHARACTERISTICS</b>						
GRR	Receive Gain Relative to Gain at 1020 Hz (0dBm0)	f = 0 Hz - 3000 Hz	-0,15		+ 0,15	dB
		f = 3000 Hz - 3400 Hz	-0,7		+ 0,15	dB
		f = 3400 Hz - 3600 Hz			+ 0,15	dB
		f = 3600 Hz - 4000 Hz			0	dB
		f = 4000 Hz - 4600 Hz			- 14	dB
SOS	Spurious Out-of-Band Signals at the channel Output	Image Signals at VFRO :				dB
		f = 4600 Hz to 7600 Hz f = 7600 Hz to 8400 Hz			- 30 - 40	dB dB



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**TRANSMISSION CHARACTERISTICS (continued)**

Unless otherwise specified :  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = 0V$ ,  $f = 1.02\text{ kHz}$ ,  $V_{IN} = 0\text{ dBm0}$ , transmit input amplifier connected for unity-gain non inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>NOISE</b>						
NXC	Transmit Idle Channel Noise, C Message Weighted	HC 3052, HC 3053, HC 3054 $V_{FXI} = 0V$		12	15	dBmCO
NXP	Transmit Noise, P Message Weighted	HC 3057 $V_{FXI} = 0V$ Note 1 Note 2		-74 -70	-69 -67	dBmOp dBmOp
NRC	Receive Idle Channel Noise C Message Weighted	HC 3052, HC 3053, HC 3054 PCM Code equals alternating Positive and Negative Zero		8	11	dBmCO
NRP	Receive Idle Channel Noise P Message Weighted	HC 3057 PCM Code equals Positive Zero		-82	-79	dBmOp
NRS	Noise, Single Frequency	$f = 0\text{ KHz}$ to $100\text{ KHz}$ , Loop Around Measurement, $V_{FXI} = 0\text{ Vrms}$			-53	dBm0
<b>POWER SUPPLY REJECTION</b>						
PPSRX	Positive Power Supply Rejection Transmit	$V_{FXI} = 0\text{ Vrms}$ $V_{CC} = 5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0 - 50\text{ KHz}$	40			dB
NPSRX	Negative Power Supply Rejection Transmit	$V_{FXI} = 0\text{ Vrms}$ $V_{BB} = -5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0 - 50\text{ KHz}$	40			dB
PPSR	Positive Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{CC} = 5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0.4000\text{ Hz}$ $f = 0 - 50\text{ KHz}$	40 25			dB dB
NPSR	Negative Power Supply Rejection Receive	PCM Code equals Positive Zero $V_{BB} = -5.0\text{ VDC} + 100\text{ mVrms}$ $f = 0 - 4000\text{ Hz}$ $f = 0 - 50\text{ KHz}$	40 25			dB dB
<b>DISTORTION</b>						
STD <sub>X/R</sub>	Signal to Total Distortion Transmit or Receive Channel	Sinusoidal Test Method Level = $3.0\text{ dBm0}$ = $0\text{ dBm0}$ to $-30\text{ dBm0}$ = $-40\text{ dBm0}$ XMT RCV = $-55\text{ dBm0}$ XMT RCV	33 36 29 30 14 15			dB dB dB dB dB dB
SFD <sub>X</sub>	Single Frequency Distortion Transmit				-46	dB
SFD <sub>R</sub>	Single Frequency Distortion Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement. $V_{FXI} = -4\text{ dBm0}$ to $-21\text{ dBm0}$ , two frequencies in the range $300\text{ Hz}$ to $3400\text{ Hz}$			-41	dB
<b>CROSSTALK</b>						
CT <sub>X-R</sub>	Transmit to Receive Crosstalk $0\text{ dBm0}$ Transmit Level	$f = 300\text{ Hz} - 3400\text{ Hz}$ $D_R = \text{Steady PCM Code}$		-90	-75	dB
CT <sub>R-X</sub>	Receive to Transmit Crosstalk $0\text{ dBm0}$ Receive Level	$f = 300\text{ Hz} - 3400\text{ Hz}$ $V_{FXI} = 0V$		-90	-70	dB

**Note 1** : Quantization Noise, measured by extrapolation from the distortion result.

**Note 2** : Idle Channel Noise, due to alternating sign bit of a perfectly zeroed encoder.

**TIMING SPECIFICATIONS**

Unless otherwise specified  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ,  $GND = 0V$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1/TPM	Frequency of Master Clocks	Depends on the Device Used and the BCLK <sub>R</sub> /CLKSEL Pin MCLK <sub>X</sub> and MCLK <sub>R</sub>		1.536 1.544 2.048		MHz MHz MHz
tWMH	Width of Master Clock High	MCLK <sub>X</sub> and MCLK <sub>R</sub>	160			ns
tWML	Width of Master Clock Low	MCLK <sub>X</sub> and MCLK <sub>R</sub>	160			ns
tSBFM	Set-Up Time from BCLK <sub>X</sub> High (and FS <sub>X</sub> in Long Frame Sync Mode) to MCLK <sub>X</sub> Falling Edge	First Bit Clock after the Leading Edge of FS <sub>X</sub>	100			ns
tWBH	Width of Bit Clock High	$V_{IH} = 2.2V$	160			ns
tWBL	Width of Bit Clock Low	$V_{IL} = 0.6V$	160			ns
tHBF	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
tHOLD	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
tSBF	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
tDBD	Delay Time from BCLK <sub>X</sub> High to Data Valid	Load = 150 pF plus 2 LSTTL loads	0		140	ns
tXDP	Delay Time to $\overline{TS}_X$ Low	Load = 150 pF plus 2 LSTTL loads			140	ns
tDZC	Delay Time from BCLK <sub>X</sub> Low to Data Output Disabled	$C_L = 0\text{ pF}$ to 150 pF	50		165	ns
tDZF	Delay Time to Valid Data from FS <sub>X</sub> or BCLK <sub>X</sub> , Whichever Comes later	$C_L = 0\text{ pF}$ to 150 pF	20		165	ns
tSSFF	Set-Up Time from SF <sub>X/R</sub> High to FS <sub>X/R</sub>	HC 3053 Only	60			ns
tSSFB	Set-Up Time from Signal Frame Sync High to BCLK <sub>X/R</sub> Clock	HC 3053 Only	60			ns
tSSGB	Set-Up Time from SIG <sub>X</sub> to BCLK <sub>X</sub>	HC 3052 and HC 3053	100			ns
tHBSG	Hold Time from BCLK <sub>X</sub> High to SIG <sub>X</sub>	HC 3052 and HC 3053	50			ns
tSDB	Set-Up Time from D <sub>R</sub> Valid to BCLK <sub>R/X</sub> Low		50			ns
tHBD	Hold Time from BCLK <sub>R/X</sub> Low to D <sub>R</sub> Invalid		50			ns
tHBSF	Hold Time from BCLK <sub>X/R</sub> Low to Signaling Frame Sync	HC 3053 Only	100			ns
tSF	Set-Up Time from FS <sub>X/R</sub> to BCLK <sub>X/R</sub> Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
tHF	Hold Time from BCLK <sub>X/R</sub> Low to FS <sub>X/R</sub> Low	Short frame Sync Pulse (1 Bit Clock Period Long)	100			ns
tHBF1	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS <sub>X</sub> or FS <sub>R</sub> )	Long Fram Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
tWFL	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns



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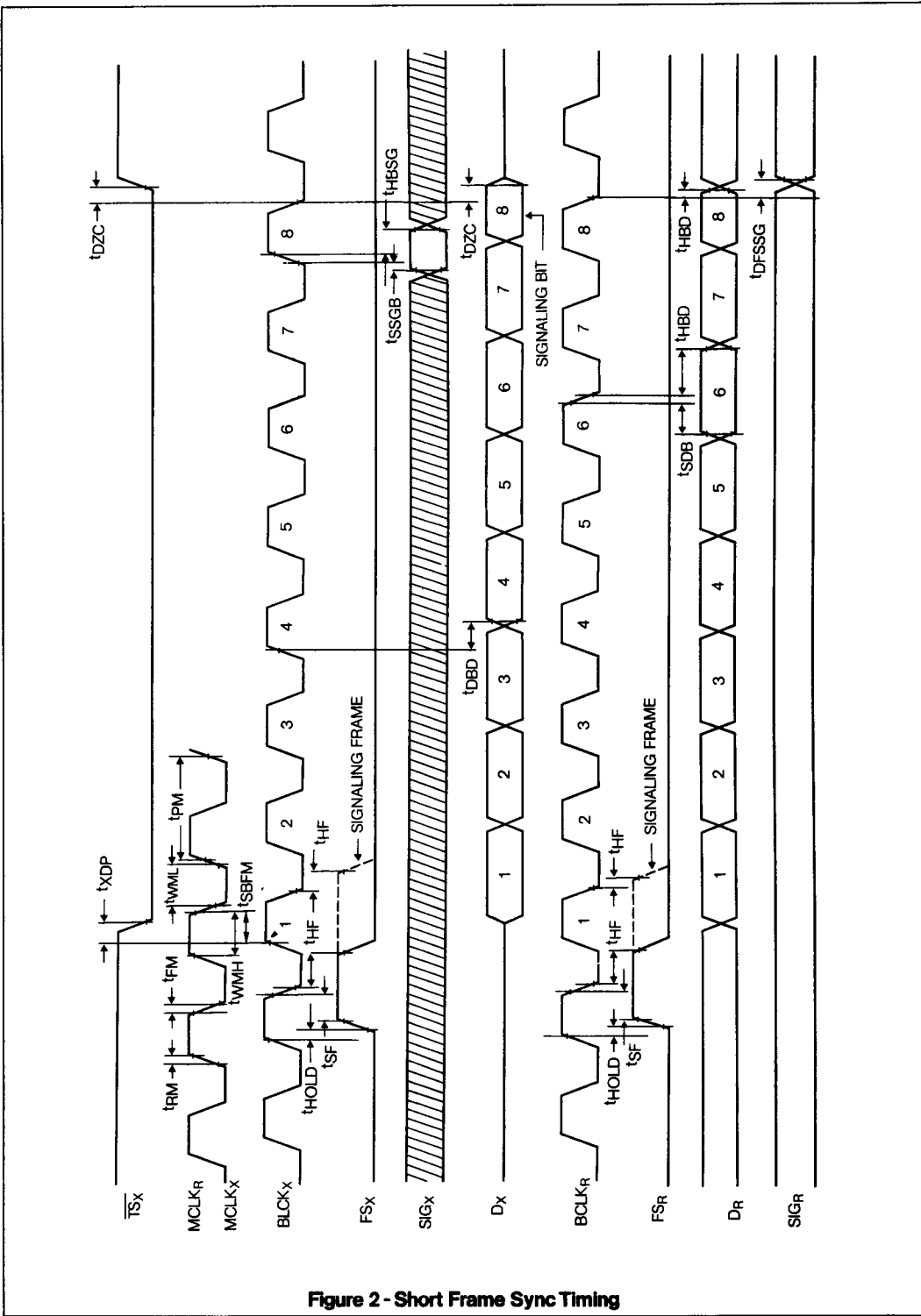


Figure 2 - Short Frame Sync Timing

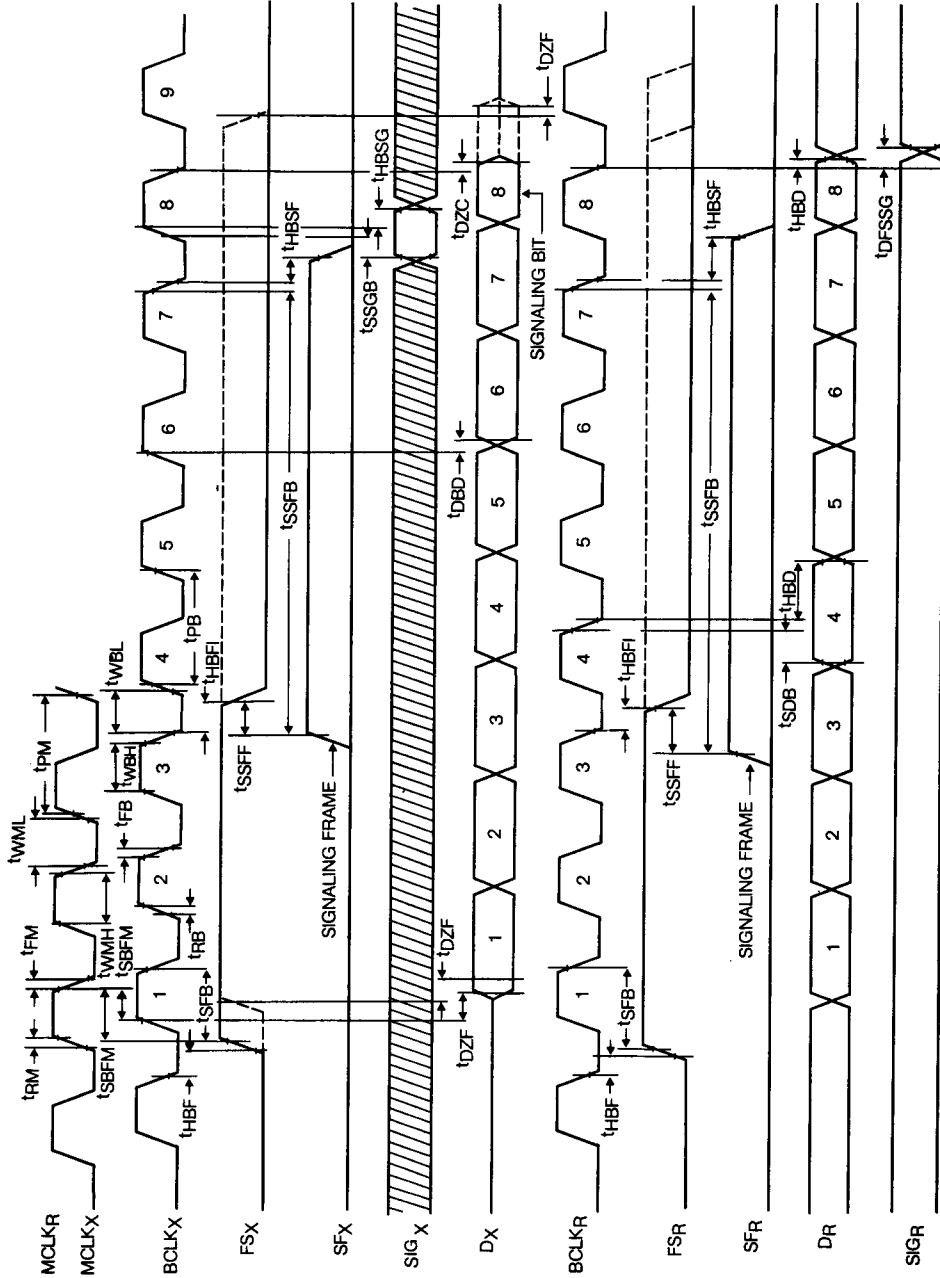


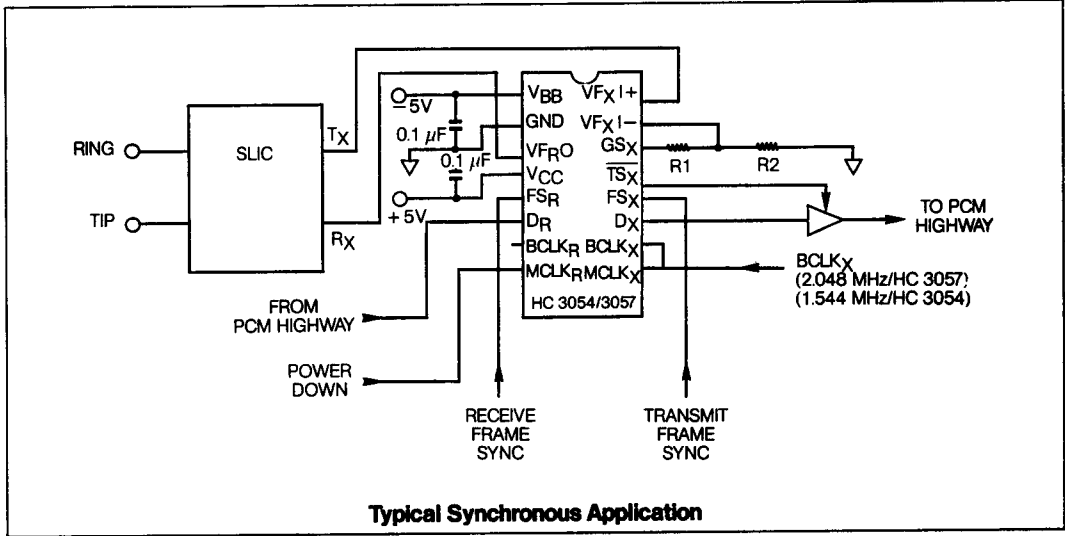
Figure 3 - Long Frame Sync Timing



**OPERATING INSTRUCTIONS**

Ground should be applied to the device before any other connection. Although VCC and VBB can be connected in any order, one should check that voltages on all inputs and on supply rails stay within absolute maximum ratings even for very short periods to avoid any latch-up. All ground connections to each

device should meet at a common point as close as possible to the GND pin. Two 0.1  $\mu$ F decoupling capacitors are required from the common ground point to VCC and VBB. The ground point of each COFIDEC should be tied to a common card ground in star formation, rather than via a ground bus.



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