CA3202

TV Horizontal/Vertical Countdown Digital Sync System

Features:

- *Automatic forced asynchronous mode to remove jitter*
- *Improved low voltage start-up operation*
- *Lower zero-state horizontal-drive pulse output*
- *Improved symmetry for horizontal-drive output*
- *Improved automatic standard operation*
- *Noise detector*
- *Handles standard NTSC and non-standard signals*
- *Automatic mode recognition*
- *Clock input*
- *Vertical ramp (sawtooth) generator*
- *Vertical amplifier*
- *Vertical blanking generator*
- *Horizontal drive pulse output*
- *Ratio-voltage regulator*
- *Inherent interlace for NTSC signals*
- *Vertical-hold control eliminated*
- *Supply-voltage range=10.8 to 13.2 V*
- *Rapid pull-in*
- *Co-channel sync lockout for NTSC signals*
- *I^2L logic*

The RCA CA3202E is an improved version of RCA CA3157. In some video playback units, there are incorrect frequency relationships between horizontal and field frequencies. Automatic forced asynchronous mode eliminates jitter when equalizer pulses are correct, but these incorrect frequency relationships exist.

Automatic standard mode occurs upon detection of nine or more equalizing pulses during a six-line-width vertical driving period after seven fields of coincidence between integrated vertical (IV) sync and internal counter output. Standard mode is retained for seven fields of missing or mutilated vertical sync pulses.

If two or more noise pulses are detected at terminal 12 during a 384-line active scan time, a noise detector reverts the system to standard mode at the next field of coincidence (without the seven fields of coincidence delay). Thus, the unit stays in standard mode during tuner channel changes.

As in the CA3157, an automatic mode-recognition system places the unit in standard mode for NTSC signals or into non-synchronous mode for non-standard sync signals.

Fig. 1 shows that the chip includes a sawtooth generator, vertical amplifier, ratio-voltage regulator, and a countdown and phasing circuit that eliminates an external vertical hold control.

An external oscillator (CA3154) supplies an input to terminal 9 that is 32 times the horizontal rate. An internal divide-by-16 counter converts this input ($32f_H$) to $2f_H$ for use elsewhere. This $2f_H$ signal is further divided to f_H, which is available at terminal 11 to drive the horizontal deflection circuits. A divide-by-525 counter further divides the $2f_H$ signal to generate the vertical ramp generator timing pulses and the vertical blanking pulse.

A phasing circuit (part of the mode recognition and vertical regeneration circuits) insures that the 525 counter is reset in coincidence with the vertical sync. It does this by comparing the internally generated vertical pulse with an external integrated vertical sync signal applied to terminal 12. The automatic mode recognition circuit forces the CA3202E into the standard mode for NTSC signals or into the non-synchronous mode for non-standard sync signals such as video games. An input control signal (or no connection) at terminal 8 places the CA3202E into non-synchronous operation.

A phasing and timing logic circuit checks to see if the line counter is in sync with the IV signal at terminal 12. Seven consecutive fields of in-phase coincidence with the IV signal are needed to achieve standard mode unless two or more noise pulses are de-detected at input terminal 12 during the active scan time. In this case, normal mode will be acquired in one field.

In the standard divide-by-525 mode, the integrated vertical pulse is used only to provide coincidence with the 545 count (counter preset=20, 545−20=525) in the phase detector circuit. The vertical ramp is timed by the output of the 525 counter. In standard mode, the CA3202E will maintain the divide-by-525 count for six fields of lost or mutilated sync. If the seventh field does not have the correct coincidence, the unit will switch to non-standard mode. In this mode, the vertical sync is derived from the integrated vertical pulse on a field-to-field basis. A noise immunity of 384 lines is provided. In the absence of sync pulses, the count will be 684 instead of 525 so that rapid vertical capture may be achieved when sync is restored. Non-standard mode still may be selected by removing ground from terminal 8.

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The vertical retrace signal is converted to a ramp signal if a capacitor is connected between terminal 3 and ground. The ramp's slope corresponds to vertical size and is controlled by changing the input current to terminal 2. The ramp is connected to the inverting input of a difference amplifier. The output of this amplifier, connected to terminal 6, is used to drive the vertical output stage. The non-inverting input of the difference amplifier is at terminal 5. A voltage derived from yoke current may be applied to this terminal for linearity improvement.

The pulse width of the vertical blanking signal at terminal 7 is 608 clocks wide in the synchronous mode, and is adjustable in width by changing the monostable rc network at terminal 10 for the non-synchronous mode.

The proportional voltage regulator output at terminal 4 is about 43% of the supply voltage at terminal 12. The maximum external load current is 20-mA peak.

The CA3202E is supplied in the 14-lead dual-in-line plastic package.

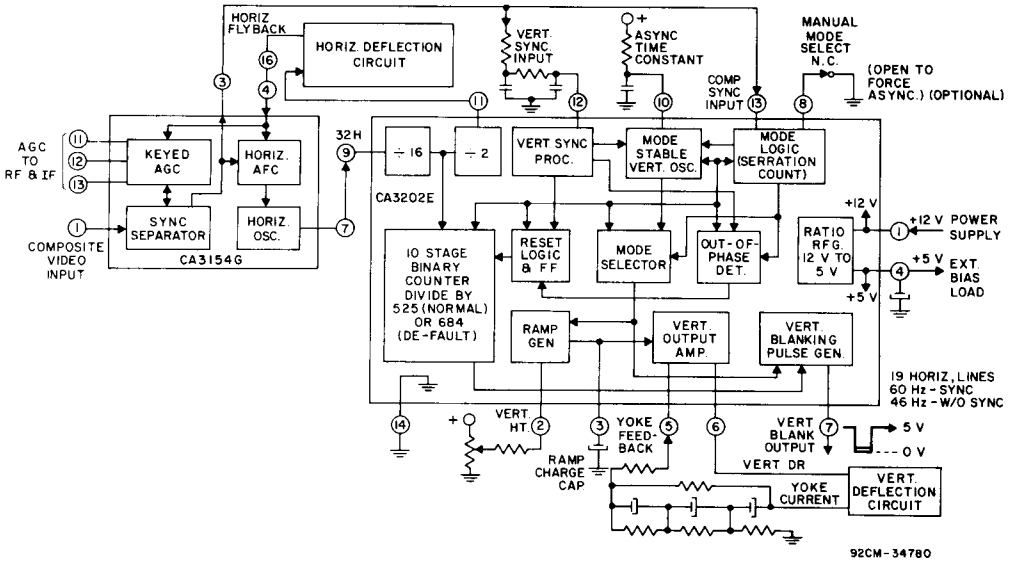

Fig. 1 - CA3202E horizontal/vertical countdown integrated circuit.

CA3202

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 15 V

DEVICE DISSIPATION:

Up to T_A=70°C ..... 530 mW

Above T_A=70°C ..... derate linearly at 6.7 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to 70°C

Storage ..... −55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A=25° C, all switches open unless otherwise specified.
See Fig. 2, Test Points 2 and 14=Gnd.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Amplifier Gain, V6	S2,S5,S6 Closed, Note 1, Test pt. 1=12 V, 16=1 V_{RMS} at 1 kHz	0.178	3.16	V_{RMS}
Horizontal Frequency Divider Ratio, $f_g \div f_{11}$	S3,S7,S8 Closed, Note 7, Test pt. 1=14.4 V	32	32	RATIO
Horizontal Pulse Width, Term. 11	S3,S7,S8 Closed, Notes 9,10, Test pt. 1=8.4 V	28	34	μs
	S3,S7,S8 Closed, Notes 9,10,11, Test pt. 1=14.4 V	28	34	
Asynchronous Non-Coincident Frequency Divide Ratio, $f_g \div f_3$	S3,S7,S8 Closed, Notes 9,12,13,14,15, Test pt. 1=14.4 V, 8=0.2 V, 12 =1.5 V	10944	10944	RATIO
Ramp Charge Pulse Width, Term. 3	S3,S7,S8 Closed, Notes 13,15, Test pt. 1=14.4 V, 8=0.2 V, 12=1.5 V	585	985	μs
Asynchronous Coincident Noise Immunity, Hold-Off Freq. Divider Ratio, $f_8 \div f_3$	Notes 9,12,13,15,16,17, Test pt. 1=14.4 V, 8=0.2 V	7872	7872	RATIO
Synchronous Divider Ratio, $f_g \div f_3$	S3,S7,S8 Closed, Notes 9,13,15,18,19, Test pt. 1=14.4 V, 8=0.2 V, 12=1.5 V	8400	8400	RATIO
Ramp Charge Pulse Width, Term. 3	S3,S7,S8 Closed, Notes 9,10,13,15,18,20, Test pt. 1=14.4 V, 8=0.2 V, 12=1.5 V	190	194	CLOCKS
Vertical Blanking Pulse Width, Term. 7	S3,S7,S8 Closed, Notes 9,10,13,15,18,21 Test pt. 1=14.4 V, 8=0.2, 12=1.5 V	606	610	CLOCKS

ELECTRICAL CHARACTERISTICS at T_A=25° C, all switches open unless otherwise specified.
See Fig. 2, Test Points 2 and 14=Gnd.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Mode Recognition Field Count, Freq. Divider Ratio, $f_g \div f_3$ Synchronous to Non-Synchronous	S3,S7,S8 Closed, Notes 9,13,14,15,18,22, Test pt. 1=12.0 V, 8=0.2 V, 12=1.5 V			RATIO
	Initial Fields 9 Serrations	8400	8400	
	First Field, 8 Ser.	8400	8400	
	Second Field, 8 Ser.	8400	8400	
	Third Field, 8 Ser.	8400	8400	
	Fourth Field, 8 Ser.	8400	8400	
	Fifth Field, 8 Ser.	8400	8400	
	Sixth Field, 8 Ser.	8400	8400	
	Seventh Field, 8 Ser.	10944	10944	
Mode-Recognition Field Count, Freq. Divider Ratio, $f_g \div f_3$ Non-Synchronous to Synchronous	S3,S7,S8 Closed, Notes 9,13,15,18,23, Test pt. 1=12.0 V, 8=0.2 V			RATIO
	First Field	8384	8384	
	Second Field	8384	8384	
	Third Field	8384	8384	
	Fourth Field	8384	8384	
	Fifth Field	8384	8384	
	Sixth Field	8384	8384	
	Seventh Field	8384	8384	
	Eighth Field	8400	8400	
	Ninth Field	8400	8400	
Fast Standard-Mode Resynchronization	S3,S7,S8 Closed, Notes 9,13,15, Test pt. 1=12.0 V, 8=0.2 V			

NOTES:

1. Stop clock when terminal 7 is high.
2. Stop clock when terminal 9 is low.
3. Stop clock when terminal 9 is high.
4. Stop clock when terminal 7 is low.
5. Stop clock when terminal 11 is high.
6. Stop clock when terminal 11 is low.
7. Clock frequency=600 kHz; clock amplitude: low ≤ 0.45 V, high ≥ 0.95 V (5 V max.).
8. Frequency at terminal 9 (clock) divided by frequency at terminal 11 (hor. out).
9. Clock frequency=500 kHz, clock amplitude same as in Note 7.
10. Pulse width measured at 2 V point on output waveform.
11. Total capacity=50 pF when measuring pulse width.
12. Sync serrations=8 (see Fig. 4).
13. Sync amplitude: low state ≤ 1.2 V; high state ≥ 4 V (6 V max. with positive sync tips).
14. Frequency at terminal 9 (clock) divided by frequency at terminal 3 (ramp control).
15. Initialize or repeat initialization procedure before doing this test (see Fig. 2).
16. Apply a pulse 1 clock wide, 7808 clocks after first positive transition at terminal 3 (see Fig. 5).
17. Default count determined by 684 x 16(H)=10944.
18. Sync serrations=9.
19. Hold-off count determined by 492 x 16(H)=7872.
20. Number of clocks occurring within ramp gate period (see Fig. 6).
21. Number of clocks occurring during the blanking gate period (see Fig. 7).
22. This series of tests checks the mode recognition circuit. The first test after initialization applies 9 serrations at the sync input terminal. The IC should go to the synchronous count ratio of 8400. During the next seven fields only 8 serrations are applied. The CA3202E should maintain the synchronous count ratio of 8400 for the first six fields. At the seventh field the CA3202E should go to default count of 10944. The test concludes with a 9-serration input. The CA3202E should revert to a synchronous count of 8400 (see Fig. 8).
23. This test checks the operation of the out-of-sync detector by applying out-of-phase sync pulses to terminal 12. The CA3202E will count eight fields before resetting to the sync pulse (see Fig. 9).
24. Initialize by 8384 sync for eight fields before test.
25. This test verifies the operation of the fast resync performance by simulating a noise pulse (5 to 50 clocks wide) applied to the I.V. terminal 4000 to 6000 clocks (8 ms to 12 ms) after I.V. sync. Initialize to non-sync mode before performing this test. The IC should resync in the next field and be maintained for the standard confidence count of seven fields.

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STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=12 V, Switches open unless otherwise specified. See Fig. 2. Test Points 2, 8, 12 and 14 grounded unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	CONNECT TEST POINTS AS SHOWN BELOW — TEST POINT NOS.								LIMITS		UNITS
		1	3	4	5	6	10	11	13	Min.	Max.	
Ratio Regulator Voltage, V_4:												
Load	S2 Closed, Note 1	12V		−20 mA	2V					4.9	5.5	V
No Load		14.4V			2V					5.8	6.8	
Vertical Blanking Output, V_7:												
Unblanked	S2 Closed,	12V		−20 mA	G					2.5	5	V
Blanked	Notes 1, 4	12V			G					0.09	0.5	
Horizontal Output Voltage, V_{11}:	Test pt. 15=8V,											
High	S2 Closed,	14.4			G					7	8.1	V
Low	Notes 5, 6	12V			G			20 mA		0	0.12	
Vertical Output Voltage, V_6:												
Off	S4 Closed, Note 1	12V			G	1 mA				0.6	1.4	V
On	S3 Closed, Note 1	12V	G			−20 mA				3.4	5.1	
Difference Voltage, V_3-V_5	S2 Closed, Note 1	12V			4V	−20 mA				-0.15	0.15	V
Supply Current, I_1	S2 Closed, Note 1	14.4V			2V					10	35	mA
Clock Current, I_9: Low	Test pt. 9=GND S2 Closed, Note 2	14.4V			2V					−180	−70	μA
Voltage, V_9	S2 Closed, Note 3	14.4V			2V					—	0.75	V
Composite Sync Input Current, I_{13}:												
Sync High	S2 Closed, Note 3	12V			2V				4V	100	700	μA
Sync Low		14.4V			2V				0V	−25	25	
Forced Asynchronous Current, I_8	S2 Closed, Note 3, Test pt. 8=4.5V	12V			2V					1	3.2	mA
Ramp Current, I_3	S3 Closed, Note 1, Test pt. 2=50 μA	12V	4.5V							45	57	μA
Δ Ramp Current, ΔI_3	S3 Closed, Note 1, Test pt. 2−50 μA	12V	1.5V							−3	3	μA
Async Time Constant Current, I_{10}:												
Charge	S2 Closed, Note 4	12V			2V		3V			10	40	μA
Discharge		12V			2V		4.5V			1	5	mA
Vert. Sync. Input Current, I_{12}:												
Normal	S2 Closed, Note 4, Test pt. 12=2.3V	12V			2V					−0.1	5	μA
Overdrive	S2 Closed, Note 4, Test pt. 12=3V	12V			2V					0.1	3	mA

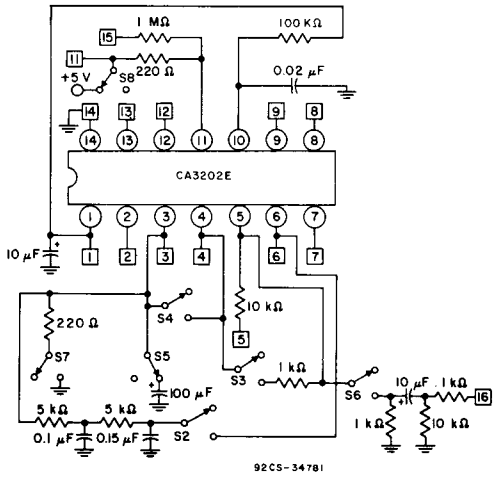

Fig. 2 - Electrical characteristics test circuit.

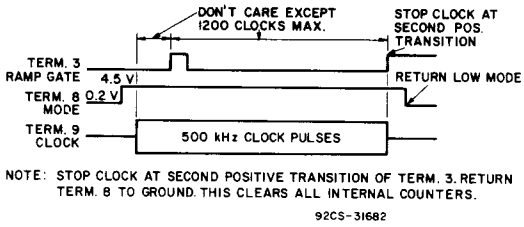

Fig. 3 - Initialization timing diagram (applies to all tests referenced to Note 15).

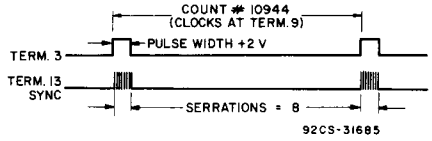

Fig. 4 - Asynchronous non-coincident divide ratio (applies to all tests referenced to Note 12).

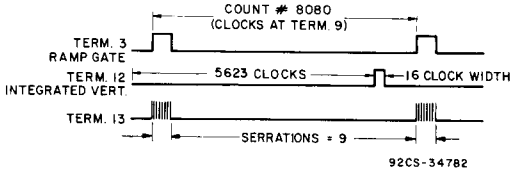

Fig. 5 - Synchronous non-coincidence noise recovery (fast resync).

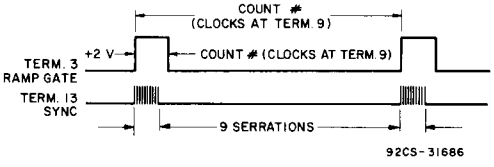

Fig. 6 - Synchronous non-coincident divider ratio and ramp gate pulse width (applies to test referenced to Note 20).

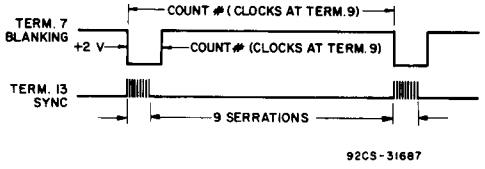

Fig. 7 - Blanking synchronous divider ratio and blanking pulse width (applies to test referenced to Note 21).

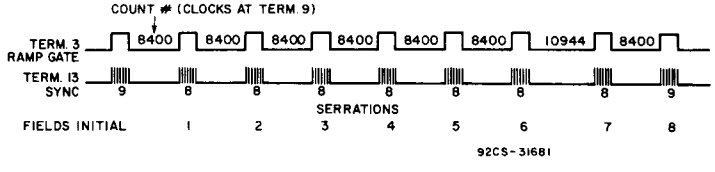

Fig. 8 - Mode recognition field count test (applies to test referenced to Note 22).

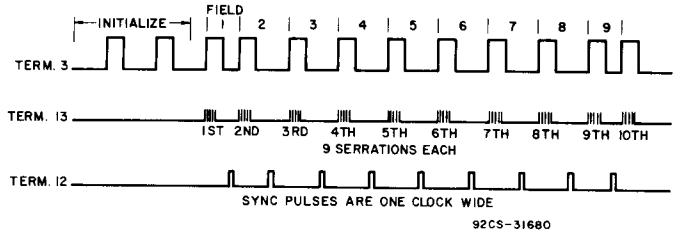

Fig. 9 - Out-of-sync detector test for confidence of coincidence field count at terminal 3 (applies to test referenced to Note 23).