IS31SE5118

8-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

Preliminary
Octorber 2020

GENERAL DESCRIPTION

IS31SE5118 is an ultra-low power, 8-channel capacitive touch controller. The controller allows sleep mode (under 10uA) and uses auto detection for wakeup. It also provides a shield output to increase moisture immunity. Built-in hardware monitors and calibrates the environment to prevent false triggers.

A host MCU is required to communicate with IS31SE5118. An on-chip I²C slave controller with 400kHz capability and programmable slave addresses serves as the communication port for the host MCU. An interrupt, INT, can be configured so it is generated when a trigger event (touch or release) occurs. Trigger or clear condition can be configured by setting the interrupt register.

IS31SE5118 is available in TSSOP-16 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +105°C.

FEATURES

- 8-channel capacitive touch controller with readable key value
- Touch threshold setting for individual key
- Optional multiple-key function
- Press and hold function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Buzzer/Melody Generator
- 400kHz fast-mode I²C interface
- Operating temperature between -40°C ~ +105°C
- TSSOP-16 package

APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control

TYPICAL APPLICATION CIRCUIT (TSSOP-16)

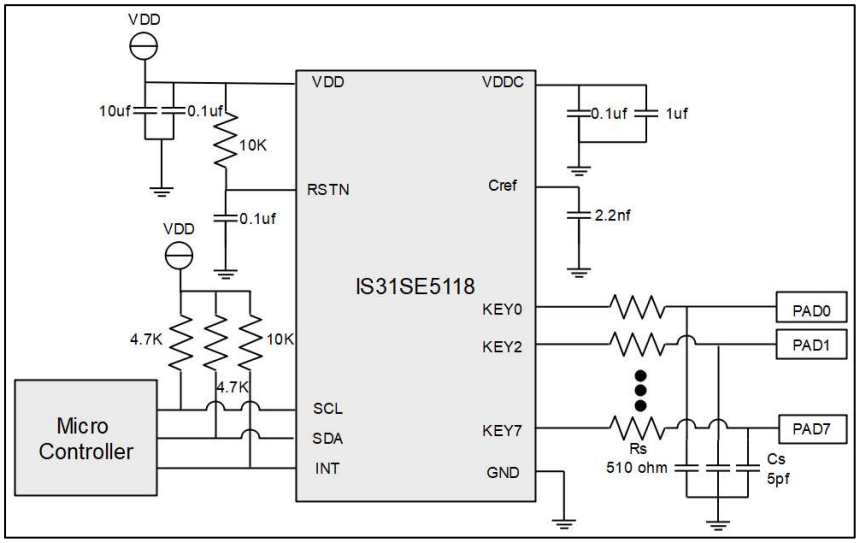
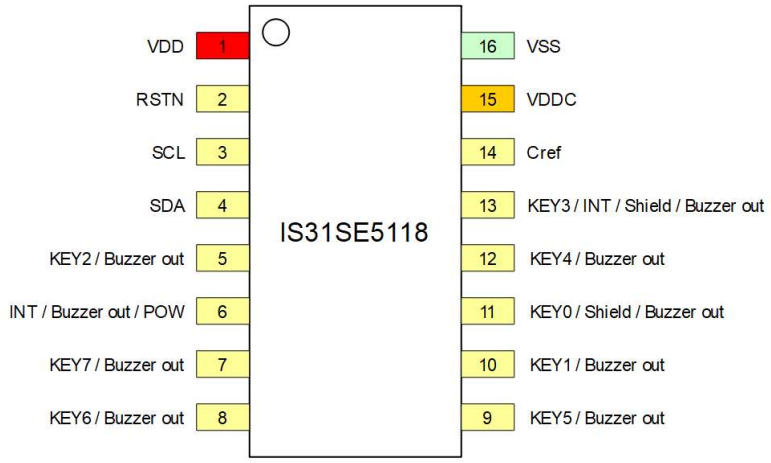


Figure 1 Typical Application Circuit (TSSOP-16)

Note 1: SE5118 should be placed far away from the noise source to prevent EMI.
Note 2: R_S and C_S should be placed as close to the chip as possible to reduce EMI.
Note 3: INT can be configured as POW pin for melody application.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
TSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
No.	**Pin**	**Description**
1	VDD	Power supply
2	RSTN	Reset Low Active
3	SDA	I2C serial data
4	SCL	I2C serial clock
5	KEY2/Buzzer out	Multiple functions. Can be configured to Input sense channel 2 or Buzzer output.
6	INT/Buzzer out/ POW	Multiple functions. Can be configured to or interrupt output (active low), Buzzer output or melody power control.
7 – 10	KEY7/6/5/1/ Buzzer out	Multiple functions. Can be configured to Input sensor channel (refer to the pin configuration) or Buzzer out.
11	KEY0/Shield/ Buzzer out	Multiple functions. Can be configured to Input sense channel 0, Shield output or Buzzer output.
12	KEY4/Buzzer out	Multiple functions. Can be configured to Input sense channel 4 or Buzzer output.

ORDERING INFORMATION

Industrial Range: -40°C to +105°C

Order Part No.	Package	QTY
IS31SE5118-SALS3-TR	TSSOP-16, Lead-free	2500/Reel

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +105°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}(TSSOP-16)	50.2°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7V ~ 5.5V, unless otherwise noted. Typical values are T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC} = 5.5V		50		μA
I_{SD}	Shutdown current	V_{CC} = 5.5V		1		μA
ΔC_S	Minimum detectable capacitance	C_S = 5pF (Note 4)		0.2		pF
Logic Electrical Characteristics						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC} (Note 4)		5		nA

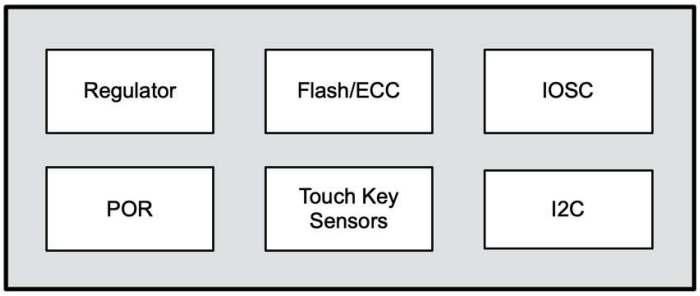
DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 5)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 5)		20+0.1C_b	300	ns

Note 4: Guaranteed by design.

Note 5: C_b = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}.

FUNCTIONAL BLOCK DIAGRAM



I2C INTERFACE

IS31SE5118 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. IS31FL5118 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command.

The complete slave address is:

Bit	A7:A1	A0
Value	0111100	1/0

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31SE5118.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for IS31SE5118's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If IS31SE5118 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5118, the register address byte is sent, most significant bit first. IS31SE5118 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31SE5118 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the address of IS31SE5118 with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31SE5118 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from IS31SE5118 to the master (Figure 5).

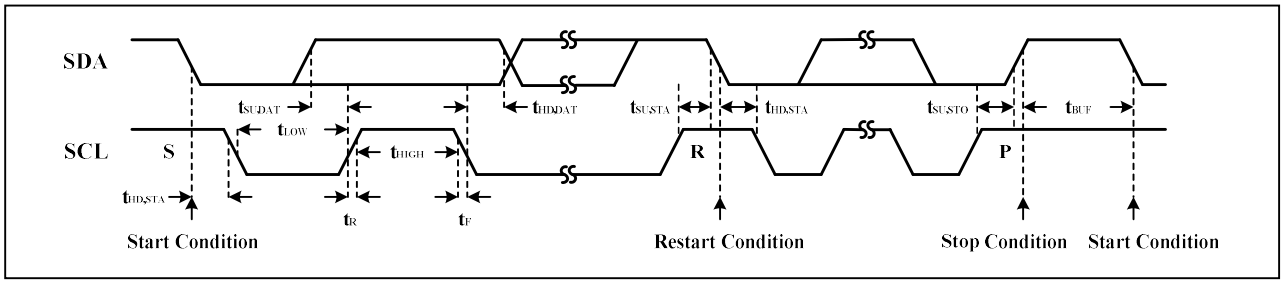


Figure 2 Interface Timing

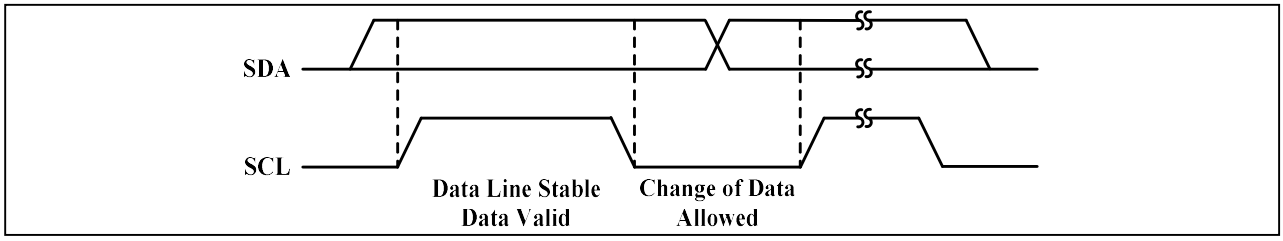


Figure 3 Bit Transfer

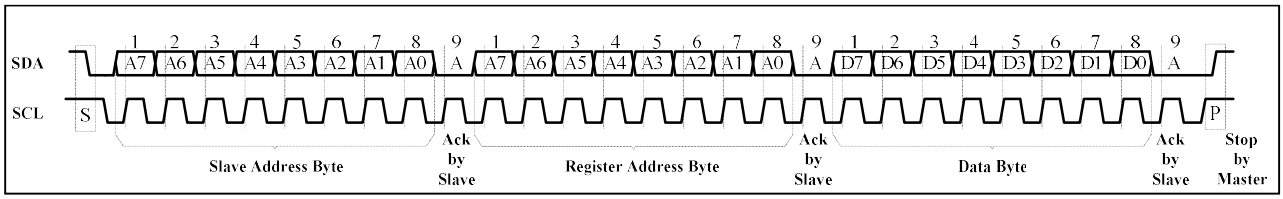


Figure 4 Writing to IS31SE5118

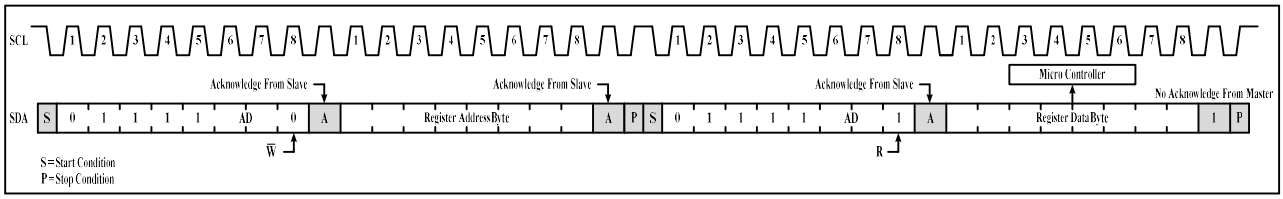


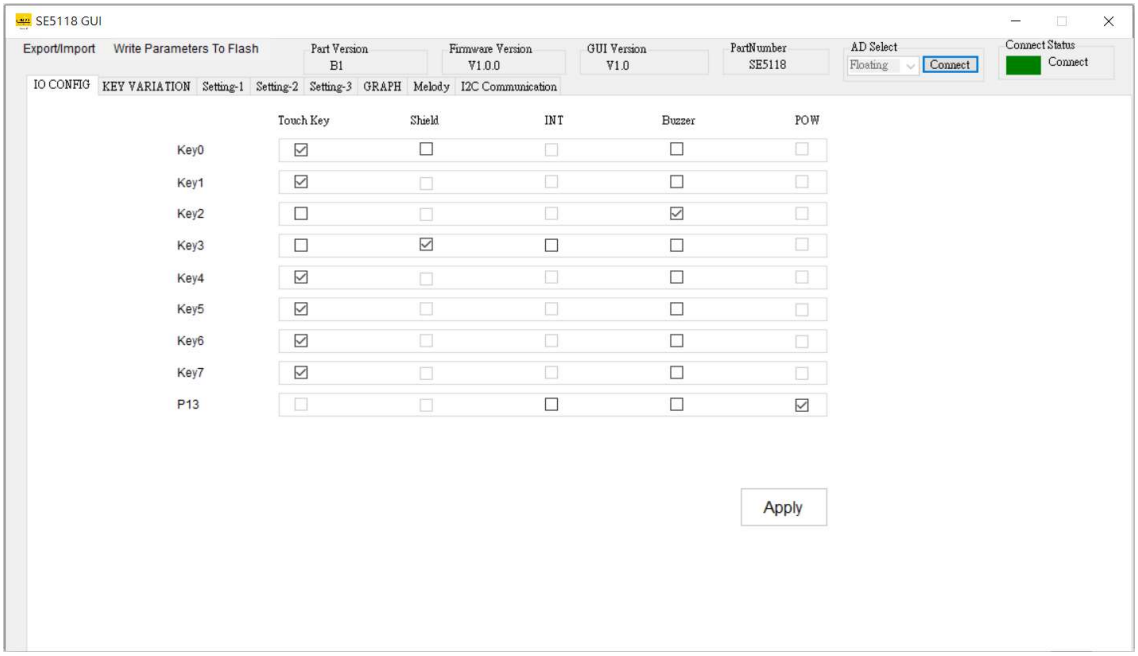
Figure 5 Reading from IS31SE5118

IS31SE5118 GUI

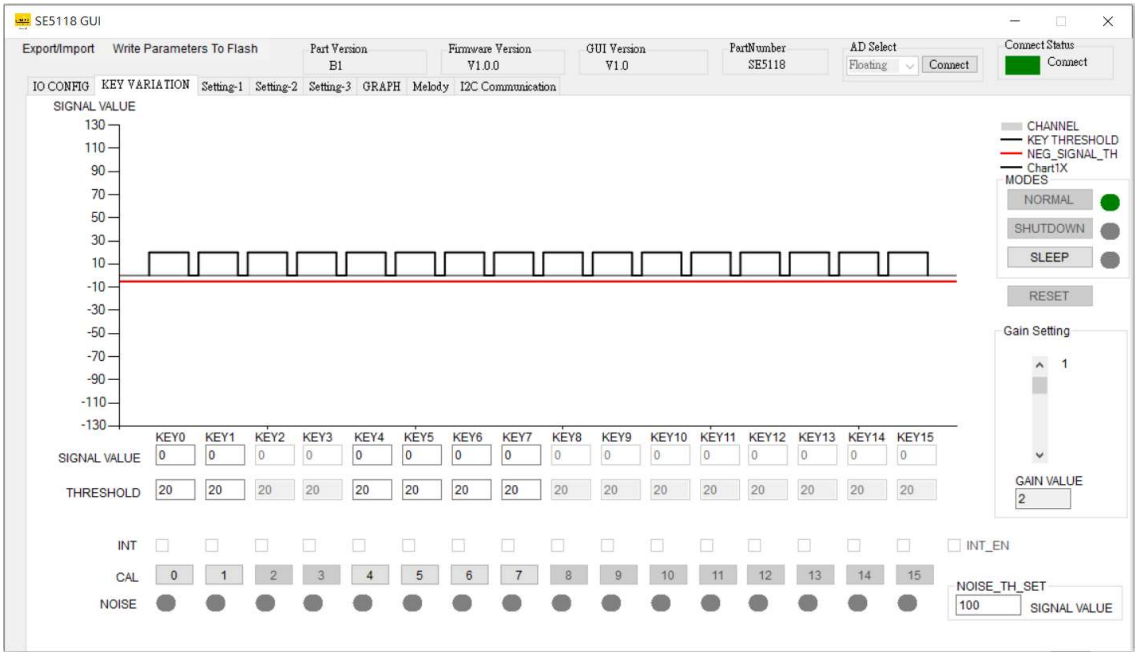
IS31SE5118 GUI is a windows-based Integrated Design Environment (IDE). User can use it to develop touch key applications without firmware coding. With the GUI user can design the touch key system easily. With the GUI you can set or monitor following items:

1. I/O Configuration
2. Key Variation
3. Setting-1, Tune System Parameters
4. Setting-2, Tune System Parameters
5. Setting-3, Tune TK3 System Parameters
6. Graph, Track Touch Key Values
7. Melody, Buzzer/Melody Control
8. I2C Communication

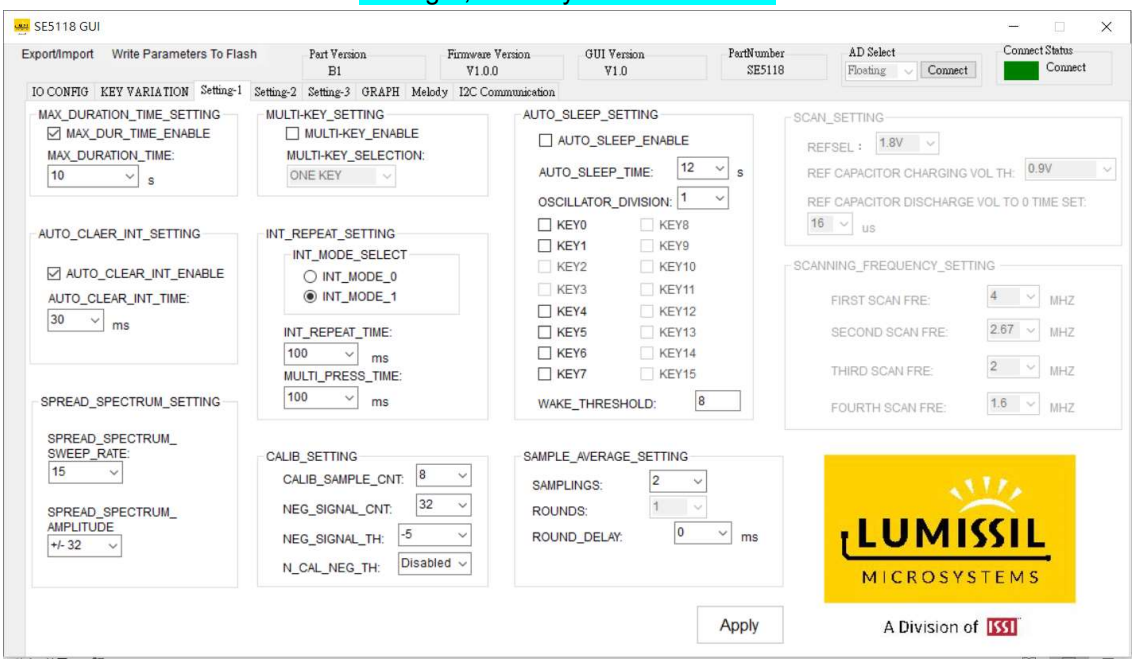
I/O Configuration



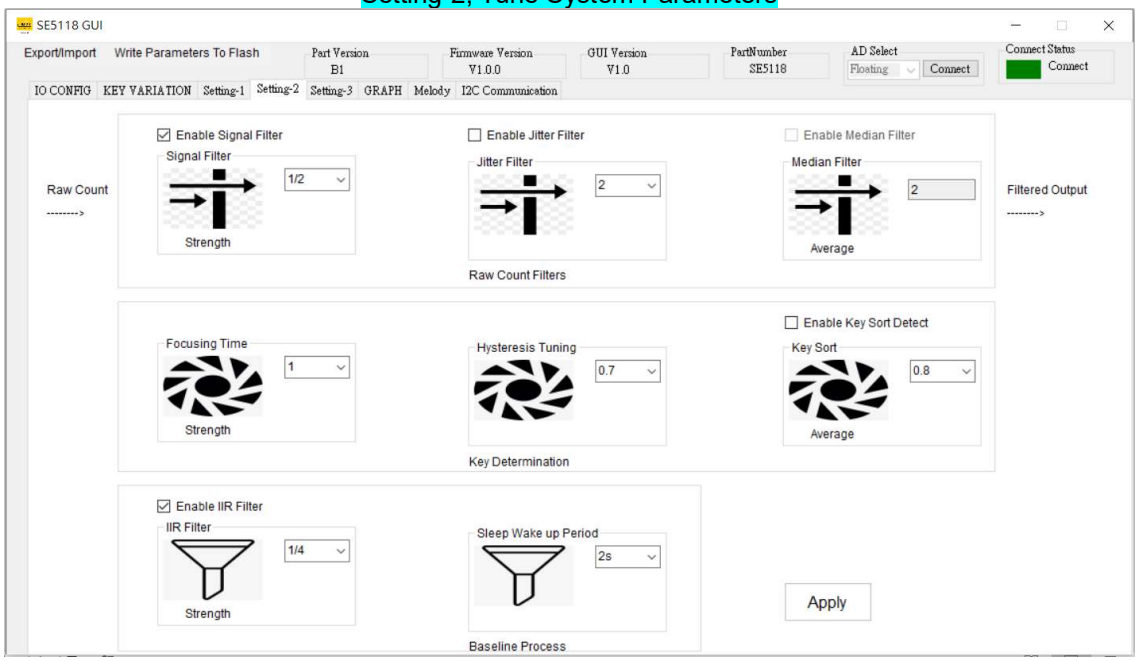
Key Variation



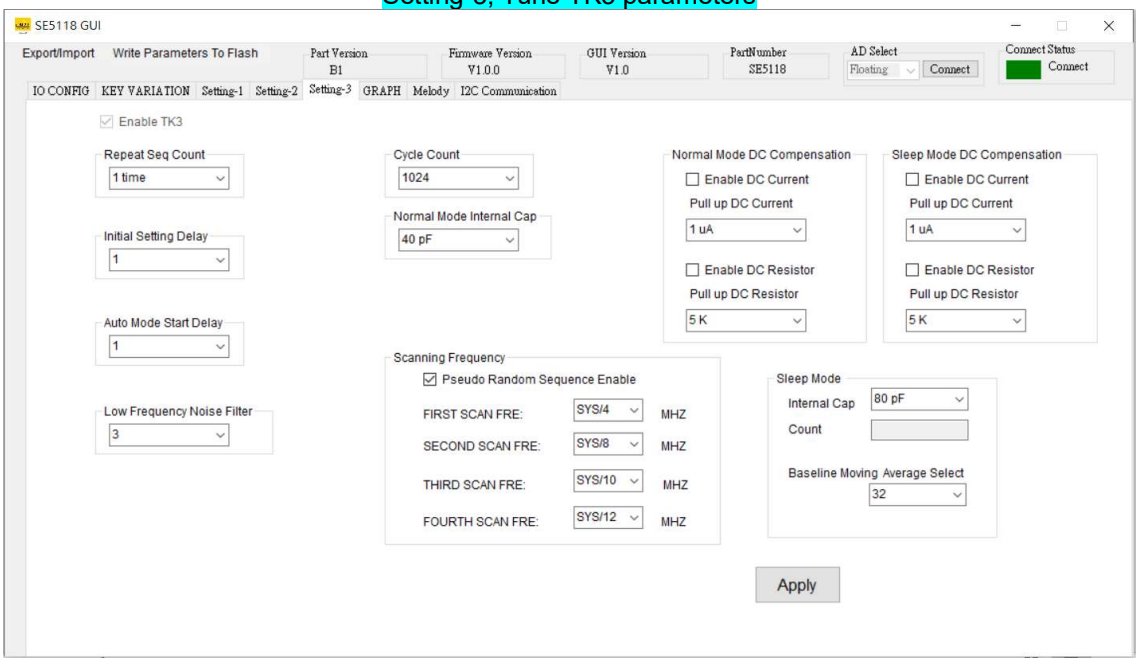
Setting-1, Tune System Parameters



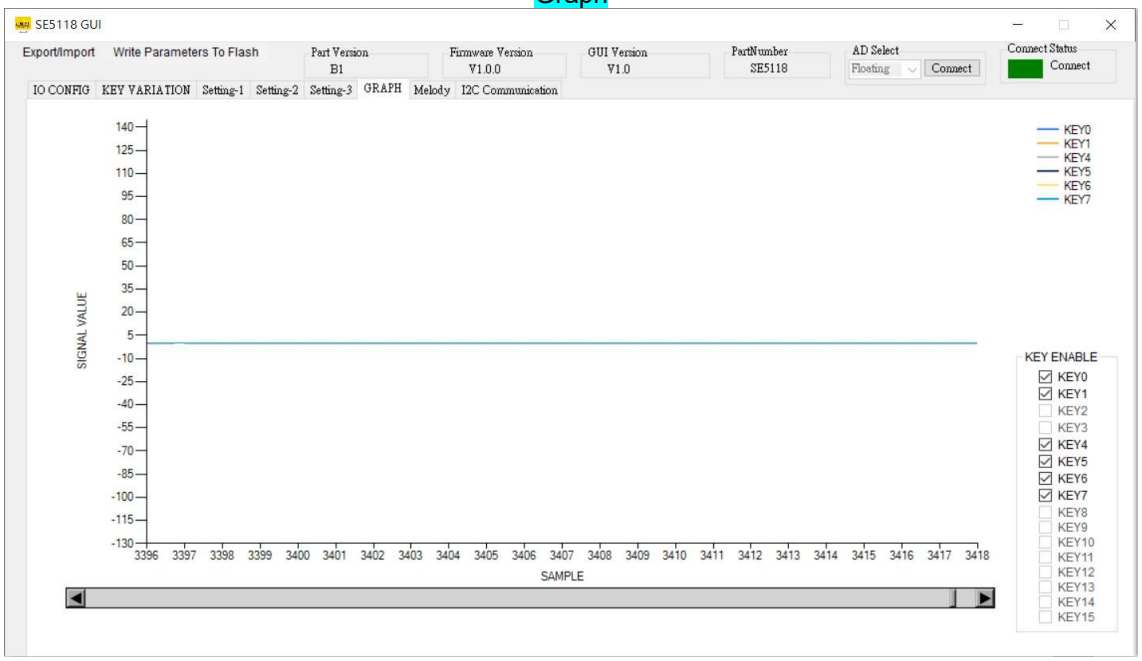
Setting-2, Tune System Parameters



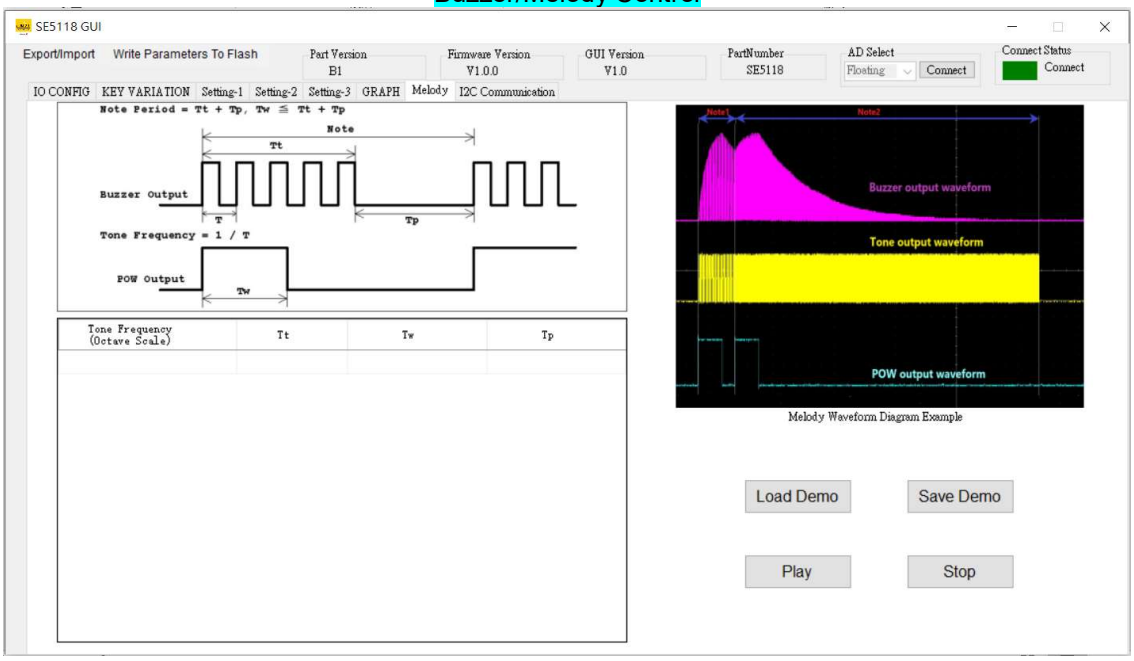
Setting-3, Tune TK3 parameters



Graph



Buzzer/Melody Control



I2C Communication

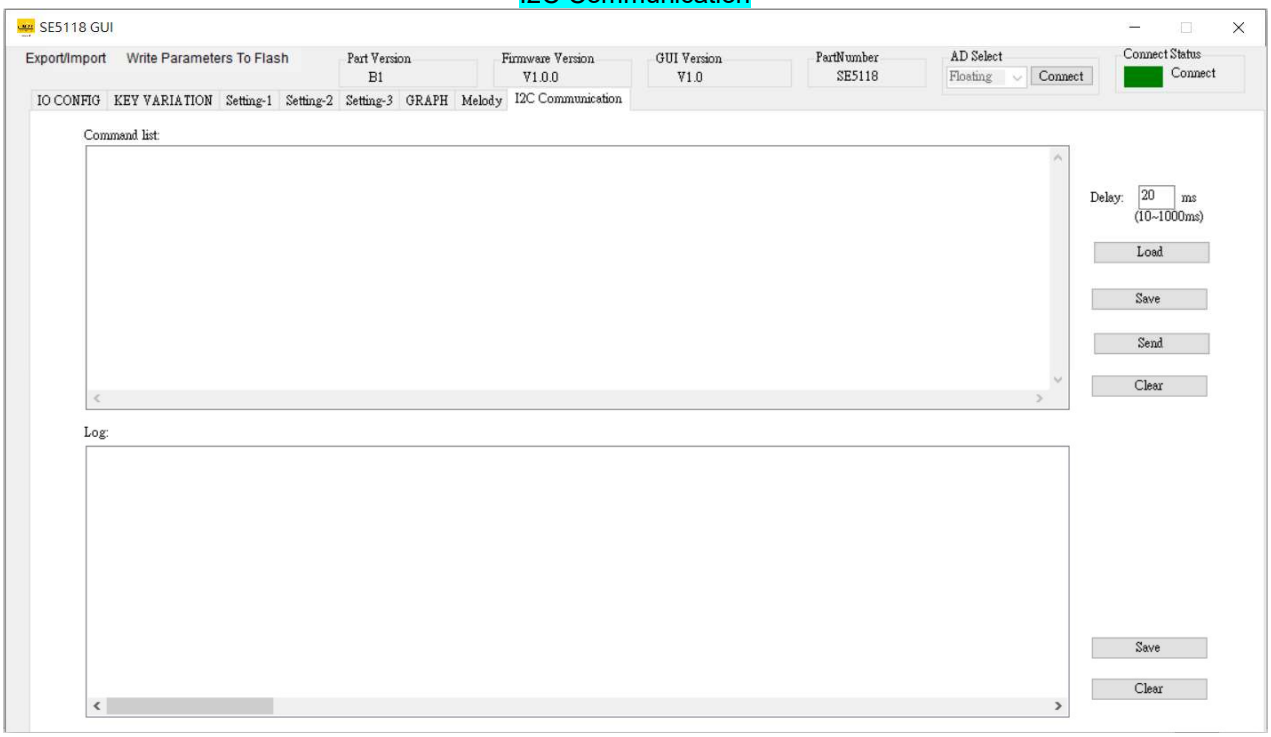


Table 2 Register Function

Address	Name	Function	R/W	Default
00h	Main Control Register	Controls general power states and power dissipation	W	0000 0000
00h	Main Control Register	Return chip's part number	R	0001 1000
01h	INT Configuration Register	Interrupt configuration	R/W	0000 1100
02h	Key Status Register 1	Key0~Key7 status bits	R	0000 0000
04h	Interrupt Enable Register 1	Key0~key7 Enables Interrupts associated with capacitive touch sensor inputs	R/W	0000 0000
06h	Key Enable Register 1	Key0~key7 sets the channels enable		1111 0011
08h	Multiple Touch Key Configure Register	Multiple touch key function setting		0000 0000
09h	Auto-Clean Interrupt Register	Set auto-clean interrupt time and enable		0000 1010
0Ah	Interrupt Repeat Time Register	Set repeat cycle for pressing key interrupt		0010 0010
0Bh	Auto-SLEEP Mode Register	Set auto enter SLEEP Mode time		0000 1111
0Ch	Exit SLEEP Mode Register 1	Set press Key0~Key7 to exit SLEEP Mode		0000 0000

0Eh	Gain and Press Time Setting Register	Set gain and pressing trigger time		0001 1010
0Fh	Key Touch Sampling Configure Register	Set sampling times and cycle time		0001 0000
10h	Calibration Configure Register	Set auto-calibration cycle and negative value trigger setting		0011 0001
11h	Key Calibration Register 1	Key0~Key7 compel calibrate enable set		0000 0000
13h	Noise Threshold Register	Set noise threshold value		0110 0100
14h	Noise Indication Register 1	Key0~Key7 noise indication		0000 0000
16h	Signal/Baseline filter	Touch Key filters. Can adjuster IIR, Jitter		1001 1000
17h	Negative Threshold Register	Set negative threshold and compel calibration threshold		0000 0101
18h	Wake Up Threshold Register	Set wake up threshold		0000 1000
19h	Scan Voltage Register	Set scanning voltage		1000 0000
1Ah	CDTIME Configure Register 1	Set scanning frequency	R/W	0010 0001
1Bh	CDTIME Configure Register 2	Set scanning frequency	R/W	0100 0011
1Ch	TKIII Control Register 1	Set repeat sequence, discard starting edges, inserts an inter-sequence idle time, and low frequency noise filter	R/W	0001 0011
1Dh	TKIII Control Register 2	Set pull-up current enable, internal charge capacitance.	R/W	0011 0000
1Eh	TKIII Control Register 3	Set operation mode, internal charge capacitance, and pull-up resistors	R/W	0111 0000
1Fh	TKIII Control Register 4	TKIII enable, clock stretching, set sleep	R/W	1011 1000
20h~27h	Variation Value Register	Keys delta count value	R	0000 0000
30h~37h	Threshold Set Register	Keys threshold setting	R/W	0001 0100
40h,42h	Calibration Low Bit Register	Internal calibration low 8-bit for KEY0~KEY7	R	0000 0000
41h,43h	Calibration High Bit Register	Internal calibration high 8-bit for KEY0~KEY7	R	0000 0000
7Ch	Set GPIO Shield function 1	Set GPIOs shield mode for KEY0-KEY7	R/W	0000 1000
7Eh	Noise Rejections	Noise filters	R/W	0101 1010

7Fh	Filter Setting Register	Filter setting	R/W	1000 1101
80h-81h	Sleep Mode Register 1 - 2	Sleep mode control related registers	R/W	0000 0000
8Fh	Spread Spectrum Registers	Spread spectrum register	R/W	1111 1100
90h	Version Control Register	Firmware Version Control	R/W	0100 0000
95h-96h	Chip Version Control Register	Chip's Version Control	R	-
F0h	Buzzer Buffer Setting Register	Maximum tone buffer set	R	0000 1010
F0h	Buzzer Buffer Setting Register	Buzzer/Melody commands set	W	0000 0000
F8h-F9h	Buzzer Pin Selection Registers	I/O configuration for Buzzer/Melody Tone	R/W	0000 0100
FAh-FBh	Buzzer Power Pin Selection Registers	I/O configuration for Buzzer/Melody Power	R/W	0000 0000
FCh-FDh	INT Pin Selection Registers	I/O configuration for INT	R/W	0000 0000

00h **Main Control Register (W)**

Bit	D7	D6	D5	D4	D3	D2:D0
Name	SR	RD	SDM	SP	SS	-
Default	0	0	0	0	0	000

SS **Save user defined Parameters**

0 No function

1 Save parameters into Flash.

SR **System Reset**

0 Normal Mode

1 System Reset

RD **Reset all parameters to default**

0 Normal Mode

1 Reset user defined parameters

SDM **Shutdown Mode**

0 Normal Mode

1 Shutdown Mode

SP **Sleep Mode**

0 Normal Mode

1 SLEEP Mode

00h **Main Control Register (R)**

Return Chip's part Number 18h

01h **Interrupt Configuration Register**

Bit	D7:D4	D3	D2	D1	D0
Name	-	MDE	INM	INE	-
Defaul	0000	1	1	0	0

MDEN **Maximum Duration Time Enable**

0 Disable

1 Enable

Maximum press function is used to prevent key pressing all the time by accident. When maximum press function is enabled, once key keep pressing at programmed time the key calibration value will be updated.

INM **Interrupt Mode**

0 Interrupt Mode 0(Touch key trigger once interrupt)

1 Interrupt Mode 1(Touch key trigger repeated interrupt)

INM bit sets interrupt time for once or multiple. Multiple interrupt is used for key pressing detection.

INE **Interrupt Function Enable**

0 Enable

1 Disable

02h **Key Status Register 1 (Read only)**

Bit	D7:D0
Name	KS[7:1]
Defaul	0000 0000

KSx **Key0~Key7 Status**

0 No action

1 Press or release keys

If the value of KSx is detected over programmed threshold, the corresponding bit will be set to "1".

04h **Interrupt Enable Register 1**

Bit	D7:D0
Name	KINT[7:1]
Default	0000 0000

The Interrupt Enable Register determines whether a sensor pad touch or release (if enabled) causes the interrupt pin to be asserted.

KINTx **Key Interrupt Enable**

0 Disable

1 Enable

The default value for Interrupt Enable Registers is interrupt enable. Only set INE bit of Interrupt Configuration Register (01h) to "0", INT pin will generate interrupt signal.

06h **Key Enable Register 1**

Bit	D7:D0
Name	KEN[7:0]
Default	1111 0011

KENx **Touch Key Enable Setting**

0 Disable

1 Enable

08h Multiple Touch Key Configure Register

Bit	D7:D3	D2	D1:D0
Name	-	MKEN	MTK
Default	0000 0	0	00

MKEN **Multi- Key Enable**

0 Disable

1 Enable

MTK **Multi -Key Selection**

01 Allow one key triggered at same time

10 Allow two keys triggered at same time

11 Allow three keys triggered at same time

09h Auto-Clear Interrupt Register

Bit	D7:D4	D3	D2:D0
Name	-	ACEN	ACT
Default	0000	1	010

ACEN **Auto-Clear Interrupt Enable**

0 Disable

1 Enable

ACT **Auto-Clear Interrupt Time**

000 10ms

001 20ms

010 30ms

011 40ms

100 50ms

101 100ms

110 150ms

111 200ms

When ACEN=0, the INT will keep low until MCU read 02h and 03h registers. When ACEN=1, if MCU don't read 02h and 03h registers within programmed time (ACT=10ms~200ms), INT pin will be release automatically.

0Ah Interrupt Repeat Time Register

Bit	D7:D4	D3:D0
Name	INTRT	MPT
Default	0010	0010

INTRT **Interrupt Repeat Time**

0000 Close

0001 50ms

0010 100ms

0011 150ms

0100 200ms

0101 250ms

0110 300ms

0111 350ms

1000 400ms

1001 450ms

1010 500ms

1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

MPT	**Multi-key Press Time**
0000	Close
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

When set the INM as 1 and several keys are pressed, it will generate the second interrupt until M_PRESS_TIME after the first interrupt. Then wait for INT_RPT_TIME to trigger the third interrupt. After all of these if the keys are still pressing, wait for INT_RPT_TIME to trigger others interrupt until keys release.

0Bh Auto-SLEEP Mode Register

Bit	D7	D6:D4	D3:D0
Name	ASEN	OSCD	AST
Defaul	0	000	1111

ASEN	**Auto-SLEEP Enable**
0	Disable
1	Enable

OSCD	**Auto-Sleep Oscillator Division**
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

AST	**Auto-SLEEP Time**
0000	0.5s
0001	1s
0010	1.5s
0011	2s
0100	2.5s
0101	3s
0110	3.5s
0111	4s
1000	4.5s
1001	5s
1010	6s
1011	7s
1100	8s
1101	9s
1110	10s

When ASEN=1 and no actions on touch key and I2C interface, the IC will enter into SLEEP Mode after programmed time (AST).

0Ch Exit SLEEP Mode Register

Bit	D7:D0
Name	ESMEN[7:0]
Default	0000 0000

ESMENx	**Exit Sleep Mode Enable**
0	Touch key can't trigger exiting SLEEP Mode
1	Touch key trigger exiting SLEEP Mode

When IC is in Normal Mode and ASEN=1, set ESMENx=1 will exit from SLEEP Mode by pressing the corresponding key.

0Eh Gain and Press Time Setting Register

Bit	D7:D4	D3:D0
Name	GAIN	MDT
Default	0001	1010

GAIN	**Gain Control**
0000	0.5X
0001	1X
0010	2X
0011	3X
0100	4X
0101	5X

0110	6X
0111	7X
1000	8X
1001	9X
1010	10X
1011	11X
1100	12X
1101	13X
1110	14X
1111	15X

The GAIN bits are used to set the gain factor. Internal count will count the final value and put it into KEYx_ΔCOUNT.

MDT	Max Duration Time
0000	0.5s
0001	1s
0010	2s
0011	3s
0100	4s
0101	5s
0110	6s
0111	7s
1000	8s
1001	9s
1010	10s
1011	11s
1100	12s
1101	13s
1110	14s
1111	15s

MPT bits set the pressing time. When key pressed continue over the programmed time (MDT), system will force to calibrate the pressed key. Set MDEN to "1" will enable this function.

0Fh Key Touch Sampling Configure Register

Bit	D7:D4	D3:D2	D1:D0
Name	SC	-	CDS
Default	0001	-	00

SC is used to set sampling average times for each channel.

Higher SC value will increase stability and anti-interference ability, but decrease reaction speed.

0000	1,
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

CDS	Cycle Delay Time
00	0ms
01	10ms
10	20ms
11	40ms

Sampling 16 channels is for one cycle.

10h Calibration Configure Register

Bit	D7	D6:D4	D3:D2	D1:D0
Name	-	CSC	-	NDC
Default	0	011	00	01

CSC	Calibrate Sample Count
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

If there is no action on keys, environmental capacitance will be calibrated after CSC times.

NDC	Negative Delta Count
00	4
01	8
10	16
11	32

If channel detects the value over negative threshold (NDTH) for NDC times, it will be calibrated forcibly.

11h Individual Force Calibration Register 1

Bit	D7:D0
Name	FCK7:FCK0
Default	0000 0000

FCKx Individual Force Calibrate Key

0 Close

1 Enable

When enable FCKx, the corresponding bit will be set to "1".

13h Noise Threshold Register

Bit	D7:D0
Name	NTH
Default	0110 0100

The noise threshold is from 0~127. It is invalid if NTH>127.

If difference value between samplings is over the programmed threshold, the corresponding noise bit will be set to "1".

14h Noise Indication Register

Bit	D7:D0
Name	NK7:NK0
Default	0000 0000

NKx Noise Indication

0 No noise

1 Noise

16h TK Filter

Bit	D3	D2	D1:D0
Name	BLIIR	-	TKMA
Default	1	-	01

Bit	D7	D6	D5	D4
Name	SIGIIR	SIGM	SIGJ	-
Default	1	0	0	-

TKMA TK Moving Average

00 32 average

01 64 average

10 128 average

11 256 average

Hardware baseline slow moving average setting

BLIIR TK IIR Filter for Baseline

0 Disable BLIIR

1 Enable BLIIR

SIGJ Signal Jitter Filter

0 Disable jitter filter

1 Enable jitter filter

SIGM Signal Median Filter

0 Disable SIGM filter

1 Enable SIGM filter

SIGIIR Signal IIR filter

0 Disable IIR filter

1 Enable IIR filter

17h Negative Threshold Register

Bit	D3:D0	D3:D0
Name	NCTH	NDTH
Default	0000	1001

NCTH Negative Calibrate Threshold Setting.

0000 Disable

0001 -10

0010 -20

0011 -30

0100 -40

0101 -50

0110 -60

0111 -70

1000 -80

1001 -90

1010 -100

1011 -110

1100 -120

1101 NA

1110 NA

1111 NA

When negative value is over the programmed threshold (NCTH), the channel will be calibrated forcibly.

NDTH	Negative Delta Threshold Setting
0000	Disable
0001	-1
0010	-3
0011	-4
0100	-5
0101	-6
0110	-7
0111	-8
1000	-9
1001	-10
1010	-11
1011	-12
1100	-13
1101	-14
1110	-15
1111	-16

When negative value is over the programmed threshold (NCTH), the channel will be calibrated forcibly.
If negative value is detected over threshold for NDTH times continually, the channel will be calibrated forcibly.

18h Wake Up Threshold Register

Bit	D7	D6:D0
Name	-	WTH[6:0]
Default	0	000 1000

Wake up threshold range from 0 to 127

19h Scan Voltage Register

Bit	D7:D3	D2:D0
Name	-	CCNT
Default	-	000

CCNT	Cycle Count of Each Conversion Sequence
000	1024
001	2048
010	4096
011	8192
100	12288
101	16384
110	32768
111	65536

1Ah Scanning Frequency Set

Bit	D7:D4	D3:D0
Name	Second scan frequency (SSF)	First scan frequency (FSF)
Default	0010	0001

Scanning frequency	First scan frequency
0000	8 MHZ
0001	4 MHZ
0010	2.67 MHZ
0011	2 MHZ
0100	1.6 MHZ
0101	1.33 MHZ
0110	1.14 MHZ
0111	1 MHZ
1000	0.89 MHZ
1001	0.8 MHZ
1010	0.73 MHZ
1011	0.67 MHZ
1100	0.62 MHZ
1101	0.57 MHZ
1110	0.53 MHZ
1111	0.5M HZ

Scanning frequency	Second scan frequency
0000	8 MHZ
0001	4 MHZ
0010	2.67 MHZ
0011	2 MHZ
0100	1.6 MHZ
0101	1.33 MHZ
0110	1.14 MHZ
0111	1 MHZ
1000	0.89 MHZ
1001	0.8 MHZ
1010	0.73 MHZ
1011	0.67 MHZ
1100	0.62 MHZ
1101	0.57 MHZ
1110	0.53 MHZ
1111	0.5M HZ

1Bh Scanning Frequency Set

Bit	D7:D4	D3:D0
Name	Fourth scan frequency (OSF)	Third scan frequency (TSF)
Default	0100	0011

Scanning frequency	Third scan frequency
0000	8 MHZ
0001	4 MHZ
0010	2.67 MHZ

0011	2 MHZ
0100	1.6 MHZ
0101	1.33 MHZ
0110	1.14 MHZ
0111	1 MHZ
1000	0.89 MHZ
1001	0.8 MHZ
1010	0.73 MHZ
1011	0.67 MHZ
1100	0.62 MHZ
1101	0.57 MHZ
1110	0.53 MHZ
1111	0.5M HZ

Scanning frequency	Fourth scan frequency
0000	8 MHZ
0001	4 MHZ
0010	2.67 MHZ
0011	2 MHZ
0100	1.6 MHZ
0101	1.33 MHZ
0110	1.14 MHZ
0111	1 MHZ
1000	0.89 MHZ
1001	0.8 MHZ
1010	0.73 MHZ
1011	0.67 MHZ
1100	0.62 MHZ
1101	0.57 MHZ
1110	0.53 MHZ
1111	0.5M HZ

1Ch TKIII Control1

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT[1:0	INI[1:0]	ASTDL	LFNF
Default	00	01	00	11

LFNF Low Frequency Noise Filter Setting

Low Frequency Noise Filter Setting

00 disable LFNE

Noise injection longer than LFNF[1-0]*8 time is ignored.

ASTDLY Auto Mode Start Delay

ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0]+1) * 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.

INI Initial Setting Delay

INI[1-0] defines the number of TKCLK period for initial settling of CREF. The delay is (INI[1-0] + 1) *4*TKCLK.

RPT	Repeat Sequence Count
00	No repeat
01	Repeat 4 times
10	Repeat 8 times
11	Repeat 16 times

1Dh TKIII Control2

Bit	D7	D6:D4	D3:D0
Name	PUREN	CCHG	PU[3:0]
Default	0	011	0000

PUREN	Pull up DC Current Enable
0	disable pull up DC current
1	enable pull up DC current

CCHG	Internal Reference Capacitance Select
000	10pF
001	20pF
010	30pF
011	40pF
100	50pF
101	60pF
110	70pF
111	80pF

PU	Pull up DC Current
1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

1Eh TKIII Control3

Bit	D7	D6:D4	D3:D0
Name	PUREN	SCCHG	SPU[3:0]
Default	0	111	0000

PUREN	Pull up DC Current Enable in Sleep Mode
0	disable pull up DC current
1	enable pull up DC current

SCCHG Internal Reference Capacitance Select in Sleep Mode

000 10pF
001 20pF
010 30pF
011 40pF
100 50pF
101 60pF
110 70pF
111 80pF

SPU Pull up DC Current in Sleep Mode

1000 Enable 8uA current source.
0100 Enable 4uA current source.
0010 Enable 2uA current source.
0001 Enable 1uA current source.

1Fh TKIII Control 4

Bit	D3	D2:D1	D0
Name	-	FOT	TK3AS
Default	-	00	0

Bit	D7	D6	D5	D4
Name	TK3E	CLKS	PRS	TK3S
Default	1	0	1	1

TK3AS Enable TK3 Auto Sleep Mode

0 disable TK3 Auto Sleep Mode
1 enable TK3 Auto Sleep Mode

FOT Focus Times

How many consecutive

00 2 times
01 3 times
10 4 times
11 5 times

TK3S TK3 Sleep

Set wake up threshold before entering sleep mode (put the baseline count on Sleep Count Registers)

0 disable TK3S
1 enable TK3S

PRS Pseudo Random Sequence (only for TKIII)

0 disable PRS
1 enable PRS

CLKS Clock Stretching (For I2C)

0 disable stretching
1 enable stretching

TK3E TK3 Enable

0 enable TK2
1 enable TK3

20h~27h KEY0~KEY7 Variation Value Register

Bit	D7	D6:D0
Name	SIGN	KEYx_ΔCOUNT
Default	0	000 0000

SIGB Sign bit

0 Positive
1 Negative

KEYx_ΔCOUNT Key Value Count

30h~37h KEY0~KEY7 Threshold Set Register

Bit	D7	D6:D0
Name		KEYx_TH
Default	0	001 0100

KEYx_TH Key Threshold

0~127

40h, 42h … 4Ch, 4Eh KEY0~KEY7 Calibration Low Byte Register (Read Only)

Bit	D7:D0
Name	KEYX_CAL_L
Default	0000 0000

41h, 43h … 4Dh, 4Fh KEY0~KEY7 Calibration High Byte Register (Read only)

Bit	D7:D0
Name	KEYX_CAL_H
Default	0000 0000

KEYX_CAL_H/L Information of baseline calibration for each key.

7Ch Shield Setting Register 1

Bit	D7:D1
Name	SHDE [7:0]
Default	0000 1000

SHDE Shield Enable (only for bit0 and bit3)
0 disable shield driver
1 enable shield driver

7Eh Noise Rejections Setting Register

Bit	D3	D2:D0
Name	NIBF	IBP[2:0]
Default	1	010

Bit	D7:D6	D5:D4
Name	ISP[1:0]	NIBP[1:0]
Default	01	01

IBP **IIR Baseline Parameters.**
000 1
001 1/2
010 1/4
011 1/8
100 1/16
101 1/32
110 1/64
111 1/128

NIBF Negative IIR Baseline Flag
0 disable Negative IIR
1 detect negative sensing values

NIBP Negative IIR Parameters
00 1
01 2
10 -1
11 -2

ISP IIR Sensing Parameters
00 1
01 1/2
10 1/4
11 1/8

7Fh Filter Parameter Register

Bit	D4:D3	D2	D1:D0
Name	JD	MR	SD
Default	01	1	01

Bit	D7:D6	D5
Name	HYP	SORT
Default	10	0

SD Sort Delta Parameters
00 1
01 0.8
10 0.6
11 0.4

MR Multiple Rate
0 disable MR
1 enable MR
Multiple rate is used for frequency hopping

JD Jitter Delta
00 1
01 2
10 3
11 4

SORT **A**nti-threshold Sorting
0 disable sorting
1 enable sorting

HYP Hysteresis Parameters
00 0.9
01 0.8
10 0.7
11 0.6

80h Sleep Mode Count Register 1

Bit	D7:D1
Name	SLPC [7:0]
Default	0000 0000

81h Sleep Mode Count Register 2

Bit	D67D0
Name	SLPC [15:8]
Default	0000 0000

SLPC **Sleep Mode Count**
Read only, reference value

8Fh Spread Spectrum Register

Bit	D7:D1		
Name	SSR[3:0]	SSA[1:0]	-
Default	1111	11	-

SSS Spread Spectrum Setting Register

Spread spectrum is a technique by which electromagnetic energy produced over a particular bandwidth is spread in the frequency domain. Two parameters are listed as follows:

SSR [3:0] defines the spread spectrum sweep rate. If the SSR[3:0]=0, then spread spectrum is disabled

SSA[1:0] defines the amplitude of spread spectrum frequency change. The frequency is changed by adding SSA[1:0] range to the actual internal OSC control reqtister.

00 +/- 32

01 +/1 16

10 +/- 8

11 +/- 4

90h Version Control Register 6

Bit	D7:D0		
ame	VCR1 [1:0]	VCR2[2:0]	VCR3[2:0]
Default	01	000	000

VCR Version Control Reister

SSMR [7:0] is used to do slider calibration. User can enable the calibration via GUI.

95h Chip Version Control Register 1

Bit	D7:D1
Name	CVR1 [7:0]
Default	-

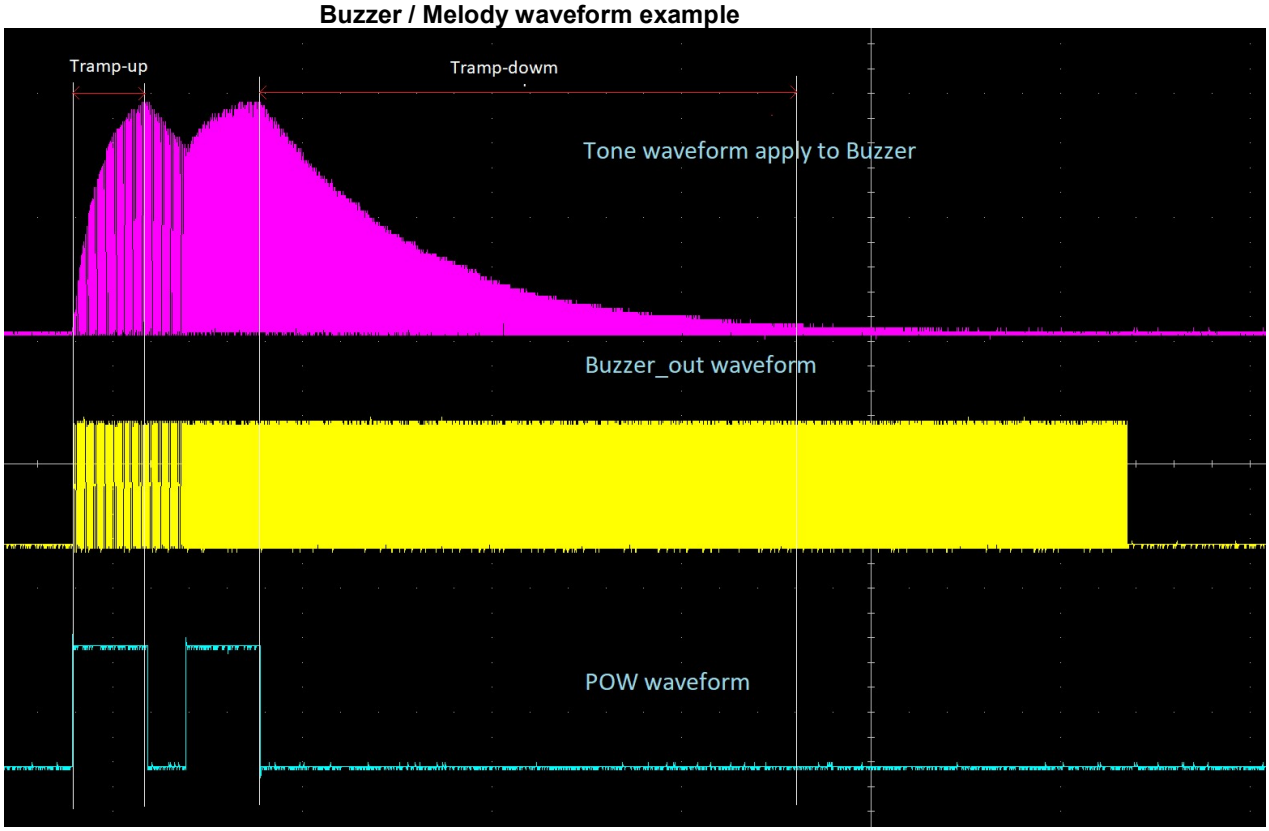
96h Chip Version Control Register 2

Bit	D7:D0
Name	CVR2 [15:8]
Default	

CVR Chip Version Register

These 2 bytes contain chip revision. The first byte indicates mask set version. The 2nd byte indicates minor revision.

Buzzer / Melody waveform example

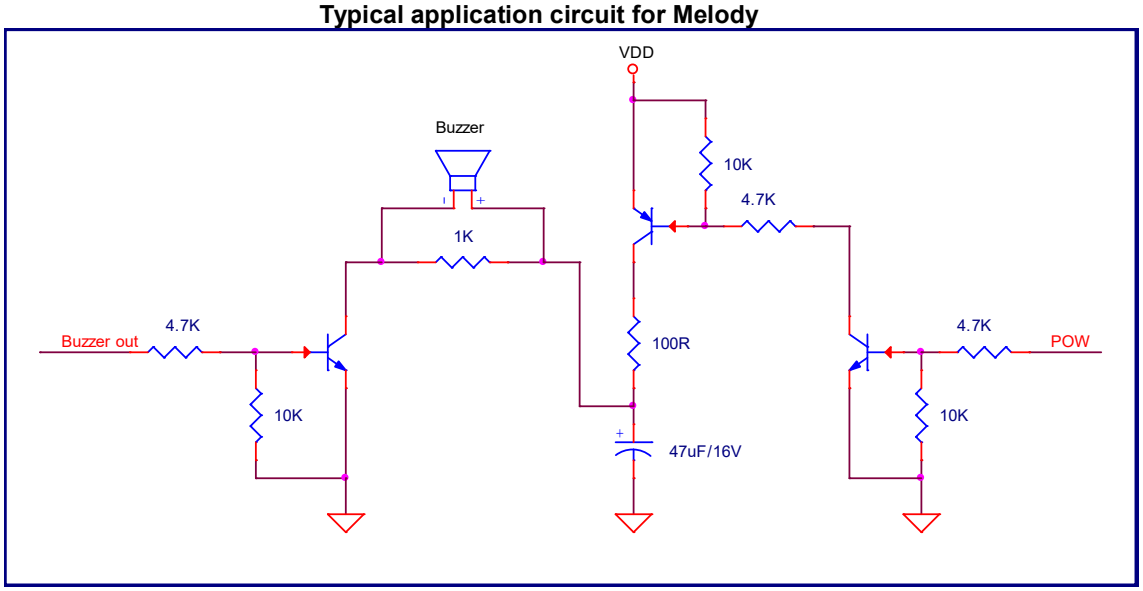


Note:

$T_{ramp-up}$: 100R decides the signal ramp up rate.

$T_{ramp-down}$: The signal ramp down due to POW is low and 47uF capacitor decide the ramp down rate.

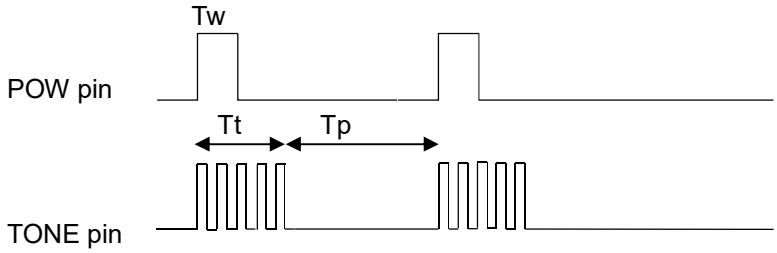
Typical application circuit for Melody



F0h Buzzer/Melody Register (W)

Bit	N*(4 byte)
Name	BMRR
Default	-

1st byte	2nd byte	3rd byte	forth byte
Scale ID	Tt	Tw	Tp



Tt, Tw and Tp range from 0 to 255 @ 4ms time unit

A Tone play duration is defined as Tt + Tp

The support scale from 3A to 8G#

Frequencies for equal-tempered scale, A**4** = 440 Hz "Middle C" is C4												
	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%

	6	freq	divisor	freq error	7	freq	divisor	freq error	8	freq	divisor	freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%

C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%
D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B ….

F0h Buzzer/Melody Register (W)

Bit	D7:D0 = 0xFF
Name	BMRR
Default	-

Clear Melody buffer and stop play

F0h Buzzer/Melody Register (R)

Bit	D7:D0
Name	BMRR
Default	-

BMMR Buzzer/Melody Register Read. It shows the available tone buffer size. SE5118 has 10 note buffer built-in.

I2C command format (each node is composed of 4 byte data, the incomplete note will be ignored, and the incoming note data will be ignored if the FIFO is full)

0x78, 0xF0, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp), ….

0x78, 0xF0, 0xFF stop the melody play and clear the FIFO

0x78, 0xF0 set the register number to 0xF0

0x79 read FIFO remain length

F8h Buzzer Pin Select Register 1

Bit	D7:D0
Name	BPS1 [7:0]
Default	0000 0100

F9h Buzzer Pin Select Register 2

Bit	D0
Name	BPS2 [0]
Default	0

BPS1/2 Buzzer output Select 1/2

BPS1[7:0] maps to KEY[7:0], write 1 will enable the related Key as Buzzer output

BPS2[0] maps to P13, write 1 will enable P13 as Buzzer output

FAh Enable Buzzer Power Register 1

Bit	D7:D0
Name	EBP1 [7:0]
Default	0000 0000

FBh Enable Buzzer Power Register 2

Bit	D0
Name	EBP2 [0]
Default	1

EBP1/2 Buzzer Power Select ½

EBP1[7:0] maps to KEY[7:0], write 1 will enable the related Key as Buzzer Power

EBP2[0] maps to P13, write 1 will enable P13 as Buzzer Power

FCh INT Pin Select Register 1

Bit	D7:D0
Name	IPS1 [7:0]
Default	0000 0000

FDh INT Pin Select Register 2

Bit	D0
Name	IPS2 [8:8]
Default	0

IPS1/2 INT Pin Select ½

IPS1[7:0] maps to KEY[7:0], write 1 will enable the related Key as INT

IPS[0] maps to P13, write 1 will enable P13 as INT.

GENERAL DESCRIPTION

The IS31SE5118 is an ultra-low power, fully integrated 8-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic.

SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor

or internal register.

The value of capacitor is higher the sensitivity is lower; value of capacitor is lower the sensitivity is higher.

INTERRUPTION

The changing of action can be signed by the INT pin. The INT pin will be driven to low when sensitivity channel is pressed or released.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SDM bit of the Configuration Register (00h) to “1”, the IS31SE5118 will operate in software shutdown mode.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	 150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

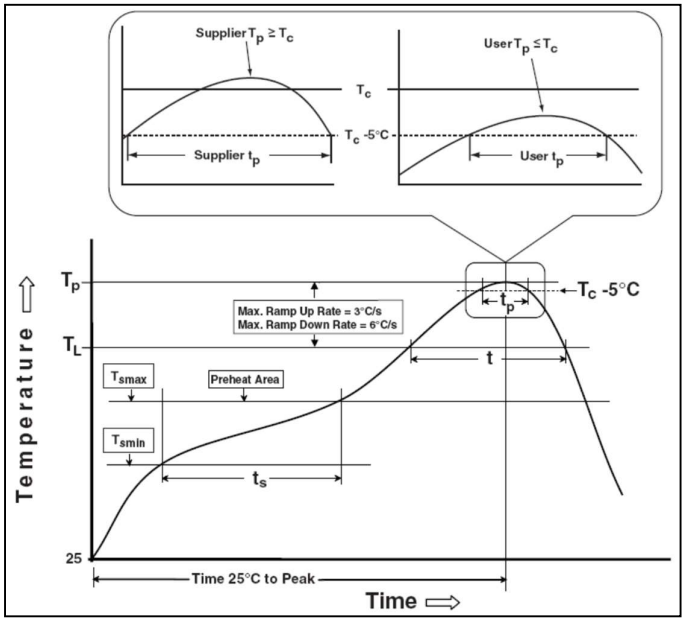
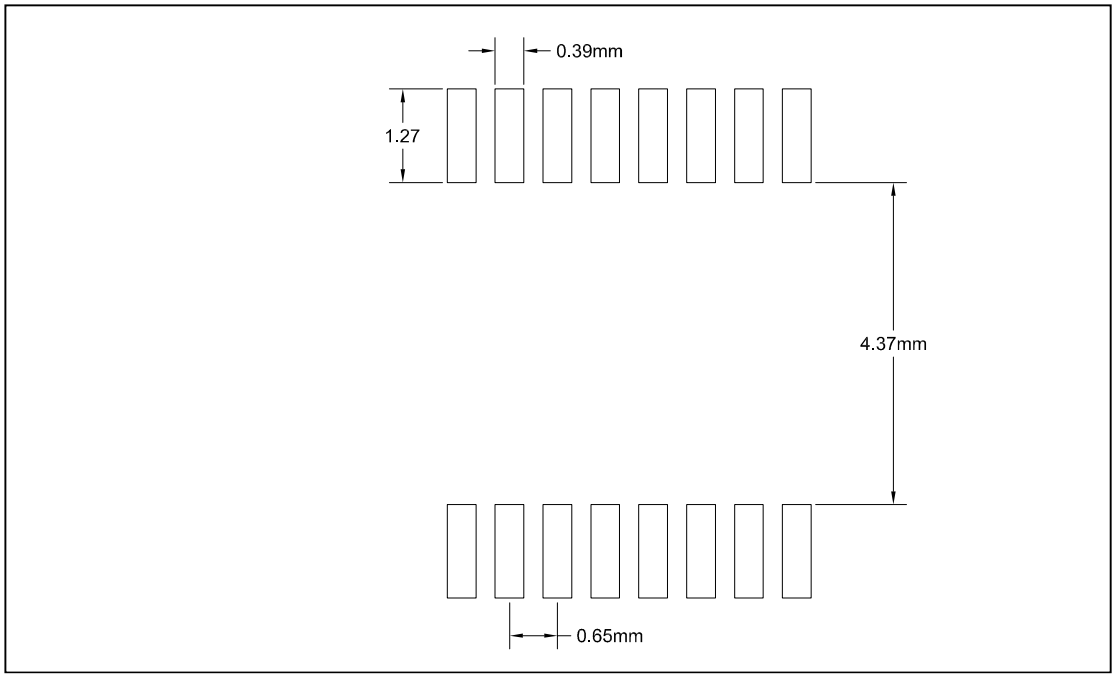


Figure 6 Classification Profile

PACKAGE INFORMATION

TSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release.	2020.06.06