SSI 32P544
Read Data Processor and Servo Demodulator

December 1992

DESCRIPTION

The SSI 32P544 Read Data Processor and Servo Demodulator has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

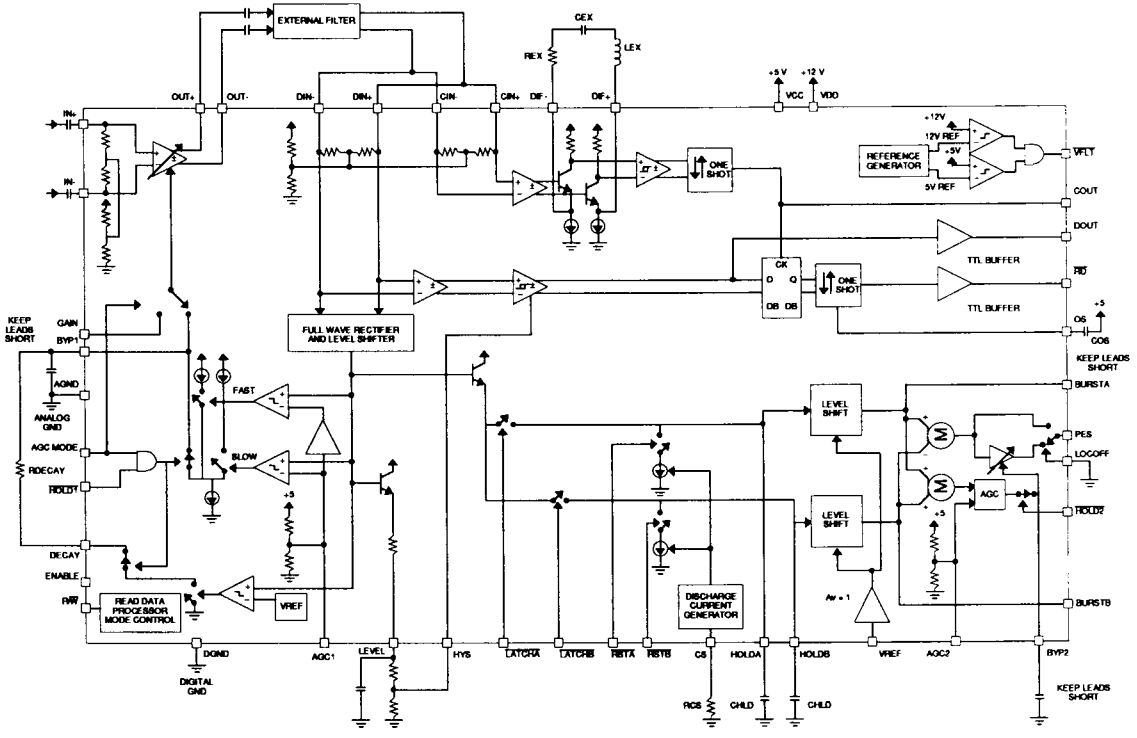
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant imput amplitude for the level qualifier. Level qualification can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

FEATURES

- **Wide bandwidth AGC input amplifier**
- **Level qualification supports MFM and RLL encoded data retrieval**
- **Fast and slow AGC attack and decay regions for fast transient recovery**
- **Embedded servo channel provides servo burst capture and difference circuits**
- **Local servo AGC provided based on servo burst output amplitude sum**
- **Standard ±10%, 12V and 5V supplies**
- **Write to Read transient suppression**

BLOCK DIAGRAM



DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by an AGC signal based on maintaining the amplitude of the sum of both channels.

The circuit also provides a voltage fault flag that indicates a low voltage condition on either supply.

The SSI 32P544 requires standard ±10% tolerance +5V and +12V supplies and is available in a 44-pin PLCC package.

CIRCUIT OPERATION

READ MODE

In Read Mode the SSI 32P544 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and an error signal based on amplitude comparison is made available.

DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

Two attack modes are entered depending on the instantaneous level at DIN±. For DIN± levels above 125% of desired level a fast attack mode is invoked that supplies 1.7 mA charging current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charging current. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is in range.

Two decay modes are available that apply a discharge current to the BYP1 pin network when DIN± falls below the desired level. An internal decay current sink will supply 4.0 µA of discharge current. Also, if |(DIN+) - (DIN-)| is above 200 mV0-pk a decay current, controlled by a resistor from BYP1 to DECAY, is switched in to decrease decay time. The amount of charge pulled from the AGC timing capacitor on each data pulse is:

$$Q_{DECAY} = K_1(Ton + Ts)/R_{DECAY}$$

Where:

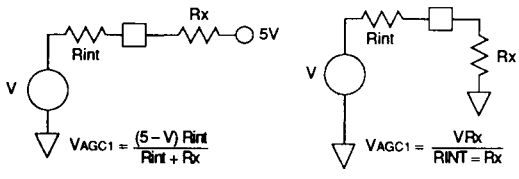
K_1 = 4.0V typ.

Ton = Time in seconds that the data pulse at DIN± is greater than 200 mVop

Ts = Switching time in seconds (<2 µs, max)

The AGC1 pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp at nominal conditions. The AGC1 voltage can be modified by tying a resistor between AGC1 and ground or VCC. A resistor to ground decreases the voltage level while a resistor to VCC increases it. The resultant AGC1 voltage level is:

Where:



V = Voltage at AGC1 with pin open (2.2V, nom.)

Rint = AGC1 pin input impedance (6.7 kΩ, typ.)

Rx = External resistor.

The new DIN± input target level is nominally 0.48 Vpp/ V_{AGC1}

The AGC amplifier can swing 3.0 Vpp at OUT± which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

Gain of the AGC amplifier is nominally:

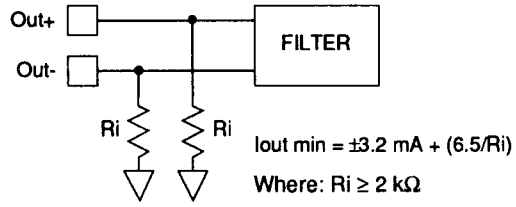
$$Av1/Av2 = e^{[6.9\,(V2 - V1)]}$$

Where:

Av1, Av2 are initial and final amplifier gains.

V1, V2 are initial and final voltages on the BYP1 pin.

The minimum output current from the AGC amplifier is ±3.2 mA. In cases where more current is required to drive a low impedance load the current can be increased by connecting load resistors Ri from OUT± to GND, as shown below.



One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 2.0 V0-pk nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 1.0 V0-pk at the HYS pin. This will result in a nominal ±0.210V threshold or a 42% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin provides a buffered TTL compatible comparator output signal for testing purposes or for use in the servo circuit if required.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-1000(Abuf)(Cs)}{2LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components
20 pF < C < 150 pF
Abuf = Gain From CIN± to DIF±
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width. Width is controlled by an external capacitor from the OS pin to VCC.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Several methods are made available for maintaining channel gain during servo signal processing.

SERVO READ MODE (Continued)

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low for a sample period. Additionally, a hold capacitor discharge current of up to 1.0 mA can be turned on by pulling $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low. The discharge current is determined by a resistor tied between CS and ground. Its magnitude is:

$$I_{CS} = 2.6/(R_{CS} + 750)\ A, \text{ typ.}$$

Where: R_{CS} = resistor from CS to ground

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

As noted, several methods are used to determine channel gain in Servo Read Mode. These methods make use of the data read mode AGC loop, the servo AGC loop and external or fixed AGC loop gain. Two methods are used that control the channel gain based on maintaining the sum of A & B channel amplitudes.

In one case (see Figure 1) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{\text{HOLD2}}$ pin is pulled high. The current magnitude and direction is determined by:

$$I_C = K_4[(K_5 \cdot V_{AGC2}) - Va(DIN)pp - Vb(DIN)pp]$$

Where:

V_{AGC2} = AGC2 pin voltage

K_4 = 650 µA/Vpp

K_5 = 0.39 V/V

Va/b(DIN)pp = peak to peak A or B servo pattern Signal voltages at DIN±

The other case (see Figure 2) controls the channel by fixing the Read Data channel gain by taking $\overline{\text{HOLD1}}$ low and closing the loop about the Servo Channel AGC (LOCOFF is held low for this mode).

$\overline{\text{HOLD2}}$ is used to update the control voltage on the AGC capacitor at the BYP2 pin. This AGC function has a time constant defined by:

$$\text{Time Constant} = K_6 \cdot C_{BYP2}$$

Where: K_6 = 1.64 to 7.5 kΩ

C_{BYP2} = BYP2 pin capacitor value in farads

Another method (see Figure 5) uses either a fixed voltage at the GAIN pin to determine channel gain or a gain based on preamble data amplitude. In this case no AGC methods are used that are based on servo signal amplitudes. Gain, as determined by an external voltage has been covered above. In the preamble method $\overline{\text{HOLD1}}$ is taken low during a preamble and the channel gain, determined by that necessary to maintain DIN± as programmed by the AGC1 voltage, is held during servo data processing.

WRITE MODE

In Write Mode the SSI 32P544 is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is set to maximum and the AGC amplifier input impedance is reduced.

Resetting the AGC amplifier gain and input impedance shortens system Write to Read recovery times. With the AGC gain at maximum when returning to Read mode the AGC loop is in fast attack mode.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P544 and a read preamplifier such as the SSI 32R510A. Write to read timing is controlled to maintain the reduced impedance for 1.2 to 3.0 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking ENABLE pin low selects this mode. Recovery from this state can be slow due to the necessity of charging external capacitors.

LOW VOLTAGE FAULT DETECTION

A low voltage detection circuit monitors both supplies and pulls an open collector TTL output low whenever either supply drops below their trip point.

MODE CONTROL

The SSI 32P544 circuit mode is controlled by the ENABLE, R/$\overline{\text{W}}$, AGCMODE, $\overline{\text{HOLD1}}$, $\overline{\text{HOLD2}}$, and LOCOFF pins as shown in Table 1.

Data Read Mode

AGC active and controlled by data, Digital section active

Data Read Mode, Hold

AGC gain held constant, Digital section active. Gain will drift higher at rate determined by C_{BYP1} and Hold mode discharge current.

Servo Read Mode I (See Figures 1 & 3)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

Servo Read Mode II (See Figures 2 & 4)

Read amplifier AGC gain held fixed ($\overline{HOLD1}$ low). Servo AGC loop activated with $\overline{HOLD2}$ toggled to update or hold gain based on a constant servo signal sum.

Servo Mode III (See Figure 5)

Read channel gain determined by voltage on GAIN pin.

Write

Read amplifier input impedance reduced. BYP1 pin voltage pulled low to select maximum amplifier gain. Digital section deactivated.

Power Down

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held subject to Hold mode discharge current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher.

TABLE 1: SSI 32P544 Circuit Mode Control

ENABLE	R/$\overline{W}$	AGC MODE	$\overline{HOLD1}$	$\overline{HOLD2}$	LOCOFF	READ PATH MODES
1	1	1	1	-	-	Data Read Mode
1	1	1	0	-	-	Data Read Mode Hold
1	1	0	-	1	1	Servo Read Mode I
1	1	0	-	0	1	
1	1	1	0	0	0	Servo Read Mode II
1	1	1	0	1	0	
1	1	0	-	-	-	Servo Mode III
1	0	-	-	-	-	Write
0	-	-	-	-	-	Power Down

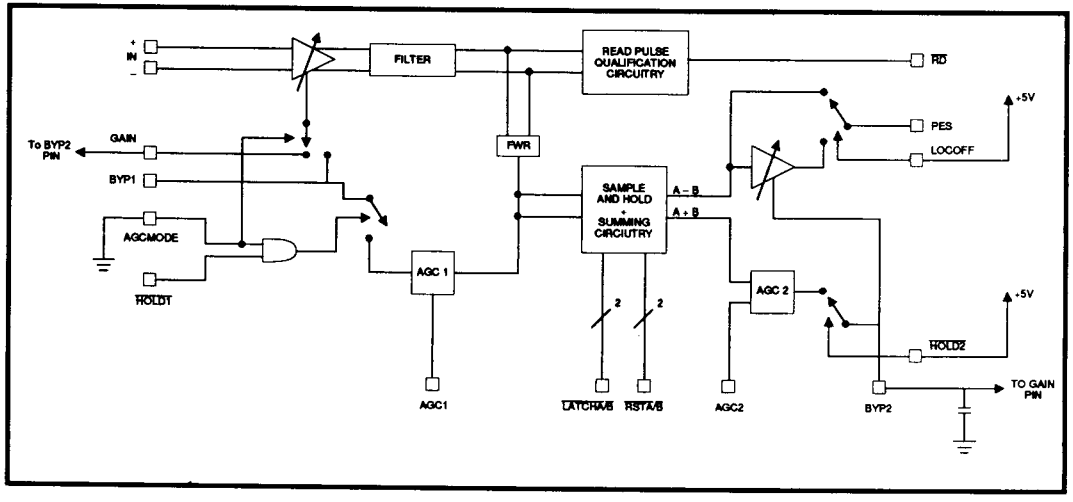


FIGURE 1: Servo Read Mode I

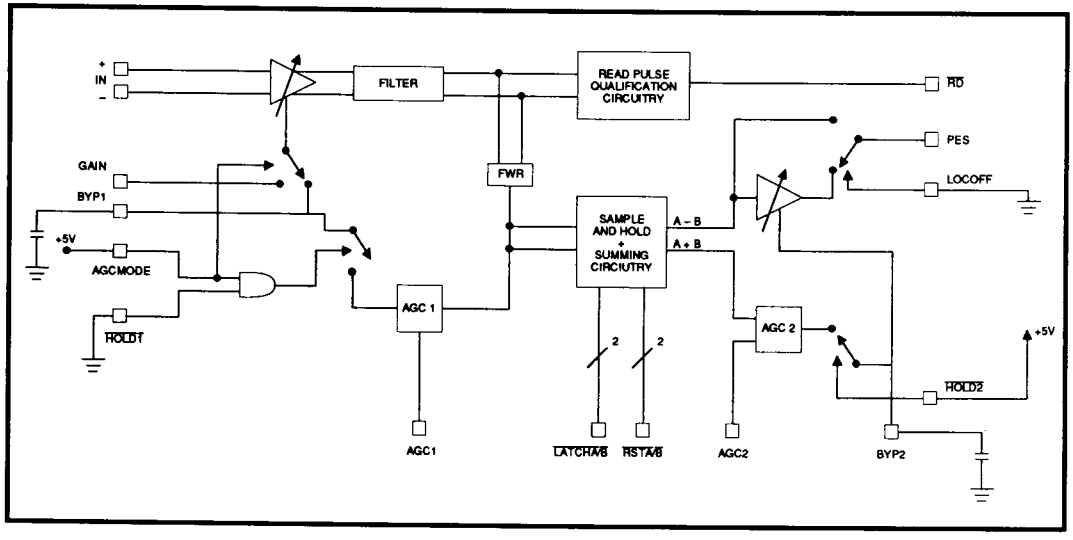


FIGURE 2: Servo Read Mode II

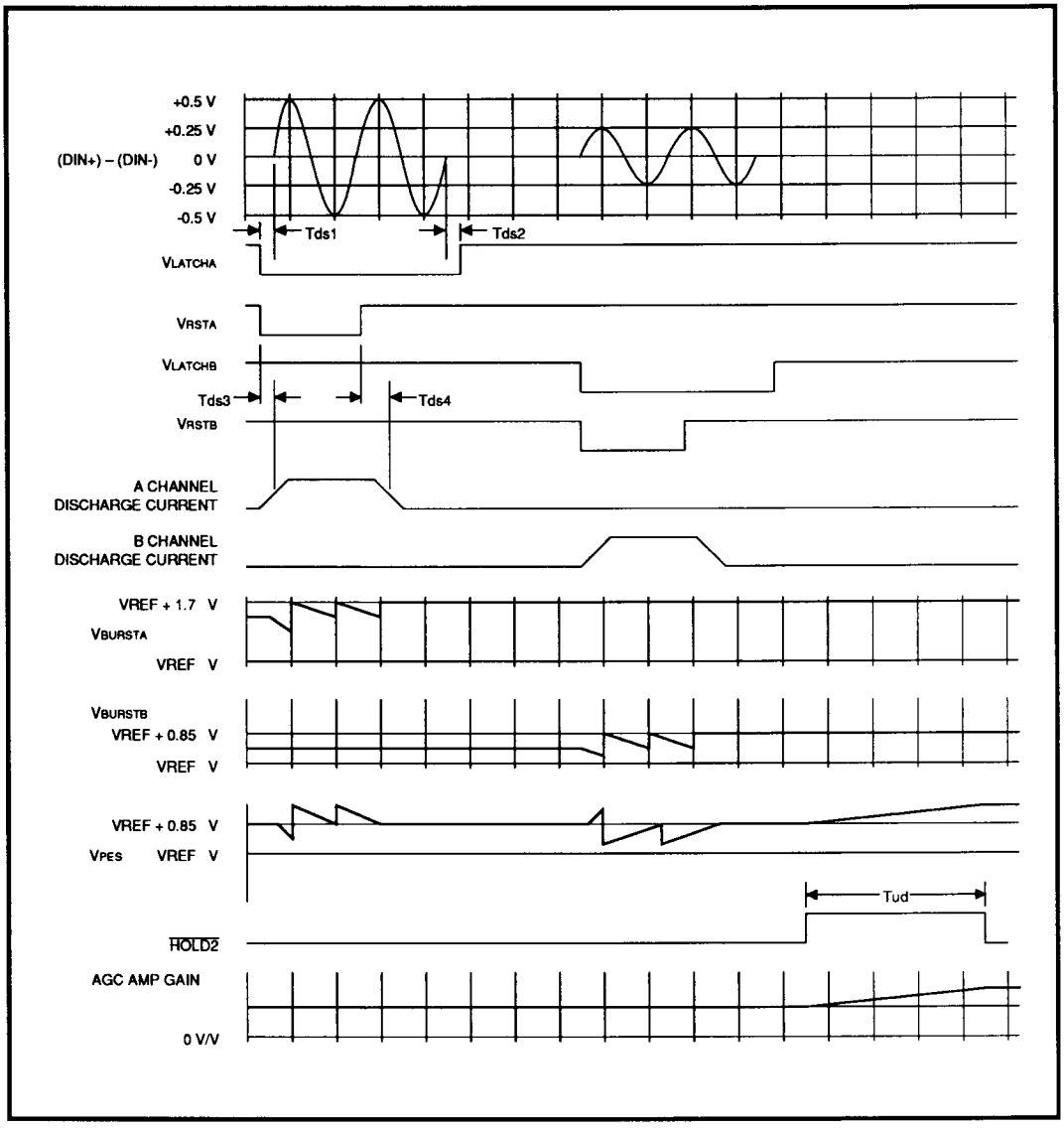


FIGURE 3: Servo Read Mode I Timing Diagram

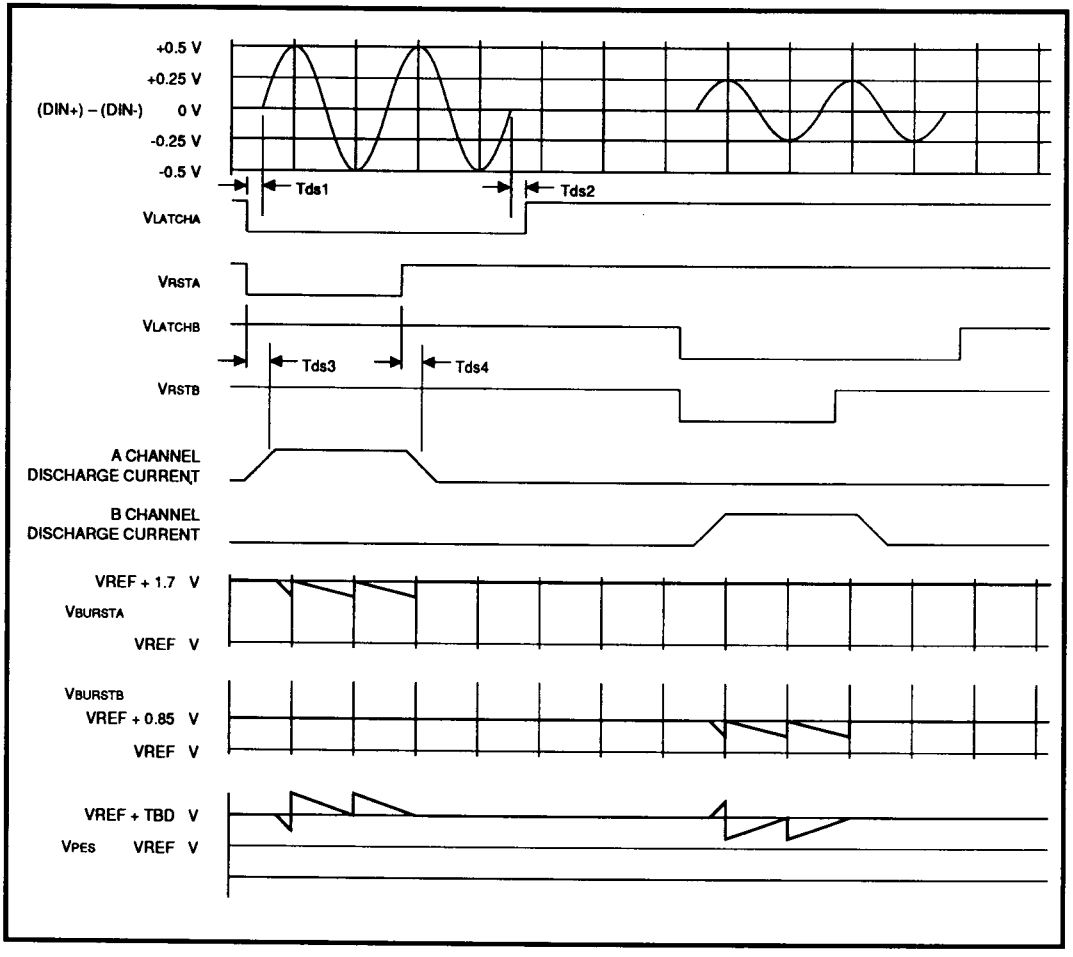


FIGURE 4: Servo Read Mode II Timing Diagram

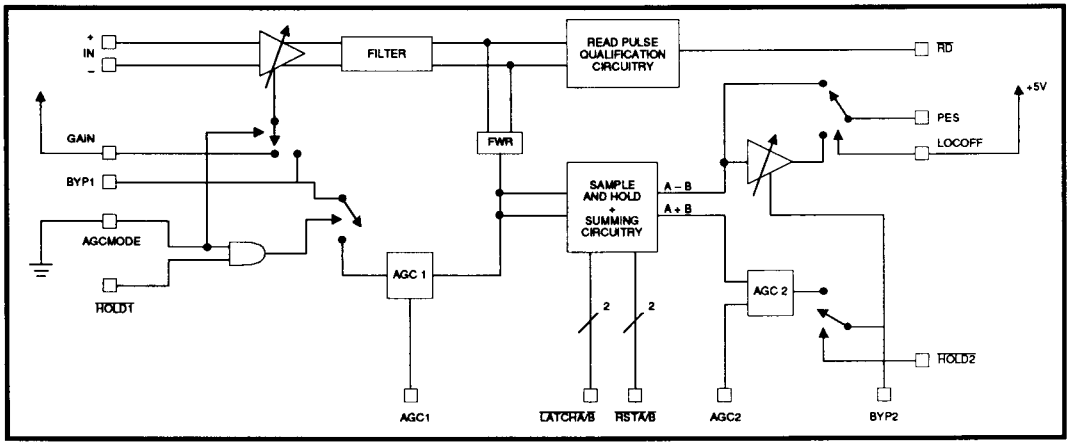


FIGURE 5: Servo Read Mode III

PIN DESCRIPTION

POWER SUPPLY AND CONTROL

NAME	DESCRIPTION
VCC	5 volt power supply.
VDD	12 volt power supply.
AGND, DGND	Analog and digital ground pins.
R/$\overline{W}$*	TTL compatible read/write control pin
ENABLE*	TTL compatible power up control pin. A low input selects a low power state.
$\overline{VFLT}$	Open collector output that goes low when a low power supply fault is detected.

AGC GAIN STAGE

IN+, IN-	Analog signal input pins.
OUT+, OUT-	Read path AGC amplifier output pins.
AGC1	Reference input voltage level for the read path AGC loop.
AGCMODE*	TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low GAIN.
BYP1	An AGC timing capacitor or network is tied between this pin and AGND.
GAIN	A voltage at this pin may be used to control AGC gain.
DECAY	A resistor to control the AGC loop decay time constant may be tied between this pin and BYP1.
$\overline{HOLD1}$*	TTL compatible control pin that holds the read path AGC loop gain constant when low.

* These inputs have internal pull-ups, so an open connection is the same as a high input.

PIN DESCRIPTION (Continued)

DIGITAL PROCESSING STAGE

NAME	DESCRIPTION
DIN+, DIN-	Analog input to the hysteresis comparator.
CIN+, CIN	Analog input to the differentiator.
DIF+, DIF-	Pins for external differentiating network.
LEVEL	Output from full wave rectifier that may be used for input to the hysteresis-comparator.
HYS	Threshold setting input to the hysteresis-comparator.
DOUT	Buffered TTL output for monitoring the flip-flop D input. Provided for testing or servo use.
COUT	Test point for monitoring the flip-flop clock input.
OS	Connection for output pulse width setting capacitor.
$\overline{RD}$	TTL compatible read output.

SERVO BURST CAPTURE STAGE

$\overline{LATCHA}$, $\overline{LATCHB}$	TTL compatible inputs that switch channels A or B into peak acquisition mode when low.
HOLDA, HOLDB	Peak holding capacitors are tied from each of these pins to AGND.
$\overline{RSTA}$, $\overline{RSTB}$	TTL compatible inputs that enable discharge of Channel A or B hold capacitors when low.
CS	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to ground.
VREF	Reference voltage input for servo outputs.
AGC2	Reference input voltage level for the servo AGC loop.
BYP2	An AGC timing capacitor or network is tied between this pin and AGND.
$\overline{HOLD2}$	TTL compatible control pin that holds the servo AGC loop gain constant when low.
BURSTA, BURSTB	Buffered hold capacitor voltage outputs.
PES	Position error signal A minus B output.
LOCOFF*	TTL compatible input to select path for PES signal. (Local On/Off) Selects between AGC amp. output or A-B output.

* These inputs have internal pull-ups, so an open connection is the same as a high input.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6.0	V
12V Supply Voltage, VDD	14.0	V
Pin Voltage GAIN, BYP1/2, AGC1/2 LEVEL, HYS, HOLDA/B, VREF BURSTA/B, PES, COUT, DIF±, OUT±	-0.3 to VDD + 0.3	V
Pin Voltage IN±, AGCMODE, $\overline{\text{HOLD1/2}}$, ENABLE, R/$\overline{\text{W}}$, $\overline{\text{LATCHA/B}}$, $\overline{\text{RSTA/B}}$, CS, LOCOFF, OS, CIN±, DIN±	-0.3 to VCC + 0.3	V
Pin Voltage RD, DOUT, DECAY, $\overline{\text{VFLT}}$	-0.3 to VCC + 0.3 or +12 mA	V
Storage Temperature	65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCC	Supply Voltage		4.5	5.0	5.5	V
VDD	Supply Voltage		10.8	12.0	13.2	V
Ta	Ambient Temperature		0		70	°C

ELECTRICAL CHARACTERISTICS

POWER SUPPLY

Recommended conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
ICC	VCC Supply Current	Outputs unloaded, ENABLE = high or open			20	mA
ICC		ENABLE = low			17	mA
IDD	VDD Supply Current	Outputs unloaded, ENABLE = high or open			90	mA
IDD		ENABLE = low			25	mA

POWER SUPPLY (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Pd	Power dissipation	Tj = 145°C, ENABLE = high, Outputs unloaded			1.0	W
		ENABLE = low, Outputs unloaded			0.35	W

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input Low Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH	Output High Voltage	IOH = 400 µA	2.4			V
	Output rise time	VOH = 2.4V*			15.0	ns
	Output full time	VOL = 0.4V*			9.0	ns

*10 - 90%, 10 pF capacitor to DGND

MODE CONTROL

Enable to/from Disable Transition Time	Settling time of external capacitors not included ENABLE pin high to/from low			10	µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC setting not included	1.2		3.0	µs
AGC On to/from AGC Off Transition Time	AGCMODE pin high to/from low			2.0	µs
$\overline{HOLD1}$ On to/from $\overline{HOLD2}$ Off Transition Time	$\overline{HOLD1}$ pin high to/from low			1.0	µs
$\overline{HOLD2}$ On to $\overline{HOLD2}$ Off Transition Time	$\overline{HOLD2}$ pin high to/from low			1.0	µs

WRITE MODE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance	R/$\overline{W}$ pin = low		250		Ω

READ MODE

READ PATH AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP1 and AGND. AGC1 pin is open. R/$\overline{W}$ is high.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	1.0 Vpp ≤ (OUT+) – (OUT-) ≤ 3.0 Vpp	4		83	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP1 pin	3.0			Vpp
Differential Input Resistance	(IN+) – (IN-) = 100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	(IN+) – (IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ = high		1.8		kΩ
	R/$\overline{W}$ = Low		250		Ω
Input Noise Voltage	Gain set to maximum, RS = 0, BW = 15 MHz			30	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	28			MHz
OUT+ to OUT- Pin Current	No DC path to AGND	±3.0			mA
Output Resistance		20		50	Ω
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40			dB

READ PATH AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSRR (Input Referred)	VDD or VCC = 100 mVpp @ 5 MHz, gain set to max	30			dB
Externally controlled Gain Constants $AV = K_2 \cdot e^{(K3 \cdot VGAIN)}$ V/V	K_2, AGCMODE = Low K_3, AGCMODE = Low	.89 1.95		2.3 2.64	
Gain pin parasitic Input current	AGCMODE & $\overline{HOLD1}$ = low	0.2		+0.2	µA
(DIN+) – (DIN-) Input Swing vs. AGC1 Input	30 mVpp ≤ (IN+) – (IN-) ≤ 550 mVpp 0.5 Vpp ≤ (DIN+) – (DIN-) ≤ 1.5 Vpp, AGCMODE & $\overline{HOLD1}$ = high	0.36		0.56	Vpp/V
(DIN+) – (DIN-) Input Voltage Swing Variation	30 mVpp ≤ (IN+) – (IN-) ≤ 550 mVpp			8.0	%
AGC1 Voltage	AGC1 open, $V_{(ACC1)}$ = 2.35V	-5		+5	%
AGC1 Pin Input Impedance		5.0		8.3	kΩ
Fast Decay Threshold (DIN+) – (DIN-)	AGCMODE = high		±0.3		V
Slow AGC Capacitor Discharge Current	(DIN+) – (DIN-) = 0V V_{BYP} = 4.5V		4.0		µA
AGC Capacitor Leakage Current	AGCMODE = high, $\overline{HOLD1}$ = low, 2.5V < V_{BYP} < 5.5V	-0.2		+0.2	µA
Slow AGC Capacitor Charge Current	(DIN+) – (DIN-) = 0.75 VDC, vary AGC1 until slow charge begins	-0.14		-0.22	mA
Fast AGC Capacitor Charge Current	(DIN+) – (DIN-) = 0.75 VDC, V_{AGC1} = 3.0V	-1.3		-2.0	mA
Fast to Slow Attack Switchover Point	[(DIN+) – (DIN-)] – [(DIN+) – (DIN-)]FINAL		0.2		Vpp
Gain Decay Time (Td) (See Figure 6a)	(IN+) – (IN-) = 300 mVpp to 150 mVpp @ 2.5 MHz DECAY pin open, (OUT+) – (OUT-) to 90% final value.		50		µs

READ PATH AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Attack Time (Ta) (See Figure 6b)	R/$\overline{W}$ = low to high (IN+) – (IN-) = 400 mVpp @ 2.5 MHz, (OUT+) – (OUT-) to 110% final value		4		µs

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) – (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 1.8 VDC is applied to the HYS pin. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) – (DIN-) = 100 mVpp @ 2.5 MHz	10		18.0	kΩ
Differential Input Capacitance	(DIN+) – (DIN-) = 100 mVpp @ 2.5 MHz			4.0	pF
Common Mode Input Impedance (Both Sides)		2.25		5.0	kΩ
Level Pin Output Voltage vs. (DIN+) – (DIN-)	0.6 Vpp < (DIN+) – (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND	1.2		2.2	V/Vpp
Level Pin Output Impedance	I_{LEVEL} = 0.5 mA		180		
Level pin Maximum Output Current		3.0			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	1 V < HYS < 3V	0.16		0.25	V/V
Hysteresis threshold margin as a % of V(DIN+) – (DIN-) peak	V(HYS) = some % of *V(AGC) or V(LEVEL) 1V < V(HYS) < 3V *see Figures 8 & 9	-15		+15	%Peak
HYS Pin Current	1 V < HYS < 3V	0.0		-20	µA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			10.0	mV

* In an open loop configuration where reference is V(AGC) tolerance can be slightly higher.

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) – (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(CIN+) – (CIN-) = 100 mVpp @ 2.5 MHz	10		18.0	kΩ
Differential Input Capacitance	(CIN+) – (CIN-) = 100 mVpp @ 2.5 MHz			4.0	pF
Common Mode Input Impedance	Both sides	2.25		5.0	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±1.2			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled			10.0	mV
COUT Pin Output Low Voltage	0 ≤ IOL ≤ 0.5 mA		VDD-3.0		V
COUT pin Output Pulse Voltage, V_{HIGH} - V_{LOW}	0 ≤ IOL ≤ 0.5 mA		0.4		V
COUT pin Output Pulse Width	0 ≤ IOH ≤ 0.5 mA		30		ns

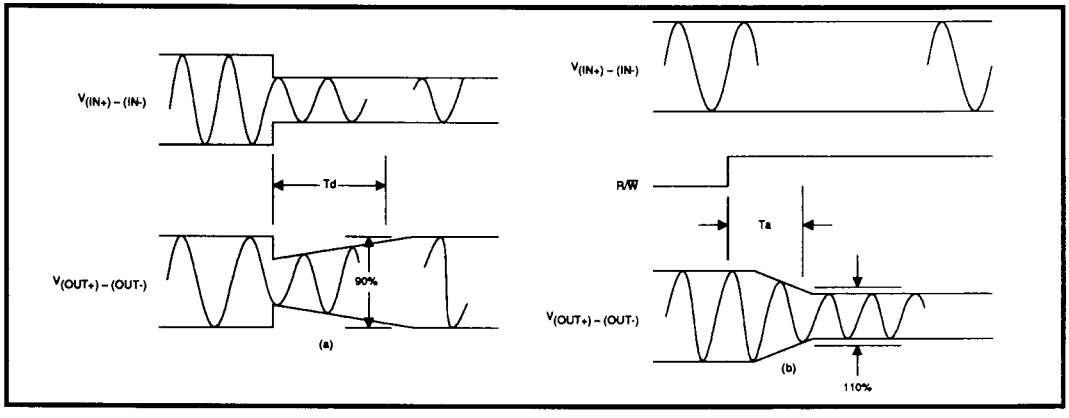


FIGURE 6: AGC Timing Diagram

OUTPUT DATA CHARACTERISITICS (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) – (CIN-) and (DIN+) – (DIN-) are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 1.8V is applied to the HYS pin. A 60 pF capacitor is tied between OS and VCC. $\overline{RD}$ is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) – (DIN-) exceeding hysterisis point to (DIF+) – (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay				110	ns
Td5	Output Pulse Width Variation	Td5 = 800(Cos) @ V_{RD} = 1.4V 50 pF ≤ Cos ≤ 200 pF			±15	%
|Td3-Td4|	Pulse Pairing				1.5	ns

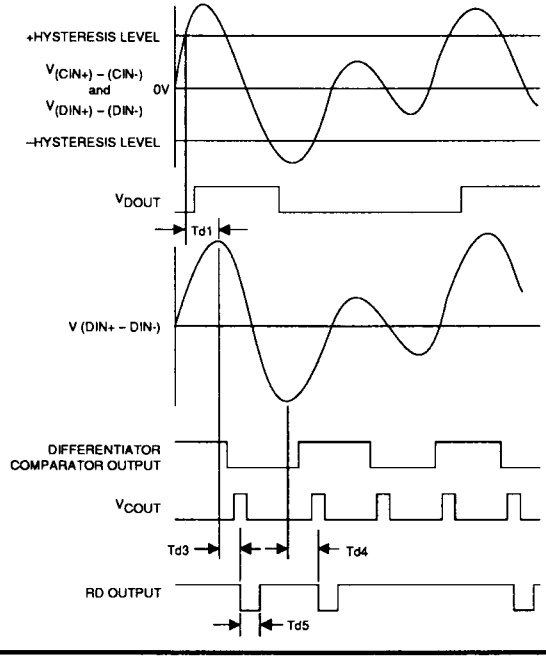


FIGURE 7: Read Mode Digital Section Timing Diagram

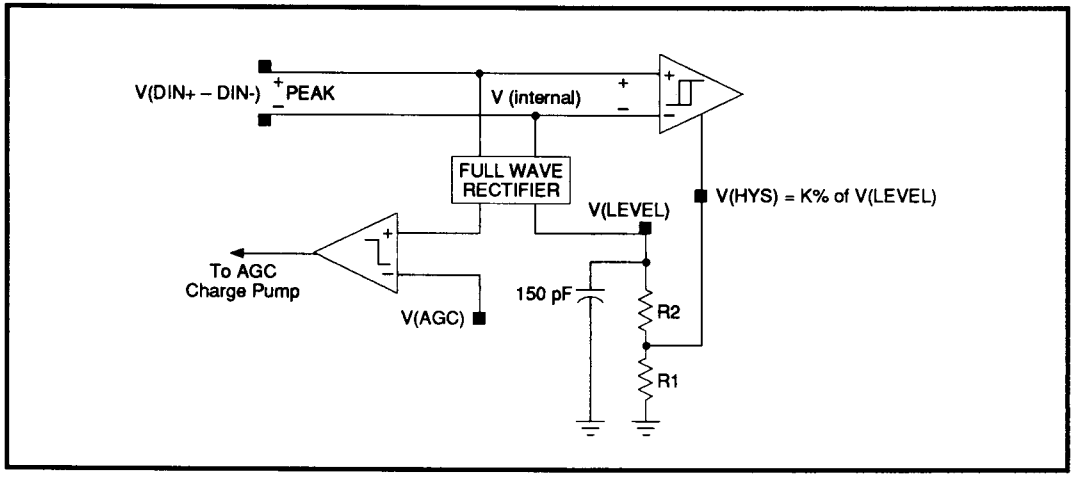


FIGURE 8: Feed Forward Mode

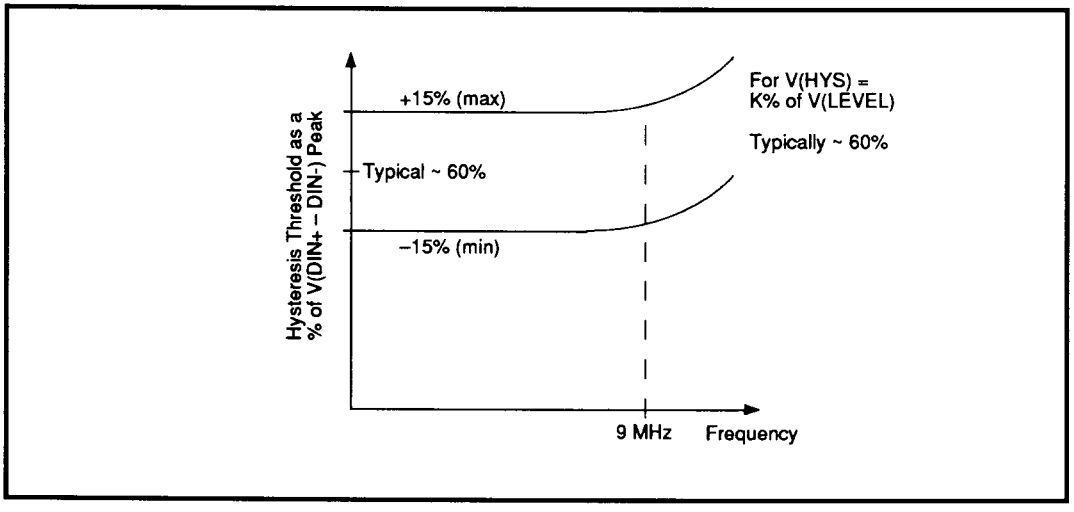


FIGURE 9: Percentage Threshold vs. Frequency

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range		3.9		6.0	V
AGC2 Pin Voltage	AGC2 Pin Open, $V_{(AGC2)}$ = 3.4V	-5		+5	%
AGC2 Pin Input Impedance		5.0		9.1	kΩ
BURSTA/B pin Output Voltage vs (DIN+) – (DIN-)	$\overline{LATCHA/B}$ = Low $\frac{V_{BURSTA/B} - VREF}{(DIN+) - (DIN-)}$ = 1.7 V/Vp-p	-6.5		+6.5	%
BURSTA/B Output Offset Voltage V_{BURST} - VREF	$\overline{LATCHA/B}$ = Low, (DIN+) = (DIN-), RCS = 38.3 kΩ	-80		+80	mV
BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-15		+15	mV
Maximum PES Pin Output Voltage	Controlled by AGC2			5.0	Vpp
PES Pin Output Offset Voltage	V_{PES} - VREF, (DIN+) = (DIN-) $\overline{LATCHA/B}$ = Low After 30 sec. temp. stable	-50		+50	mV
Output Resistance, BURSTA/B & PES pins				20	Ω
Hold A/B Charge Current	$\overline{LATCHA/B}$ = Low	25			mA
HOLDA/B Discharge Current Tolerance	$\overline{RSTA/B}$ = Low, ICS = 2.6V/(RSC + 750Ω)	-15		+15	%
	$\overline{RSTA/B}$ = High, $\overline{LATCHA/B}$ = High	-0.5		+0.5	µA
Load Resistance BURSTA/B, PES pins	Resistors to VREF	10.0			kΩ
Load Capacitance BURSTA/B, PES pins				20	pF
$\overline{LATCHA/B}$ pin set up time	(Tds1 in Figures 3 & 4)	150			ns
$\overline{LATCHA/B}$ pin Hold Time	(Tds2 in Figures 3 & 4)	150			ns
Channel A/B Discharge Current Turn On time	(Tds3 in Figures 3 & 4)			150	ns
Channel A/B discharge Current Turn Off time	(Tds4 in Figures 3 & 4)			150	ns
BYP2 Pin Parasitic Input Current	$\overline{HOLD2}$ = Low LOCOFF = Low LOCOFF = High	 -0.02 -9.0		 +0.02 +9.0	 µA µA

SERVO SECTION (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BYP2 Pin Charge/Discharge Current $I_C = K_4[(K_5 \cdot V_{AGC2}) - V_{A(DIN)}pp - V_{B(DIN)}pp]$	K_4, $\overline{HOLD2}$ = High	487	650	813	µA/Vpp
	K_5, $\overline{HOLD2}$ = High	0.35		0.43	V/V
*AGC Gain Range	LOCOFF=Low	0.6		6.0	V/Vpp
V_{PES} pp vs. V_{AGC2}	V_{PES} pp/V_{AGC2} LOCOFF = Low	1.24	1.38	1.52	Vpp/V
	LOCOFF = High	1.42	1.5	1.58	
	V_{PES} pp/V_{AGC2} AGC2=Open LOCOFF = Low	5.03	5.3	5.56	Vpp Vpp/V
	LOCOFF = High	5.32	5.6	5.88	
BURSTA/B Pin Output vs. V_{AGC2}	(V_A + V_B - 2VREF)/V_{AGC2} LOCOFF = High		0.77		V/V
	V_A + V_B - 2VREF, AGC2=Open LOCOFF = High		2.85		V

*Av = (VPES - VREF)/($V_{A(DIN)}$pp + $V_{B(DIN)}$pp)

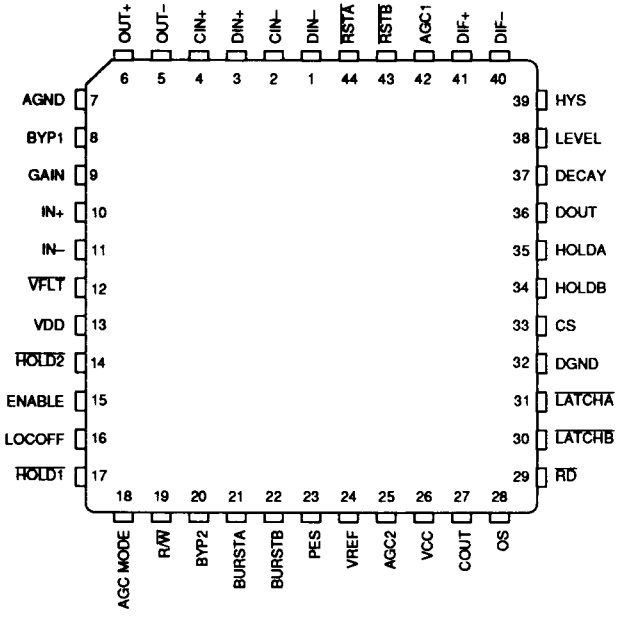
Supply Voltage Fault Detection

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD Fault Threshold		9.1		10.5	V
VCC Fault Threshold		4.1		4.4	V
VOL Output Low	4.5 < VCC < 5.5V, IOL = 1.6 mA			0.4	V
	1.0 < VCC < 4.5, IOL = 0.5 mA			0.4	V
IOH Output High Current				25	µA

PACKAGE PIN DESIGNATIONS
(Top View)

Thermal Characteristics: θjA

44-lead PLCC	60° C/W



44-Lead PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P544 - 44-Lead PLCC	32P544-CH	32P544-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914