Memories

UT8CR512K32

16Megabit SRAM Memory

Datasheet

CobhamAES.com/HiRel

March 2020

The most important thing we build is trust

FEATURES

- ❑ 17ns maximum access time
- ❑ Asynchronous operation for compatibility with industry-standard 512K x 32 SRAMs
- ❑ CMOS compatible inputs and output levels, three-state bidirectional data bus
  - I/O Voltage 3.3 volts, 1.8 volt core
- ❑ Operational environment:
  - Intrinsic total-dose: 100K rad(Si)
  - SEL Immune >100 MeV-cm^2/mg
  - LET_{th}: 9.0 MeV-cm^2/mg
  - Memory Cell Saturated xSection: 1.67E-7 cm^2/bit
  - Neutron Fluence: 3.0E14n/cm^2
  - Dose Rate
    - Upset 1.0E9 rad(Si)/sec
    - Latchup >1.2E12 rad(Si)/sec
- ❑ Packaging options:
  - 68-lead ceramic quad flatpack (20.238 grams with lead frame)
- ❑ Standard Microcircuit Drawing 5962-04227
  - QML Q & V compliant part

INTRODUCTION

The UT8CR512K32 is a high-performance CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 words by 8 bit SRAMs with common output enable. Easy memory expansion is provided by active LOW chip enables ($\overline{E}$n), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to each memory device is accomplished by taking the corresponding chip enable ($\overline{E}$n) input LOW and write enable ($\overline{W}$n) input LOW. Data on the eight I/O pins is then written into the location specified on the address pins (A_0 through A_{18}). Reading from the device is accomplished by taking the chip enable ($\overline{E}$n) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$n) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ($\overline{E}$n HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E}$n LOW and $\overline{W}$n LOW). Perform 8, 16, 24, or 32 bit accesses by making $\overline{W}$n along with $\overline{E}$n a common input to any combination of the discrete memory die.

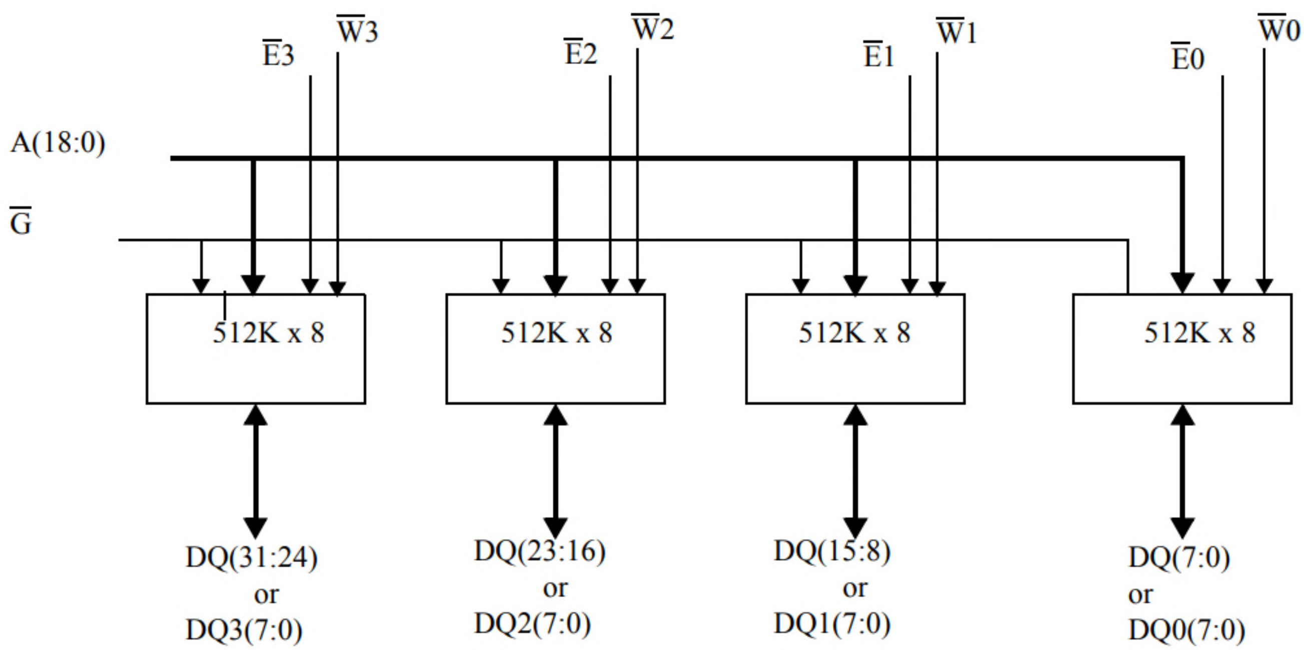


Figure 1: UT8CR512K32 SRAM Block Diagram

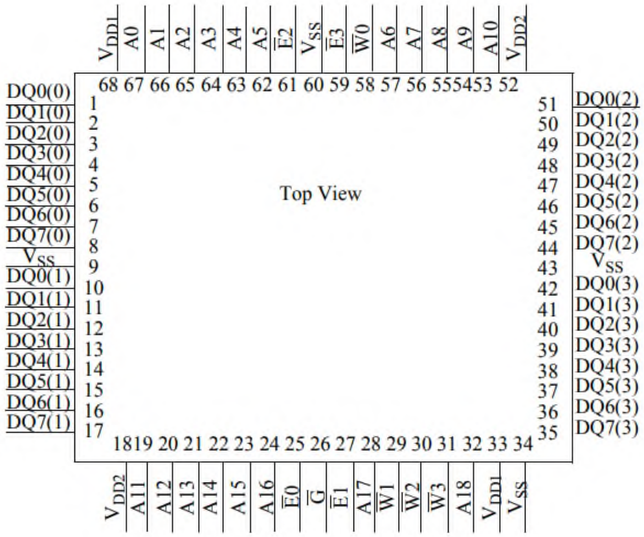


Figure 2: 17ns SRAM Pinout (68)

DEVICE OPERATION

PIN NAMES

A(18:0)	Address—	$\overline{G}$	Output Enable
DQ(7:0)	Data Input/Output	V_{DD1}	Power (1.8V)
$\overline{E}$n(4:1)	Chip Enable (active low)	V_{DD2}	Power (3.3V)
$\overline{W}$n(4:1)	Write Enable	V_{SS}	Ground

Each die in the UT8CR512K32 has three control inputs called Chip Enable ($\overline{E}$n), Write Enable ($\overline{W}$n), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). The chip enable ($\overline{E}$n) controls device selection, active, and standby modes. Asserting $\overline{E}$n enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to each memory die by selecting the 2,048,000 bytes of memory. $\overline{W}$n controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{E}$	I/O Mode	Mode
X	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read[2]
0	1	0	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}$n greater than V_{IH} (min) with $\overline{E}$n and $\overline{G}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of Chip Enable, Output Enable, or valid address to valid data output. Read cycles initiate with the assertion of any chip enable or any address change while any chip enable is asserted.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$n deasserted. Valid data appears on data outputs DQn(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as Chip Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}). Changing addresses prior to satisfying t_{AVAV} minimum results in an invalid operation. Invalid read cycles will require re-initialization.

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by $\overline{E}$n going active while $\overline{G}$ remains asserted, $\overline{W}$n remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQn(7:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E}$n is asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$n less than V_{IL}(max) and $\overline{E}$n less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$n is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access is defined by a write terminated by $\overline{W}$n going high, with $\overline{E}$n still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$n, and by t_{ETWH} when the write is initiated by $\overline{E}$n. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQn(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access is defined by a write terminated by the former of $\overline{E}$n or $\overline{W}$n going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$n, and by t_{ETEF} when the write is initiated by $\overline{E}$n going active. For the $\overline{W}$n initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQn(7:0) to avoid bus contention.

OPERATIONAL ENVIRONMENT

The UT8CR512K32 SRAM incorporates special design and layout features which allows operation in a limited environment.

Table 2. Operational Environment Design Specifications[1]

Total Dose	100K	rad(Si)
Heavy Ion Error Rate[2]	8.9×10^{-10}	Errors/Bit-Day

Notes:

1. The SRAM is immune to latchup to particles >100MeV-cm^2/mg.
2. 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

SUPPLY SEQUENCING

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage	-0.3 to 2.4V
V_{DD2}	DC supply voltage	-0.3 to 4.5V
$V_{I/O}$	Voltage on any pin	-0.3 to 4.5V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	5°C/W
I_I	DC input current	±5 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	Positive supply voltage	1.7 to 1.9V[1]
V_{DD2}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	(P) Screening: -25°C (C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

Notes:

1. For increased noise immunity, supply voltage (V_{DD1}) can be increased to 2.0V. If not tested, all applicable DC and AC characteristics are guaranteed by characterization at V_{DD1} (max) = 2.0V.

DC ELECTRICAL CHARACTERISTICS (PRE AND POST-RADIATION)*

Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IH}	High-level input voltage			$.7*V_{DD2}$		V
V_{IL}	Low-level input voltage				$.3*V_{DD2}$	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, V_{DD2} = V_{DD2} (min)			$.2*V_{DD2}$	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA, V_{DD2} = V_{DD2} (min)		$.8*V_{DD2}$		V
C_{IN} [1]	Input capacitance	f = 1MHz @ 0V			44	pF
C_{IO} [1]	Bidirectional I/O capacitance	f = 1MHz @ 0V			21	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}		-2	2	μA
I_{OZ}	Three-state output leakage current	V_O = V_{DD2} and V_{SS}, V_{DD2} = V_{DD2} (max) $\overline{G}$ = V_{DD2} (max)		-2	2	μA
I_{OS} [2, 3]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}		-100	+100	mA
I_{DD1} (OP_1)	Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD2} = V_{DD2} (max)	V_{DD1} = 1.9V		70	mA
			V_{DD1} = 2.0V		76	mA
I_{DD1} (OP_2)	Supply current operating @58.8MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD2} = V_{DD2} (max)	V_{DD1} = 1.9V		122	mA
			V_{DD1} = 2.0V		150	mA
I_{DD2} (OP_1)	Supply current operating @ 1MHz	Inputs : V_{IL} = V_{SS} + 0.2V V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max) V_{DD2} = V_{DD2} (max)			.35	mA
I_{DD2} (OP_2)	Supply current operating @58.8MHz	Inputs : V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} - 0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			11	mA

$I_{DD1}(SB)$[4]	Supply current standby @ 0Hz	CMOS inputs , I_{OUT} = 0 $\overline{E}$ = V_{DD2} - 0.2 V_{DD2} = V_{DD2} (max)	V_{DD1} = 1.9V		65	mA
			V_{DD1} = 2.0V		72	mA
$I_{DD2}(SB)$[4]			V_{DD1} = V_{DD1} (max)		8	μA
$I_{DD1}(SB)$[4]	Supply current standby A(18:0) @ 58.8MHz	CMOS inputs , I_{OUT} = 0 $\overline{E}$ = V_{DD2} - 0.2 V_{DD2} = V_{DD2} (max)	V_{DD1} = 1.9V		65	mA
			V_{DD1} = 2.0V		72	mA
$I_{DD2}(SB)$[4]			V_{DD1} = V_{DD1} (max)		8	μA

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. V_{IH} = V_{DD2} (max), V_{IL} = 0V.

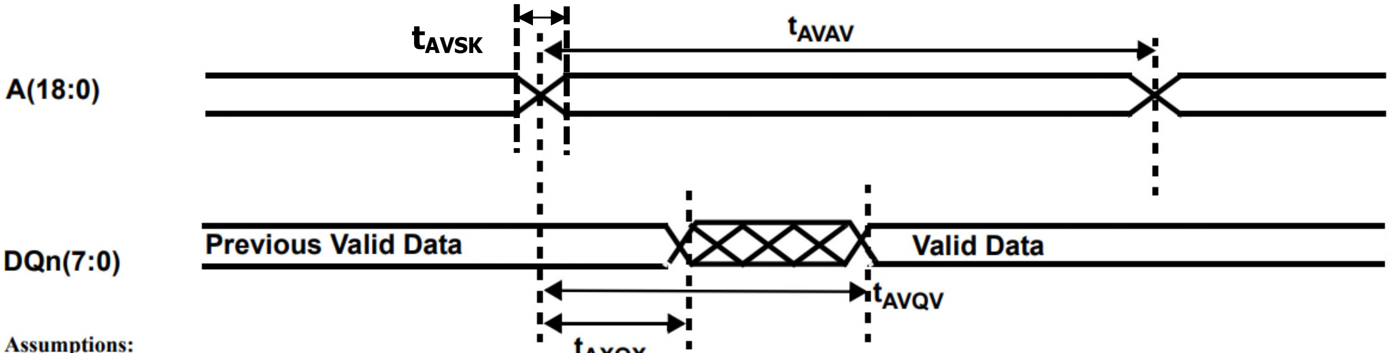
AC CHARACTERISTICS READ CYCLE (PRE AND POST-RADIATION)*

$V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min); Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	8CR512-17		UNIT
		MIN	MAX	
t_{AVAV}[1,6]	Read cycle time	17		ns
t_{AVSK}[5]	Address valid to address valid skew time		4	ns
t_{AVQV}	Read access time		17	ns
t_{AXQX}[2]	Output hold time	3		ns
t_{GLQX}[1,2]	$\overline{G}$-controlled output enable time	0		ns
t_{GLQV}	$\overline{G}$-controlled read access time		7	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		7	ns
t_{ETQX}[2,3]	E-controlled output enable time	5		ns
t_{AVET2}[5]	Address setup time for read (E-Controlled)	-4		ns
t_{ETQV}[3]	E-controlled access time		17	ns
t_{EFQZ}[4]	E-controlled output three-state time[2]		10	ns

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed, but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the latter falling edge of $\overline{E}$. SEU immunity does not affect the read parameters.
4. The EF (chip enable false) notation refers to the latter rising edge of $\overline{E}$. SEU immunity does not affect the read parameters.
5. Guaranteed by design
6. Address changes prior to satisfying t_{AVAV} minimum is an invalid operation



Assumptions:
1. $\overline{E}$ and $\overline{G} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access

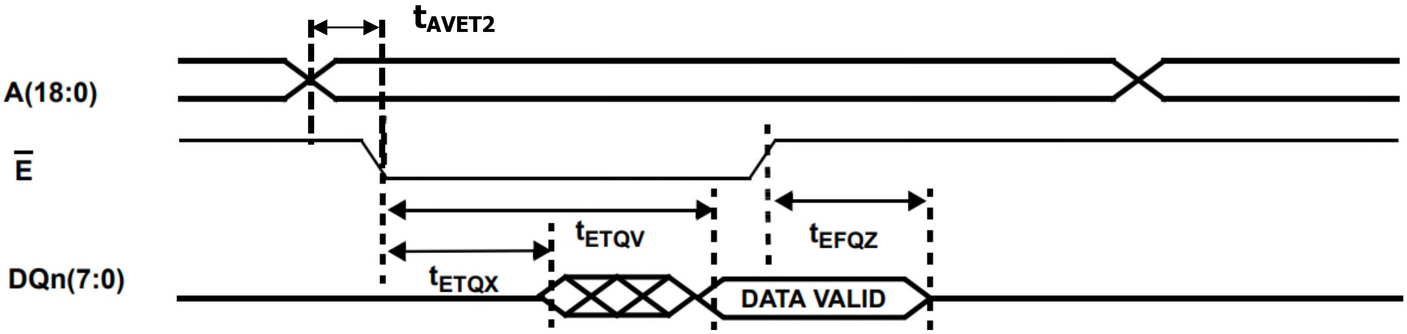
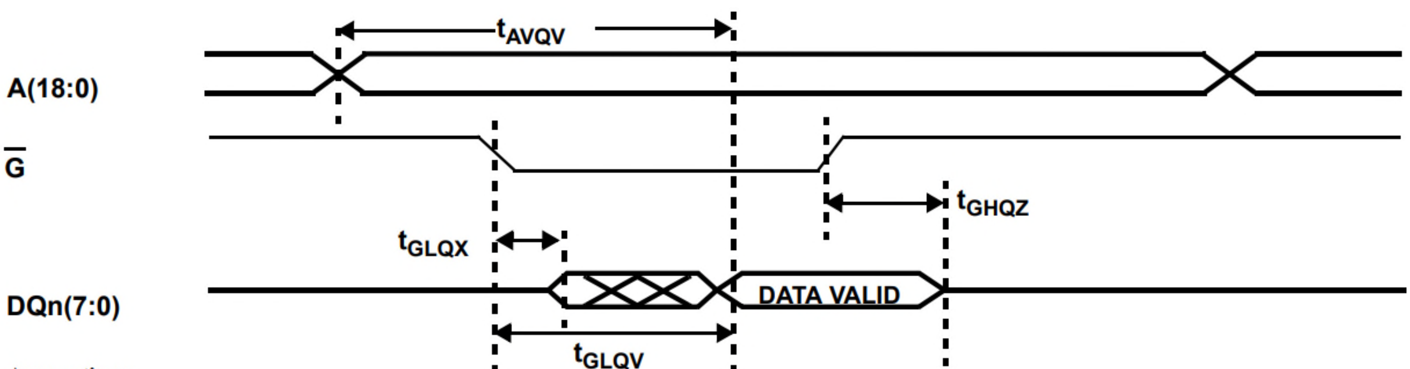


Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:
1. $\overline{E} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

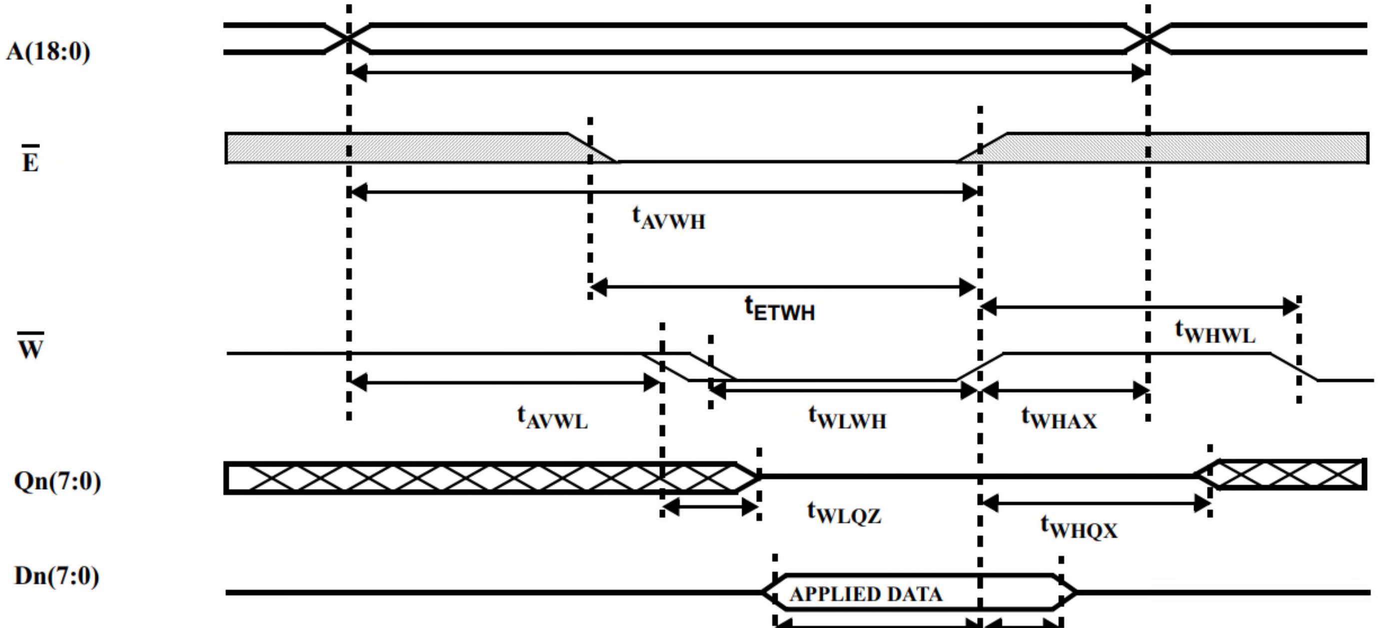
AC CHARACTERISTICS WRITE CYCLE (PRE AND POST-RADIATION)*

$V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min); Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	8CR512		UNIT
		MIN	MAX	
t_{AVAV}[1]	Write cycle time	17		ns
t_{ETWH}	Chip enable to end of write	12		ns
t_{AVET}	Address setup time for write ($\overline{E}$- controlled)	0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		ns
t_{WLWH}	Write pulse width	12		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	2		ns
t_{EFAX}	Address hold time for chip enable ($\overline{E}$- controlled)	0		ns
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		5	ns
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	4		ns
t_{ETEF}	Chip enable pulse width ($\overline{E}$ - controlled)	12		ns
t_{DVWH}	Data setup time	7		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Chip enable controlled write pulse width	12		ns
t_{DVEF}	Data setup time	12		ns
t_{EFDX}	Data hold time	0		ns
t_{AVWH}	Address valid to end of write	12		ns
t_{WHWL}[1]	Write disable time	3		ns

Notes:
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

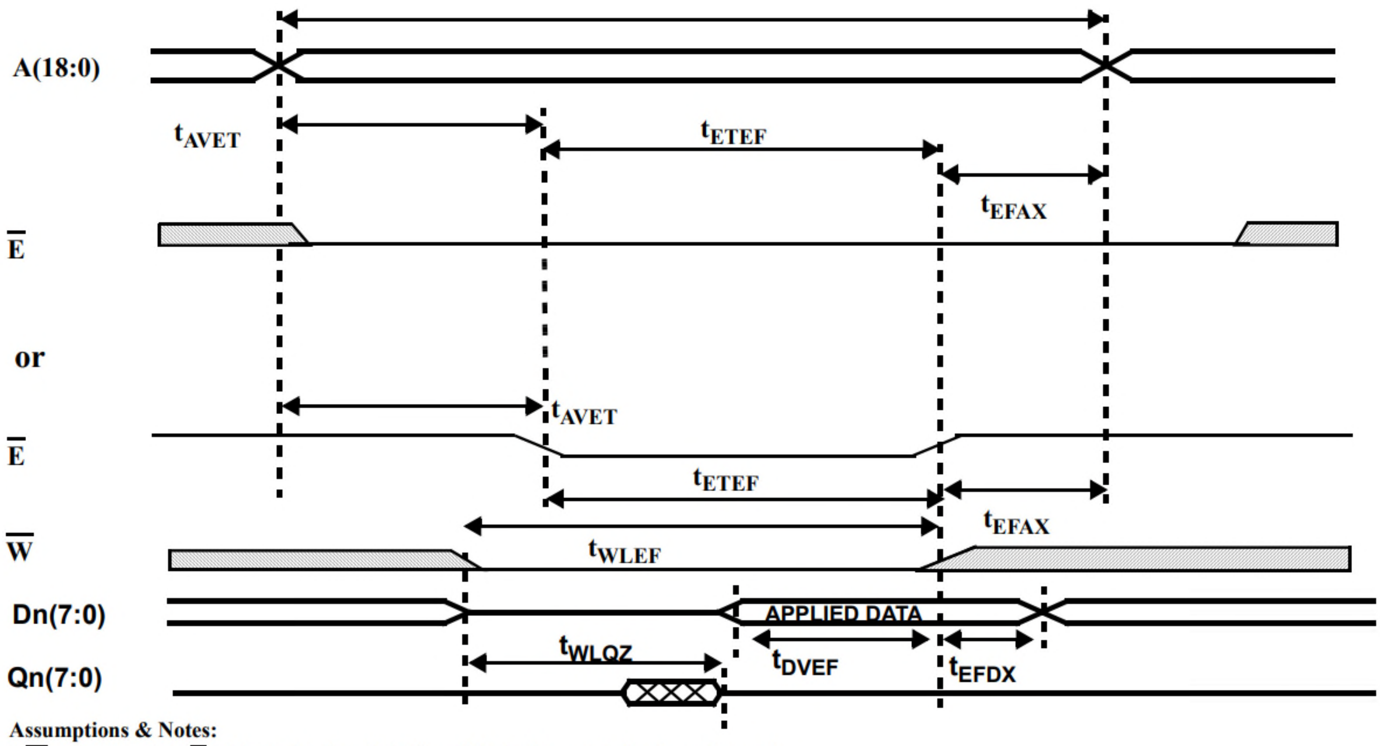
1. Test with $\overline{G}$ high.
2. Three-state is defined as 200mV change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(8:0) will be in three-state for the entire cycle.

Figure 4a. SRAM Write Cycle 1: Write Enable - Controlled Access



Assumptions & Notes:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2. Either $\overline{E}$ scenario above can occur.

Figure 4b. SRAM Write Cycle 2: Chip Enable - Controlled Access

DATA RETENTION CHARACTERISTICS (PRE-RADIATION)*

(V_{DD2} = V_{DD2} (min), 1 Sec DR Pulse)

SYMBOL	PARAMETER	TEMP	MINIMUM	MAXIMUM	UNIT
V_{DR}	VDD1 for data retention	--	1.0	--	V
I_{DDR} [1] Device Type 1	Data retention current	-55°C	--	700	µA
		25°C	--	700	µA
		125°C	--	55	mA
I_{DDR} [1] Device Type 2	Data retention current	-40°C	--	700	µA
		25°C	--	700	µA
		125°C	--	55	mA
t_{EFR} [1,2]	Chip deselect to data retention time	--	0	--	ns
t_R [1,2]	Operation recovery time	--	t_{AVAV}	--	ns

Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. $\overline{E}$ = V_{DD2} all other inputs = V_{DD2} or V_{SS}
2. V_{DD2} = 0 volts to V_{DD2} (max)

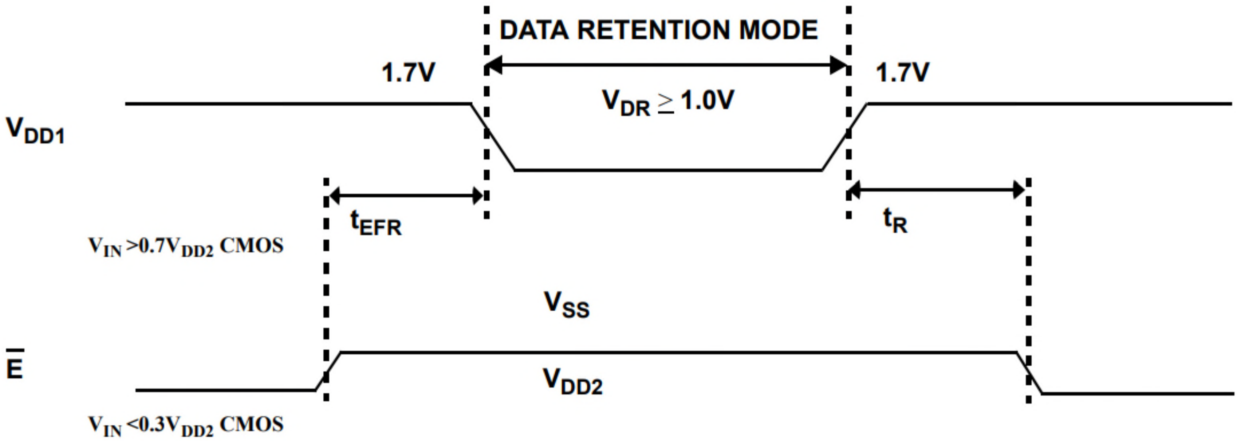
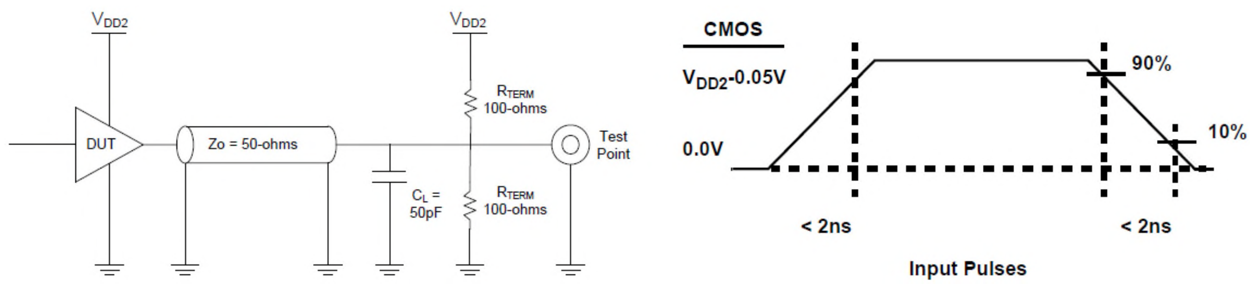
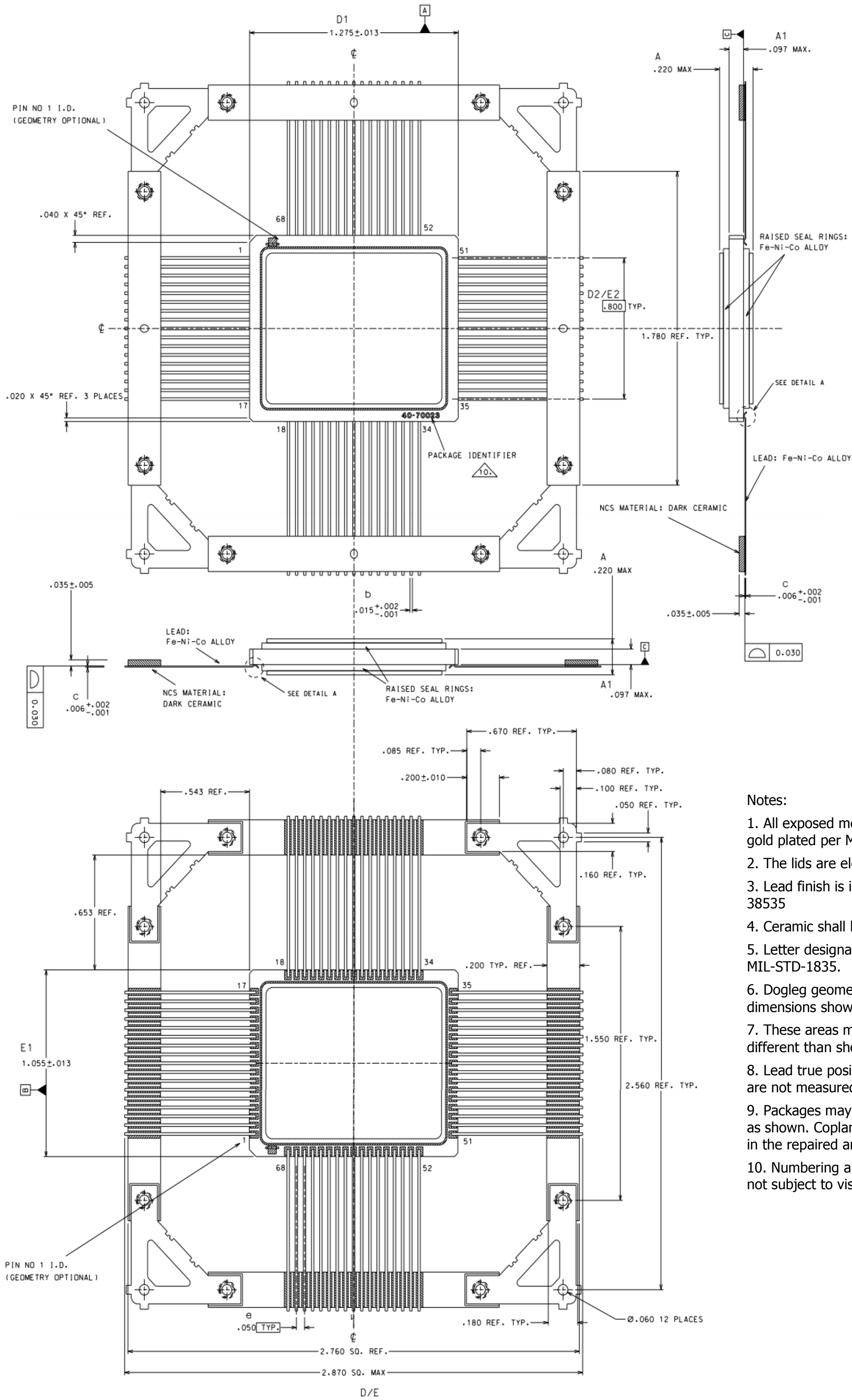


Figure 5. Low V_{DD} Data Retention Waveform



Notes:
1. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$).

Figure 6. AC Test Loads and Input Waveforms



Notes:

1. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
2. The lids are electrically connected to Vss.
3. Lead finish is in accordance with MIL-PRF-38535
4. Ceramic shall be dark alumina.
5. Letter designations are to cross reference to MIL-STD-1835.
6. Dogleg geometries are optional within dimensions shown.
7. These areas may have notches and tabs different than shown.
8. Lead true position tolerances and coplanarity are not measured.
9. Packages may be shipped with repaired lead as shown. Coplanarity requirements do not apply in the repaired area.
10. Numbering and lettering on the ceramic are not subject to visual or making criteria.

Figure 7. 68-pin Ceramic FLATPACK

9.0 ORDERING INFORMATION

9.1 COBHAM PART NUMBER ORDERING INFORMATION

Generic Datasheet Part Numbering

UTxxxxx * * * *

Lead Finish:
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (Gold or Solder)

Screening Level:

(P)	**=**	**Prototype Flow**	**(25°C only)**
(W)	**=**	**Extended industrial temperature range flow**	**(-40°C to +125°C)**
(C)	**=**	**HiRel temperature range Flow**	**(-55°C to +125°C)**

Package Type:
(V) = 68 lead ceramic FP

Access Time:
(17) = 17ns access time

Device Type:
(8CR512K32) = 512K x 32 SRAM

NOTES:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. HiRel Temperature Range flow per Cobham Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
5. Extended Industrial Range flow per Cobham Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

9.2 SMD PART NUMBER ORDERING INFORMATION

SMD Part Numbering

5962 * ***** ** * * *

Lead Finish:

(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (Gold or Solder)

Case Outline:

(X) = 68 lead ceramic flatpack

QML/JAN Class:

(Q) = Class Q
(V) = Class V

Device Type: (Note: 5)

(01) = 17ns access time, CMOS I/O, 68-lead flatpack package (-55°C to +125°C)
(02) = 17ns access time, CMOS I/O, 68-lead flatpack package (-40°C to +125°C)

SMD Project Number: (04227)

Radiation Hardness Assurance:

(R) = 100 krad(Si)

Federal Stock Class Designator

NOTES:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening

10.0 REVISION HISTORY

Date	Revision	Change Description
March 2020	A	Added wording addressing read ap note AN-MEM-002 and added timing parameters to AC Characteristics Read Cycle table, figure 3a, and 3b; Updated VDD1, VDD2, VIO abs max limits to match burn-in testing; Obsolete 300krad TID option. 100krad TID is now the maximum available; typo fixes

Cobham Semiconductor Solutions – Datasheet Definitions

	Definition
Advanced Datasheet	Cobham reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet ***is subject to change***. Specifications can be ***TBD*** and the part package and pinout are ***not final***.
Preliminary Datasheet	Cobham reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in Production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

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