

Features

- 5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 100 MHz
- 36 macrocells with 800 usable gates
- Up to 34 user I/O pins
- 5 V in-system programmable (ISP)
 - Endurance of 10,000 program/erase cycles
 - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
 - 90 product terms drive any or all of 18 macrocells within Function Block
 - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-5, -7, -10 speed grades)
- Advanced 0.6 μ m CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 44-pin PLCC and 44-pin VQFP packages
- Plug-in compatible non-ISP XC9536F available in 44-pin PLCC and 44-pin VQFP packages

Description

The XC9536 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of two 36V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9536 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC9536 device.

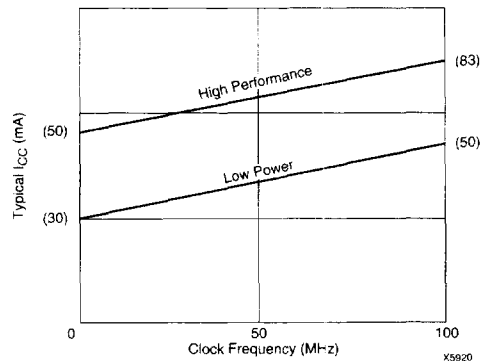


Figure 1: Typical I_{CC} vs. Frequency For XC9536

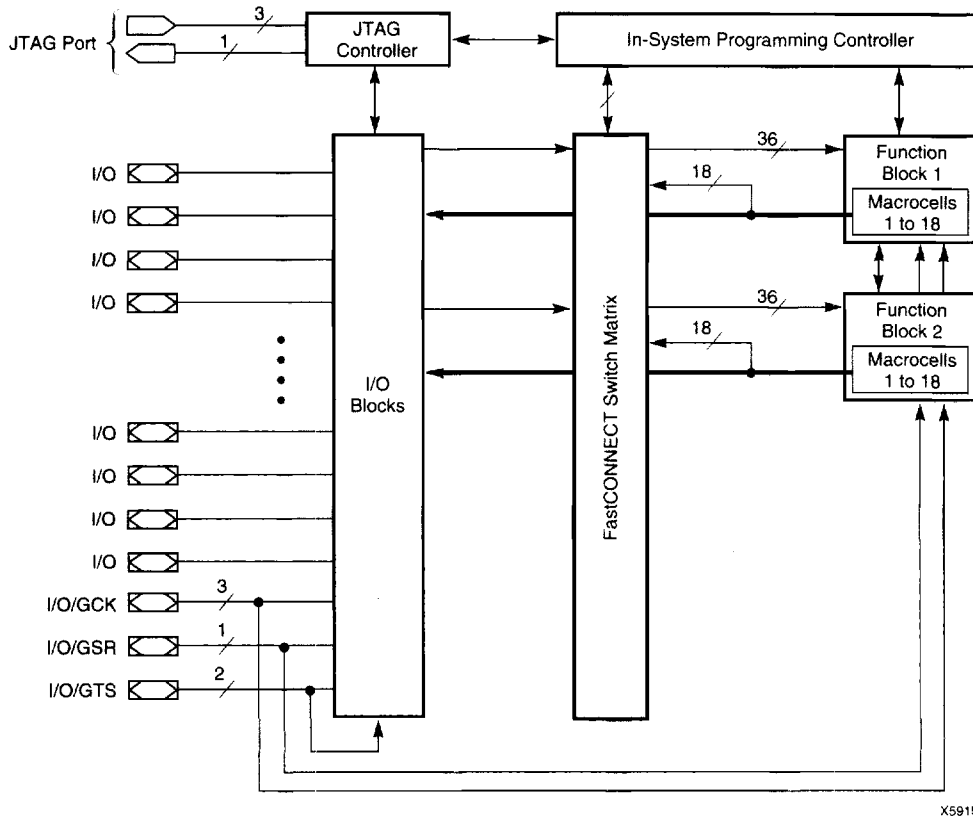


Figure 2: XC9536 Architecture

Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions¹

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
V_O	Output voltage	0	$V_{CCINT} + 0.5$	V

Note 1. Numbers in parenthesis are for industrial-temperature range versions.

Endurance Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles	10,000	-	Cycles

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V _{OH}	Output high voltage for 5 V operation	I _{OH} = -4.0 mA V _{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I _{OH} = -3.2 mA V _{CC} = Min	2.4		V
V _{OL}	Output low voltage for 5 V operation	I _{OL} = 24 mA V _{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I _{OL} = 10 mA V _{CC} = Min		0.4	V
I _{IL}	Input leakage current	V _{CC} = Max V _{IN} = GND or V _{CC}		±10.0	μA
I _{IH}	I/O high-Z leakage current	V _{CC} = Max V _{IN} = GND or V _{CC}		±10.0	μA
C _{IN}	I/O capacitance	V _{IN} = GND f = 1.0 MHz		10.0	pF
I _{CC}	Operating Supply Current (low power mode, active)	V _I = GND, No load f = 1.0 MHz	30 (Typ)		mA

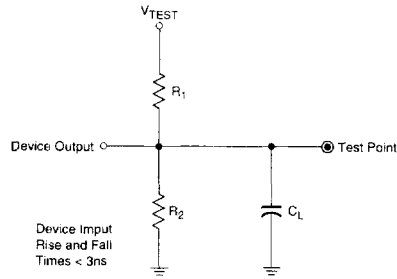
AC Characteristics

Symbol	Parameter	XC9536-5		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	I/O to output valid		5.0		7.5		10.0		15.0	ns
t _{SU}	I/O setup time before GCK	4.5		5.5		6.5		8.0		ns
t _H	I/O hold time after GCK	0.0		0.0		0.0		0.0		ns
t _{CO}	GCK to output valid		4.5		5.5		6.5		8.0	ns
f _{CNT} ¹	16-bit counter frequency	100		83		67		56		MHz
f _{SYSTEM} ²	Multiple FB internal operating frequency	100		83		67		56		MHz
t _{PSU}	I/O setup time before p-term clock input	0.5		1.5		2.5		4.0		ns
t _{PH}	I/O hold time after p-term clock input	4.0		4.0		4.0		4.0		ns
t _{PCO}	P-term clock to output valid		8.5		9.5		10.5		12.0	ns
t _{OE}	GTS to output valid		6.0		7.0		10.0		15.0	ns
t _{OD}	GTS to output disable		6.0		7.0		10.0		15.0	ns
t _{P OE}	Product term OE to output enabled		10.5		13.0		15.5		18.0	ns
t _{POD}	Product term OE to output disabled		10.5		13.0		15.5		18.0	ns
t _{WLH}	GCK pulse width (High or Low)		4.0		4.0		4.5		5.5	ns

Note: 1. f_{CNT} is the fastest 16-bit counter frequency available.

f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.

2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



V _{CCIO} Level	V _{TEST}	R ₁	R ₂	C _L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC9536-5		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Buffer Delays										
t _{IN}	Input buffer delay		1.5		2.5		3.5		4.5	ns
t _{GCK}	GCK buffer delay		2.0		2.5		3.0		3.0	ns
t _{GSR}	GSR buffer delay		4.0		4.5		6.0		7.5	ns
t _{GTS}	GTS buffer delay		6.0		7.0		10.0		15.0	ns
t _{OUT}	Output buffer delay		2.0		2.5		3.0		4.5	ns
t _{EN}	Output buffer enable/disable delay		0.0		0.0		0.0		0.0	ns
Product Term Control Delays										
t _{PTCK}	Product term clock delay		4.5		4.0		3.5		2.5	ns
t _{PTSR}	Product term set/reset delay		1.0		2.0		2.5		3.0	ns
t _{PTTS}	Product term 3-state delay		9.0		10.5		12.0		13.5	ns
Internal Register and Combinatorial delays										
t _{PDI}	Combinatorial logic propagation delay		0.5		0.5		1.0		3.0	ns
t _{SUI}	Register setup time	4.0		3.5		3.5		3.5		ns
t _{HI}	Register hold time	0.5		2.0		3.0		4.5		ns
t _{COI}	Register clock to output valid time		0.5		0.5		0.5		0.5	ns
t _{AOI}	Register async. S/R to output delay		6.0		6.5		7.0		8.0	ns
t _{RAI}	Register async. S/R recovery before clock	5.0		7.5		10.0		15.0		ns
t _{LOGI}	Internal logic delay		1.0		2.0		2.5		3.0	ns
t _{LOGILP}	Internal low power logic delay		9.0		10.0		11.0		11.5	ns
Feedback Delays										
t _F	FastCONNECT matrix feedback delay		4.5		6.0		8.5		11.0	ns
t _{LF}	Function Block local feedback delay		4.5		6.0		8.5		11.0	ns
Time Adders										
t _{PTA} ³	Incremental Product Term Allocator delay		1.0		1.0		1.0		1.5	ns
t _{SLEW}	Slew-rate limited delay		3.5		4.0		4.5		5.0	ns
Preliminary										

Note: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

XC9536 I/O Pins

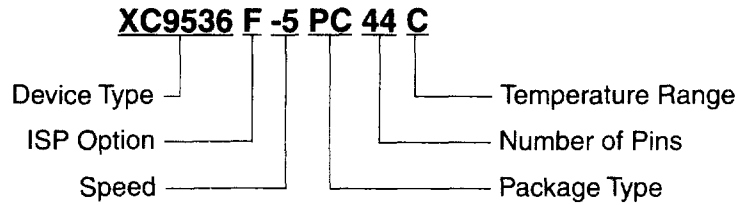
Function Block	Macrocell	PC44	VQ44	BScan Order	Notes	Function Block	Macrocell	PC44	VQ44	BScan Order	Notes
1	1	2	40	105		2	1	1	39	51	
1	2	3	41	102		2	2	44	38	48	
1	3	5	43	99	[1]	2	3	42	36	45	[1]
1	4	4	42	96		2	4	43	37	42	
1	5	6	44	93	[1]	2	5	40	34	39	[1]
1	6	8	2	90		2	6	39	33	36	[1]
1	7	7	1	87	[1]	2	7	38	32	33	
1	8	9	3	84		2	8	37	31	30	
1	9	11	5	81		2	9	36	30	27	
1	10	12	6	78		2	10	35	29	24	
1	11	13	7	75		2	11	34	28	21	
1	12	14	8	72		2	12	33	27	18	
1	13	18	12	69		2	13	29	23	15	
1	14	19	13	66		2	14	28	22	12	
1	15	20	14	63		2	15	27	21	9	
1	16	22	16	60		2	16	26	20	6	
1	17	24	18	57		2	17	25	19	3	
1	18	-	-	54		2	18	-	-	0	

Note: [1] Global control pin

XC9536 Global, JTAG and Power Pins

Pin Type	PC44	VQ44
I/O/GCK1	5	43
I/O/GCK2	6	44
I/O/GCK3	7	1
I/O/GTS1	42	36
I/O/GTS2	40	34
I/O/GSR	39	33
TCK	17	11
TDI	15	9
TDO	30	24
TMS	16	10
V _{CCINT} 5 V	21,41	15,35
V _{CCIO} 3.3 V/5 V	32	26
GND	23,10,31	17,4,25
No Connects	—	—

Ordering Information



ISP Options

- With ISP (blank)
- F Without ISP

Speed Options

- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay
- 7 7.5 ns pin-to-pin delay
- 5 5 ns pin-to-pin delay

Packaging Options

- PC44 44-Pin Plastic Leaded Chip Carrier (PLCC)
- VQ44 44-Pin Thin Quad Pack (VQFP)

Temperature Options

- C Commercial 0°C to 70°C
- I Industrial -40°C to 85°C

Component Availability

Pins		44	
Type		Plastic PLCC	Plastic VQFP
Code		PC44	VQ44
XC9536	-15	C(I)	C(I)
	-10	C(I)	C(I)
	-7	C	C
	-5	C	C
XC9536F	-15	C(I)	C(I)
	-10	C(I)	C(I)
	-7	C	C
	-5	C	C

C = Commercial = 0° to +70°C I = Industrial = -40° to 85°C