NEC

MOS INTEGRATED CIRCUIT

MC-421000AA64FA

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FA is a 1,048,576 words by 64 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA64-60	60 ns	110 ns	10.42 W	420 mW (CMOS level input)
MC-421000AA64-70	70 ns	130 ns	8.74 W	
MC-421000AA64-80	80 ns	150 ns	7.90 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

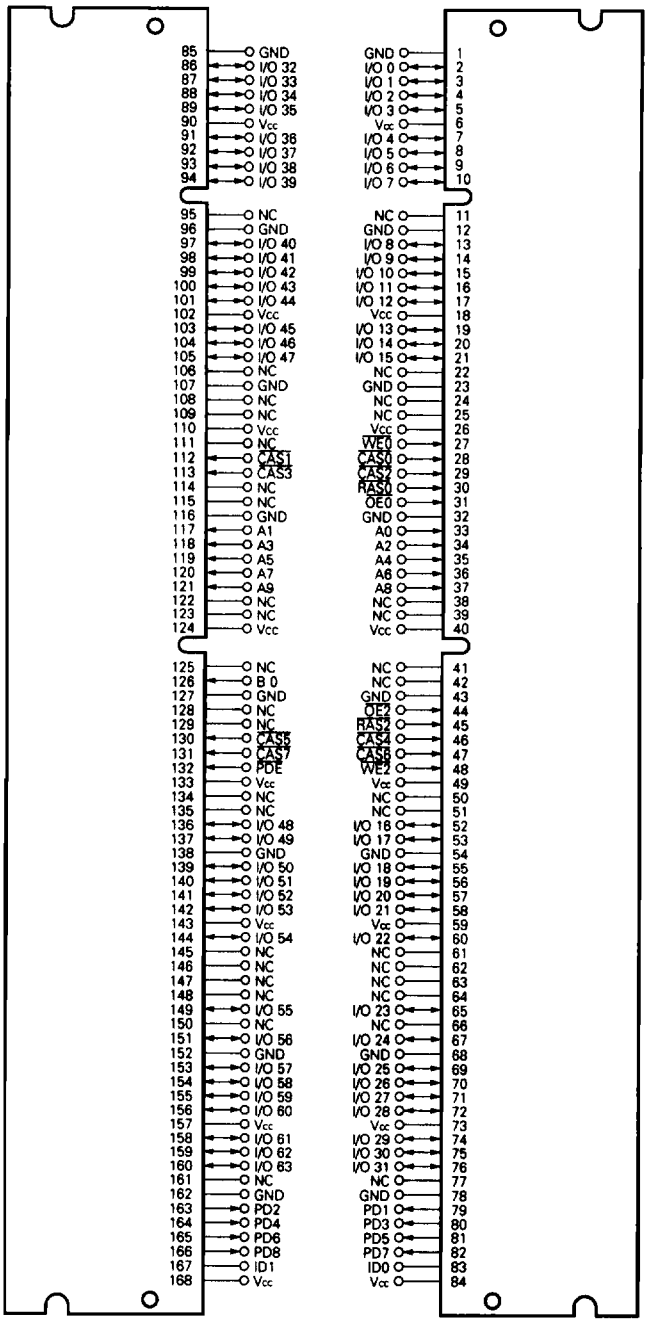
Document No. IC-3557A (Japan)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FA-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	16 pieces of μPD424400LA (300 mil SOJ) (Double side)
MC-421000AA64FA-70	70 ns		
MC-421000AA64FA-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



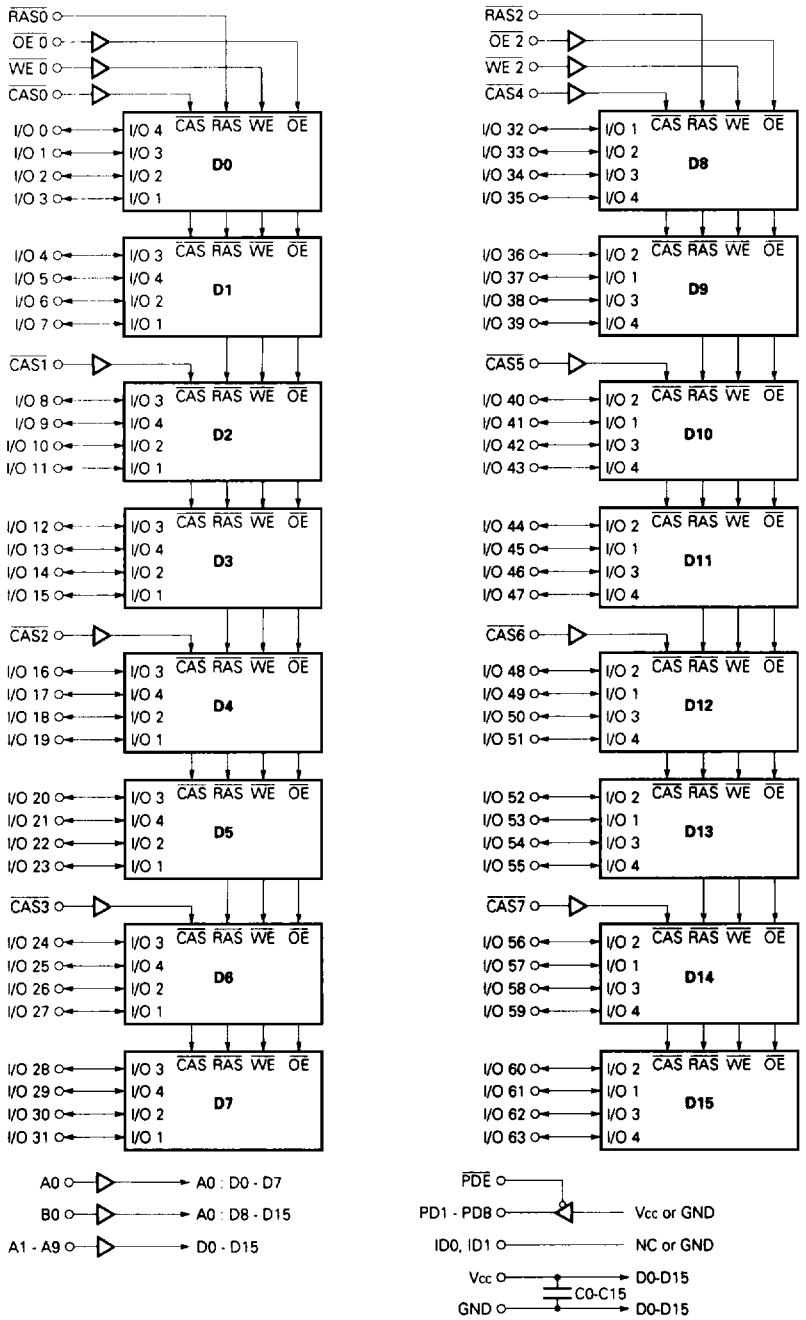
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D15 : μPD424400

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		18	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	C_{VO}	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,984	mA	3, 4, 7
			t_{RAC} = 70 ns			1,664		
			t_{RAC} = 80 ns			1,504		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA			96	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA			80		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,984	mA	3, 4, 5, 7
			t_{RAC} = 70 ns			1,664		
			t_{RAC} = 80 ns			1,504		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,504	mA	3, 4, 6
			t_{RAC} = 70 ns			1,344		
			t_{RAC} = 80 ns			1,184		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,984	mA	3, 4
			t_{RAC} = 70 ns			1,664		
			t_{RAC} = 80 ns			1,504		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		$\overline{RAS}$	–10	+10	μA	
				Others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)			–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA				0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) [Notes 8, 9]

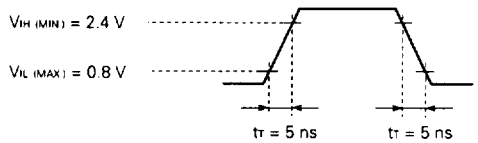
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		ns	
Read Modify Write Cycle Time	t_{RWC}	165		190		225		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	80		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	90		100		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	55		60		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55		60		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		ns	
$\overline{WE}$ Setup Time	t_{WSR}	0		0		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	10		10		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

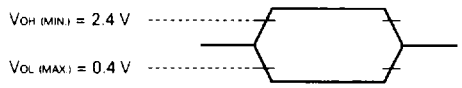
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

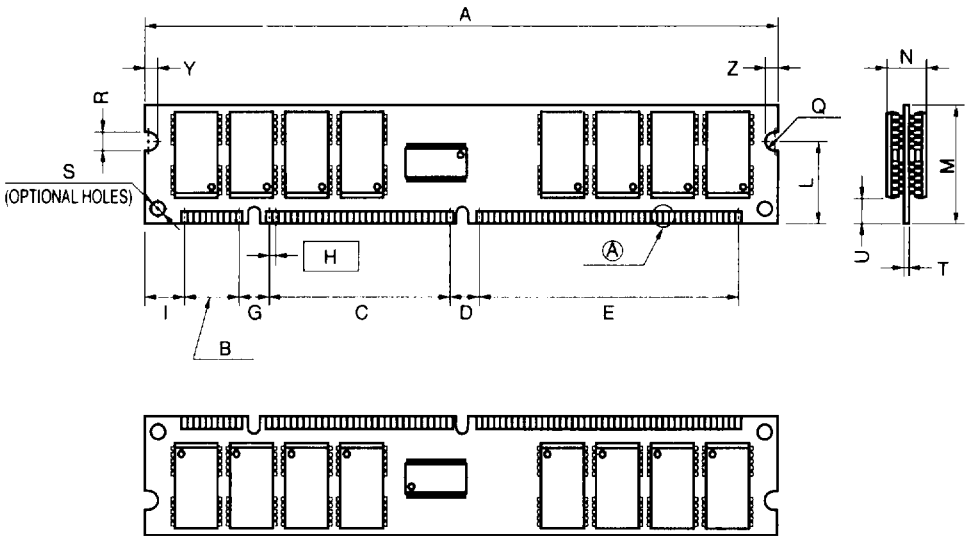
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

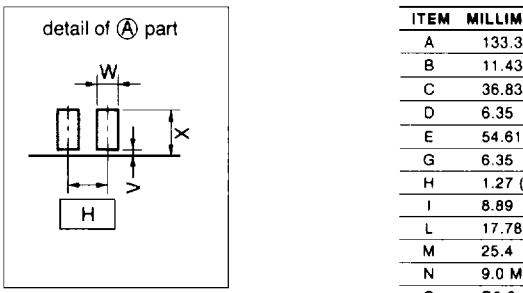
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
L	17.78	0.700
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

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