RAMBUS®

ADVANCE INFORMATION

Direct RDRAM™
32/36-Mbit (256Kx16/18x8d)

Overview

The Rambus Direct RDRAM™ is a general purpose high-performance memory device suitable for use in a broad range of applications including computer memory, graphics, video, and any other application where high bandwidth and low latency are required.

The 32/36-Mbit Direct Rambus DRAMs (RDRAM®) are extremely high-speed CMOS DRAMs organized as 2M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz or 800MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10ns per sixteen bytes).

The architecture of the Direct RDRAMs allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's eight banks support up to four simultaneous transactions.

System oriented features for mobile, graphics and large memory systems include power management, byte masking, and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth or for error correction.

Features

- Highest sustained bandwidth per DRAM device
  - 1.6GB/s sustained data transfer rate
  - Separate control and data buses for maximized efficiency
  - Separate row and column control buses for easy scheduling and highest performance
  - 8 banks: four transactions can take place simultaneously at full bandwidth data rates
- Low latency features
  - Write buffer to reduce read latency
  - 3 precharge mechanisms for controller flexibility
  - Interleaved transactions
- Advanced power management:
  - Multiple low power states allows flexibility in power consumption versus time to transition to active state
  - Power-down self-refresh
- Organization: 1Kbyte pages and 8 banks, x 16/18
  - x18 organization allows ECC configurations or increased storage/bandwidth
  - x16 organization for low cost applications
- Uses Rambus Signaling Level (RSL) for up to 800MHz operation

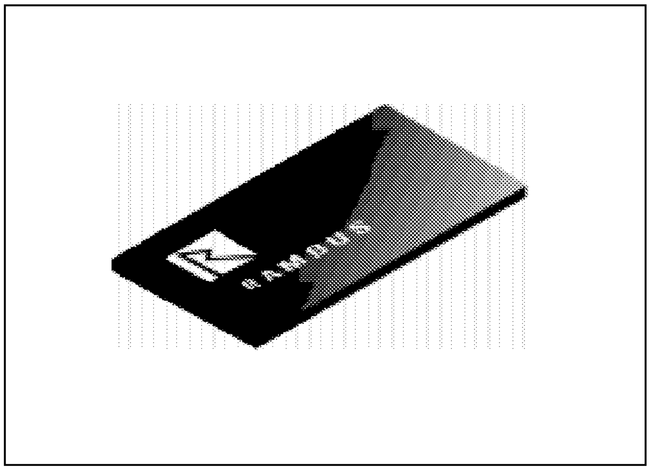


Figure 1: Direct RDRAM CSP Package

The 32/36-Mbit Direct RDRAMs are offered in a CSP horizontal package suitable for desktop as well as low-profile add-in card and mobile applications.

Direct RDRAMs operate from a 2.5 volt supply.

Key Timing Parameters/Part Numbers

Organization[a]	I/O Freq. MHz	Core Access Time (ns)	Part Number
256Kx16x8d	1000	TBD	32MD-TBD-1000
256Kx16x8d	1000	TBD	32MD-TBD-1000
256Kx16x8d	800	50	32MD-50-800
256Kx16x8d	800	45	32MD-45-800
256Kx16x8d	800	40	32MD-40-800
256Kx18x8d	1000	TBD	36MD-TBD-1000
256Kx18x8d	1000	TBD	36MD-TBD-1000
256Kx18x8d	800	50	36MD-50-800
256Kx18x8d	800	45	36MD-45-800
256Kx18x8d	800	40	362MD-40-800

[a] The “8d” designation indicates that this RDRAM core is composed of 8 banks which use a “doubled” bank architecture.

Related Documentation

Direct RDRAM Architectural Data Sheet	DL-0061-00.7
Direct RAC Data Sheet	DL-0064-00.7
Direct RMC.d1 Data Sheet	DL-0036-00.7
RIMM Data Sheet	DL-0053-00.7
SPD Application Brief	DL-0054-00.7

Pinouts and Definitions

Edge-Bonded Devices

This table shows the pin assignments of the edge-bomded RDRAM package from the top-side of the package (the view looking down on the package as it is mounted on the circuit board). The mechanical dimensions of this package are shown in a later section. Refer to Section "Edge-Bonded uBGA Package" on page 58.

Table 1: Edge-Bonded Device (top view)

7		GND	VDD	GND	VDD	GND	V-REF	VDD	GND	VDD	GND	VDD	GND	VDD	GND	
6	GND	DQA7	DQA5	DQA3	DQA1	CFMN	CTMN	RQ7	RQ5	RQ3	RQ1	DQB1	DQB3	DQB5	DQB7	GND
5	DQA8	DQA6	DQA4	DQA2	DQA0	CFM	CTM	RQ6	RQ4	RQ2	RQ0	DQB0	DQB2	DQB4	DQB6	DQB8
4			GND	VDD	VDD	GND	GNDa	GNDa	VDDa	VDDa	GND	VDD	VDD	GND		
3					SCK	CMD	VCMOS	GND	GND	VCMOS	SIO1	SIO0				
2																
1				VDD	GND	VDD	GND			VDD	GND	VDD	GND			
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
		x16														
	x18															

Center-Bonded Devices - Preliminary

This table shows the pin assignments of the center-bonded RDRAM package from the top-side of the package (the view looking down on the package as it is mounted on the circuit board). The mechanical dimensions of this package are shown in a later sectio. Refer to Section "Center-Bonded uBGA Package" on page 59.

Table 2: Center-Bonded Device (top view)

8	GND	VDD	GND	VDD	GND	VDD	GND	GND	VDD
7	CMD	DQA7	DQA1	CTM	RQ7	RQ1	RQ0	DQB6	DQB7
6	SCK	DQA4	DQA0	CTMN	RQ6	RQ2	DQB0	DQB4	DQB8
5									
4									
3	VCMOS	DQA5	DQA2	CFMN	VREF	RQ3	DQB1	DQB5	SIO0
2	DQA8	DQA6	DQA3	CFM	RQ5	RQ4	DQB2	DQB3	SIO1
1	GND	VDD	GND	GNDa	VDDa	GND	VDD	GND	VCMOS
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**

Table 3: Pin Description

Signal	I/O	Type	# Pins edge	# Pins center	Description
SIO1,SIO0	I/O	CMOS	2	2	Serial input/output. Pins for reading from and writing to the control registers using a serial access protocol. Also used for power management.
CMD	I	CMOS	1	1	Command input. Pins used in conjunction with SIO0 and SIO1 for reading from and writing to the control registers. Also used for power management.
SCK	I	CMOS	1	1	Serial clock input. Clock source used for reading from and writing to the control registers
V_{DD}			14	6	Supply voltage for the RDRAM core and interface logic.
V_{DDa}			2	1	Supply voltage for the RDRAM analog circuitry.
V_{CMOS}			2	2	Supply voltage for CMOS input/output pins.
GND			19	9	Ground reference for RDRAM core and interface.
GNDa			2	1	Ground reference for RDRAM analog circuitry.
DQA8..DQA0	I/O	RSL	9	9	Data byte A. Nine pins which carry a byte of read or write data between the Channel and the RDRAM. DQA8 is not used by RDRAMs with a x16 organization.
CFM	I	RSL	1	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	I	RSL	1	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity
V_{REF}			1	1	Logic threshold reference voltage for RSL signals
CTMN	I	RSL	1	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
CTM	I	RSL	1	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RQ7..RQ5 or ROW2..ROW0	I	RSL	3	3	Row access control. Three pins containing control and address information for row accesses.
RQ4..RQ0 or COL4..COL0	I	RSL	5	5	Column access control. Five pins containing control and address information for column accesses.
DQB8.. DQB0	I/O	RSL	9	9	Data byte B. Nine pins which carry a byte of read or write data between the Channel and the RDRAM. DQB8 is not used by RDRAMs with a x16 organization.
Total pin count per package			74	54	

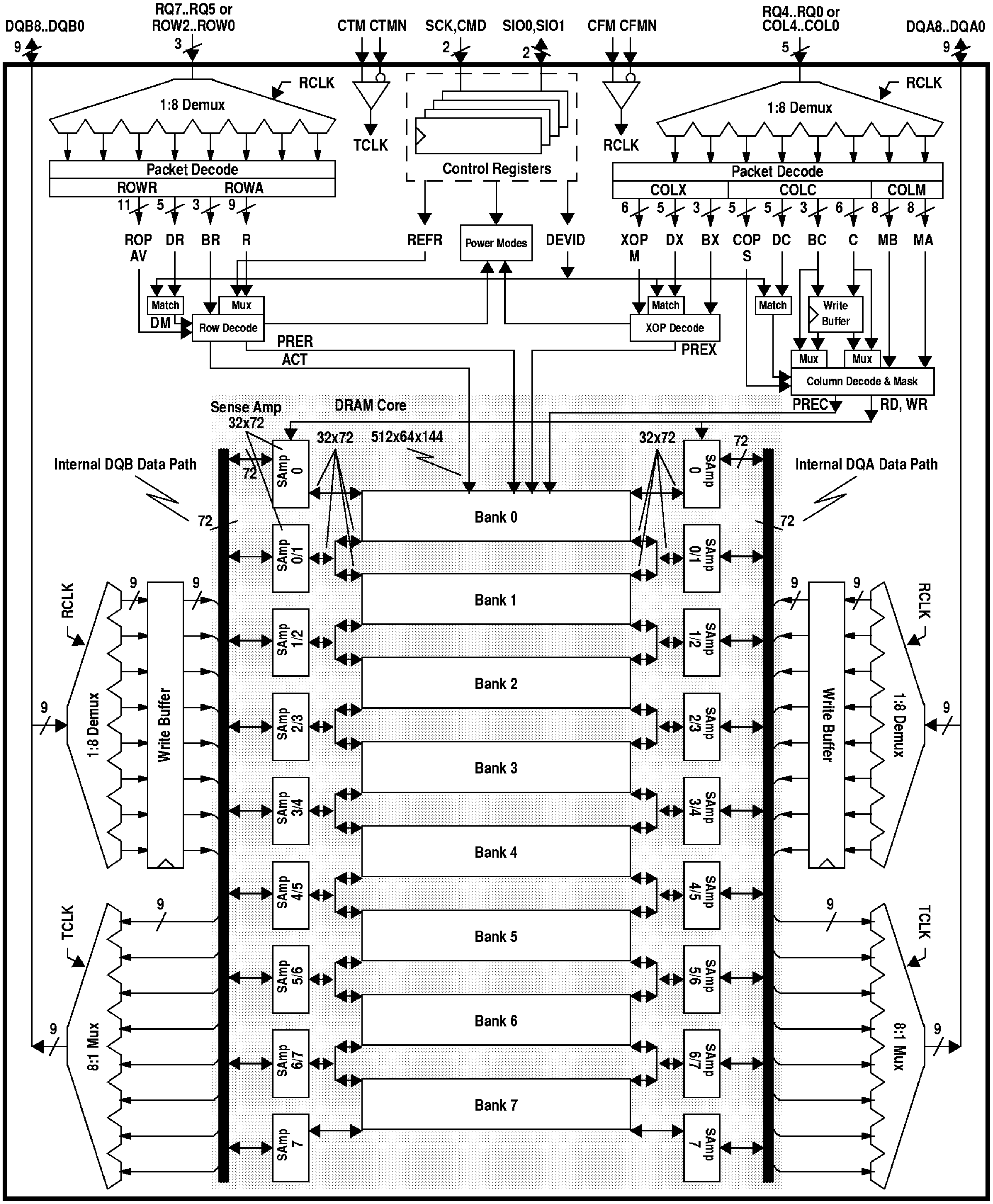


Figure 2: 32/36 Mbit Direct RDRAM Block Diagram

General Description

Figure 2 is a block diagram of the 32/36 Mbit Direct RDRAM. It consists of two major blocks: a "core" block built from banks and sense amps similar to those found in other types of DRAM, and a Direct Rambus interface block which permits an external controller to access this core at up to 1.6GB/s.

Control Registers: The CMD, SCK, SIO0, and SIO1 pins appear in the upper center of Figure 2. They are used to write and read a block of control registers. These registers supply the RDRAM configuration information to a controller and they select the operating modes of the device. The nine bit REFR value is used for tracking the last refreshed row. Most importantly, the five bit DEVID specifies the device address of the RDRAM on the Channel.

Clocking: The CTM and CTMN pins (Clock-To-Master) generate TCLK (Transmit Clock), the internal clock used to transmit read data. The CFM and CFMN pins (Clock-From-Master) generate RCLK (Receive Clock), the internal clock signal used to receive write data and to receive the ROW and COL pins.

DQA,DQB Pins: These 18 pins carry read (Q) and write (D) data across the Channel. They are multiplexed/de-multiplexed from/to two 72-bit data paths (running at one-eighth the data frequency) inside the RDRAM.

Banks: The 4Mbyte core of the RDRAM is divided into eight 0.5Mbyte banks, each organized as 512 rows, with each row containing 64 dualocts, and each dualoct containing 16 bytes. A dualoct is the smallest unit of data that can be addressed.

Sense Amps: The RDRAM contains 9 sense amps. Each sense amp consists of 512 bytes of fast storage (256 for DQA and 256 for DQB) and can hold one-half of one row of one bank of the RDRAM. The sense amp may hold any of the 512 half-rows of an associated bank. However, each sense amp is shared between two adjacent banks of the RDRAM (except for numbers 0 and 7). This introduces the restriction that adjacent banks may not be simultaneously accessed.

RQ Pins: These pins carry control and address information. They are broken into two groups. RQ7..RQ5 are also called ROW2..ROW0, and are used primarily for controlling row accesses. RQ4..RQ0 are also called COL4..COL0, and are used primarily for controlling column accesses.

ROW Pins: The principle use of these three pins is to manage the transfer of data between the banks and the sense amps of the RDRAM. These pins are de-multiplexed into a 24-bit ROWA (row-activate) or ROWR (row-operation) packet.

COL Pins: The principle use of these five pins is to manage the transfer of data between the DQA/DQB pins and the sense amps of the RDRAM. These pins are de-multiplexed into a 23-bit COLC (column-operation) packet and either a 17-bit COLM (mask) packet or a 17-bit COLX (extended-operation) packet.

ACT Command: An ACT (activate) command from an ROWA packet causes one of the 512 rows of the selected bank to be loaded to its associated sense amps (two 256 byte sense amps for DQA and two for DQB).

PRER Command: A PRER (precharge) command from an ROWR packet causes the selected bank to release its two associated sense amps, permitting a different row in that bank to be activated, or permitting adjacent banks to be activated.

RD Command: The RD (read) command causes one of the 64 dualocts of one of the sense amps to be transmitted on the DQA/DQB pins of the Channel.

WR Command: The WR (write) command causes a dualoct received from the DQA/DQB data pins of the Channel to be loaded into the write buffer. There is also space in the write buffer for the BC bank address and C column address information. The data in the write buffer is automatically retired (written with optional bytemask) to one of the 64 dualocts of one of the sense amps during a subsequent COP command. A retire can take place during a RD, WR, or NOCOP to another device, or during a WR or NOCOP to the same device. The write buffer will not retire during a RD to the same device. The write buffer reduces the delay needed for the internal DQA/DQB data path turn-around.

PREC Precharge: The RDA and WRA commands are similar to RD and WR, except that a precharge operation (PREC) is scheduled at the end of the data transfer. These commands provide a second mechanism for performing precharge.

PREX Precharge: After a RD command, or after a WR command with no byte masking (M=0), a COLX packet may be used to specify an extended operation (XOP). The most important XOP command is PREX. This command provides a third mechanism for performing precharge.

Packet Format

Figure 3 shows the formats of the ROWA and ROWR packets on the ROW pins. Table 4 describes the fields which comprise these packets. DR4T and DR4F bits are encoded to contain both the DR4 device address bit and a framing bit which allows the ROWA or ROWR packet to be recognized by the RDRAM.

The AV (ROWA/ROWR packet selection) bit distinguishes between the two packet types. Both the ROWA and ROWR packet provide a five bit device address and a three bit bank address. An ROWA packet uses the remaining bits to specify a nine bit row address, and the ROWR packet uses the remaining bits for an eleven bit opcode field. Note the use of the "RsvX" notation to reserve bits for future address field extension.

Table 4: Field Description for ROWA Packet and ROWR Packet

Field	Description
DR4T,DR4F	Bits for framing (recognizing) a ROWA or ROWR packet. Also encodes highest device address bit.
DR3..DR0	Device address for ROWA or ROWR packet.
BR2..BR0	Bank address for ROWA or ROWR packet. RsvB denotes bits reserved for future address extension.
AV	Selects between ROWA packet (AV=1) and ROWR packet (AV=0).
R8..R0	Row address for ROWA packet. RsvR denotes bits reserved for future row address extension.
ROP10..ROP0	Opcode field for ROWR packet. Specifies precharge, refresh, and power management functions.

Figure 3 also shows the formats of the COLC, COLM, and COLX packets on the COL pins. Table 5 describes the fields which comprise these packets.

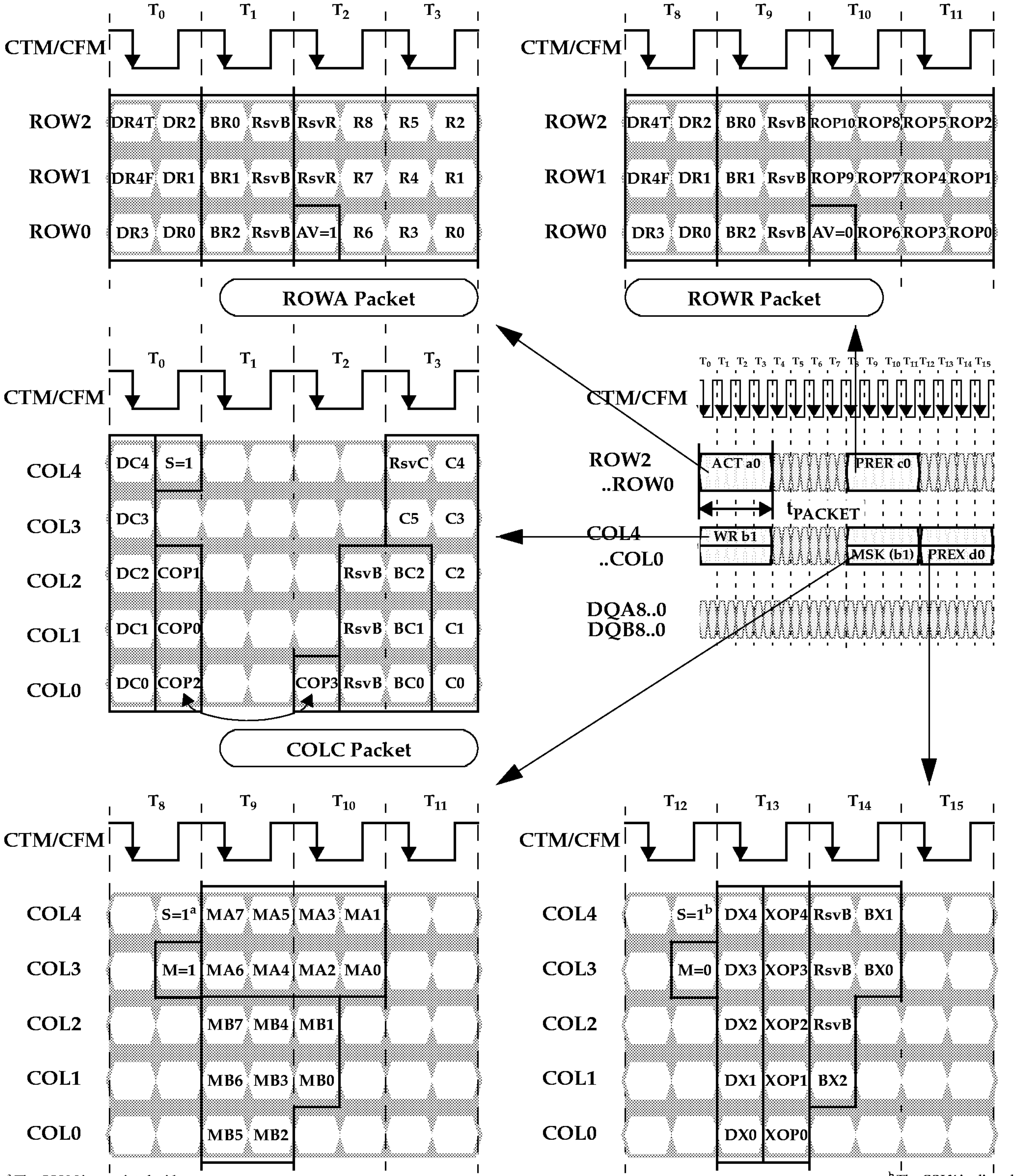
The COLC packet uses the S (Start) bit for framing. A COLM or COLX packet is aligned with this COLC packet, and is also framed by the S bit.

The 23 bit COLC packet has a five bit device address, a three bit bank address, a six bit column address, and a four bit opcode. The COLC packet specifies a read or write command, as well as some power management commands.

The remaining 17 bits are interpreted as a COLM (M=1) or COLX (M=0) packet. A COLM packet is used for a COLC write command which needs bytemask control. The COLM packet is associated with the COLC packet from a time t_{RTR} earlier. An COLX packet may be used to specify an independent precharge command. It contains a five bit device address, a three bit bank address, and a five bit opcode. The COLX packet may also be used to specify some housekeeping and power management commands. The COLX packet is framed within a COLC packet but is not otherwise associated with any other packet.

Table 5: Field Description for COLC Packet, COLM Packet, and COLX Packet

Field	Description
S	Bit for framing (recognizing) a COLC packet, and indirectly for framing COLM and COLX packets.
DC4..DC0	Device address for COLC packet.
BC2..BC0	Bank address for COLC packet. RsvB denotes bits reserved for future bank address extension.
C5..C0	Column address for COLC packet. RsvC denotes bits reserved for future column address extension.
COP3..COP0	Opcode field for COLC packet. Specifies read, write, precharge, and power management functions.
M	Selects between COLM packet (M=1) and COLX packet (M=0).
MA7..MA0	Bytemask write control bits. 1=write, 0=no-write. MA0 controls the earliest byte on DQA8..0.
MB7..MB0	Bytemask write control bits. 1=write, 0=no-write. MB0 controls the earliest byte on DQB8..0.
DX4..DX0	Device address for COLX packet.
BX2..BX0	Bank address for COLX packet. RsvB denotes bits reserved for future bank address extension.
XOP4..XOP0	Opcode field for COLX packet. Specifies precharge, I_{OL} control, and power management functions.



[a] The COLM is associated with a previous COLC, and is aligned with the present COLC, indicated by the Start bit (S=1) position.

[b] The COLX is aligned with the present COLC, indicated by the Start bit (S=1) position.

Figure 3: Packet Formats

Field Encoding Summary

Table 6 shows how the six device address bits are decoded for the ROWA and ROWR packets. The DR4T and DR4F encoding merges a fifth device bit with a framing bit. When neither bit is asserted, the device is not selected. Note that a broadcast operation is indicated when both bits are set. Broadcast operation would typically be used for refresh and power management commands. If the device is selected, the DM (DeviceMatch) signal is asserted and an ACT or ROP command is performed.

Table 6: Device Field Encodings for ROWA Packet and ROWR Packet

DR4T	DR4F	Device Selection	Device Match signal (DM)
1	1	All devices (broadcast)	DM is set to 1
0	1	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {0,DR3..DR0} else DM is set to 0
1	0	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {1,DR3..DR0} else DM is set to 0
0	0	No packet present	DM is set to 0

Table 7 shows the encodings of the remaining fields of the ROWA and ROWR packets. An ROWA packet is specified by asserting the AV bit. This causes the specified row of the specified bank of this device to be loaded into the associated sense amps.

An ROWR packet is specified when AV is not asserted. An 11 bit opcode field encodes a command for one of the banks of this device. The PRER command causes a bank and its two associated sense amps to precharge, so another row or an adjacent bank may be activated. The REFA (refresh-activate) command is similar to the ACT command, except the row address comes from an internal register REFR, and REFR is incremented at the largest bank address. The REFP (refresh-precharge) command is identical to a PRER command.

The NAPR, NAPRC, PDNR, ATTN, and RLXR commands are used for managing the power dissipation of the RDRAM and are described in more detail in "Power State Management" on page 38. The TCEN and TCAL commands are used to adjust the output driver slew rate and they are described in more detail in "Current and Temperature Control" on page 43.

Table 7: ROWA Packet and ROWR Packet Field Encodings

DM[a]	AV	ROP10..ROP0 Field									Name	Command Description
		10	9	8	7	6	5	4	3	2:0		
0	-	-	-	-	-	-	-	-	-	---	-	No operation.
1	1	Row address									ACT	Activate row R8..R0 of bank BR3..BR0 of device and move device to ATTN[b].
1	0	1	1	0	0	0	x[c]	x	x	000	PRER	Precharge bank BR3..BR0 of this device.
1	0	0	0	0	1	1	0	0	x	000	REFA	Refresh (activate) row REFR8..REFR0 of bank BR2..BR0 of device. Increment REFR if BR2..BR0 = 1111 (see Figure 49).
1	0	1	0	1	0	1	0	0	x	000	REFP	Precharge bank BR2..BR0 of this device after REFA (see Figure 49).
1	0	x	x	0	0	0	0	1	x	000	PDNR	Move this device into the powerdown (PDN) power state (see Figure 46).
1	0	x	x	0	0	0	1	0	x	000	NAPR	Move this device into the nap (NAP) power state (see Figure 46).
1	0	x	x	0	0	0	1	1	x	000	NAPRC	Move this device into the nap (NAP) power state conditionally
1	0	x	x	x	x	x	x	x	0	000	ATTN[b]	Move this device into the attention (ATTN) power state (see Figure 44).
1	0	x	x	x	x	x	x	x	1	000	RLXR	Move this device into the standby (STBY) power state (see Figure 45).
1	0	0	0	0	0	0	0	0	x	001	TCAL	Temperature calibrate this device (see Figure 51).
1	0	0	0	0	0	0	0	0	x	010	TCEN	Temperature calibrate/enable this device (see Figure 51).
1	0	0	0	0	0	0	0	0	0	000	NOROP	No operation.

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[a] The DM (Device Match signal) value is determined by the DR4T,DR4F, DR3..DR0 field of the ROWA and ROWR packets. See Table 6.

[b] The device's power state remains unchanged for a broadcast operation (DR4T/DR4F=1/1).

[c] An "x" entry indicates which commands may be combined. For instance, the three commands PRER/NAPRC/RLXR may be specified in one ROP value (011000111000).

Table 8 shows the COP field encoding. The device must be in the ATTN power state in order to receive COLC packets. The COLC packet is used primarily to specify RD (read) and WR (write) commands. Retire operations (moving data from the write buffer to a sense amp) happen automatically. See Figure 17 for a more detailed description.

The COLC packet can also specify a PREC command, which precharges a bank and its associated sense amps. The RDA/WRA commands are equivalent to a RD/WR followed by a PREC. RLXC (relax) performs a power mode transition. See "Power State Management" on page 38.

Table 8: COLC Packet Field Encodings

S	DC4.. DC0 (select device)[a]	COP3..0	Name	Command Description
0	----	-----	-	No operation.
1	/= (DEVID4 ..0)	-----	-	Retire write buffer of this device.
1	== (DEVID4 ..0)	x000[b]	NOCOP	Retire write buffer of this device.
1	== (DEVID4 ..0)	x001	WR	Retire write buffer of this device, then write column C5..C0 of bank BC2..BC0 to write buffer.
1	== (DEVID4 ..0)	x010	RSRV	Reserved, no operation.
1	== (DEVID4 ..0)	x011	RD	Read column C5..C0 of bank BC2..BC0 of this device.
1	== (DEVID4 ..0)	x100	PREC	Retire write buffer of this device, then precharge bank BC2..BC0 (see Figure 14).
1	== (DEVID4 ..0)	x101	WRA	Same as WR, but precharge bank BC2..BC0 after write buffer (with new data) is retired.
1	== (DEVID4 ..0)	x110	RSRV	Reserved, no operation.
1	== (DEVID4 ..0)	x111	RDA	Same as RD, but precharge bank BC2..BC0 afterward.
1	== (DEVID4 ..0)	1xxx	RLXC	Move this device into the standby (STBY) power state (see Figure 45).

a. "/=" means not equal, "==" means equal.
b. An "x" entry indicates which commands may be combined. For instance, the two commands WR/RLXC may be specified in one COP value (1001).

Table 9 shows the COLM and COLX field encodings. The M bit is asserted to specify a COLM packet with two 8 bit bytemask fields MA and MB. If the M bit is not asserted, an COLX is specified. It has device and bank address fields, and an opcode field. The primary use of the COLX packet is to permit an independent PREX (precharge) command to be specified without consuming control bandwidth on the ROW pins. It is also used for the CAL(calibrate) and SAM (sample) current control commands (see "Current and Temperature Control" on page 43), and for the RLXX power mode command (see "Power State Management" on page 38).

Table 9: COLM Packet and COLX Packet Field Encodings

M	DX4 .. DX0 (selects device)	XOP4..0	Name	Command Description
1	----	-	MSK	MB/MA bytemasks used by WR/WRA.
0	/= (DEVID4 ..0)	-	-	No operation.
0	== (DEVID4 ..0)	00000	NOXOP	No operation.
0	== (DEVID4 ..0)	1xxx0[a]	PREX	Precharge bank BX2..BX0 of this device (see Figure 14).
0	== (DEVID4 ..0)	x1xx0	CAL	Calibrate (drive) I_{OL} current for this device (see Figure 50).
0	== (DEVID4 ..0)	xx1x0	SAM	Sample (update) I_{OL} current for this device (see Figure 50).
0	== (DEVID4 ..0)	xxx10	RLXX	Move this device into the standby (STBY) power state (see Figure 45).
0	== (DEVID4 ..0)	xxxx1	RSRV	Reserved, no operation.

a. An "x" entry indicates which commands may be combined. For instance, the two commands PREX/RLXX may be specified in one XOP value (10010).

DQ Packet Timing

Figure 4 shows the timing relationship of COLC packets with D and Q data packets. This document uses a specific convention for measuring time intervals between packets: all packets on the ROW and COL pins (ROWA, ROWR, COLC, COLM, COLX) use the trailing edge of the packet as a reference point, and all packets on the DQA/DQB pins (D and Q) use the leading edge of the packet as a reference point.

An RD or RDA command will transmit a dualoct of read data Q a time t_{CAC} later. This time includes one to five cycles of round-trip propagation delay on the Channel. The t_{CAC} parameter may be programmed to a one of a range of values (7, 8, 9, 10, 11, or 12 t_{CYCLE}). The value chosen depends upon the number of RDRAM devices on the Channel and the RDRAM timing bin. See Figure 39 for more information.

A WR or WRA command will receive a dualoct of write data D a time t_{CWD} later. This time does not need to include the round-trip propagation time of the Channel since the COLC and D packets are traveling in the same direction.

When a Q packet follows a D packet (shown in the left half of the figure), a gap (t_{CAC} -t_{CWD}) will automatically appear between them because the t_{CWD} value is always less than the t_{CAC} value. There will be no gap between the two COLC packets with the WR and RD commands which schedule the D and Q packets.

When a D packet follows a Q packet (shown in the right half of the figure), no gap is needed between them because the t_{CWD} value is less than the t_{CAC} value. However, , a gap of t_{CAC} -t_{CWD} or greater must be inserted between the COLC packets with the RD WR commands by the controller so the Q and D packets do not overlap.

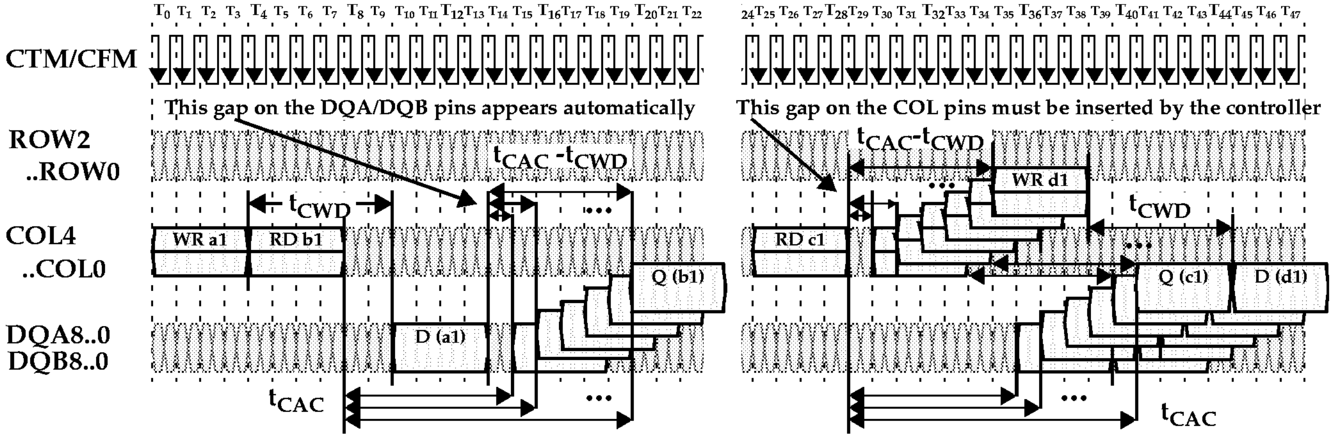


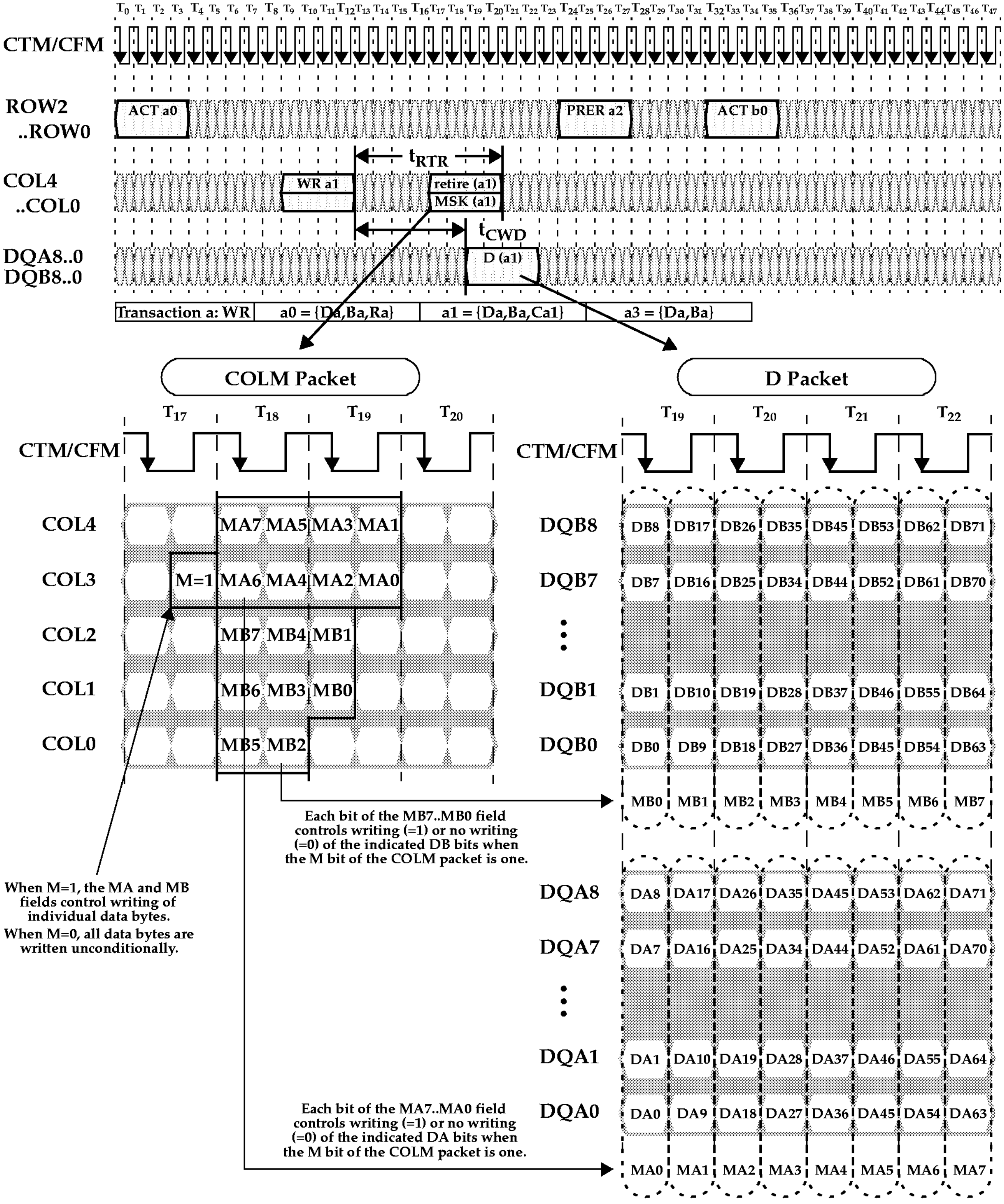
Figure 4: Read (Q) and Write (D) Data Packet - Timing for t_{CAC} = 7, 8, 9, 10, 11, or 12 t_{CYCLE}

COLM Packet to D Packet Mapping

Figure 5 shows a write operation initiated by a WR command in a COLC packet. If a subset of the 16 bytes of write data are to be written, then a COLM packet is transmitted on the COL pins a time t_{RTR} after the COLC packet containing the WR command. The M bit of the COLM packet is set to indicate that it contains the MA and MB mask fields. Note that this COLM packet is aligned with the COLC packet which causes the write buffer to be retired. See Figure 17 for more details.

If all 16 bytes of the D data packet are to be written, then no further control information is required. The packet slot that would have been used by the COLM packet (t_{RTR} after the COLC packet) is available to be used as an COLX packet. This could be used for a PREX precharge command or for a housekeeping command (this case is not shown). The M bit is not asserted in an COLX packet and causes all 16 bytes of the previous WR to be written unconditionally. Note that a RD command will never need a COLM packet, and will always be able to use the COLX packet option (a read operation has no need for the byte-write-enable control bits).

Figure 5 also shows the mapping between the MA and MB fields of the COLM packet and bytes of the D packet on the DQA and DQB pins. Each mask bit controls whether a byte of data is written (=1) or not written (=0).



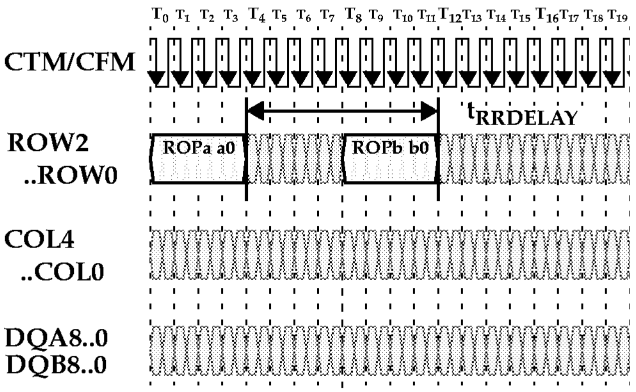
Each bit of the MB7..MB0 field controls writing (=1) or no writing (=0) of the indicated DB bits when the M bit of the COLM packet is one.

When M=1, the MA and MB fields control writing of individual data bytes.
When M=0, all data bytes are written unconditionally.

Each bit of the MA7..MA0 field controls writing (=1) or no writing (=0) of the indicated DA bits when the M bit of the COLM packet is one.

Figure 5: Mapping Between COLM Packet and D Packet for WR Command

ROW-to-ROW Packet Interaction



Transaction a: ROPa	a0 = {Da,Ba,Ra}
Transaction b: ROPb	b0= {Db,Bb,Rb}

Figure 6: ROW-to-ROW Packet Interaction- Timing

Figure 6 shows two packets on the ROW pins separated by an interval $t_{RRDELAY}$ which depends upon the packet contents. No other ROW packets are sent to banks {Ba,Ba+1,Ba-1} between packet "a" and packet "b" unless noted otherwise. Table 10 summarizes the $t_{RRDELAY}$ values for all possible cases.

Cases RR1 through RR4 show two successive ACT commands. In case RR1, there is no restriction since the ACT commands are to different devices. In case RR2, the t_{RR} restriction applies to the same device with non-adjacent banks. Cases RR3 and RR4 are illegal (as shown) since bank Ba needs to be precharged. If a PRER to Ba, Ba+1, or Ba-1 is inserted, $t_{RRDELAY}$ is t_{RC} (t_{RAS} to the PRER command, and t_{RP} to the next ACT).

Cases RR5 through RR8 show an ACT command followed by a PRER command. In cases RR5 and RR6, there are no restrictions since the commands are to different devices or to non-adjacent banks of the same device. In cases RR7 and RR8, the t_{RAS} restriction means the activated bank must wait before it can be precharged.

Cases RR9 through RR12 show a PRER command followed by an ACT command. In cases RR9 and RR10, there are essentially no restrictions since the commands are to different devices or to non-adjacent banks of the same device. RR10a and RR10b depend upon whether a bracketed bank (Ba+-1) is precharged or activated. In cases RR11 and RR12, the same and adjacent banks must all wait t_{RP} for the sense amp and bank to precharge before being activated.

Table 10: ROW-to-ROW Packet Interaction - Rules

Case #	ROPa	Da	Ba	Ra	ROPb	Db	Bb	Rb	$t_{RRDELAY}$	Example
RR1	ACT	Da	Ba	Ra	ACT	/= Da	xxxx	x..x	t_{PACKET}	Figure 11
RR2	ACT	Da	Ba	Ra	ACT	== Da	/= {Ba,Ba+1,Ba-1}	x..x	t_{RR}	Figure 11
RR3	ACT	Da	Ba	Ra	ACT	== Da	== {Ba+1,Ba-1}	x..x	t_{RC} - illegal unless PRER to Ba/Ba+1/Ba-1	Figure 10
RR4	ACT	Da	Ba	Ra	ACT	== Da	== {Ba}	x..x	t_{RC} - illegal unless PRER to Ba/Ba+1/Ba-1	Figure 10
RR5	ACT	Da	Ba	Ra	PRER	/= Da	xxxx	x..x	t_{PACKET}	Figure 11
RR6	ACT	Da	Ba	Ra	PRER	== Da	/= {Ba,Ba+1,Ba-1}	x..x	t_{PACKET}	Figure 11
RR7	ACT	Da	Ba	Ra	PRER	== Da	== { Ba+1,Ba-1}	x..x	t_{RAS}	Figure 10
RR8	ACT	Da	Ba	Ra	PRER	== Da	== {Ba}	x..x	t_{RAS}	Figure 15
RR9	PRER	Da	Ba	Ra	ACT	/= Da	xxxx	x..x	t_{PACKET}	Figure 12
RR10	PRER	Da	Ba	Ra	ACT	== Da	/= {Ba,Ba+-1,Ba+-2}	x..x	t_{PACKET}	Figure 12
RR10a	PRER	Da	Ba	Ra	ACT	== Da	== {Ba+2}	x..x	t_{PACKET}/t_{RP} if Ba+1 is precharged/activated.	
RR10b	PRER	Da	Ba	Ra	ACT	== Da	== {Ba-2}	x..x	t_{PACKET}/t_{RP} if Ba-1 is precharged/activated.	
RR11	PRER	Da	Ba	Ra	ACT	== Da	== {Ba+1,Ba-1}	x..x	t_{RP}	Figure 10
RR12	PRER	Da	Ba	Ra	ACT	== Da	== {Ba}	x..x	t_{RP}	Figure 10
RR13	PRER	Da	Ba	Ra	PRER	/= Da	xxxx	x..x	t_{PACKET}	Figure 12
RR14	PRER	Da	Ba	Ra	PRER	== Da	/= {Ba,Ba+1,Ba-1}	x..x	t_{PP}	Figure 12
RR15	PRER	Da	Ba	Ra	PRER	== Da	== {Ba+1,Ba-1}	x..x	t_{PP}	Figure 12
RR16	PRER	Da	Ba	Ra	PRER	== Da	== Ba	x..x	t_{PP}	Figure 12

ROW-to-ROW Interaction - continued

Cases RR13 through RR16 summarize the combinations of two successive PRER commands. In case RR13 there is no restriction since two devices are addressed. In RR14, t_{PP} applies, since the same device is addressed. In RR15 and RR16, the same bank or an adjacent bank may be given repeated PRER commands with only the t_{PP} restriction.

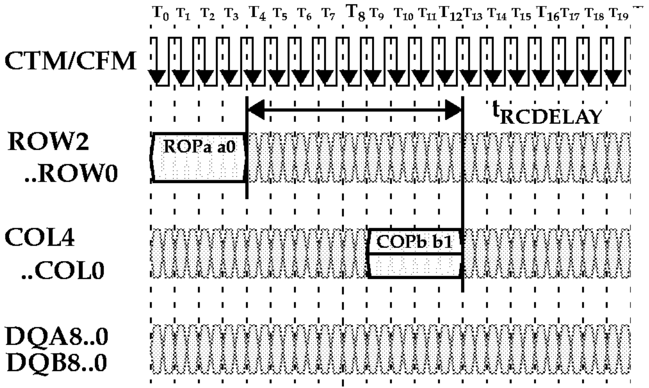
Two adjacent banks can't be activate simultaneously. A precharge command to one bank will thus affect the state of the adjacent banks (and sense amps). If bank Ba is activate and a PRER is directed to Ba, then bank Ba will be precharged along with sense amps Ba-1/Ba and Ba/Ba+1. If bank Ba+1 is activate and a PRER is directed to Ba, then bank Ba+1 will be precharged along with sense amps Ba/Ba+1 and Ba+1/Ba+2. If bank Ba-1 is activate and a PRER is directed to Ba, then bank Ba-1 will be precharged along with sense amps Ba/Ba-1 and Ba-1/Ba-2.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, NAPRC, PDNR, RLXR, ATTN, TCAL, and TCEN commands are discussed in later sections (see Table 7 for cross-ref).

ROW-to-COL Packet Interaction

Figure 7 shows two packets on the ROW and COL pins. They must be separated by an interval $t_{RCDELAY}$ which depends upon the packet contents. Table 11 summarizes the $t_{RCDELAY}$ values for all possible cases. Note that if the COL packet is earlier than the ROW packet, it is considered a COL-to-ROW packet interaction.

Cases RC1 through RC5 summarize the rules when the ROW packet has an ACT command. Figure 15 and Figure 16 show examples of RC5 - an activation followed by a read or write. RC4 is an illegal situation, since a read or write of a precharged banks is being attempted (remember that for a bank to be activated, adjacent banks must be precharged). In cases RC1, RC2, and RC3, there is no interaction of the ROW and COL packets.



Transaction a: ROPa	a0 = {Da,Ba,Ra}
Transaction b: COPb	b1= {Db,Bb,Cb1}

Figure 7: ROW-to-COL Packet Interaction- Timing

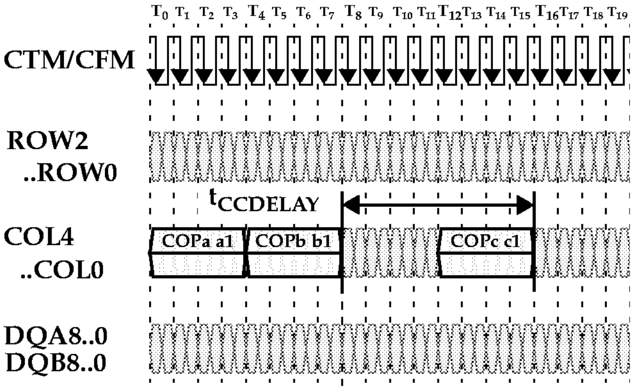
Cases RC6 through RC8 summarize the rules when the ROW packet has a PRER command. There is either no interaction (RC6 through RC9) or an illegal situation with a read or write of a precharged bank (RC9).

The COL pins can also schedule a precharge operation with a RDA, WRA, or PREC command in a COLC packet or a PREX command in a COLX packet. The constraints of these precharge operations may be converted to equivalent PRER command constraints using the rules summarized in Figure 14.

Table 11: ROW-to-COL Packet Interaction - Rules

Case #	ROPa	Da	Ba	Ra	COPb	Db	Bb	Cb1	$t_{RCDELAY}$	Example
RC1	ACT	Da	Ba	Ra	NOCOP,RD,WR	/= Da	xxxx	x..x	0	
RC2	ACT	Da	Ba	Ra	NOCOP	== Da	xxxx	x..x	0	
RC3	ACT	Da	Ba	Ra	RD,WR	== Da	/= {Ba,Ba+1,Ba-1}	x..x	0	
RC4	ACT	Da	Ba	Ra	RD,WR	== Da	== {Ba+1,Ba-1}	x..x	Illegal	
RC5	ACT	Da	Ba	Ra	RD,WR	== Da	== Ba	x..x	t_{RCD}	Figure 15
RC6	PRER	Da	Ba	Ra	NOCOP,RD,WR	/= Da	xxxx	x..x	0	
RC7	PRER	Da	Ba	Ra	NOCOP	== Da	xxxx	x..x	0	
RC8	PRER	Da	Ba	Ra	RD,WR	== Da	/= {Ba,Ba+1,Ba-1}	x..x	0	
RC9	PRER	Da	Ba	Ra	RD,WR	== Da	== {Ba+1,Ba-1}	x..x	Illegal	

COL-to-COL Packet Interaction



Transaction a: COPa	a1 = {Da,Ba,Ca1}
Transaction b: COPb	b1 = {Db,Bb,Cb1}
Transaction c: COPc	c1 = {Dc,Bc,Cc1}

Figure 8: COL-to-COL Packet Interaction- Timing

Figure 8 shows three arbitrary packets on the COL pins. Packets "b" and "c" must be separated by an interval $t_{CCDELAY}$ which depends upon the command and address values in all three packets. Table 12 summarizes the $t_{CCDELAY}$ values for all possible cases.

Cases CC1 through CC5 summarize the rules for every situation other than the case when COPb is a WR command and COPc is a RD command. In CC3, when a RD command is followed by a WR command, a gap of t_{CAC} -t_{CWD} must be inserted between the two COL packets. See Figure 4 for more explanation of why this gap is needed. For cases CC1, CC2, CC4, and CC5, there is no restriction ($t_{CCDELAY}$ is t_{CC}).

In cases CC6 through CC10, COPb is a WR command and COPc is a RD command. The $t_{CCDELAY}$ value needed between these two packets depends upon the command and address in the packet with COPa. In particular, in case CC6 when there is WR-WR-RD command sequence directed to the same device, a gap will be needed between the packets with COPb and COPc. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place. Figure 18 (right) provides a more detailed explanation of this case.

In case CC10, there is a RD-WR-RD sequence directed to the same device. If a prior write to the same device is unretired when COPa is issued, then a gap will be needed between the packets with COPb and COPc as in case CC6. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place.

Cases CC7, CC8, and CC9 have no restriction ($t_{CCDELAY}$ is t_{CC}).

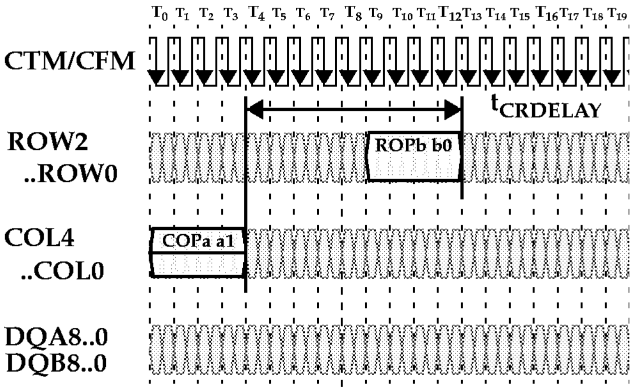
For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation PREC to take place. This precharge may be converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 14.

Table 12: COL-to-COL Packet Interaction - Rules

Case #	COPa	Da	Ba	Ca1	COPb	Db	Bb	Cb1	COPc	Dc	Bc	Cc1	$t_{CCDELAY}$	Example
CC1	xxxx	xxxxx	x..x	x..x	NOCOP	Db	Bb	Cb1	xxxx	xxxxx	x..x	x..x	t_{CC}	
CC2	xxxx	xxxxx	x..x	x..x	RD,WR	Db	Bb	Cb1	NOCOP	xxxxx	x..x	x..x	t_{CC}	
CC3	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	t_{CC}+t_{CAC} -t_{CWD}	Figure 4
CC4	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	RD	xxxxx	x..x	x..x	t_{CC}	Figure 15
CC5	xxxx	xxxxx	x..x	x..x	WR	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	t_{CC}	Figure 16
CC6	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{RTR}	Figure 17
CC7	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	/= Db	x..x	x..x	t_{CC}	
CC8	WR	/= Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	
CC9	NOCOP	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	
CC10	RD	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC} or t_{RTR}[a]	

[a] If the write buffer was full from an earlier WR command, and had not been retired when COPa=RD is executed, $t_{CCDELAY}$ will be constrained by the t_{RTR} parameter. Otherwise, the t_{CC} parameter will apply.

COL-to-ROW Packet Interaction



Transaction a: COPa	a1= {Da,Ba,Ca1}
Transaction b: ROPb	b0= {Db,Bb,Rb}

Figure 9: COL-to-ROW Packet Interaction- Timing

Figure 9 shows arbitrary packets on the COL and ROW pins. They must be separated by an interval $t_{CRDELAY}$ which depends upon the command and address values in the packets. Table 13 summarizes the $t_{CRDELAY}$ value for all possible cases.

Cases CR1, CR2, CR3, and CR9 show no interaction between the COL and ROW packets, either because one of the commands is a NOP or because the packets are directed to different devices or to non-adjacent banks.

Case CR4 is illegal because an already-activated bank is to be re-activated without being precharged Case CR5 is illegal because an adjacent bank can't be activated or precharged until bank Ba is precharged first.

In case CR6, the COLC packet contains a RD command, and the ROW packet contains a PRER command for the same bank. The t_{RDP} parameter specifies the required spacing.

Likewise, in case CR7, the COLC packet causes an automatic retire to take place, and the ROW packet contains a PRER command for the same bank. The t_{RTP} parameter specifies the required spacing.

Case CR8 is labeled "Hazardous" because a WR command should always be followed by an automatic retire before a precharge is scheduled. Figure 19 shows an example of what can happen when the retire is not able to happen before the precharge.

For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation to take place. This precharge may converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 14.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, PDNR, and RLXR commands are discussed in a later section.

Table 13: COL-to-ROW Packet Interaction - Rules

Case #	COPa	Da	Ba	Ca1	ROPb	Db	Bb	Rb	$t_{CRDELAY}$	Example
CR1	NOCOP	Da	Ba	Ca1	x..x	xxxxx	xxxx	x..x	0	
CR2	RD/WR	Da	Ba	Ca1	x..x	/= Da	xxxx	x..x	0	
CR3	RD/WR	Da	Ba	Ca1	x..x	== Da	/= {Ba,Ba+1,Ba-1}	x..x	0	
CR4	RD/WR	Da	Ba	Ca1	ACT	== Da	== {Ba}	x..x	Illegal	
CR5	RD/WR	Da	Ba	Ca1	x..x	== Da	== {Ba+1,Ba-1}	x..x	Illegal	
CR6	RD	Da	Ba	Ca1	PRER	== Da	== {Ba,Ba+1,Ba-1}	x..x	t_{RDP}	Figure 15
CR7	retire[a]	Da	Ba	Ca1	PRER	== Da	== {Ba,Ba+1,Ba-1}	x..x	t_{RTP}	Figure 16
CR8	WR[b]	Da	Ba	Ca1	PRER	== Da	== {Ba,Ba+1,Ba-1}	x..x	0	Figure 19
CR9	xxxx	Da	Ba	Ca1	NOROP	xxxxx	xxxx	x..x	0	

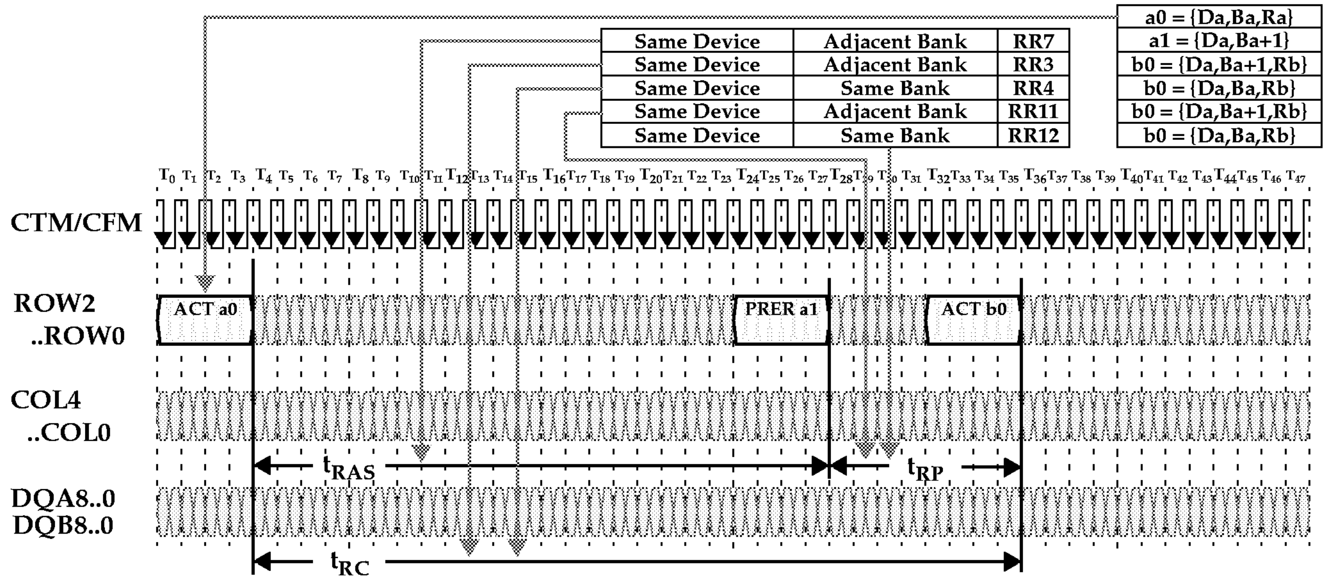
[a] This is any command which permits the write buffer of device Da to retire (see Table 8). "Ba" is the bank address in the write buffer.

[b] This situation is hazardous because the write buffer will be left unretired while the targeted bank is precharged. See Figure 19.

ROW-to-ROW Examples

Figure 10 shows examples of some of the the ROW-to-ROW packet spacings from Table 10. A complete sequence of activate and precharge commands is directed to a bank. The RR8 and RR12 rules apply to this sequence. In addition to satisfying the t_{RAS} and t_{RP} timing parameters, the separation between ACT commands to the same bank must also satisfy the t_{RC} timing parameter (RR4).

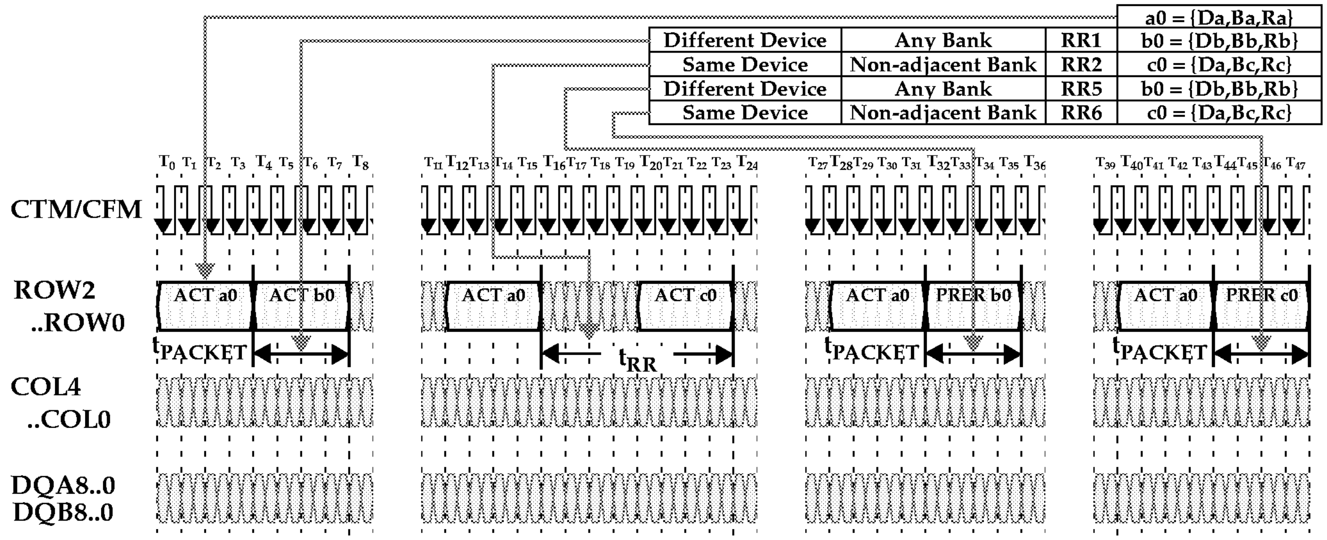
When a bank is activated, it is necessary for adjacent banks to remain precharged. As a result, the adjacent banks will also satisfy parallel timing constraints; in the example, the RR11 and RR3 rules are analogous to the RR12 and RR4 rules.



			a0 = {Da,Ba,Ra}
Same Device	Adjacent Bank	RR7	a1 = {Da,Ba+1}
Same Device	Adjacent Bank	RR3	b0 = {Da,Ba+1,Rb}
Same Device	Same Bank	RR4	b0 = {Da,Ba,Rb}
Same Device	Adjacent Bank	RR11	b0 = {Da,Ba+1,Rb}
Same Device	Same Bank	RR12	b0 = {Da,Ba,Rb}

Figure 10: Row Packet Example

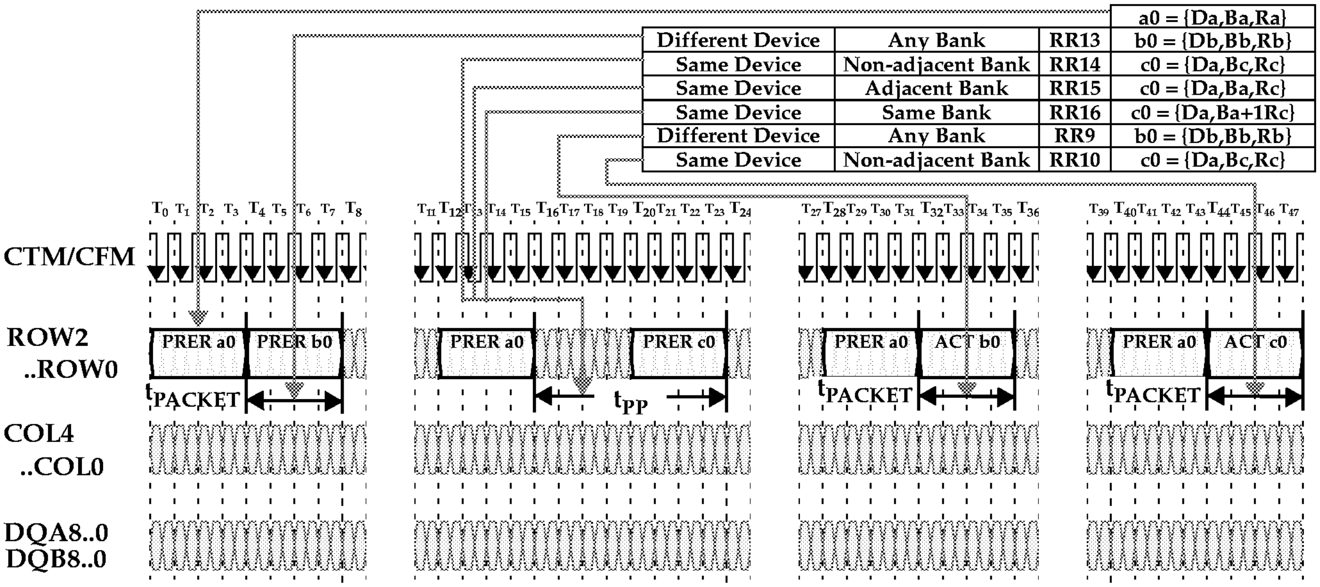
Figure 11 shows examples of the ACT-to-ACT (RR1, RR2) and ACT-to-PRER (RR5, RR6) command spacings from Table 10. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same or adjacent banks or unless they are a similar command type (both PRER or both ACT) directed to the same device.



			a0 = {Da,Ba,Ra}
Different Device	Any Bank	RR1	b0 = {Db,Bb,Rb}
Same Device	Non-adjacent Bank	RR2	c0 = {Da,Bc,Rc}
Different Device	Any Bank	RR5	b0 = {Db,Bb,Rb}
Same Device	Non-adjacent Bank	RR6	c0 = {Da,Bc,Rc}

Figure 11: Row Packet Example

Figure 12 shows examples of the PRER-to-PRER (RR13, RR14) and PRER-to-ACT (RR9, RR10) command spacings from Table 10. The RR15 and RR16 cases (PRER-to-PRER to same or adjacent banks) are not shown, but are similar to RR14. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same or adjacent banks or unless they are a similar command type (both PRER or both ACT) directed to the same device.



			a0 = {Da,Ba,Ra}
Different Device	Any Bank	RR13	b0 = {Db,Bb,Rb}
Same Device	Non-adjacent Bank	RR14	c0 = {Da,Bc,Rc}
Same Device	Adjacent Bank	RR15	c0 = {Da,Ba,Rc}
Same Device	Same Bank	RR16	c0 = {Da,Ba+1Rc}
Different Device	Any Bank	RR9	b0 = {Db,Bb,Rb}
Same Device	Non-adjacent Bank	RR10	c0 = {Da,Bc,Rc}

Figure 12: Row Packet Examples

Row and Column Cycle Description

Activate: A row cycle begins with the activate (ACT) operation. The activation process is destructive; the act of sensing the value of a bit in a bank's storage cell transfers the bit to the sense amp, but leaves the original bit in the storage cell with an incorrect value.

Restore: Because the activation process is destructive, a hidden operation called restore is automatically performed. The restore operation rewrites the bits in the sense amp back into the storage cells of the activated row of the bank.

Read/Write: While the restore operation takes place, the sense amp may be read (RD) and written (WR) using column operations. If new data is written into the sense amp, it is automatically forwarded to the storage cells of the bank so the data in the activated row and the data in the sense amp remain identical.

Precharge: When both the restore operation and the column operations are completed, the sense amp and bank are precharged (PRE). This leaves them in the proper state to begin another activate operation.

Intervals: The activate operation requires the interval $t_{RCD,MIN}$ to complete. The hidden restore operation requires the interval $t_{RAS,MIN}$ - $t_{RCD,MIN}$ to complete. Column read and write operations are also performed during the $t_{RAS,MIN}$ - $t_{RCD,MIN}$ interval (if more than about four column operations are performed, this interval must be increased). The precharge operation requires the interval $t_{RP,MIN}$ to complete.

Adjacent Banks: An RDRAM with a "d" designation (256Kx16dx16/18) indicates it contains "doubled banks". This means the sense amps are shared between two adjacent banks. The only exception is that sense amp 0 and sense amp 15 are not shared. When a row in a bank is activated, the two adjacent sense amps are connected to (associated with) that bank and are not available for use by the two adjacent banks. These two adjacent banks must remain precharged while the selected bank goes through its activate, restore, read/write, and precharge operations.

For example (referring to the block diagram of Figure 2), if bank 5 is accessed, sense amp 4/5 and sense amp 5/6 will both be loaded with one of the 512 rows (with 512 bytes loaded into each sense amp from the 1Kbyte row - 256 bytes to the DQA side and 256 bytes to the DQB side). While this row from bank 5 is being accessed, no rows may be accessed in banks 4 or 6 because of the sense amp sharing.

Precharge Mechanisms

Figure 13 shows an example of precharge with the ROWR packet mechanism. The PRER command must occur a time t_{RAS} after the ACT command, and a time t_{RP} before the next ACT command. This timing will serve as a baseline aginst which the other precharge mechanisms can be compared.

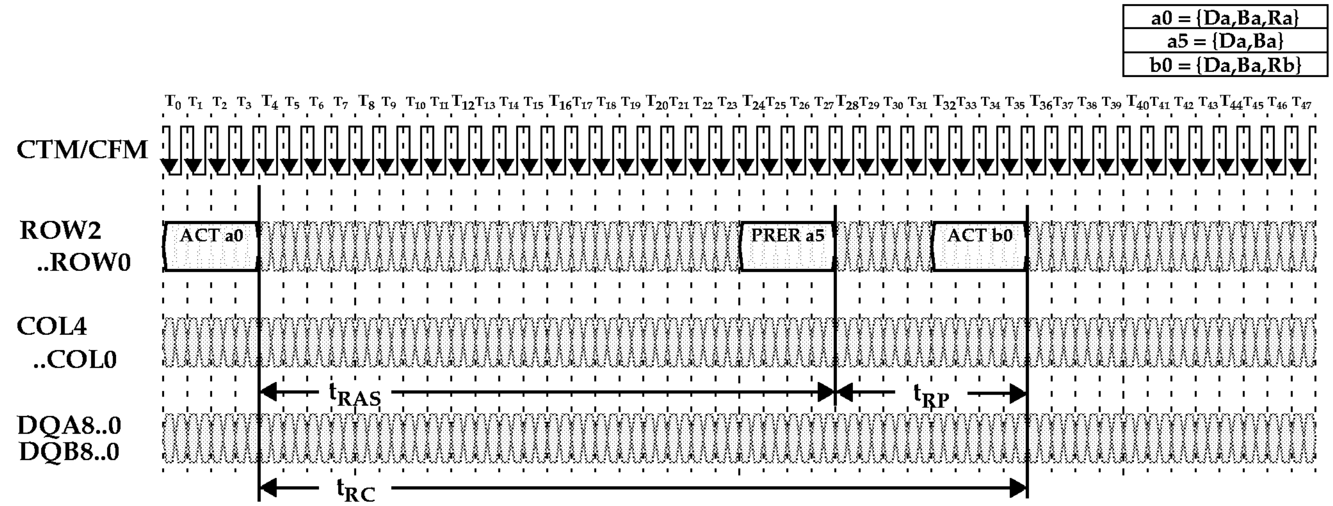


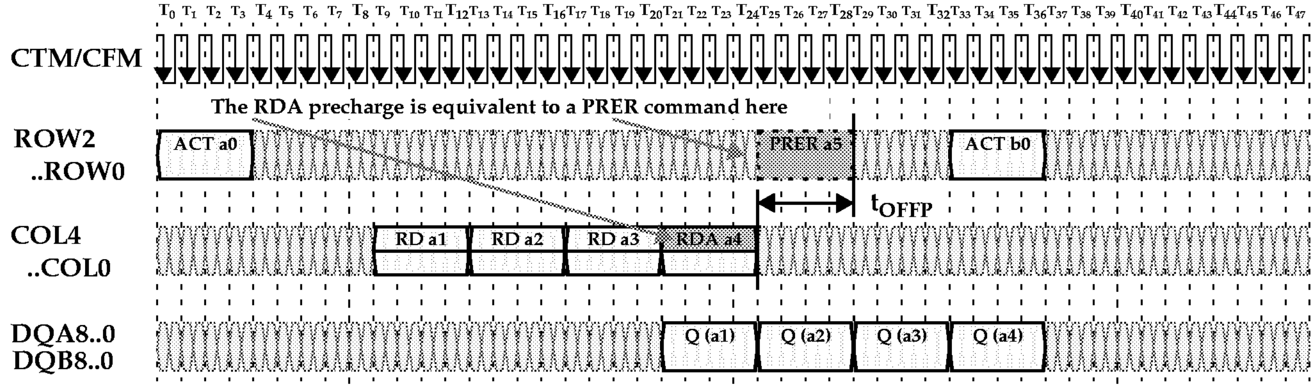
Figure 13: Precharge via PRER Command in ROWR Packet

Figure 14 (top) shows an example of precharge with a RDA command. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these commands is a RDA, which causes the bank to automatically precharge when the final read has finished. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLC packet with the RDA command. The RDA command should be treated as a RD command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets.

Figure 14 (middle) shows an example of precharge with a WRA command. As in the RDA example, a bank is activated with an ROWA packet on the ROW pins. Then, two dualocts are written with WR commands in COLC packets on the COL pins. The second of these commands is a WRA, which causes the bank to automatically precharge when the final write has been retired. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLC packet that causes the automatic retire. The WRA command should be treated as a WR command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets. Note that the automatic retire is triggered by a COLC packet a time t_{RTR} after the COLC packet with the WR command unless the second COLC contains a RD command to the same device. This is described in more detail in Figure 17.

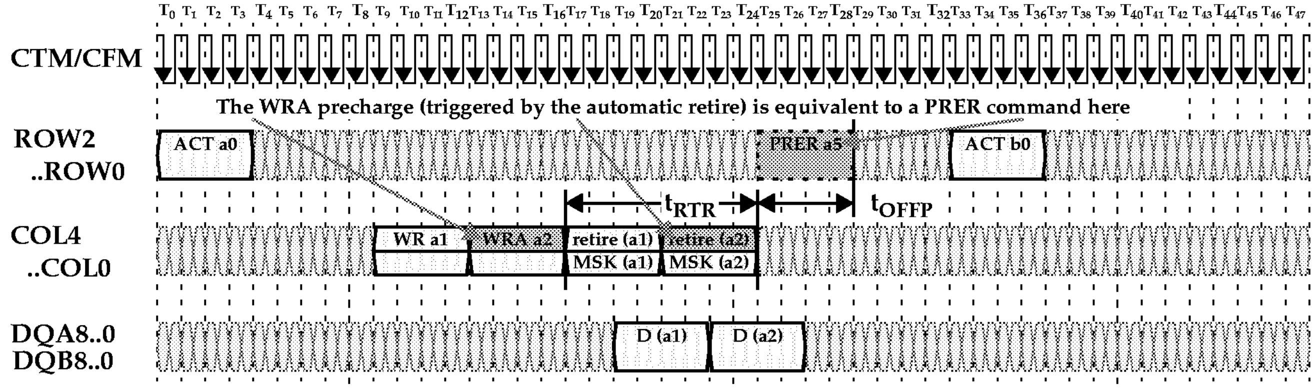
Figure 14 (bottom) shows an example of precharge with a PREX command in an COLX packet. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these COLC packets includes an COLX packet with a PREC command. This causes the bank to precharge with timing equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLX packet with the PREX command.

COLC Packet: RDA Precharge Offset



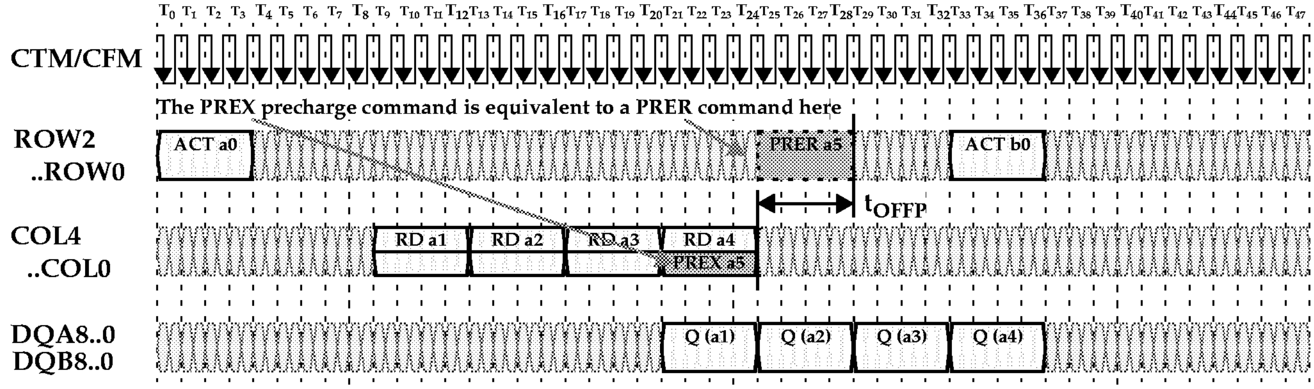
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	
		a3 = {Da,Ba,Ca3}	a4 = {Da,Ba,Ca4}	a5 = {Da,Ba}

COLC Packet: WDA Precharge Offset



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a5 = {Da,Ba}

COLX Packet: PREX Precharge Offset



Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	
		a3 = {Da,Ba,Ca3}	a4 = {Da,Ba,Ca4}	a5 = {Da,Ba}

Figure 14: Offsets for Alternate Precharge Mechanisms

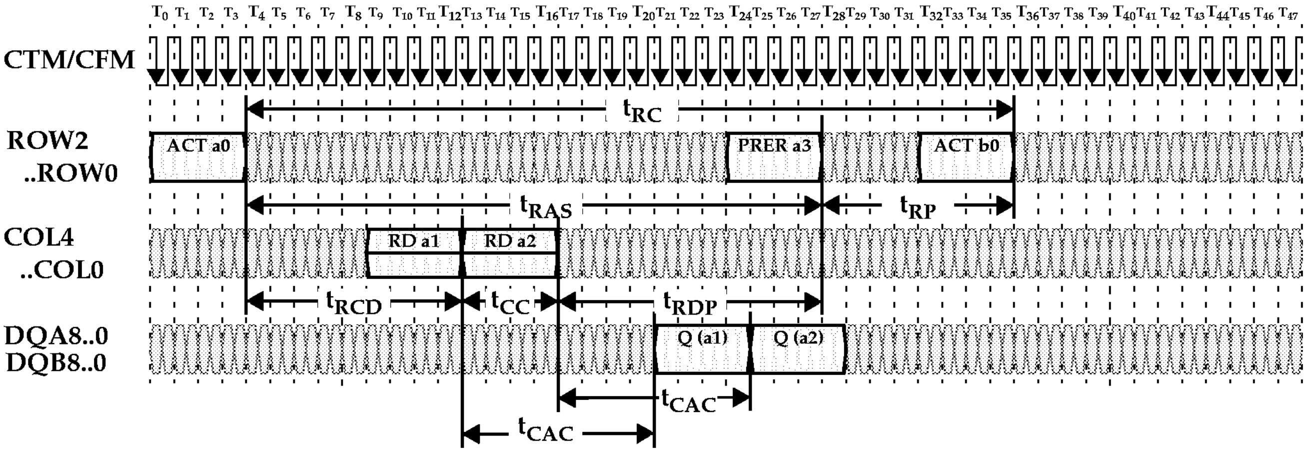
Read Transaction - Example

Figure 15 shows an example of a read transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time t_{RCD} later a RD a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the RD command includes device, bank, and column address (abbreviated as a1). A time t_{CAC} after the RD command the read data dualoct Q(a1) is returned by the device. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

A time t_{CC} after the first COLC packet on the COL pins a second is issued. It contains a RD a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CAC} after the second RD command a second read data dualoct Q(a2) is returned by the device.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval). The PRER command must also occur a time t_{RDP} or more after the last RD command. Note that the t_{RDP} value shown is greater than the $t_{RDP,MIN}$ specification in Table 22. This transaction example reads two dualocts, but there is actually enough time to read three dualocts before t_{RDP} becomes the limiting parameter rather than t_{RAS}. If four dualocts were read, the packet with PRER would need to shift right (be delayed) by one t_{CYCLE} (note - this case is not shown).

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.



Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: xx	b0 = {Da,Ba,Rb}			

Figure 15: Read Transaction Example

Write Transaction - Example

Figure 16 shows an example of a write transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time t_{RCD} later a WR a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the WR command includes device, bank, and column address (abbreviated as a1). A time t_{CWD} after the WR command the write data dualoct D(a1) is issued. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

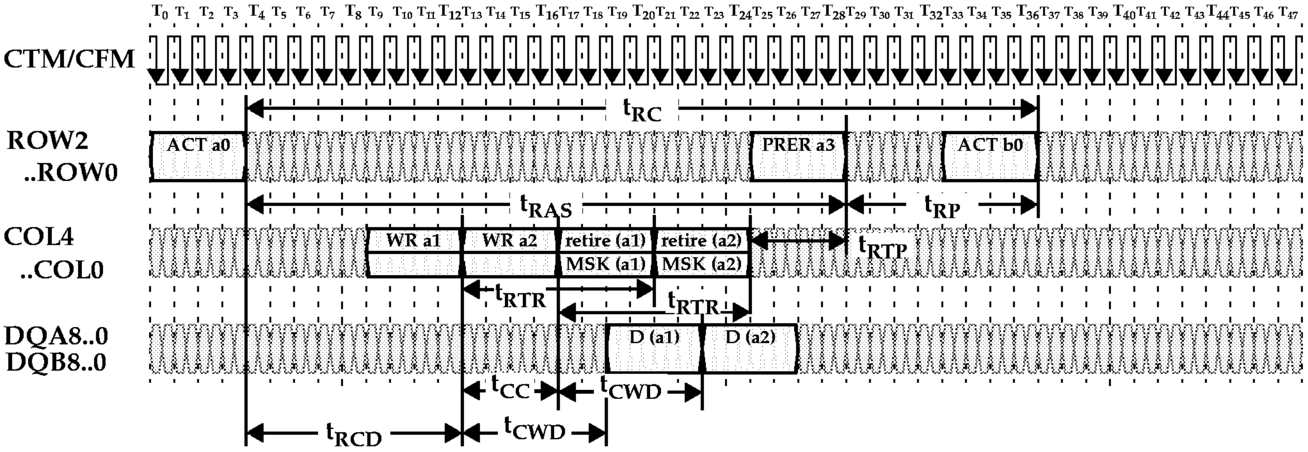
A time t_{CC} after the first COLC packet on the COL pins a second COLC packet is issued. It contains a WR a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CWD} after the second WR command a second write data dualoct D(a2) is issued.

A time t_{RTR} after each WR command an optional COLM packet MSK (a1) is issued, and at the same time a COLC packet is issued causing the write buffer to automatically retire. See Figure 17 for more detail on the write/retire mechanism. If a COLM packet is not used, all data bytes are unconditionally written. If the COLC packet which causes the write buffer to retire is delayed, then the COLM packet (if used) must also be delayed.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval).

A PRER a3 command is issued in an ROWR packet on the ROW pins. The PRER command must occur a time t_{RTP} or more after the last COLC which causes an automatic retire.

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: xx	b0 = {Da,Ba,Rb}			

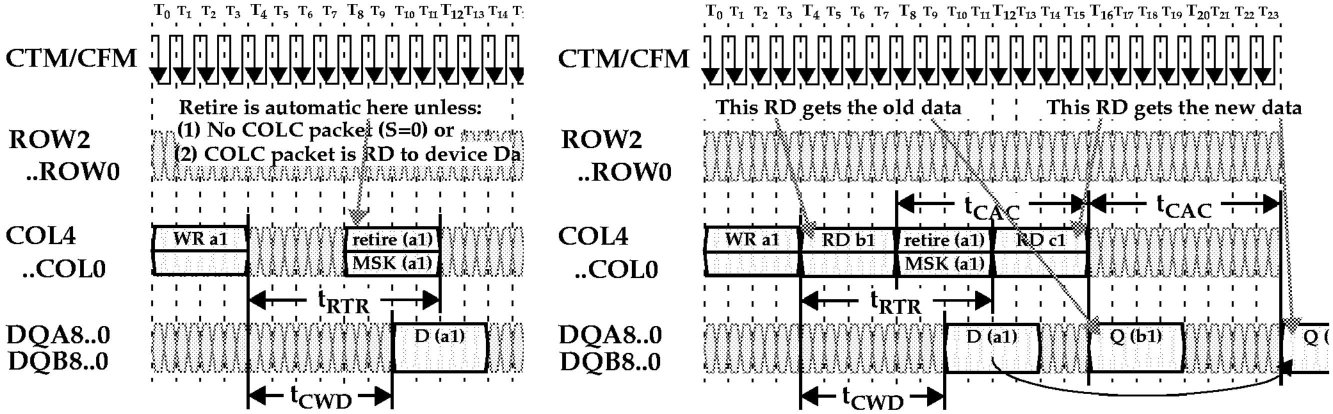
Figure 16: Write Transaction Example

Write/Retire - Examples

The process of writing a dualoct into a sense amp of an RDRAM bank occurs in two steps. The first step consists of transporting the write command, write address, and write data into the write buffer. The second step happens when the RDRAM automatically retires the write buffer (with an optional bytemask) into the sense amp. This two-step write process reduces the natural turn-around delay due to the internal bidirectional data pins.

Figure 17 (left) shows an example of this two step process. The first COLC packet contains the WR command and an address specifying device, bank and column. The write data dualoct follows a time t_{CWD} later. This information is loaded into the write buffer of the specified device. The COLC packet which follows a time t_{RTR} later will retire the write buffer. The retire will happen automatically unless (1) a COLC packet is not framed (no COLC packet is present and the S bit is zero), or (2) the COLC packet contains a RD command to the same device. If the retire does not take place at time t_{RTR} after the original WR command, then the device continues to frame COLC packets, looking for the first that is not a RD directed to itself. A bytemask MSK(a1) may be supplied in a COLM packet aligned with the COLC that retires the write buffer at time t_{RTR} after the WR command.

The memory controller must be aware of this two-step write/retire process. Controller performance can be improved, but only if the controller design accounts for several side effects.



Transaction a: WR	a1= {Da,Ba,Ca1}

Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: RD	b1= {Da,Ba,Ca1}
Transaction c: RD	c1= {Da,Ba,Ca1}

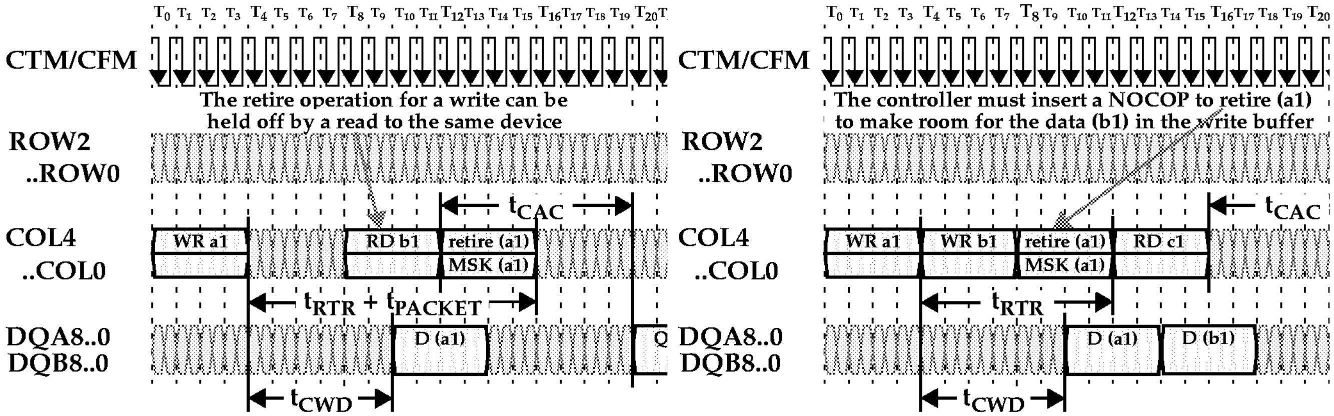
Figure 17: Normal Retire (left) and Retire/Read Ordering (right)

Figure 17 (right) shows the first of these side effects. The first COLC packet has a WR command which loads the address and data into the write buffer. The third COLC causes an automatic retire of the write buffer to the sense amp. The second and fourth COLC packets (which bracket the retire packet) contain RD commands with the same device, bank and column address as the original WR command. In other words, the same dualoct address that is written is read both before and after it is actually retired. The first RD returns the old dualoct value from the sense amp before it is overwritten. The second RD returns the new dualoct value that was just written.

Figure 18 (left) shows the result of performing a RD command to the same device in the same COLC packet slot that would normally be used for the retire operation. The read may be to any bank and column address; all that matters is that it is to the same device as the WR command. The retire operation and MSK(a1) will be delayed by a time t_{PACKET} as a result. If the RD command used the same bank and column address as the WR command, the old data from the sense amp would be returned. If many RD commands to the same device were issued instead of the single one that is shown, then the retire operation would be held off an arbitrarily long time. However, once a RD to another device or a WR or NOCOP to any device is issued, the retire will take place. Figure 18 (right) illustrates a situation in which the controller wants to issue a WR-WR-RD COLC packet sequence, with all commands addressed to the same device, but addressed to any combination of banks and columns.

Write/Retire Examples - continued

The RD will prevent a retire of the first WR from automatically happening. But the first dualoct D(a1) in the write buffer will be overwritten by the second WR dualoct D(b1) if the RD command is issued in the third COLC packet. Therefore, it is required in this situation that the controller issue a NOCOP command in the third COLC packet, delaying the RD command by a time of t_{PACKET}. This situation is explicitly shown in Table 12 for the cases in which $t_{CCDELAY}$ is equal to t_{RTR}.

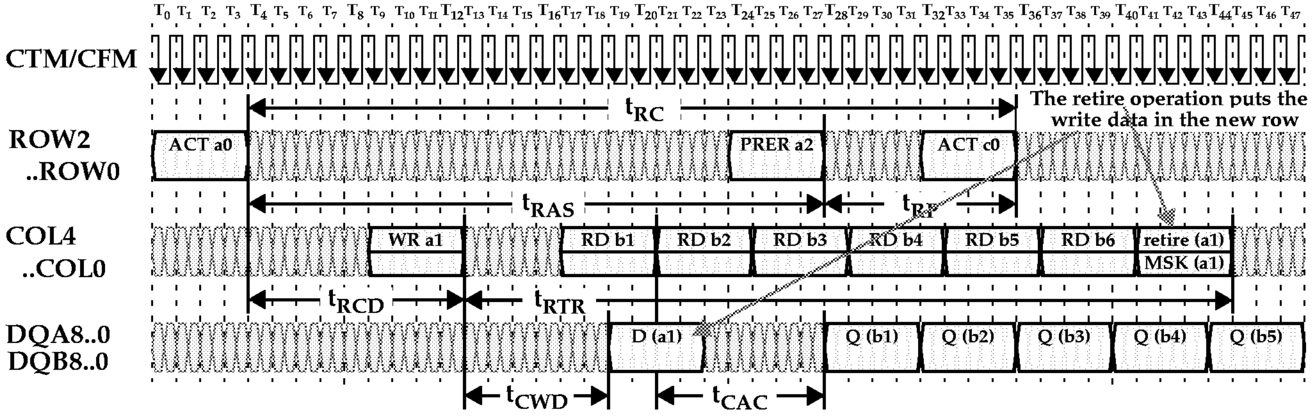


Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: RD	b1= {Da,Bb,Cb1}

Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: WR	b1= {Da,Bb,Cb1}
Transaction c: RD	c1= {Da,Bc,Cc1}

Figure 18: Retire Held Off by Read (left) and Controller Forces WWR Gap (right)

Figure 19 shows a possible result when a retire is held off for a long time (an extended version of Figure 18-left). After a WR command, a series of six RD commands are issued to the same device (but to any combination of bank and column addresses). In the meantime, the bank Ba to which the WR command was originally directed is precharged, and a different row Rc is activated. When the retire is automatically performed, it is made to this new row, since the write buffer only contains the bank and column address, not the row address. The controller can insure that this doesn't happen by never precharging a bank with an unretired write buffer. Note that in a system with more than one RDRAM, there will never be more than two RDRAMs with unretired write buffers. This is because a WR command issued to one device automatically retires the write buffers of all other devices written a time t_{RTR} before or earlier.



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba}
Transaction b: RD	b1 = {Da,Bb,Cb1}	b2 = {Da,Bb,Cb2}	b3= {Da,Bb,Cb3}
	b4 = {Da,Bb,Cb4}	b5 = {Da,Bb,Cb5}	b6 = {Da,Bb,Cb6}
Transaction c: WR	c0 = {Da,Ba,Rc}		

WARNING
This sequence is hazardous and must be used with caution

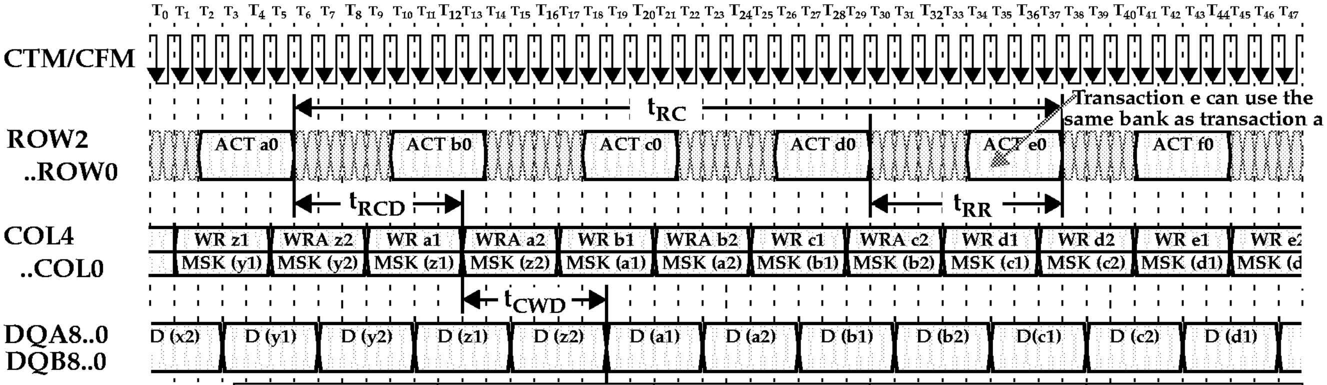
Figure 19: Retire Held Off by Reads to Same Device, Write Buffer Retired to New Row

Interleaved Write - Example

Figure 20 shows an example of an interleaved write transaction. Transactions similar to the one presented in Figure 16 are directed to non-adjacent banks of a single RDRAM. This allows a new transaction to be issued once every t_{RR} interval rather than once every t_{RC} interval (four times more often). The DQ data pin efficiency is 100% with this sequence.

With two dualocts of data written per transaction, the COL, DQA, and DQB pins are fully utilized. Banks are precharged using the WRA autoprecharge option rather than the PRER command in an ROWR packet on the ROW pins.

In this example, the first transaction is directed to device Da and bank Ba. The next three transactions are directed to the same device Da, but need to use different, non-adjacent banks Bb, Bc, Bd so there is no bank conflict. The fifth transaction could be redirected back to bank Ba without interference, since the first transaction would have completed by then (t_{RC} has elapsed). Each transaction may use any value of row address (Ra, Rb, ..) and column address (Ca1, Ca2, Cb1, Cb2, ...).



Transaction y: WR	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2= {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: WR	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2= {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2= {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: WR	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2= {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: WR	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: WR	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 20: Interleaved Write Transaction with Two Dualoct Data Length

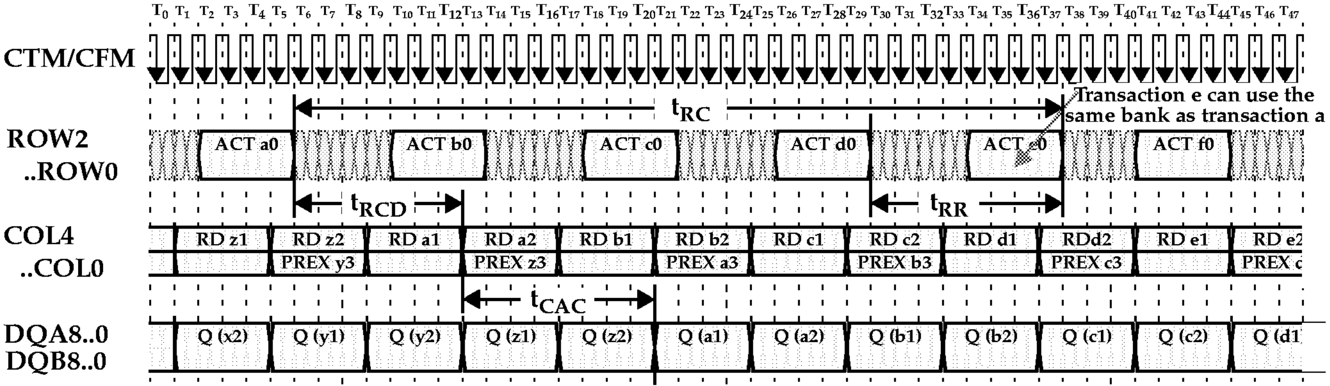
Interleaved Read - Example

Figure 21 shows an example of interleaved read transactions. Transactions similar to the one presented in Figure 15 are directed to non-adjacent banks of a single RDRAM. The address sequence is identical to the one used in the previous write example. The DQ data pins efficiency is also 100%. The only difference with the write example (aside from the use of the RD command rather than the WR command) is the use of the PREX command in a COLX packet to precharge the banks rather than the RDA command. This is done because the PREX is available for a readtransaction but is not available for a masked write transaction.

Interleaved RRWW - Example

Figure 22 shows a steady-state sequence of 2-dualoct RD/RD/WR/WR.. transactions directed to non-adjacent banks of a single RDRAM. This is similar to the interleaved write and read examples in Figure 20 and Figure 21 except that bubble cycles need to be inserted by the controller at read/write boundaries. The DQ data pin efficiency for the example in Figure 22 is 32/38 or 84%. If there were more RDRAMs on the Channel, the DQ pin efficiency would approach 32/34 or 94% for the two-dualoct RRWW sequence (this case is not shown).

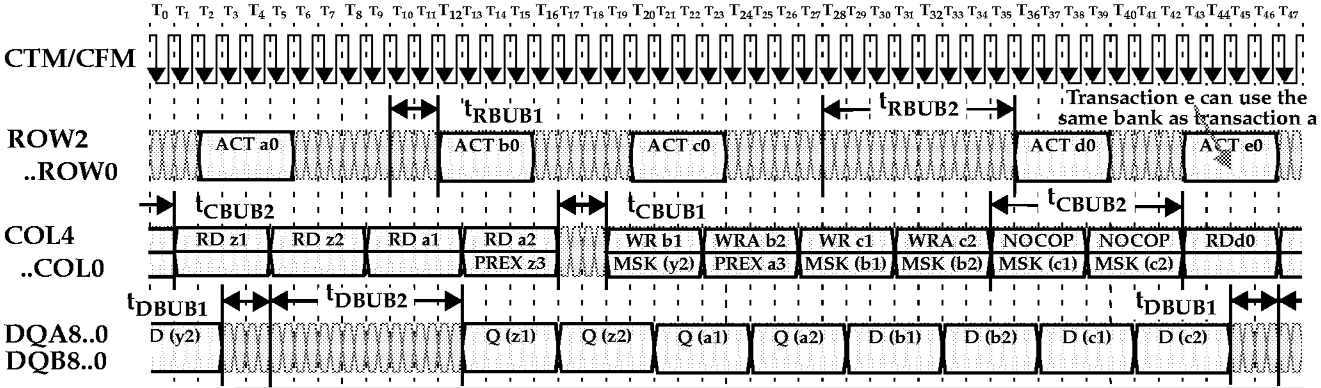
In Figure 22, the first bubble type t_{CBUB1} is inserted by the controller between a RD and WR command on the COL pins. This bubble accounts for the round-trip propagation delay that is seen by read data, and is explained in detail in Figure 4. This bubble appears on the DQA and DQB pins as t_{DBUB1} between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB1}.



Transaction y: RD	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2= {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: RD	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2= {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: RD	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: RD	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2= {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: RD	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2= {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: RD	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 21: Interleaved Read Transaction with Two Dualoct Data Length

The second bubble type t_{CBUB2} is inserted (as a NOCOP command) by the controller between a WR and RD command on the COL pins when there is a WR-WR-RD sequence to the same device. This bubble enables write data to be retired from the write buffer without being lost, and is explained in detail in Figure 18. There would be no bubble if address c0 and address d0 were directed to different devices. This bubble appears on the DQA and DQB pins as t_{DBUB2} between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB2}.



Transaction y: WR	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2= {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: RD	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2= {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2= {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: RD	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2= {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: WR	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 22: Interleaved RRWW Sequence with Two Dualoct Data Length

Control Register Transactions

The RDRAM has two CMOS input pins SCK and CMD and two CMOS input/output pins SIO0 and SIO1. These provide serial access to a set of control registers in the RDRAM. These control registers provide configuration information to the controller during the initialization process. They also allow an application to select the appropriate operating mode of the RDRAM.

SCK (serial clock) and CMD (command) are driven by the controller to all RDRAMs in parallel. SIO0 and SIO1 are connected (in a daisy chain fashion) from one RDRAM to the next. In normal operation, the data on SIO0 is repeated on SIO1, which connects to SIO0 of the next RDRAM (the data is repeated from SIO1 to SIO0 for a read data packet). The controller connects to SIO0 of the first RDRAM.

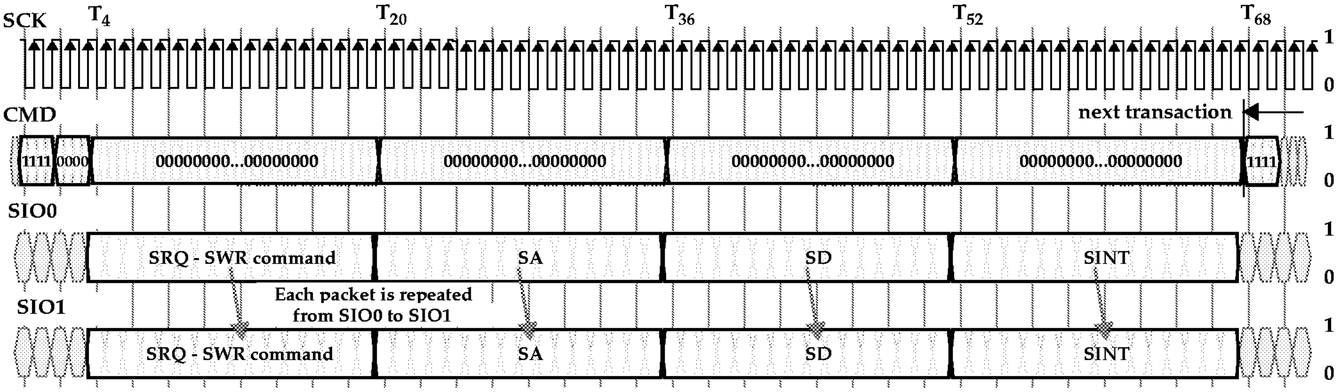


Figure 23: Serial Write (SWR) Transaction to Control Register

Write and read transactions are each composed of four packets, as shown in Figure 23 and Figure 24. Each packet consists of 16 bits, as summarized in Table 14 and Table 15. The packet bits are sampled on the falling edge of SCK. A transaction begins with a SRQ (Serial Request) packet. This packet is framed with a 11110000 pattern on the CMD input (note that the CMD bits are sampled on both the falling edge and the rising edge of SCK). The SRQ packet contains the SOP3..SOP0 (Serial Opcode) field, which selects the transaction type. The SDEV4..SDEV0 (Serial Device address) selects one of the 32 RDRAMs. If SBC (Serial Broadcast) is set, then all RDRAMs are selected. The SA (Serial Address) packet contains a 12 bit address for selecting a control register.

A write transaction has a SD (Serial Data) packet next. This contains 16 bits of data that is written into the selected control register. A SINT (Serial Interval) packet is last, providing some delay for any side-effects to take place. A read transaction has a SINT packet, then a SD packet. This provides delay for the selected RDRAM to access the control register. The SD read data packet travels in the opposite direction (towards the controller) from the other packet types. The SCK cycle time will accomodate the total delay.

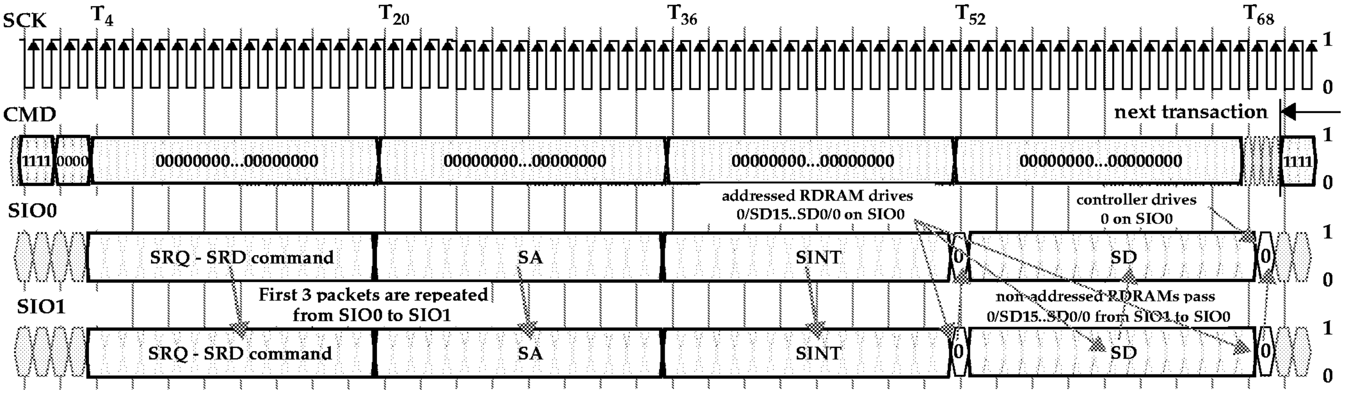


Figure 24: Serial Read (SRD) Transaction Control Register

Control Register Packets

Table 14 summarizes the formats of the four packet types for control register transactions. Table 15 summarizes the fields that are used within the packets.

Figure 25 shows the transaction format for the SETR, CLRR, and SETF commands. These transactions consist of a single SRQ packet, rather than four packets like the SWR and SRD commands. The same framing sequence on the CMD input is used, however. These commands are used during initialization prior to any control register read or write transactions.

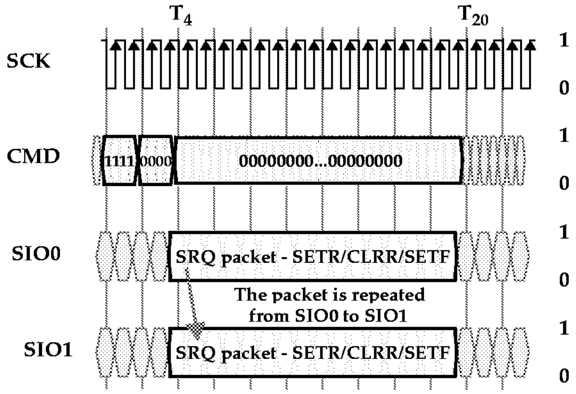


Figure 25: SETR, CLRR,SETF Transaction

Table 14: Control Register Packet Formats

SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD	SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD
0	rsrv	rsrv	0	SD15	8	SOP1	SA7	0	SD7
1	rsrv	rsrv	0	SD14	9	SOP0	SA6	0	SD6
2	rsrv	rsrv	0	SD13	10	SBC	SA5	0	SD5
3	rsrv	rsrv	0	SD12	11	SDEV4	SA4	0	SD4
4	rsrv	SA11	0	SD11	12	SDEV3	SA3	0	SD3
5	SDEV5	SA10	0	SD10	13	SDEV2	SA2	0	SD2
6	SOP3	SA9	0	SD9	14	SDEV1	SA1	0	SD1
7	SOP2	SA8	0	SD8	15	SDEV0	SA0	0	SD0

Table 15: Field Description for Control Register Packets

Field	Description
rsrv	Reserved. Should be driven as "0" by controller.
SOP3..SOP0	0000 - SRD. Serial read of control register {SA11..SA0} of RDRAM {SDEV5..SDEV0}.
	0001 - SWR. Serial write of control register {SA11..SA0} of RDRAM {SDEV5..SDEV0}.
	0010 - SETR. Set Reset bit, all control registers assume their reset values.[a] 16 t_{SCYCLE} delay until CLRR command.
	0100 - SETF. Set fast (normal) clock mode.
	1011 - CLRR. Clear Reset bit, all control registers retain their reset values.[a] 4 t_{SCYCLE} delay until next command.
	1111 - NOP. No serial operation.
	0011, 0101-1010, 1100-1110 - RSRV. Reserved encodings.
SDEV5..SDEV0	Serial device. Compared to SDEVID5..SDEVID0 field of INIT control register field to select the RDRAM to which the transaction is directed.
SBC	Serial broadcast. When set, RDRAMs ignore {SDEV5..SDEV0} for RDRAM selection.
SA11..SA0	Serial address. Selects which control register of the selected RDRAM is read or written.
SD15..SD0	Serial data. The 16 bits of data written to or read from the selected control register of the selected RDRAM.

[a] The SETR and CLRR commands must always be applied in two successive transactions to RDRAMs; i.e. they may not be used in isolation. This is called "SETR/CLRR Reset".

Initialization

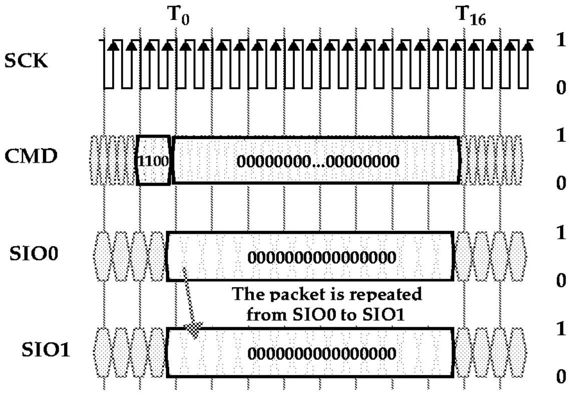


Figure 26: SIO Reset Sequence

Initialization refers to the process that a controller must go through after power is applied to the system or the system is reset. The controller prepares the RDRAM sub-system for normal Channel operation by using a sequence of control register transactions on the serial CMOS pins.

The first step in this sequence is to assign unique serial device addresses to all the RDRAMs. This is done with Algorithm InitDev, shown in the opposite column. The controller assumes that there are no more that "N" RDRAMs on the Channel (the Channel maximum is 32, but some applications may have a lower limit).

First, the SIO0 and SIO1 pin directionality is established with the sequence in step 1. The controller then resets all RDRAMs, using broadcast SETR and CLRR commands (steps 2,3,4) with a delay in between (this is also called SIO Reset). In step 5, a SETF command establishs the normal clock frequency. See Figure 25 for the format of SETR, CLRR, and SETF transactions. In step 6 the SIO0-to-SIO1 link is broken in all RDRAMs, so the controller is only talking to the first RDRAM. Also, the SDEVID field is set to its maximum value. Next, the loop index INDX is initialized (step 7). In step 8, the SDEVID field is loaded with the INDX value, and the SRP bit is set so the next RDRAM becomes accessible. In step 9, the INDX value is incremented, and in step 10, steps 8 and 9 are repeated for the remaining RDRAMs.

Finally, it will be necessary for the controller to force a 200µs pause interval to allow the RDRAM core timing circuits to stabilize. All banks of all RDRAMs must also be accessed twice. An access is an activate (ACT) and a precharge (PRE) command. This may be accomplished with the refresh commands.

At this point, Algorithm InitDev is complete and all RDRAMs have a unique device address SDEVID5..0 for control register transactions. Note that the SDEVID address value of an RDRAM indicates its position in the daisy-chained CMOS serial pins. This will not necessarily be the same value as the DEVID register which is used for memory transactions. The next steps taken by the controller will vary depending upon the application, so only a rough outline can be given here.

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Algorithm InitDev: Assign SDEVID Device Addresses

1. Issue SIO Pin Initialization sequence (see Figure 26).
2. Issue one SETR transaction:
   - SOP3..SOP0 = 0010 (SETR command)
   - SBC = 1 (Broadcast)
   - SDEV5..SDEV0 = 000000 (don't care).
3. Wait 16 SCK cycles.
4. Issue one CLRR transaction:
   - SOP3..SOP0 = 0011 (CLRR command)
   - SBC = 1 (Broadcast)
   - SDEV5..SDEV0 = 000000 (don't care).
5. Wait 4 SCK cycles.
6. Issue one SETF transaction:
   - SOP3..SOP0 = 0100 (SETF command)
   - SBC = 1 (Broadcast)
   - SDEV5..SDEV0 = 000000 (don't care).
7. Issue one register write transaction:
   - SOP3..SOP0 = 0001 (SWR command)
   - SBC = 1 (broadcast)
   - SDEV5..SDEV0 = 000000 (don't care).
   - SA11..SA0 = 021$_{16}$ (INIT control register).
   - SD15..SD0 = 401f$_{16}$ (SRP<=0, SDEVID<=3f).
8. Set INDX5..INDX0 to 000000$_2$. INDX is a counter in the Controller which acts as a loop index.
9. Issue one register write transaction (SRP<=1, SDEVID<=INDX):
   - SOP3..SOP0 = 0001 (SWR command)
   - SBC = 0 (non-broadcast)
   - SDEV5..SDEV0 = 111111.
   - SA11..SA0 = 021$_{16}$ (INIT control register).
   - SD15..SD0 = {0$_2$, INDX5, 0000100$_2$, INDX4..INDX0}.
10. Increment INDX5..INDX0.
11. Repeat Steps (8) and (9) an additional (N-1) times.
12. t_{PAUSE} delay, then t_{PDNXA}+ t_{PDNXB} delay (to allow DLLs to lock), then access all banks twice (i.e. 32xREFA/REFP).

Initialization (continued)

In essence, the controller must read all the read-only configuration registers of all RDRAMs, it must process this information, and then it must write all the read-write registers to place the RDRAMs into the proper operating mode. The most important of these read-write registers are DEVID (the device address for memory transactions) and TRDLY (which sets the delay value for memory read data).

This page is reserved for further initialization detail when that information becomes available.

Control Register Summary

Table 16 summarizes the RDRAM control registers. Detail is provided for each control register in Figure 27 through Figure 43. Read-only bits which are shaded gray are unused and return zero. Read-write bits which are shaded gray are reserved and should always be written with zero. The RIMM SPD Application Note (DL-0054) describes additional read-only configuration registers which are present on Direct RIMMs.

The state of the register fields are potentially affected by the IO Reset operation or the SETR/CLRR operation. This is indicated in the text accompanying each register diagram.

Table 16: Control Register Summary

SA11..SA0	Register	Field	read-write/ read-only	Description
021_{16}	INIT	SDEVID	read-write, 6 bits	Serial device ID. Device address for control register read/write.
		PSX	read-write, 1 bit	Power select exit. PDN/NAP exit with device addr on DQA5..0.
		SRP	read-write, 1 bit	SIO repeater. Used to initialize RDRAM.
		NSR	read-write, 1 bit	NAP self-refresh. Enables self-refresh in NAP mode.
		PSR	read-write, 1 bit	PDN self-refresh. Enables self-refresh in PDN mode.
		LSR	read-write, 1 bit	Low power self-refresh. Enables low power self-refresh.
		TEN	read-write, 1 bit	Temperature sensing enable. Enables low power self-refresh.
		TSQ	read-write, 1 bit	Temperature sensing output. Enables low power self-refresh.
		DIS	read-write, 1 bit	RDRAM disable.
022_{16}	TEST34	TEST34	read-write, 16 bits	Test register. Do not read or write after SIO reset.
023_{16}	CNFGA	REFBIT	read-only, 3 bit	Refresh bank bits. Used for multi-bank refresh.
		DBL	read-only, 1 bit	Double. Specifies doubled-bank architecture
		MVER	read-only, 6 bit	Manufacturer version. Manufacturer identification number.
		PVER	read-only, 6 bit	Protocol version. Specifies version of Direct protocol supported.
024_{16}	CNFGB	BYT	read-only, 1 bit	Byte. Specifies an 8-bit or 9-bit byte size.
		DEVTYP	read-only, 3 bit	Device type. Device can be RDRAM or some other device category.
		CORG	read-only, 6 bit	Core organization. Bank, row, column address field sizes.
		SVER	read-only, 6 bit	Stepping version. Mask version number.
040_{16}	DEVID	DEVID	read-write, 5 bits	Device ID. Device address for memory read/write.
041_{16}	REFB	REFB	read-write, 4 bits	Refresh bank. Next bank to be refreshed by self-refresh.
042_{16}	REFR	REFR	read-write, 9 bits	Refresh row. Next row to be refreshed by REFA, self-refresh.
043_{16}	CCA	CCA	read-write, 7 bits	Current control A. Controls I_{OL} output current for DQA.
		ASYMA	read-write, 2 bits	Asymmetry control. Controls asymmetry of V_{OL}/V_{OH} swing for DQA.
044_{16}	CCB	CCB	read-write, 7 bits	Current control B. Controls I_{OL} output current for DQB.
		ASYMB	read-write, 2 bits	Asymmetry control. Controls asymmetry of V_{OL}/V_{OH} swing for DQB.
045_{16}	NAPX	NAPXA	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A.
		NAPX	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A + phase B.
		DQS	read-write, 1 bits	DQ select. Selects CMD framing for NAP/PDN exit.
046_{16}	PDNXA	PDNXA	read-write, 13 bits	PDN exit. Specifies length of PDN exit phase A.
047_{16}	PDNX	PDNX	read-write, 13 bits	PDN exit. Specifies length of PDN exit phase A + phase B.
048_{16}	TPARM	TCAS	read-write, 2 bits	t_{CAS-C} core parameter. Determines t_{OFFP} datasheet parameter.
		TCLS	read-write, 2 bits	t_{CLS-C} core parameter. Determines t_{CAC} and t_{OFFP} parameters.
		TCDLY0	read-write, 3 bits	$t_{CDLY0-C}$ core parameter. Programmable delay for read data.

Table 16: Control Register Summary

SA11..SA0	Register	Field	read-write/ read-only	Description
049_{16}	TFRM	TFRM	read-write, 4 bits	$t_{FRM\text{-}C}$ core parameter. Determines ROW-COL packet framing interval.
$04a_{16}$	TCDLY1	TCDLY1	read-write, 3 bits	$t_{CDLY1\text{-}C}$ core parameter. Programmable delay for read data.
$04c_{16}$	TCYCLE	TCYCLE	read-write, 14 bits	t_{CYCLE} datasheet parameter. Specifies cycle time in 64ps units.
$04b_{16\text{-}}$	TEST75	TEST75	read-write, 16 bits	Test register. Do not read or write after SIO reset.
$04d_{16\text{-}}$	TEST77	TEST77	read-write, 16 bits	Test register. Write with zero after SIO reset.
$04e_{16\text{-}}$	TEST78	TEST78	read-write, 16 bits	Test register. Do not read or write after SIO reset.
$04f_{16\text{-}}$	TEST79	TEST79	read-write, 16 bits	Test register. Do not read or write after SIO reset.
080_{16} - $0ff_{16}$	reserved	reserved	vendor-specific	Vendor-specific test registers. Do not read or write after SIO reset.

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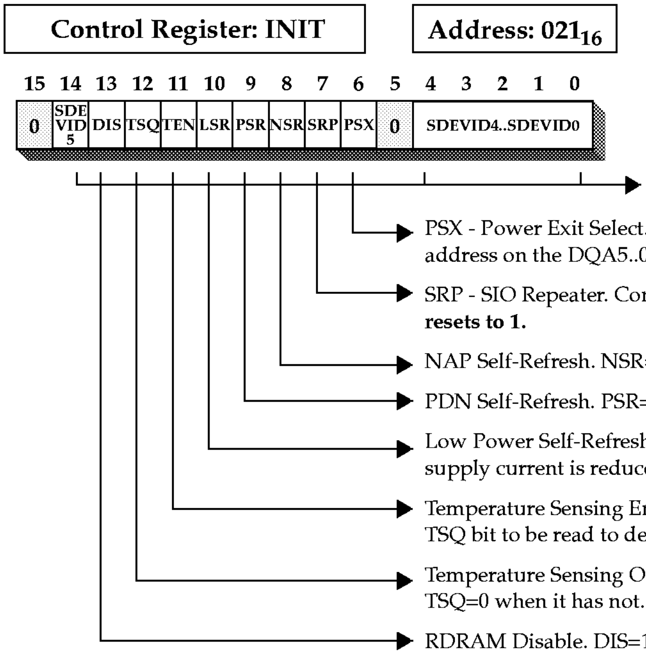


Read/write register.
Reset values are undefined except as affected by SIO Reset as noted below. SETR/CLRR Reset does not affect this register.

SDEVID5..0 - Serial Device Identification. Compared to SDEV5..0 serial address field of serial request packet for register read/write transactions. This determines which RDRAM is selected for the register read or write operation. **SDEVID resets to $3f_{16}$.**

PSX - Power Exit Select. PDN and NAP are exited with (=0) or without (=1) a device address on the DQA5..0 pins.

SRP - SIO Repeater. Controls value on SIO1; SIO1=SIO0 if SRP=1, SIO1=1 if SRP=0. **SRP resets to 1.**

NAP Self-Refresh. NSR=1 enables self-refresh in NAP mode. **NSR resets to 0.**

PDN Self-Refresh. PSR=1 enables self-refresh in PDN mode. **PSR resets to 0.**

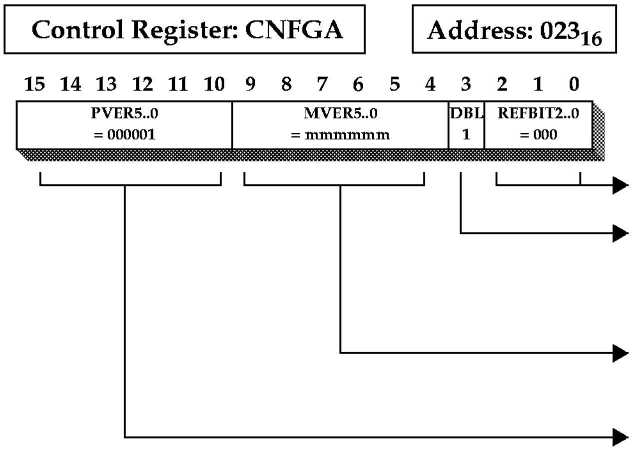
Low Power Self-Refresh. LSR=1 enables longer self-refresh interval. The self-refresh supply current is reduced. **LSR resets to 0.**

Temperature Sensing Enable. TEN=1 enables temperature sensing circuitry, permitting the TSQ bit to be read to determine if a thermal trip point has been exceeded. **TEN resets to 0.**

Temperature Sensing Output. TSQ=1 when a temperature trip point has been exceeded, TSQ=0 when it has not. TSQ is available during a current control operation (see Figure 50).

RDRAM Disable. DIS=1 causes RDRAM to ignore NAP/PDN exit sequence, DIS=0 permits normal operation. This mechanism disables an RDRAM. **DIS resets to 0.**

Figure 27: INIT Register



Read-only register.

REFBIT2..0 - Refresh Bank Bits. Specifies the number of high order bank address bits to be ignored during REFA and REFP commands. Permits multi-bank refresh in future RDRAMs.

DBL - Doubled-Bank. DBL=1 means the device uses a doubled-bank architecture with adjacent-bank dependency. DBL=0 means no dependency.

MVER5..0 - Manufacturer Version. Specifies the manufacturer identification number.

PVER5..0 - Protocol Version. Specifies the Direct Protocol version used by this device:
0 - Compliant with version 0.62 and ECO1-ECO18.
1 - Compliant with version 0.7 and ECO1-ECO38.
2 to 63 - Reserved

Figure 28: CNFGA Register

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Control Register: CNFGB

Address: 024$_{16}$

15 14 13 12 11 10	9 8 7 6 5	4	3 2 1	0
SVER5..0 = ssssss	CORG4..0 = xxxxx	SPT 0	DEVTYP2..0 = 000	BYT B

Read-only register.

BYT - Byte width. B=1 means the device reads and writes 9-bit memory bytes. B=0 means 8 bits.

DEVTYP2..0 - Device type. DEVTYP = 000 means that this device is an RDRAM.

SPT - Split-core. SPT=1 means the core is split, SPT=0 means it is not.

CORG4..0 - Core organization. This field specifies the number of bank (3, 4, 5, or 6 bits), row (9, 10, 11, or 12 bits), and column (5, 6, or 7 bits) address bits. The encoding of this field will be specified in a later version of this document.

SVER5..0 - Stepping version. Specifies the mask version number of this device.

Figure 29: CNFGB Register

Control Register: TEST34

Address: 022$_{16}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/write register.
Reset value of TEST34 is zero (from SIO Reset)
This register are used for testing purposes. It must not be read or written after SIO Reset.

Figure 30: TEST Register

Control Register: DEVID

Address: 040$_{16}$

15	14	13	12	11	10	9	8	7	6	5	4 3 2 1 0
0	0	0	0	0	0	0	0	0	0	0	DEVID4..DEVID0

Read/write register.
Reset value is undefined.
Device Identification register.
DEVID4..DEVID0 is compared to DR4..DR0, DC4..DC0, and DX4..DX0 fields for all memory read or write transactions. This determines which RDRAM is selected for the memory read or write transaction.

Figure 31: DEVID Register

Control Register: REFB **Address: 041_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	REFB2..REFB0		

Read/write register.
Reset value is zero (from SETR/CLRR).
Refresh Bank register.
REFB2..REFB0 is the bank that will be refreshed next during self-refresh. REFB2..0 is incremented after each self-refresh activate and precharge operation pair.

Figure 32: REFB Register

Control Register: CCA **Address: 043_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ASYMA 1..0		CCA6..CCA0						

Read/write register.
Reset value is zero (SETR/CLRR or SIO Reset).
CCA6..CCA0 - Current Control A. Controls the I_{OL} output current for the DQA8..DQA0 pins.

ASYMB1,ASYMB0 control the asymmetry of the V_{OL}/V_{OH} voltage swing about the V_{REF} reference voltage for the DQA8..0 pins.

Figure 33: CCA Register

Control Register: REFR **Address: 042_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	REFR8..REFR0								

Read/write register.
Reset value is zero (from SETR/CLRR).
Refresh Row register.
REFR8..REFR0 is the row that will be refreshed next by the REFP command or by self-refresh. REFR8..0 is incremented when BR2..0=111 for the REFA command. REFR8..0 is incremented when REFB2..0=111 for self-refresh.

Figure 34: REFR Register

Control Register: CCB **Address: 044_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ASYMB 1..0		CCB6..CCB0						

Read/write register.
Reset value is zero (SETR/CLRR or SIO Reset).
CCB6..CCB0 - Current Control B. Controls the I_{OL} output current for the DQB8..DQB0 pins.

ASYMB1,ASYMB0 control the asymmetry of the V_{OL}/V_{OH} voltage swing about the V_{REF} reference voltage for the DQB8..0 pins.

Figure 35: CCB Register

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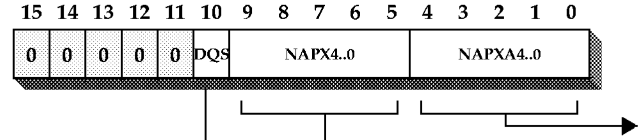
Control Register: NAPX **Address: 045_{16}**

Read/write register.
Reset value is undefined



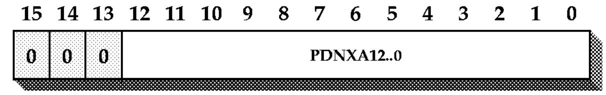
NAPXA4..0 - Nap Exit Phase A. This field specifies the number of SCK cycles during the first phase for exiting NAP mode. It must satisfy:
$NAPXA \bullet t_{SCYCLE} > t_{NAPXA,MAX}$
Do not set this field to zero.

NAPX4..0 - Nap Exit Phase A plus B. This field specifies the number of SCK cycles during the first plus second phases for exiting NAP mode. It must satisfy:
$NAPX \bullet t_{SCYCLE} > t_{NAPXA,MAX} + t_{NAPXB,MAX}$
Do not set this field to zero.

DQS - DQ Select. This field specifies the number of SCK cycles (0 => 0.5 cycles, 1 => 1.5 cycles) between the CMD pin framing sequence and the device selection on DQ5..0.

Figure 36: NAPX Register

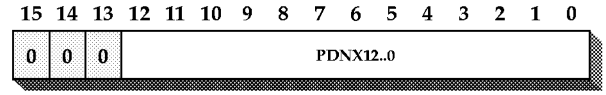
Control Register: PDNXA **Address: 046_{16}**



Read/write register.
Reset value is undefined
PDNXA4..0 - PDN Exit Phase A. This field specifies the number of (64•SCK cycle) units during the first phase for exiting PDN mode. It must satisfy:
$PDNXA \bullet 64 \bullet t_{SCYCLE} > t_{PDNXA,MAX}$
Do not set this field to zero.
Note - only PDNXA5..0 are implemented.

Figure 37: PDNXA Register

Control Register: PDNX **Address: 047_{16}**



Read/write register.
Reset value is undefined
PDNX4..0 - PDN Exit Phase A plus B. This field specifies the number of (256•SCK cycle) units during the first plus second phases for exiting PDN mode. It must satisfy:
$PDNX \bullet 256 \bullet t_{SCYCLE} > t_{PDNXA,MAX} + t_{PDNXB,MAX}$
Do not set this field to zero.
Note - only PDNX2..0 are implemented.

Figure 38: PDNX Register

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Control Register: TPARM **Address: 048_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	TCDLY0			TCLS		TCAS	

Read/write register.
Reset value is undefined.
TCAS1..0 - Specifies the $t_{CAS\text{-}C}$ core parameter in t_{CYCLE} units. This should be "10" ($2\bullet t_{CYCLE}$).

TCLS1..0 - Specifies the $t_{CLS\text{-}C}$ core parameter in t_{CYCLE} units. Should be "10" ($2\bullet t_{CYCLE}$).

TCDLY0 - Specifies the $t_{CDLY0\text{-}C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all devices to be equalized. This field may be written with the values "010" ($2\bullet t_{CYCLE}$) through "101" ($5\bullet t_{CYCLE}$).

The equations relating the core parameters to the datasheet parameters follow:

$t_{CAS\text{-}C} = 2\bullet t_{CYCLE}$
$t_{CLS\text{-}C} = 2\bullet t_{CYCLE}$
$t_{CPS\text{-}C} = 1\bullet t_{CYCLE}$ Not programmable

$t_{OFFP} = t_{CPS\text{-}C} + t_{CAS\text{-}C} + t_{CLS\text{-}C} - 1\bullet t_{CYCLE}$
$= 4\bullet t_{CYCLE}$

$t_{RCD} = t_{RCD\text{-}C} + 1\bullet t_{CYCLE} - t_{CLS\text{-}C}$
$= t_{RCD\text{-}C} - 1\bullet t_{CYCLE}$

$t_{CAC} = 3\bullet t_{CYCLE} + t_{CLS\text{-}C} + t_{CDLY0\text{-}C} + t_{CDLY1\text{-}C}$
(see table below for programming ranges)

TCDLY0	$t_{CDLY0\text{-}C}$	TCDLY1	$t_{CDLY1\text{-}C}$	t_{CAC} @ $t_{CYCLE} = 3.3ns$	t_{CAC} @ $t_{CYCLE} = 2.5ns$
010	$2\bullet t_{CYCLE}$	000	$0\bullet t_{CYCLE}$	$7\bullet t_{CYCLE}$	not allowed
010	$3\bullet t_{CYCLE}$	000	$0\bullet t_{CYCLE}$	$8\bullet t_{CYCLE}$	$8\bullet t_{CYCLE}$
011	$3\bullet t_{CYCLE}$	001	$1\bullet t_{CYCLE}$	$9\bullet t_{CYCLE}$	$9\bullet t_{CYCLE}$
011	$3\bullet t_{CYCLE}$	010	$2\bullet t_{CYCLE}$	$10\bullet t_{CYCLE}$	$10\bullet t_{CYCLE}$
100	$4\bullet t_{CYCLE}$	010	$2\bullet t_{CYCLE}$	$11\bullet t_{CYCLE}$	$11\bullet t_{CYCLE}$
101	$5\bullet t_{CYCLE}$	010	$2\bullet t_{CYCLE}$	not allowed	$12\bullet t_{CYCLE}$

Figure 39: TPARM Register

Control Register: TFRM **Address: 049_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TFRM3..0			

Read/write register.
Reset value is undefined.
TFRM3..0 - Specifies the position of the framing point in t_{CYCLE} units. This value must be greater than or equal to the $t_{FRM,MIN}$ parameter. This is the minimum offset between a ROW packet (which places a device at ATTN) and the first COL packet (directed to that device) which must be framed. This field may be written with the values "0111" ($7\bullet t_{CYCLE}$) through "1010" ($10\bullet t_{CYCLE}$). TFRM is usually set to the value which matches the largest $t_{RCD,MIN}$ parameter (modulo $4\bullet t_{CYCLE}$) that is present in an RDRAM in the memory system. Thus, if an RDRAM with $t_{RCD,MIN} = 11\bullet t_{CYCLE}$ were present, then TFRM would be programmed to $7\bullet t_{CYCLE}$.

Figure 40: TFRM Register

Control Register: TCDLY1 **Address: $04a_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	TCDLY1		

Read/write register.
Reset value is undefined.
TCDLY1 - Specifies the value of the $t_{CDLY1\text{-}C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all devices to be equalized. This field may be written with the values "000" ($0\bullet t_{CYCLE}$) through "010" ($2\bullet t_{CYCLE}$). Refer to Figure 39 for more details.

Figure 41: TRDLY Register

Control Register: TCYCLE **Address: $04c_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	TCYCLE13..TCYCLE0													

Read/write register.
Reset value is undefined
TCYCLE13..0 - Specifies the value of the t_{CYCLE} datasheet parameter in 64ps units. For the $t_{CYCLE,MIN}$ of 2.5ns (2500ps), this field should be written with the value "00027_{16}" (39•64ps).

Figure 42: TCYCLE Register

Control Register: TEST75	**Address: $04b_{16}$**
Control Register: TEST77	**Address: $04d_{16}$**
Control Register: TEST78	**Address: $04e_{16}$**
Control Register: TEST79	**Address: $04f_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/write registers.
Reset value of TEST75,78,79 is zero (SIO Reset).
Do not read or write TEST75,78,79 after SIO reset.
TEST77 must be written with zero after SIO reset.
These registers must only be used for testing purposes.

Figure 43: TEST Registers

Power State Management

Table 17 summarizes the power states available to a Direct RDRAM. In general, the lowest power states have the longest operational latencies. For example, the relative power levels of PDN state and STBY state have a ratio of about 1:110, and the relative access latencies to get read data have a ratio of about 250:1.

PDN state is the lowest power state available. The information in the RDRAM core is usually maintained with self-refresh; an internal timer automatically refreshes all rows of all banks. PDN has a relatively long exit latency because the TCLK/RCLK block must resynchronize itself to the external clock signal.

NAP state is another low-power state in which either self-refresh or REFA-refresh are used to maintain the core. See "Refresh" on page 42 for a description of the two refresh mechanisms. NAP has a shorter exit latency than PDN because the TCLK/RCLK block maintains its synchronization state relative to the external clock signal at the time of NAP entry. This imposes a limit (t_{NLIMIT}) on how long an RDRAM may remain in NAP state before briefly returning to STBY or ATTN to update this synchronization state.

Table 17: Power State Summary

Power State	Description	Blocks consuming power	Power State	Description	Blocks consuming power
PDN	Powerdown state.	Self-refresh	NAP	Nap state. Similar to PDN except lower wake-up latency.	Self-refresh or REFA-refresh TCLK/RCLK-Nap
STBY	Standby state. Ready for ROW packets.	REFA-refresh TCLK/RCLK ROW demux receiver	ATTN	Attention state. Ready for ROW and COL packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver
ATTNR	Attention read state. Ready for ROW and COL packets. Sending Q (read data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ mux transmitter Core power	ATTNW	Attention write state. Ready for ROW and COL packets. Ready for D (write data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ demux receiver Core power

Figure 44 summarizes the transition conditions needed for moving between the various power states. Note that NAP and PDN have been divided into two substates (NAP-A/NAP-S and PDN-A/PDN-S) to account for the fact that a NAP or PDN exit may be made to either ATTN or STBY states.

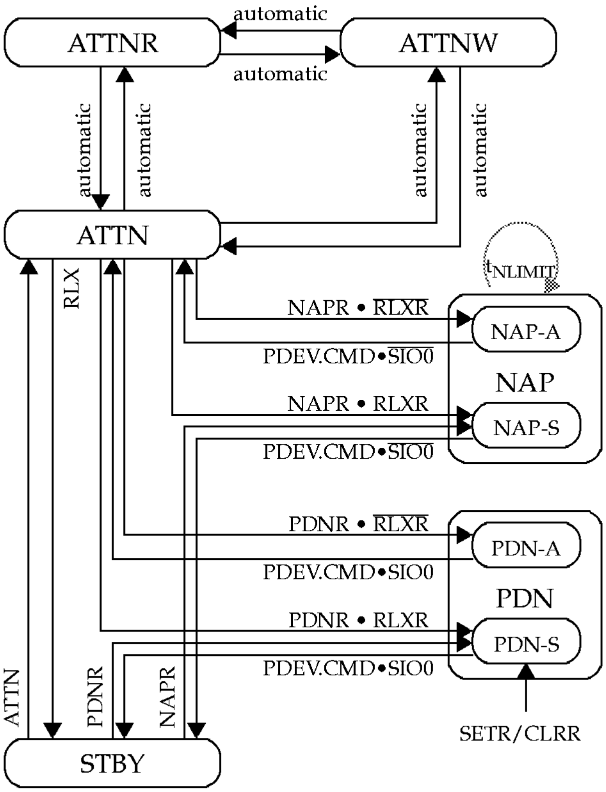
At initialization, the SETR/CLRR Reset sequence will put the RDRAM into PDN-S state. The PDN exit sequence involves an optional PDEV specification and bits on the CMD and SIO_{IN} pins.

Once the RDRAM is in STBY, it will move to the ATTN/ATTNR/ATTNW states when it receives a non-broadcast ROWA packet or non-broadcast ROWR packet with the ATTN command. The RDRAM returns to STBY from these three states when it receives a RLX command. Alternatively, it may enter NAP or PDN state from ATTN or STBY states with a NAPR or PDNR command in an ROWR packet. The PDN or NAP exit sequence involves an optional PDEV specification and bits on the CMD and SIO0 pins. The RDRAM returns to the ATTN or STBY state it was originally in when it first entered NAP or PDN.

An RDRAM may only remain in NAP state for a time t_{NLIMIT}. It must periodically return to ATTN or STBY.

The NAPRC command causes a napdown operation if the RDRAM's NCBIT is set. The NCBIT is not directly visible. It is undefined on reset. It is set by a NAP or NAPRC command to the RDRAM, and it is cleared by an ACT command to the RDRAM. It permits a controller to manage a set of RDRAMs in a mixture of power states.

STBY state is the normal idle state of the RDRAM. In this state all banks and sense amps have usually been left precharged and ROWA and ROWR packets on the ROW pins are being monitored. When a non-broadcast ROWA packet or non-broadcast ROWR packet (with the ATTN command) packet addressed to the RDRAM is seen, the RDRAM enters ATTN state (see the right side of Figure 45). This requires a time t_{SA} during which the RDRAM activates the specified row of the specified bank. A time TFRM•t_{CYCLE} after the ROW packet, the RDRAM will be able to frame COL packets (TFRM is a control register field - see Figure 40). Once in ATTN state, the RDRAM will automatically transition to the ATTNW and ATTNR states as it receives WR and RD commands.



Notation:
SETR/CLRR - SETR/CLRR Reset sequence in SRQ packets
PDNR - PDNR command in ROWR packet
NAPR - NAPR command in ROWR packet
RLXR - RLX command in ROWR packet
RLX - RLX command in ROWR,COLC,COLX packets
SIO0 - SIO0 input value
PDEV.CMD - (PDEV=DEVID)•(CMD=01)
ATTN - ROWA packet (non-broadcast) or ROWR packet
(non-broadcast) with ATTN command

Figure 44: Power State Transition Diagram

Once the RDRAM is in ATTN, ATTNW, or ATTNR states, it will remain there until it is explicitly returned to the STBY state with a RLX command. A RLX command may be given in an ROWR, COLC , or COLX packet (see the left side of Figure 45). It is usually given after all banks of the RDRAM have been precharged; if other banks are still activated, then the RLX command would probably not be given.

If a broadcast ROWA packet or ROWR packet (with the ATTN command) is received, the RDRAM's power state doesn't change. If a broadcast ROWR packet with RLXR command is received, the RDRAM goes to STBY.

Figure 46 shows the NAP entry sequence (left). NAP state is entered by sending a NAPR command in a ROW packet. A time t_{ASN} is required to enter NAP state (this specification is provided for power calculation purposes). The clock on CTM/CFM must remain stable for a time t_{CD} after the NAPR command.

The RDRAM may be in ATTN or STBY state when the NAPR command is issued. When NAP state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and a RLXR command is specified with NAPR, then the RDRAM will return to STBY state when NAP is exited.

Figure 46 also shows the PDN entry sequence (right). PDN state is entered by sending a PDNR command in a ROW packet. A time t_{ASP} is required to enter PDN state (this specification is provided for power calculation purposes). The clock on CTM/CFM must remain stable for a time t_{CD} after the PDNR command.

The RDRAM may be in ATTN or STBY state when the PDNR command is issued. When PDN state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and a RLXR command is specified with PDNR, then the RDRAM will return to STBY state when PDN is exited.

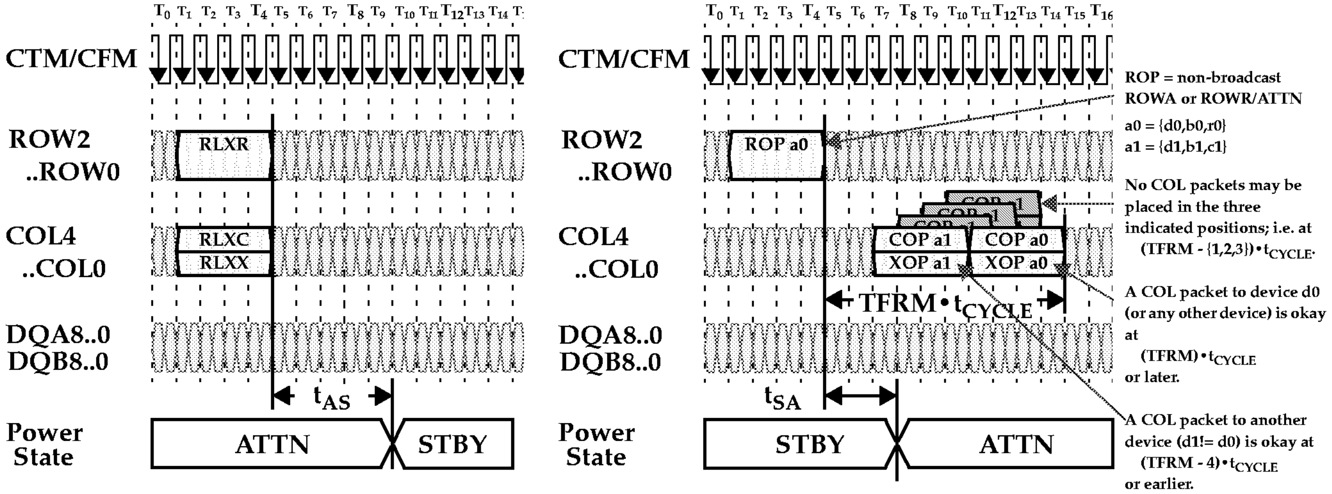
The RDRAM's write buffer must be retired with the appropriate COP command before NAP or PDN are entered. Also, all the RDRAM's banks must be precharged before NAP or PDN are entered. The exception to this is if NAP is entered with the NSR bit of the INIT register cleared (disabling self-refresh in NAP). The commands for relaxing, retiring, and precharging may be given to the RDRAM as late as the ROPa0, COPa0, and XOPa0 packets in Figure 46. No broadcast packets nor packets directed to the RDRAM entering Nap or PDN may overlay the quiet window. This window extends for a time t_{NPQ} after the packet with the NAPR or PDNR command.

Figure 47 shows the NAP and PDN exit sequences. These sequences are virtually identical; the minor differences will be highlighted in the following description.

Before NAP or PDN exit, the CTM/CFM clock must be stable for a time t_{CE}. Then, on a falling and rising edge of SCK, if there is a "01" on the CMD input, NAP or PDN state will be exited. Also, on the falling SCK edge the SIO0 input must be at a 0 for NAP exit and 1 for PDN exit.

If the PSX bit of the INIT register is 0, then a device PDEV5..0 is specified for NAP or PDN exit on the DQA5..0 pins. This value is driven on the rising SCK edge 0.5 or 1.5 SCK cycles after the original falling edge, depending upon the value of the DQS bit of the NAPX register. If the PSX bit of the INIT register is 1, then the RDRAM ignores the PDEV5..0 address packet and exits NAP or PDN when the wake-up sequence is presented on the CMD wire. The ROW and COL pins must be quiet at a time t_{S4}/t_{H4} around the indicated falling SCK edge (timed with the PDNX or NAPX register fields). After that, ROW and COL packets may be directed to the RDRAM which is now in ATTN or STBY state.

Figure 48 shows the constraints for entering and exiting NAP and PDN states. On the left side, an RDRAM exits NAP state at the end of cycle T_3. This RDRAM may not re-enter NAP state for an interval of t_{NU0}. The RDRAM enters NAP state at the end of cycle T_{13}. This RDRAM may not re-exit NAP state for an interval of t_{NU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. NAPX is the value in the NAPX field in the NAPX register.



ROP = non-broadcast ROWA or ROWR/ATTN

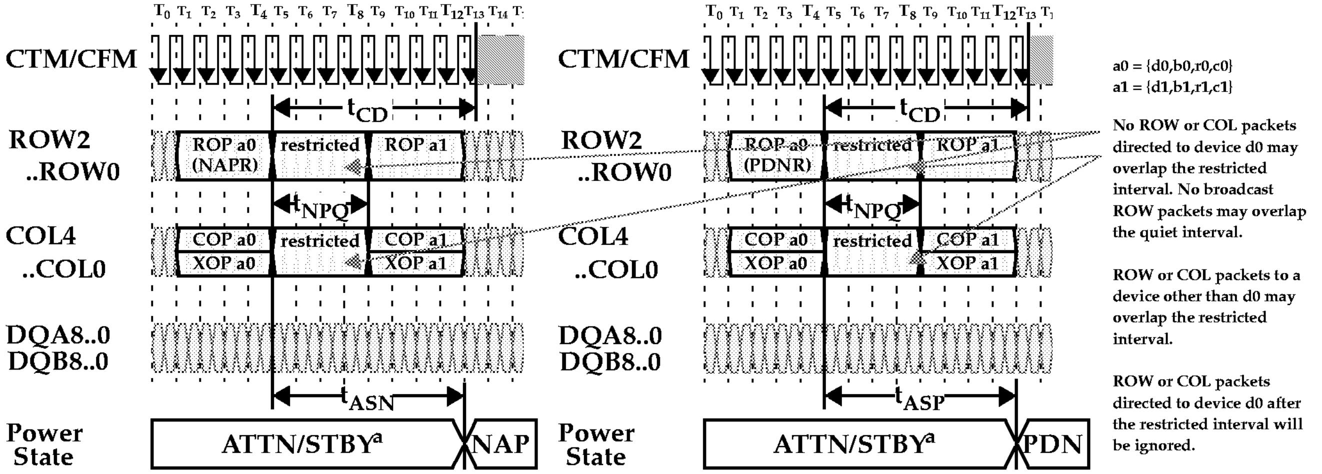
a0 = {d0,b0,r0}
a1 = {d1,b1,c1}

No COL packets may be placed in the three indicated positions; i.e. at (TFRM - {1,2,3}) • t_{CYCLE}.

A COL packet to device d0 (or any other device) is okay at (TFRM) • t_{CYCLE} or later.

A COL packet to another device (d1!= d0) is okay at (TFRM - 4) • t_{CYCLE} or earlier.

Figure 45: STBY Entry (left) and STBY Exit (right)



a0 = {d0,b0,r0,c0}
a1 = {d1,b1,r1,c1}

No ROW or COL packets directed to device d0 may overlap the restricted interval. No broadcast ROW packets may overlap the quiet interval.

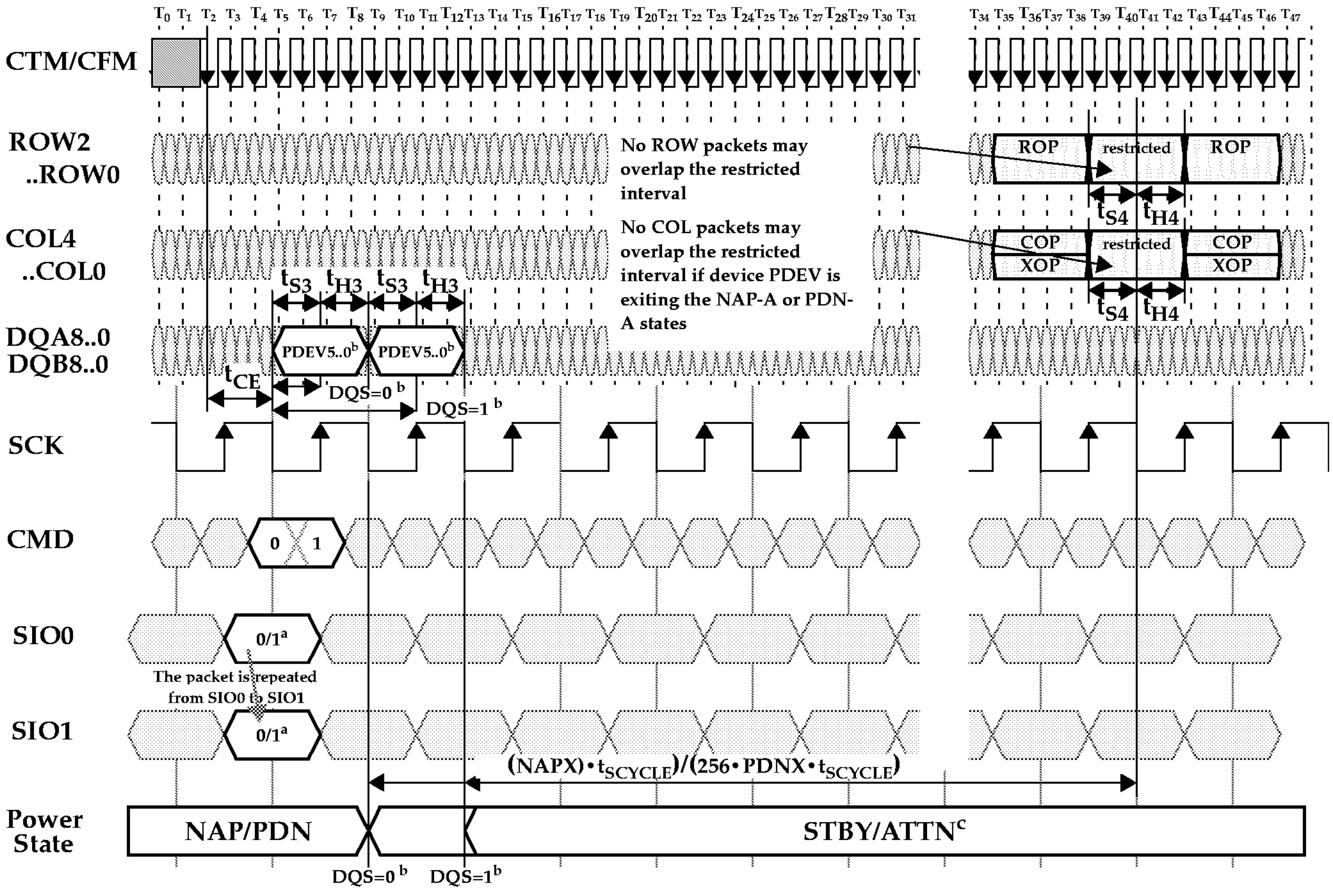
ROW or COL packets to a device other than d0 may overlap the restricted interval.

ROW or COL packets directed to device d0 after the restricted interval will be ignored.

[a] The (eventual) NAP/PDN exit will be to the same ATTN/STBY state the RDRAM was in prior to NAP/PDN entry

Figure 46: NAP Entry (left) and PDN Entry (right)

On the right side of Figure 47, an RDRAM exits PDN state at the end of cycle T_3. This RDRAM may not re-enter PDN state for an interval of t_{PU0}. The RDRAM enters PDN state at the end of cycle T_{13}. This RDRAM may not re-exit PDN state for an interval of t_{PU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. PDNX is the value in the PDNX field in the PDNX register.

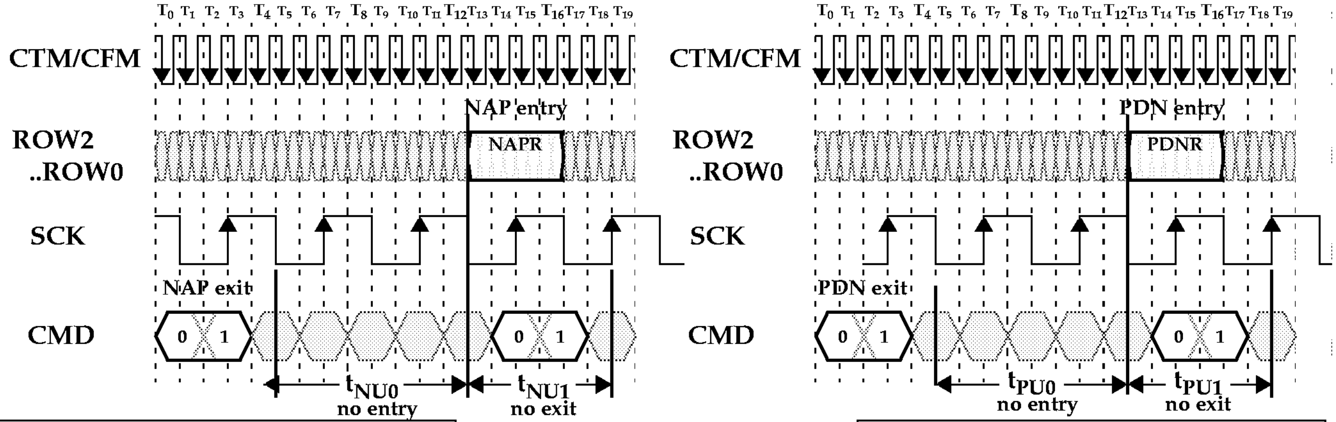


[a] Use 0 for NAP exit, 1 for PDN exit

[b] Device selection timing slot is selected by DQS field of NAPX register

[c] Exit to STBY or ATTN depends upon whether RLXR was asserted at NAP or PDN entry time

Figure 47: NAP and PDN Exit



$t_{NU0} = 5\cdot t_{CYCLE} + (2+NAPX)\cdot t_{SCYCLE}$

$t_{NU1} = 8\cdot t_{CYCLE} - (0.5\cdot t_{SCYCLE})$ if NSR=1

$= 23\cdot t_{CYCLE}$ if NSR=0

$t_{PU0} = 5\cdot t_{CYCLE} + (2+256\cdot PDNX)\cdot t_{SCYCLE}$

$t_{PU1} = 8\cdot t_{CYCLE} - (0.5\cdot t_{SCYCLE})$ if PSR=1

$= 23\cdot t_{CYCLE}$ if PSR=0

Figure 48: NAP Entry/Exit Windows (left) and PDN Entry/Exit Windows (right)

Refresh

RDRAMs, like any other DRAM technology, use volatile storage cells which must be periodically refreshed. This is accomplished with the REFA command. Figure 49 shows an example of this.

The REFA command in the transaction is typically a broadcast command (DR4T and DR4F are both set in the ROWR packet), so that in all devices bank number Ba is activated with row number REFR, where REFR is a control register in the RDRAM. When the command is broadcast and ATTN is set, the power state of the RDRAMs (ATTN or STBY) will remain unchanged. The controller increments the bank address Ba for the next REFA command. When Ba is equal to its maximum value, the RDRAM automatically increments REFR for the next REFA command.

On average, these REFA commands are sent once every $t_{REF}/2^{BBIT+RBIT}$ (where BBIT are the number of bank address bits and RBIT are the number of row address bits) so that each row of each bank is refreshed once every t_{REF} interval.

The REFA command is equivalent to an ACT command, in terms of the way that it interacts with other packets (see Table 10). In the example, an ACT command is sent after t_{RR} to address b0, a different (non-adjacent) bank than the REFA command.

A second ACT command can be sent after a time t_{RC} to address c0, the same bank (or an adjacent bank) as the REFA command.

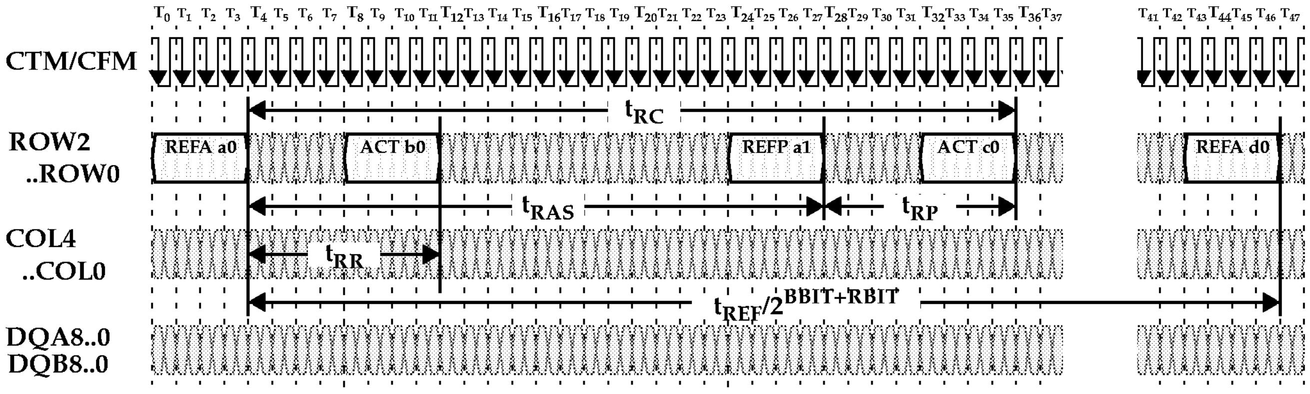
Note that a broadcast REFP command is issued a time t_{RAS} after the initial REFA command in order to precharge the refreshed bank in all RDRAMs. After a bank is given a REFA command, no other core operations (activate or precharge) should be issued to it until it receives a REFP.

It is also possible to interleave refresh transactions (not shown). In the figure, the ACT b0 command would be replaced by a REFA b0 command. The b0 address would be broadcast to all devices, and would be {Broadcast,Ba+2,REFR}. Note that the bank address should skip by two to avoid adjacent bank interference. A possible bank incrementing pattern would be: {0, 2, 4, 6, 1, 3, 5, 7}. Every time bank 7 is reached, the REFA command would automatically increment the REFR register.

A second refresh mechanism is available for use in PDN and NAP power states. This mechanism is called self-refresh mode. When the PDN power state is entered, or when NAP power state is entered with the NSR control register bit set, then self-refresh is automatically started for the RDRAM.

Self-refresh uses an internal time base reference in the RDRAM. This causes an activate and precharge to be carried out once in every $t_{REF}/2^{BBIT+RBIT}$ interval. The REFB and REFR control registers are used to keep track of the bank and row being refreshed.

Before a controller places an RDRAM into self-refresh mode, it should perform REFA/REFP refreshes until the bank address is equal to the maximum value. This ensures that no rows are skipped. Likewise, when a controller returns an RDRAM to REFA/REFP refresh, it should start with the minimum bank address value (zero).



Transaction a: REFA	a0 = {Broadcast,Ba,REFR}	a1 = {Broadcast,Ba}
Transaction b: xx	b0 = {Db, /={Ba,Ba+1,Ba-1}, Rb}	
Transaction c: xx	c0 = {Dc, ==Ba, Rc}	
Transaction d: REFA	d0 = {Broadcast,Ba+1,REFR}	

BBIT = # bank address bits
RBIT = # row address bits
REFB = REFB2..REFB0
REFR = REFR8..REFR0

Figure 49: REFA/REFP Refresh Transaction Example

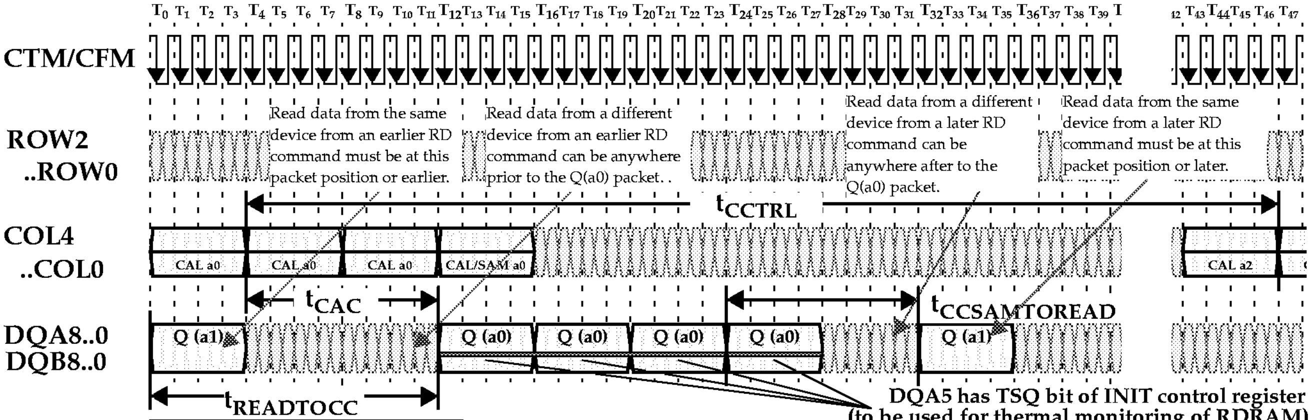
Current and Temperature Control

Figure 50 shows an example of a transaction which performs current control calibration. It is necessary to perform this operation once to every RDRAM in every t_{CCTRL} interval in order to keep the I_{OL} output current in its proper range.

This example uses four COLX packets with a CAL command. These cause the RDRAM to drive four calibration packets Q(a0) a time t_{CAC} later. An offset of t_{RDTOCC} must be placed between the Q(a0) packet and read data Q(a1)from the same device. These calibration packets are driven on the DQA4..3 and DQB4..3 wires. The TSQ bit of the INIT register is driven on the DQA5 wire during same interval as the calibration packets. The remaining DQA and DQB wires are not used during these calibration packets. The last COLX packet also contains a SAM command (concatenated with the CAL command). The RDRAM samples the last calibration packet and adjusts its I_{OL} current value.

Unlike REF commands, CAL and SAM commands cannot be broadcast. This is because the calibration packets from different devices would interfere. Therefore, a current control transaction must be sent every t_{CCTRL}/N, where N is the number of RDRAMs on the Channel. The device field Da of the address a0 in the CAL/SAM command should be incremented after each transaction.

Figure 51 shows an example of a temperature calibration sequence to the RDRAM. This sequence is broadcast once every t_{TEMP} interval to all the RDRAMs on the Channel. The TCEN and TCAL are ROP commands, and cause the slew rate of the output drivers to adjust for temperature drift. During the quiet interval $t_{TCQUIET}$ the devices being calibrated can't be read, but they can be written.



Transaction a0: CAL/SAM	a0 = {Da, Bx}
Transaction a1: RD	a1 = {Da, Bx}
Transaction a2: CAL/SAM	a2 = {Da+1, Bx}

Figure 50: Current Control CAL/SAM Transaction Example

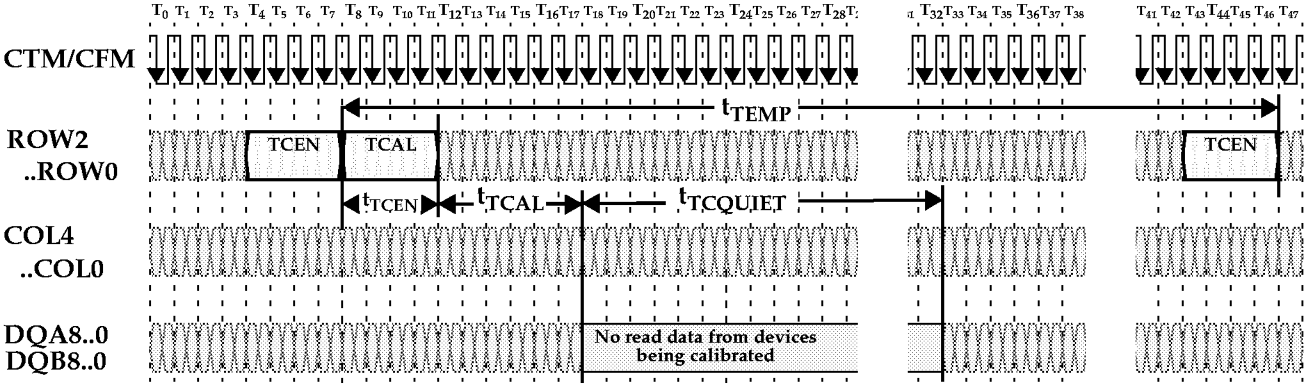


Figure 51: Temperature Calibration (TCEN-TCAL) Transactions to RDRAM

Electrical Conditions

Table 18: Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
T_J	Junction temperature under bias	TBD	TBD	°C
V_{DD}, V_{DDA}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
$V_{DD,N}$, $V_{DDA,N}$	Supply voltage droop (DC) during NAP interval (t_{NLIMIT})	-	2.0	%
$v_{DD,N}$, $v_{DDA,N}$	Supply voltage ripple (AC) during NAP interval (t_{NLIMIT})	-2.0	2.0	%
V_{CMOS}	Supply voltage for CMOS pins (2.5V controllers)	2.50 - 0.13	2.50 + 0.25	V
	Supply voltage for CMOS pins (1.8V controllers)	1.80 - 0.1	1.80 + 0.2	V
V_{TERM}	Termination voltage	1.80 - 0.1	1.80 + 0.1	V
V_{REF}	Reference voltage	1.40 - 0.2	1.40 + 0.2	V
V_{DIL}	RSL data input - low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{DIH}	RSL data input - high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
V_{DIS}	RSL data input swing: $V_{DIS} = V_{DIH} - V_{DIL}$	0.4	1.0	V
A_{DI}	RSL data asymmetry: $A_{DI} = [(V_{DIH} - V_{REF}) + (V_{DIL} - V_{REF})]/V_{DIS}$	-10	10	%
V_X	RSL clock input - crossing point of true and complement signals	1.3	1.8	V
$V_{CIS,CTM}$	RSL clock input swing: $V_{CIS} = V_{CIH} - V_{CIL}$ (CTM,CTMN pins).	0.35	0.70	V
$V_{CIS,CFM}$	RSL clock input swing: $V_{CIS} = V_{CIH} - V_{CIL}$ (CFM,CFMN pins).	0.10	0.70	V
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3	$V_{CMOS}/2 - 0.25$	V
$V_{IH,CMOS}$	CMOS input high voltage	$V_{CMOS}/2 + 0.25$	$V_{CMOS}+0.7$	V

Timing Conditions

Table 19: Timing Conditions

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_{CYCLE}	CTM and CFM cycle times (-1000)	2.00	2.51	ns	Figure 52
	CTM and CFM cycle times (-800)	2.50	3.34	ns	Figure 52
t_{CR}, t_{CF}	CTM and CFM input rise and fall times	0.2	0.5	ns	Figure 52
t_{CH}, t_{CL}	CTM and CFM high and low times	40%	60%	t_{CYCLE}	Figure 52
t_{TR}	CTM-CFM differential	0.0	1.0	t_{CYCLE}	Figure 52
t_{DCW}	Domain crossing window	-0.1	0.1	t_{CYCLE}	Figure 58
t_{DR}, t_{DF}	DQA/DQB/ROW/COL input rise/fall times	0.2	0.65	ns	Figure 53
t_S, t_H	DQA/DQB/ROW/COL-to-CFM setup/hold t_{CYCLE}=2.5ns @ t_{CYCLE}=2.0ns	0.200 TBD	-	ns	Figure 53
t_{DR1}, t_{DF1}	SIO0, SIO1 input rise and fall times	-	5.0	ns	Figure 55
t_{DR2}, t_{DF2}	CMD, SCK input rise and fall times	-	2.0	ns	Figure 55

Table 19: Timing Conditions

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_{CYCLE1}	SCK cycle time - Serial control register transactions	1000	-	ns	Figure 55
	SCK cycle time - Power transitions	10	-	ns	Figure 55
t_{CH1}, t_{CL1}	SCK high and low times	4.25	-	ns	Figure 55
t_{S1}	CMD setup time to SCK rising or falling edge	1	-	ns	Figure 55
t_{H1}	CMD hold time to SCK rising or falling edge	1	-	ns	Figure 55
t_{S2}	SIO0 setup time to SCK falling edge	40	-	ns	Figure 55
t_{H2}	SIO0 hold time to SCK falling edge	40	-	ns	Figure 55
t_{S3}	PDEV setup time on DQA5..0 to SCK rising edge.	0	-	ns	Figure 47, Figure 56
t_{H3}	PDEV hold time on DQA5..0 to SCK rising edge.	5.5	-	ns	Figure 47, Figure 56
t_{S4}	ROW2..0, COL4..0 setup time for quiet window	-1	-	t_{CYCLE}	Figure 47
t_{H4}	ROW2..0, COL4..0 hold time for quiet window	5	-	t_{CYCLE}	Figure 47
$v_{IL,CMOS}$	CMOS input low voltage - over/undershoot voltage duration is less than or equal to 5ns	- 0.7	$V_{CMOS}/2 - 0.6$	V	
$v_{IH,CMOS}$	CMOS input high voltage - over/undershoot voltage duration is less than or equal to 5ns	$V_{CMOS}/2 + 0.6$	$V_{CMOS} + 0.7$	V	
t_{NPQ}	Quiet on ROW/COL bits during NAP/PDN entry	4	-	t_{CYCLE}	Figure 46
$t_{READTOCC}$	Offset between read data and CC packets (same device)	12	-	t_{CYCLE}	Figure 50
$t_{CCSAMTOREAD}$	Offset between CC packet and read data (same device)	8	-	t_{CYCLE}	Figure 50
t_{CE}	CTM/CFM stable before NAP/PDN exit	2	-	t_{CYCLE}	Figure 47
t_{CD}	CTM/CFM stable after NAP/PDN entry	25	-	t_{CYCLE}	Figure 46
t_{FRM}	ROW packet to COL packet ATTN framing delay	7	-	t_{CYCLE}	Figure 45
t_{NLIMIT}	Maximum time in NAP mode		10.0	µs	Figure 44
t_{REF}	Refresh interval		32	ms	Figure 49
t_{CCTRL}	Current control interval	0.0001	100	ms	Figure 50
t_{TEMP}	Temperature control interval		100	ms	Figure 51
t_{TCEN}	TCE command to TCAL command	4	250	t_{CYCLE}	Figure 51
t_{TCAL}	TCAL command to quiet window	6	6	t_{CYCLE}	Figure 51
$t_{TCQUIET}$	Quiet window (no read data)	140	-	t_{CYCLE}	Figure 51
t_{RAS}	RAS interval (time a row may stay activated)		64	µs	Figure 15 Figure 16
t_{PAUSE}	RDRAM delay (no RSL operations allowed)		200.0	µs	page 28

Electrical Characteristics

Table 20: Electrical Characteristics

Symbol	Parameter and Conditions	Min	Max	Unit
Θ_{JC}	Junction-to-Case thermal resistance		TBD	°C/Watt
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10	10	μA
I_{OH}	RSL output high current @ $(0 \le V_{OUT} \le V_{DD})$	-10	10	μA
I_{ALL}	RSL I_{OL} current @ $V_{OL} = 0.9V$, $V_{DD,MIN}$, $T_{J,MAX}$[a]	30.0	90.0	mA
ΔI_{OL}	RSL I_{OL} current resolution step	-	1.5	mA
r_{OUT}	Dynamic output impedance	150	-	Ω
$I_{I,CMOS}$	CMOS input leakage current @ $(0 \le V_{I,CMOS} \le V_{CMOS})$	-10.0	10.0	μA
$V_{OL,CMOS}$	CMOS output voltage @ $I_{OL,CMOS}$= 1.0mA	-	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$= -0.25mA	V_{CMOS}-0.3	-	V

a. This measurement is made in manual current control mode; i.e. with all output device legs sinking current.

Timing Characteristics

Table 21: Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Figure(s)
t_Q	CTM-to-DQA/DQB output time @ t_{CYCLE}=2.5ns @ t_{CYCLE}=2.0ns	-0.30 TBD	+0.30 TBD	ns	Figure 54
t_{QR}, t_{QF}	DQA/DQB output rise and fall times	0.2	0.45	ns	Figure 54
t_{Q1}	SCK-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF (SD read packet).	-	10	ns	Figure 57
t_{QR1}, t_{QF1}	SIO_{OUT} rise/fall @ $C_{LOAD,MAX}$ = 20pF	-	5	ns	Figure 57
t_{PROP1}	SIO0-to-SIO1 or SIO1-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF	-	10	ns	Figure 57
t_{NAPXA}	NAP exit delay - phase A	-	50	ns	Figure 47
t_{NAPXB}	NAP exit delay - phase B	-	40	ns	Figure 47
t_{PDNXA}	PDN exit delay - phase A	-	4	μs	Figure 47
t_{PDNXB}	PDN exit delay - phase B	-	8	μs	Figure 47
t_{AS}	ATTN-to-STBY power state delay	1	4	t_{CYCLE}	Figure 45
t_{SA}	STBY-to-ATTN power state delay	-	3	t_{CYCLE}	Figure 45
t_{ASN}	ATTN/STBY-to-NAP power state delay	-	8	t_{CYCLE}	Figure 46
t_{ASP}	ATTN/STBY-to-PDN power state delay	-	8	t_{CYCLE}	Figure 46

RSL - Clocking

Figure 52 is a timing diagram which shows the detailed requirements for the RSL clock signals on the Channel.

The CTM and CTMN are differential clock inputs used for transmitting information on the DQA and DQB, outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CTM edge to the falling CTM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CTM. The t_{CR} and t_{CF} rise- and fall-time parameters are measured at the 20% and 80% points.

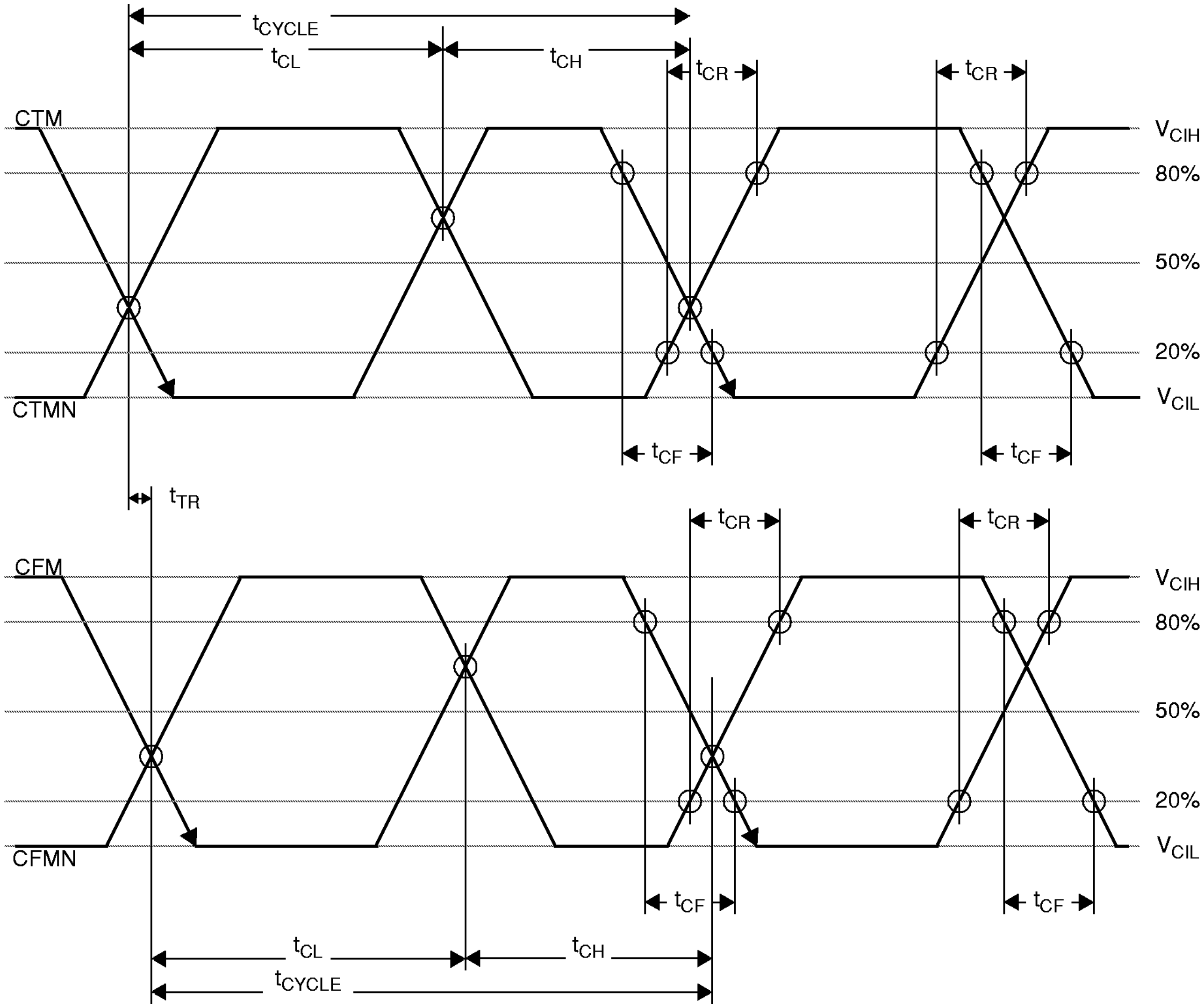


Figure 52: RSL Timing - Clock Signals

The CFM and CFMN are differential clock outputs used for receiving information on the DQA, DQB, ROW and COL outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CFM edge to the falling CFM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CFM. The t_{CR} and t_{CF} rise- and fall-time parameters are measured at the 20% and 80% points.

The t_{TR} parameter specifies the phase difference that may be tolerated with respect to the CTM and CFM differential clock inputs (the CTM pair is always earlier).