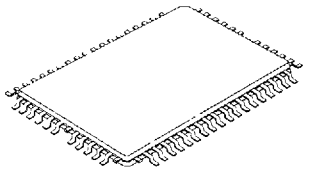
40-CHANNEL SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

The KS0065 is a LCD driver LSI which is fabricated by low power CMOS technology Bascially this LSI consists of 20X2bit bidrectional shift register, 20X2 bit data latch and 20X2 bit driver (refer to Fig 1) This LSI can be used a common or segment driver

60 QFP



FUNCTION

- **Dot matrix LCD driver with 40 channel output.**
- **Selectable function to use common/segment drivers simultaneously.**
- **Input/Output signal**
  - **— output; 20 × 2 channel waveform for LCD driving**
  - **— input ; - Serial display data and control pulse from the controller LSI.**
    - Bias voltage (V_1-V_6)

FEATURES

- **Display driving bias; static-1/5**
- **Power supply voltage; +5V ±10%**
- **Supply voltage for display: −5V**
- **interface**

driver (cascade connection)	controller
Other KS0065, KS0063	KS0066

- **CMOS Process**
- **60QFP and bare chip available**

BLOCK DIAGRAM

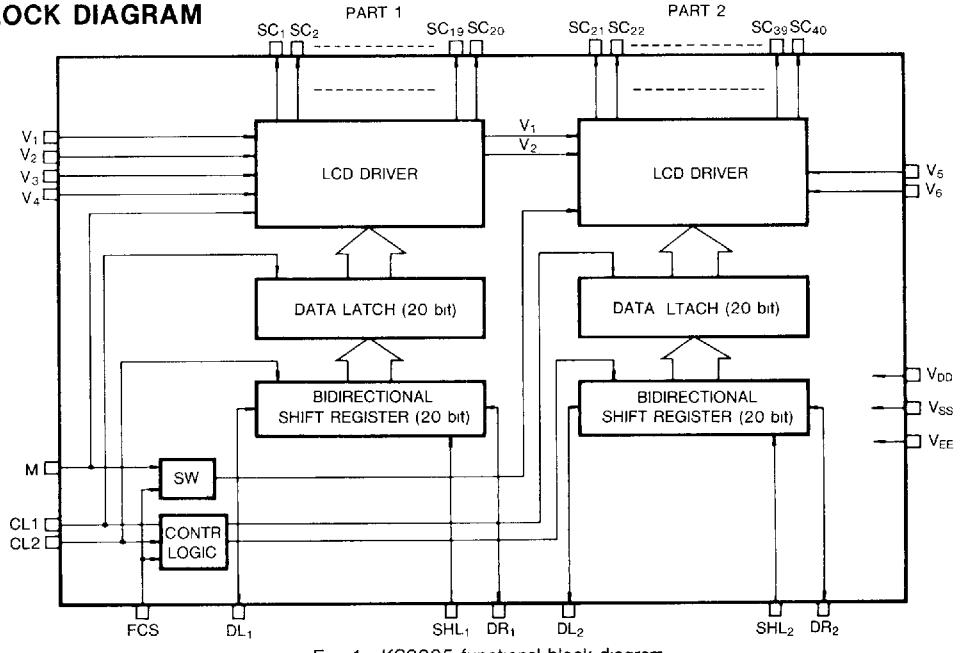


Fig 1 KS0065 functional block diagram

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PIN CONFIGURATION

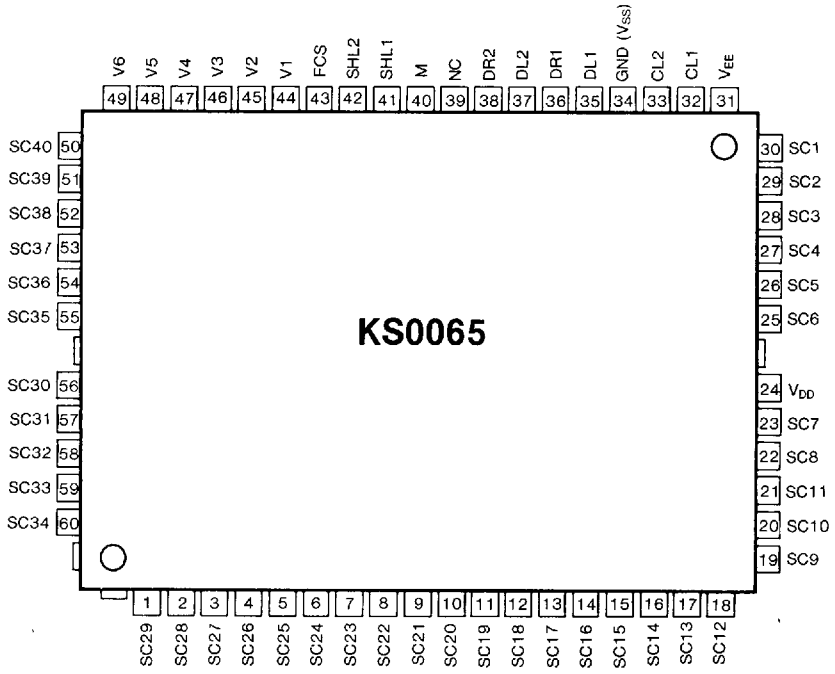

Fig 2 60 QFP Top View

PIN(No.)	INPUT/ OUTPUT	NAME		DESCRIPTION	INTERFACE
V_{DD}(24)		Power Supply		For logical circuit (+5V±10%)	Power Supply
GND(34)				0V (GND)	
V_{EE}(31)				For LCD driver circuit (−5V)	
V_1 V_2 (44, 45)	Input	Bias Vtg		Bias voltage level for LCD drive (select level)	power
SC_1~SC_{20}	Output	Part 1	LCD driver	LCD driver output	LCD
V_3 V_4 (46, 47)	Input		Bias Vtg	Bias voltage level for LCD drive (nonselect level)	power
SHL1 (41)	Input		Data interface	Selection of the shift direction of Part 1 shift register SHL1 = V_{DD}: out, in SHL1 = V_{SS}: in, out	V_{DD} or V_{SS}
DL1, DR1 (35, 36)	Input Output			Data input/output of Part 1 shift register	Controller or KS0065
SC_{21}~SC_{40}	Output	Part 2	LCD driver	LCD driver output	LCD
V5 V6 (48, 49)	Input		Bias Vtg	Bias voltage level for LCD drive (non select level)	power
SHL2 (42)	Input		Data Interface	Selection of the shift direction of Part 2 shift register SHL2 = V_{DD}: out, in SHL2 = V_{SS}: in, out	V_{DD} or V_{SS}
DL2 DR2 (37, 38)	Input Output			Data input/output of Part 2 shift register	Controller or KS0065
M (40)	Input	Alternated signal for LCD driver output		PART 1: FCS = VSS: latch clock (⌐¬), shift clock (⌐¬), M; FCS = VDD: shift clock (⌐¬), latch clock (⌐¬), $\overline{M}$ PART 2: FCS = VSS: shift clock (⌐¬), latch clock (⌐¬), $\overline{M}$; FCS = VDD: latch clock (⌐¬), shift clock (⌐¬), M Shift/latch clock of display data and polarity of M signal are changed by FCS signal By setting FCS to V_{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.	Controller
CL1 CL2 (32, 33)	Input	Data shift /latch clock			
FCS(43)	Input	Mode selection			
NC (39)				No connection pin	N C

MAXIMUM ABSOLUTE LIMIT (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	−0.3~+7.0	V
Driver supply voltage	V_{LCD}	V_{DD}−13.5~V_{DD}+0.3	V
Input voltage 1	V_{IN1}	−0.3~V_{DD}+0.3	V
Input voltage 2 (V_1-V_6)	V_{IN2}	V_{DD}+0.3~V_{EE}−0.3	V
Operating temperature	T_{opr}	−20~+75	°C
Storage temperature	T_{stg}	−55~+125	°C

* Voltage greater than above may damage to the circuit
* V_{EE}. connect a protection resistor (220Ω ±5%)

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD}=+5V±10%, V_{EE}=−5V±10%, V_{SS}=0V, T_a=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Supply current*	I_{DD}	f_{CL2}=400KHz	—	1	mA	—
	I_{EE}	f_{CL1}=1kHz	—	10	μA	
Input voltage	V_{IH}	—	0.7 V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2 DR1, DR2, SHL1, SHL2, M, FCS
	V_{IL}		0	0.3 V_{DD}		
Input leakage current	I_{IL}	V_{IN}=0-V_{DD}	−5	5	μA	
Output Voltage	V_{OH}	I_{OH}=−0.4mA	V_{DD}−0.4	—	V	DL1, DL2, DR1, DR2
	V_{OL}	I_{OL}=+0.4mA	—	0.4		
Voltage descending	V_{d1}	I_{ON}=0.1mA for one of SC1-SC40	—	1.1		V(V_1-V_6)-SC(SC1-SC40)
	V_{d2}	I_{ON}=0.05mA for each SC1-SC40	—	1.5		
Leakage current	I_{v1}	V_{IN}=V_{DD}~V_{EE} (Output SC1-SC40. floating)	−10	10	μA	V_1-V_5

AC CHARACTERISTICS (V_{DD}=+5V±10%, V_{EE}=−5V±10%, V_{SS}=0V, T_a=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	t_{CL}	—	—	400	KHz	CL2
Clock high level width	t_{CWH}	—	800	—	ns	CL1, CL2
Clock low level width	t_{CWL}	—	800	—		CL2
Clock set-up time	t_{LS}	from CL2 to CL1	500	—		CL1, CL2
	t_{TS}	from CL1 to CL2	500	—		
Clock rise/fall time	t_{CT}	—	—	200		
Data set-up time	t_{SU}	—	300	—		DL1, DL2, DR1, DR2, FLM
Data hold time	t_{DH}	—	300	—		
Data delay time	t_{PD}	CL=15pF	—	500		DL1, DL2, DR1, DR2

* Input/output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at "H" or "L".

TIMING CHARACTERISTICS

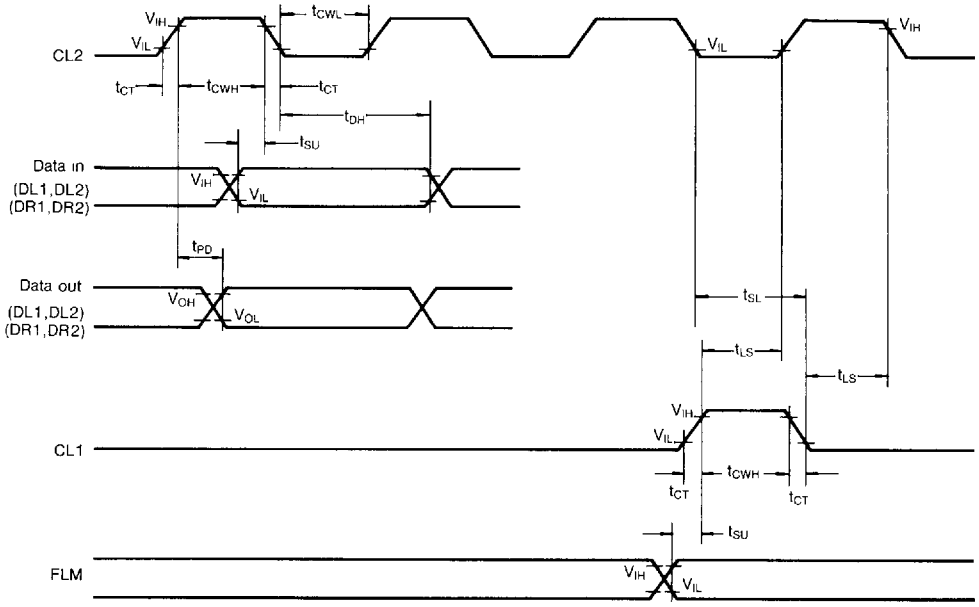

Fig 3 AC characteristics

FUNCTIONAL DESCRIPTION

1) To drive segment type

When the FCS is connected to VSS, KS0065 (SC1-SC40) is operated as segment driver (refer to fig 4)

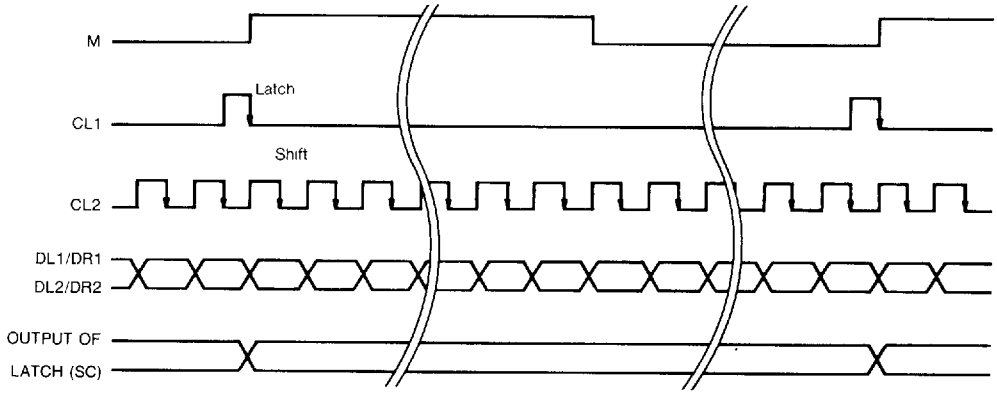

Fig 4 Segment Data Waveforms

2) To drive common type

When the FCS is connected to VDD, only part2 (SC21-SC40) of KS0065 is operated as common driver (refer to Fig 5)

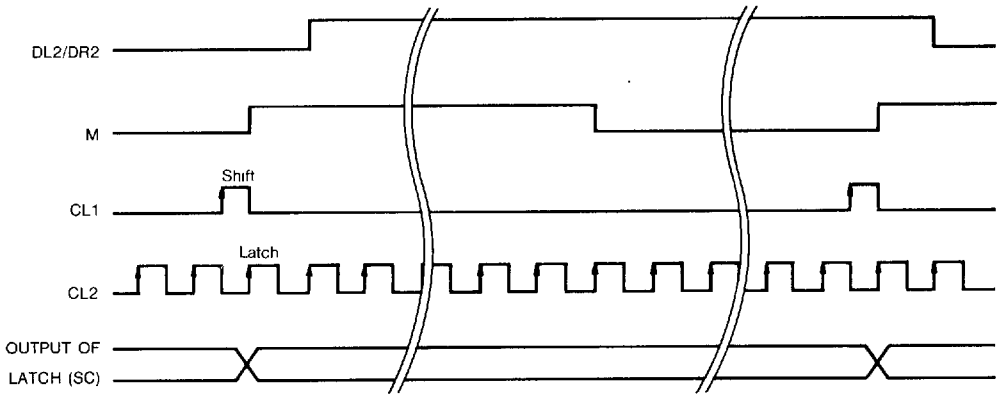

Fig 5 Common Data Waveforms

LCD OUTPUT WAVEFORMS

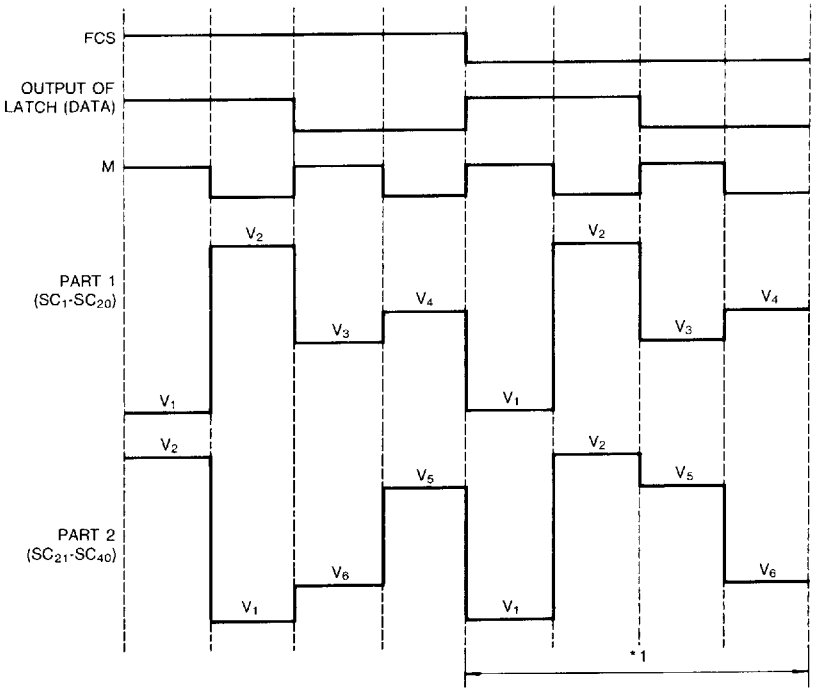

Fig 6 Output waveform

***1: To use for same function of part 1 and part 2, V3 and V5, V4 and V6 of power supply for LCD driver are short circuited respectively.**

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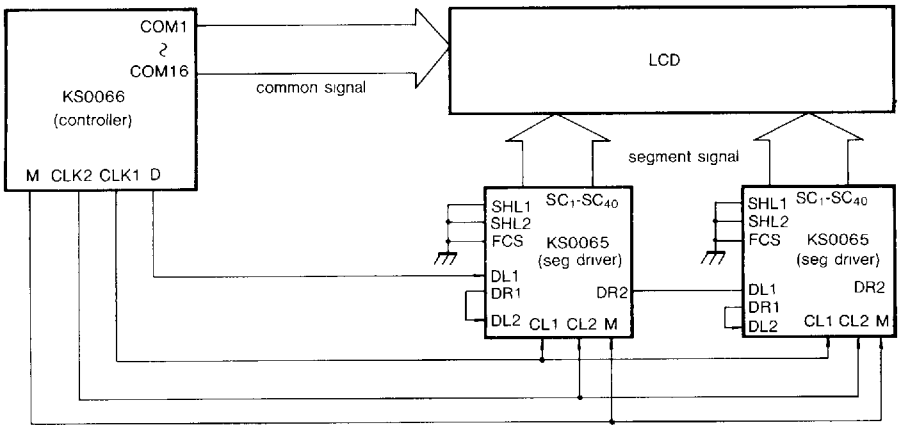
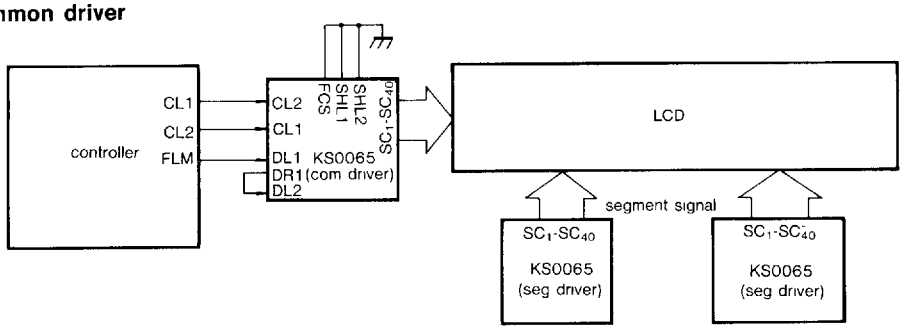
APPLICATION CIRCUIT

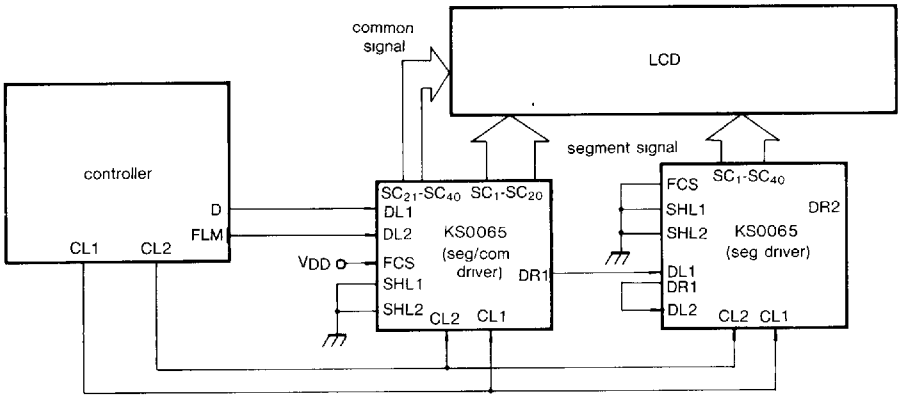
1) Segment driver



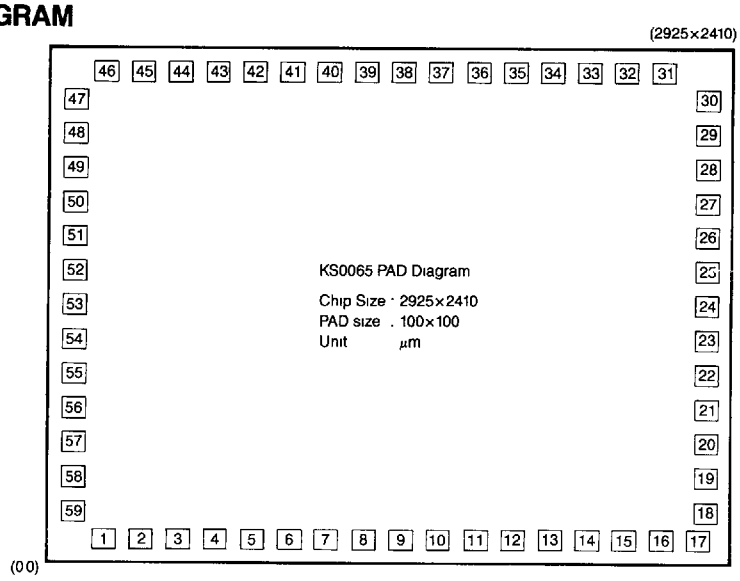
2) Common driver



3) Segment/common driver



PAD DIAGRAM



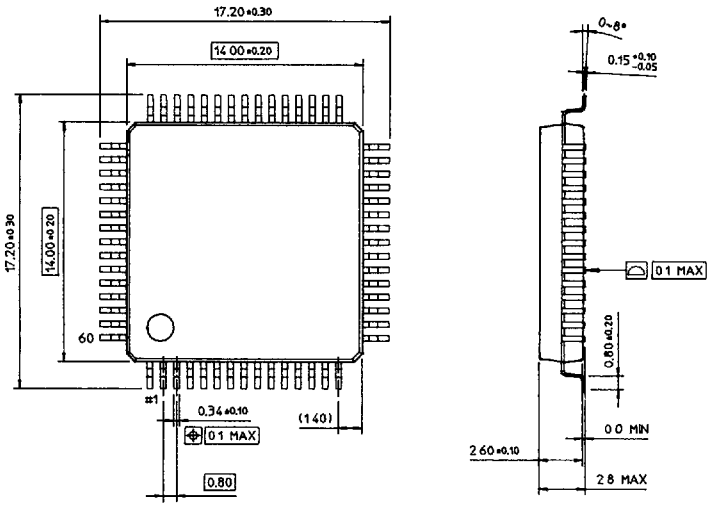
PAD LOCATION

No	name	coordinate		No	name	coordinate		No	name	coordinate	
		X	Y			X	Y			X	Y
1	V_{EE}	304.5	120	21	Y_{38}	2805	745	41	Y_{18}	1075	2290
2	CL_1	459.5	120	22	Y_{37}	2805	900	42	Y_{17}	920	2290
3	CL_2	614.5	120	23	Y_{36}	2805	1055	43	Y_{16}	765	2290
4	V_{SS}	789.5	120	24	Y_{35}	2805	1210	44	Y_{15}	610	2290
5	DL_1	924.5	120	25	Y_{30}	2805	1365	45	Y_{14}	455	2290
6	DR_1	1079.5	120	20	Y_{31}	2805	1520	46	Y_{13}	300	2290
7	DL_2	1234.5	120	27	Y_{32}	2805	1675	47	Y_{12}	120	2270
8	DR_2	1389.5	120	28	Y_{33}	2805	1830	48	Y_9	120	1915
9	M	1544.5	120	29	Y_{34}	2805	1985	49	Y_{10}	120	1760
10	SHL_1	1699.5	120	30	Y_{29}	2805	2140	50	Y_{11}	120	1605
11	SHL_2	1854.5	120	31	Y_{28}	2625	2290	51	Y_8	120	1450
12	FCS	2009.5	120	32	Y_{27}	2470	2290	52	Y_7	120	1295
13	V_1	2164.5	120	33	Y_{26}	2215	2290	53	V_{DD}	120	1140
14	V_2	2319.5	120	34	Y_{25}	2160	2290	54	Y_6	120	985
15	V_3	2474.5	120	35	Y_{24}	2005	2290	55	Y_5	120	830
16	V_4	2629.5	120	36	Y_{23}	1850	2290	56	Y_4	120	675
17	V_5	2784.5	120	37	Y_{22}	1695	2290	57	Y_3	120	520
18	V_6	2805	280	38	Y_{21}	1540	2290	58	Y_2	120	365
19	Y_{40}	2805	435	39	Y_{20}	1385	2290	59	Y_1	120	210
20	Y_{39}	2805	590	40	Y_{19}	1230	2290				

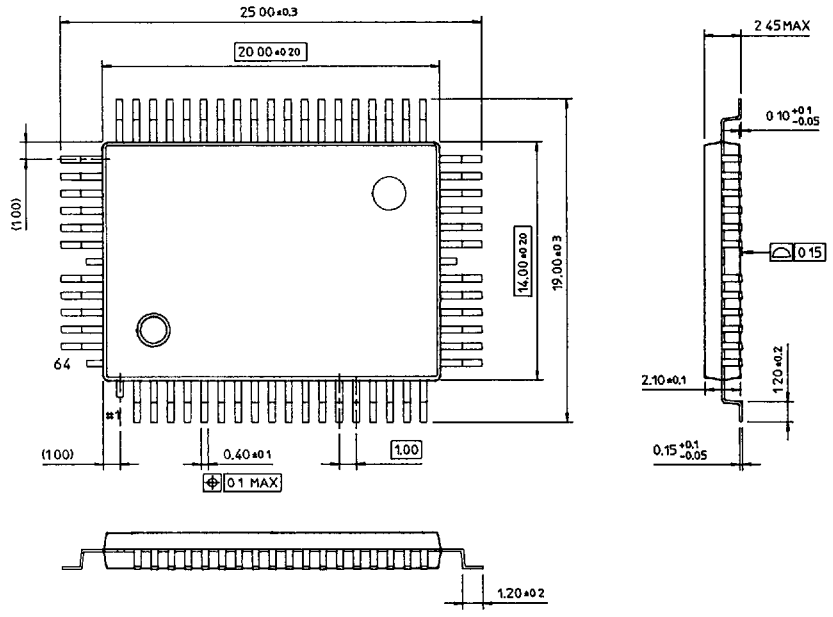
PACKAGE DIMENSIONS

Dimensions in Milimeters

60-QFP-1414A



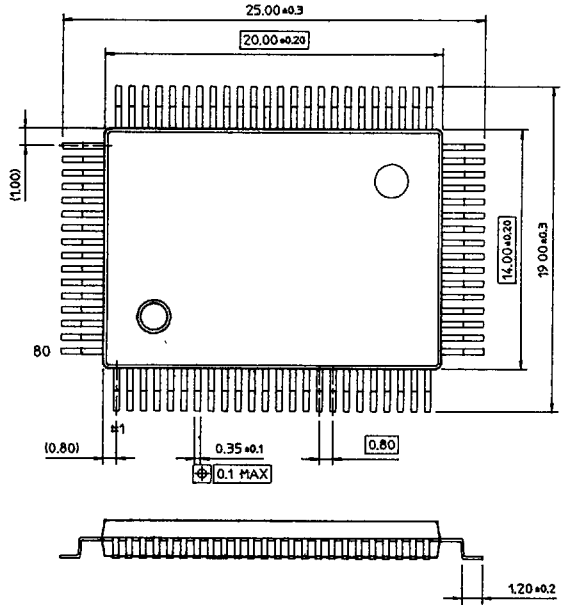
64-QFP-1420D



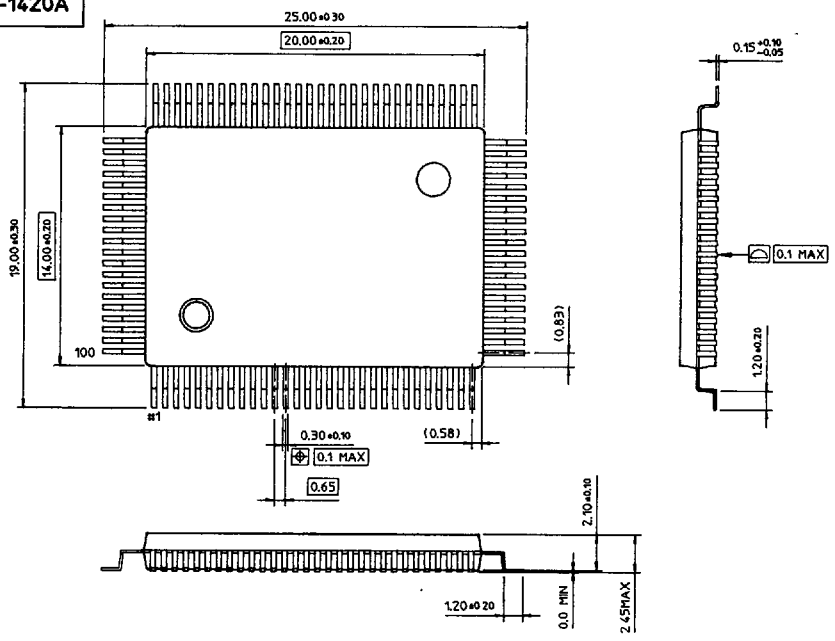
PACKAGE DIMENSIONS

Dimensions in Milimeters

80-QFP-1420A



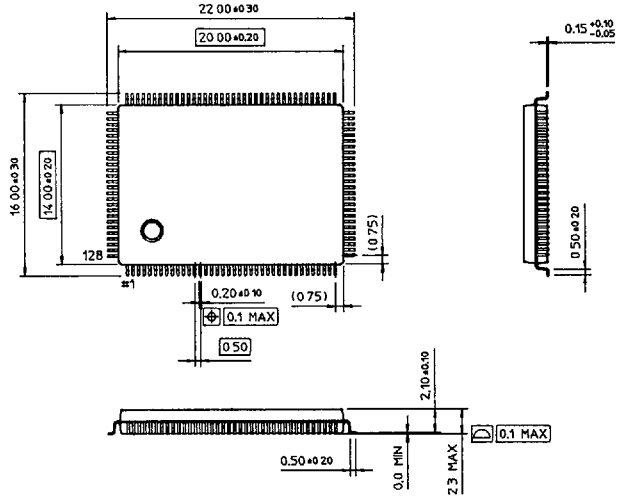
100-QFP-1420A



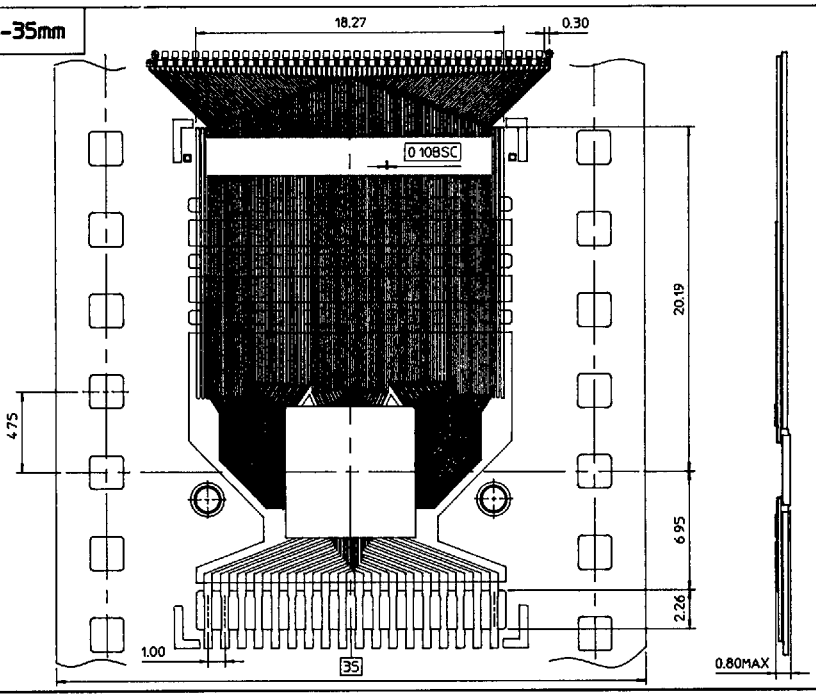
PACKAGE DIMENSIONS

Dimensions in Milimeters

128-QFP-1420



98-TAB-35mm



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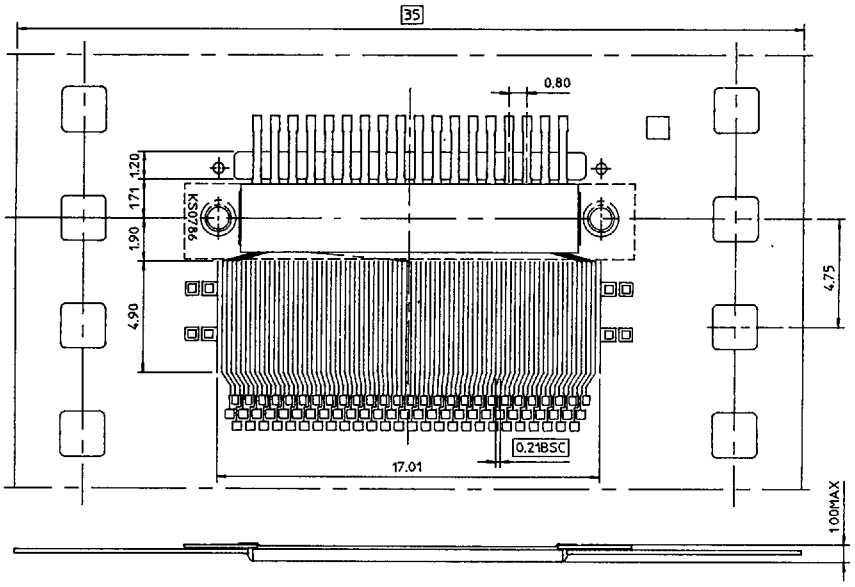
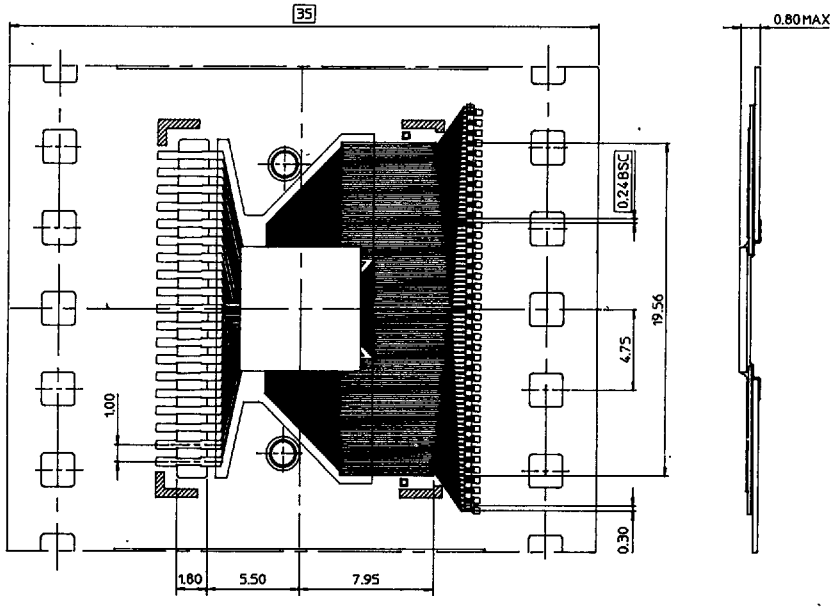
PACKAGE DIMENSIONS

Dimensions in Milimeters

98-STAB-35mm



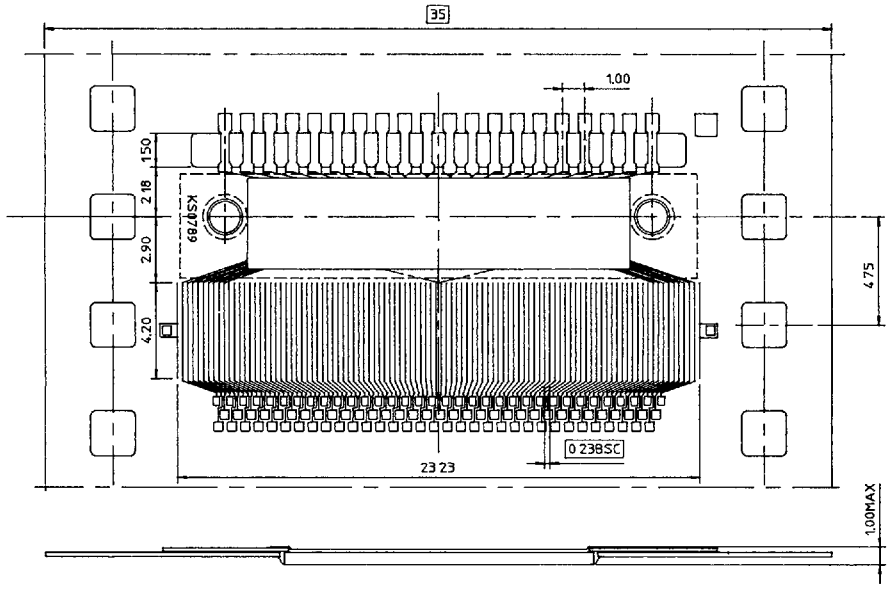
99-TAB-35mm



PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm



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