Military & Space Products

Advance Information

64 X 64 CROSSBAR

HX9100

FEATURES

- Fabricated with RICMOS™ IV Silicon on Insulator (SOI)0.8 µm Process (L_{eff} = 0.65 µm)
- CMOS Compatible I/O
- Single 5V ± 10% Power Supply
- Full Complement of Screening Flows
- Supports System Speeds Beyond 100 MHz
- Skew <2 ns
- Total Dose Hardness of ≥1x10^6 rad(SiO_2)
- Dose Rate Upset Hardness ≥1x10^{11} rad(Si)/sec (5V)
- Dose Rate Survivability ≥1x10^{12} rad(Si)/sec
- SEU Immunity ≤1x10^{-11} Errors/Bit-Day
- Neutron Fluence Hardness to 1x10^{14}/cm^2
- No Latchup

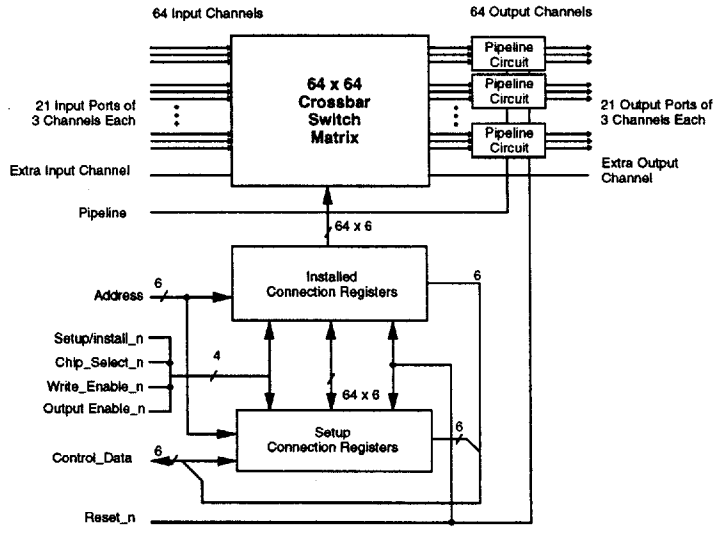
GENERAL DESCRIPTION

The HX9100 is a radiation hardened 64 x 64 crossbar switch that allows connecting any of 64 output channels to any of 64 input channels. Switching is controled by a set of Connection Registers whose value can be set or read out by using the control lines.

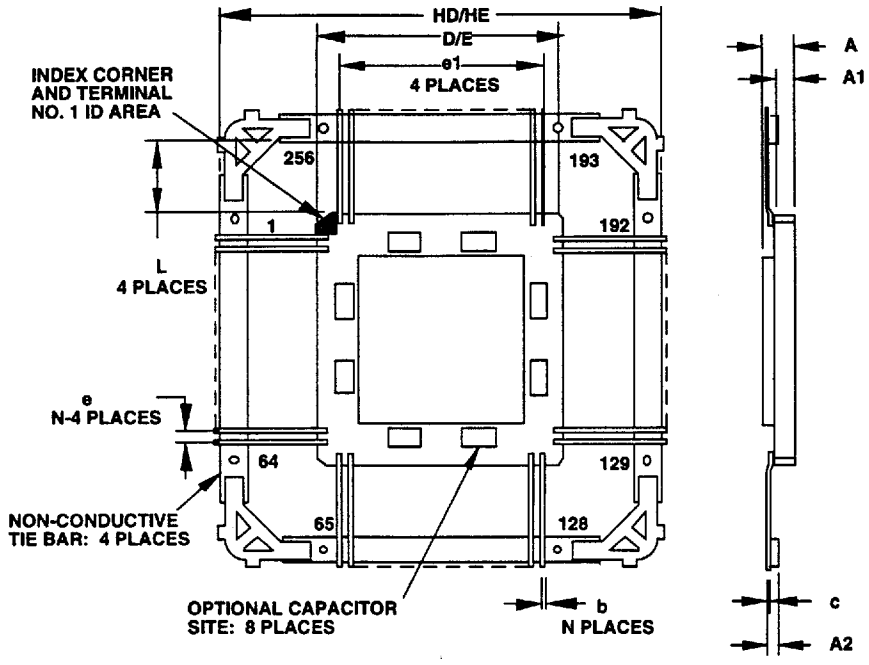
There is an installed Connection Register for each output channel which determines which input channel is connected through the crossbar switch matrix to that output channel. There is also a Setup Connection Register for each output channel that may be used to setup the next connection to be made for that simultaneously into the Installed Connection Registers into change the routing through the crossbar switch matrix. This two-stage design allows a number of Setup Connection Registers to be changed sequentially and then moved simultaneously to the Installed Connection Registers so all of the new connections are made at the same time. If no change has been made to the Setup Connection Register for a channel, there is no change in the connection of that output channel when the Setup Connection Register contents are transferred to the Installed Connection Registers.

Data_In and Data_Out channels are each divided into a set of 21 three wire ports, each port consisting of a Clock channel, a Data channel and a Sync channel. One designated "extra" input channel and output channel are not considered part of any port. There is also a set of 21 two-bit Pipeline Registers, one for each output port, which optionally allows resynchronizing the Data and Sync channels of a port to the Clock channel for that port. When pipelining is activated, using the Pipeline control line, the contents of the Data and Sync lines are latched in the Pipeline Register on the negative-going transition of the Clock channel for that port. When pipelining is not activated, the Clock, Data and Sync channels are passed directly to the Data_Out lines without being latched.

Functional Diagram



256-LEAD FLAT PACK PACKAGE



Dimensions in inches	min	max
A	0.130	0.160
A1	-	0.130
A2	0.024	0.040
b	0.005	0.009
c	0.004	0.008
D/E	1.445	1.455
e	0.020 BSC	
e1	1.260 BSC	
HD/HE	2.365	2.395
L	0.325	-
N	256	

ORDERING INFORMATION (1)

H	X	9100	S	H
SOURCE	**PROCESS**	**PART NUMBER**	**SCREEN LEVEL**	**TOTAL DOSE HARDNESS**
H=HONEYWELL	X=SOI		V=QML Class V	F=3x10^5 rad(SiO$_2$)
			Q=QML Class Q	H=1x10^6 rad(SiO$_2$)
			S=Level S	N=No Level Guaranteed
			B=Level B	
			E=Engr Device (2)	

(1) Orders may be faxed to 612-954-2051. Please contact our Customer Logistics Department at 612-954-2888 for further information.

(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed.

Contact Factory with other needs.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

Honeywell

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