

MC2045-2Y

Postamplifier/Quantizer for Applications to 200 Mbps Data Sheet

Preliminary Information

- Features
- Description
- Applications
- Pin Descriptions
- Measurement Tables
- Functional Description

Postamplifier/Quantizer for Applications to 200 Mbps

TABLE OF CONTENTS

Features	3
Applications	3
Connections	3
Description	3
Table 1 Ordering Information	3
Top Level Diagram	3
Table 2 Pin Description	4
Table 3 Absolute Maximum Ratings	5
Table 4 Recommended Operating Conditions	5
Table 5 DC Characteristics	5
Table 6 AC Characteristics	6
Typical Performance Curves	7
Assert Deassert Level	7
Functional Block Diagram	8
Functional Description	8
Data Input	8
DC Offset Compensation	8
Signal Level Detector	8
Setting Signal Detect Level	8
Typical Applications Circuit	9
Applications Information	9
JAM Function	9
PECL Termination	9
Table 7 Termination Resistor Values	10
Power supply de-coupling & optimizing sensitivity	11
Differences between die and packaged parts	11
Bare Die Information	12
Table 8 Pad Centers	12
BCC++16L Package Outline	13
TSSOP20 Package Information	14
SOIC16 Package Information	15
QSOP16 Package Information	16
Package Dimensions	17
Table 9 TSSOP20 Dimensions	17
Table 10 SOIC16 Dimensions	17
Table 11 QSOP16 Dimensions	17
Disclaimer	18
World Wide Sales Offices	19

Preliminary Information

Postamplifier/Quantizer for Applications to 200 Mbps

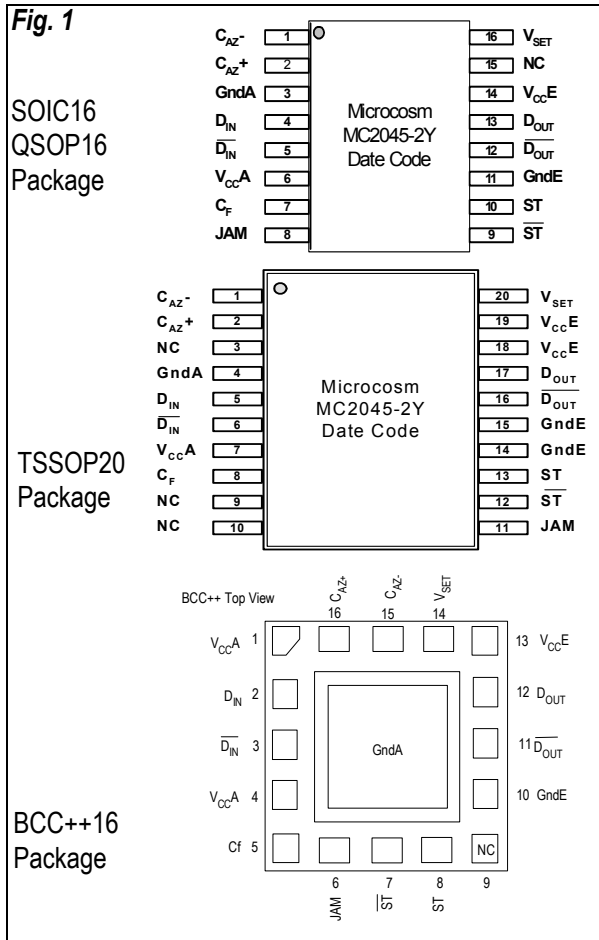
FEATURES

- ❑ Low-cost IC, fabricated in advanced sub-micron BiCMOS process
- ❑ 800 μ V input sensitivity
- ❑ Wide range programmable input-signal level detect
- ❑ Fully differential design
- ❑ Supports 3.3 V and 5 V supplies
- ❑ Available in TSSOP20, SOIC16, QSOP16 and BCC++16L package as well as die form
- ❑ Complimentary PECL data & signal detect logic outputs

APPLICATIONS

- ❑ SDH/SONET/ATM
- ❑ Fast Ethernet
- ❑ FDDI
- ❑ ESCON
- ❑ FTTH and Media Converters

CONNECTIONS



DESCRIPTION

The MC2045-2Y is an integrated, high gain limiting amplifier intended for fibre optic communication to 200 Mbps. Normally placed following the photodetector & transimpedance amplifier, the post-amplifier provides the necessary gain to give PECL compatible logic outputs.

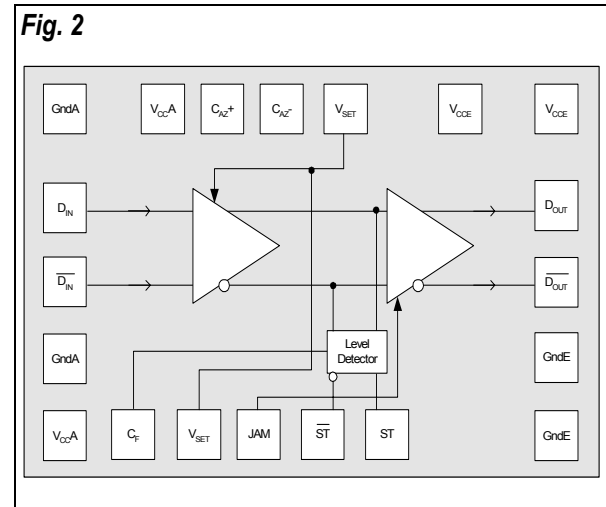
The MC2045-2Y also includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. The signal detect function has typically 2 dB (optical) of hysteresis which prevents chatter at low input levels.

A JAM function, which turns off the output when no signal is present, is provided by externally connecting the \overline{ST} output to the JAM input.

TABLE 1 ORDERING INFORMATION

Part Number	Pin Package
MC2045-2YDIEWP	Waffle pack
MC2045-2YWAFER	Expanded wafer on a grip ring
MC2045-2YS16	SOIC16
MC2045-2YQ16	QSOP16
MC2045-2YT20	TSSOP20
MC2045-2Y-06-T	BCC++16L
M02045-2-BEVM	BCC16 evaluation board
M02045-2-QEVM	QSOP evaluation board
M02045-P6EVM	QSOP Eval board inc. MC2006 TIA
M02045-P7EVM	QSOP Eval board inc. MC2007 TIA

TOP LEVEL DIAGRAM



Preliminary Information

Postamplifier/Quantizer for Applications to 200 Mbps

TABLE 2 _____ PIN DESCRIPTION

Pin Name	QSOP16 SOIC16 Pin No.	TSSOP20 Pin No.	BCC++16L Pin No	Function
C _{AZ} ⁻	1	1	15	Auto-zero capacitor pin. Connect C _{AZ} between this pin and C _{AZ} ⁺
C _{AZ} ⁺	2	2	16	Auto-zero capacitor pin. Connect C _{AZ} between this pin and C _{AZ} ⁻
GNDA	3	4	-	Analog section ground pin. Connect to most negative supply. Must be at the same potential as GNDE pin
D _{IN}	4	5	2	Differential data input
\overline{D}_{IN}	5	6	3	Inverse differential data input
V _{CCA}	6	7	1, 4	Analog section power pin. Connect to most positive supply. Must be at the same potential as V _{CCE} pin
C _F	7	8	5	Level-detect filter capacitor pin. Connect a capacitor between this pin and V _{CCA}
JAM	8	11	6	PECL compatible input controlling output buffers (\overline{D}_{OUT} and D _{OUT} pins). On chip pull down defaults to low. Can be driven from CMOS.
\overline{ST}	9	12	7	Logical inverse of ST pin. Maybe connected to JAM pin to enable automatic squelch function to operate PECL output
ST	10	13	8	Input signal level status. This PECL output is LOW when the input signal is below the threshold set by the users
GNDE	11	14, 15	10	Digital section ground pin, Connect to the most negative supply. Must be the same potential as GNDA pin
\overline{D}_{OUT}	12	16	11	Differential data output. Logical inverse of D _{OUT} pin. JAM high forces \overline{D}_{OUT} High
D _{OUT}	13	17	12	Differential data output. PECL compatible differential data output. JAM high forces D _{OUT} LOW
V _{CCE}	14	18, 19	13	Digital output section power pin. Connect the most positive supply. Must be at same potential as V _{CCA} pin.
NC	15	3, 9, 10	9	Not connected
V _{SET}	16	20	14	Input threshold-level setting circuit. Connect to GND via a resistor

Note :

Pin 17 (center pin) on the BCC++16 package should be connected to GndA.

Preliminary Information

Postamplifier/Quantizer for Applications to 200 Mbps

TABLE 3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V _{CC}	Power supply (V _{CC} -GND)	6	V
T _A	Operating ambient	-40 to +85	°C
T _{STG}	Storage temperature	-65 to +150	°C

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

TABLE 4 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Units
V _{CC}	Power supply (V _{CC} -GND)	3.0 to 5.5	V
T _A	Operating ambient	-40 to +85	°C

TABLE 5 DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{OS}	Effective input offset voltage	-	1	-	mV
V _{TH}	Input level detect programmability	2	-	20	mVpp
HYS	Level detect hysteresis (optical)	1.8	2.0	3.0	dB
I _{INJ}	JAM input current HIGH		380		µA
I _{CC}	Supply current (outputs un-loaded) ⁽²⁾	-	-	20	mA
V _{OH}	PECL ⁽¹⁾ output HIGH	V _{CC} -1.025	-	V _{CC} -0.880	V
V _{OL}	PECL ⁽¹⁾ output LOW	V _{CC} -1.810	-	V _{CC} -1.620	V

(V_{CC} = +3.3V ± 10%, T_A = -40°C to +85°C, unless otherwise noted)

1) Load is 50 Ω to V_{CC} -2 V.

2) V_{CC} = +3.3 V or +5 V.

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TABLE 6 _____ AC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
BW	Bandwidth (where gain = 60dB)	100	250	-	MHz
R _{IN}	Input resistance	-	4.5	-	kΩ
C _{IN}	Input capacitance	-	-	2	pF
t _{PWD}	Pulse width distortion	-	-	0.3	ns
t _R ,t _F	Data output rise/fall times (20-80%)	-	1.0	2.0	ns
R _F	Signal level detect filter resistance	10	25	41	kΩ
T _{LD}	Signal level detect time constant Assert level Deassert level	0.5	1 50	20	μs
V _{IN}	Input signal voltage Single ended: Differential :	0.8 1.6	- -	400 800	mVpp
V _N	Input RMS noise in 100 MHz	-	-	85	μV

(V_{CC}= +3.3 V ±10%, T_A = -40°C to +85°C, unless otherwise noted)

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TYPICAL PERFORMANCE CURVES

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Fig. 3

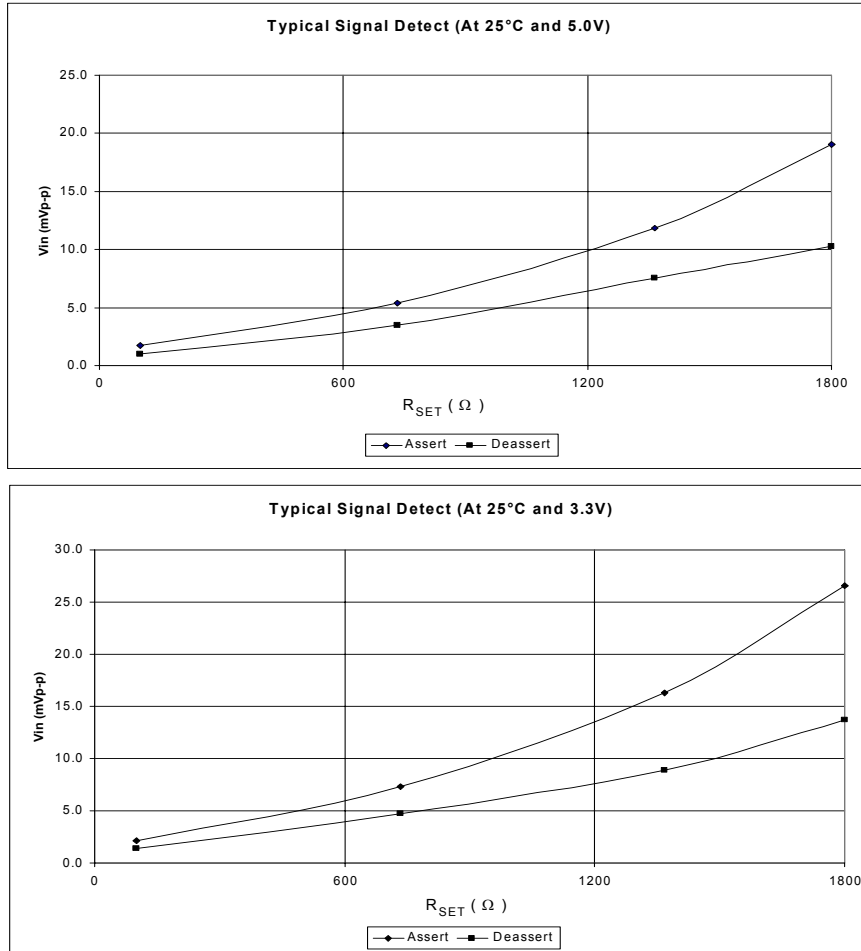
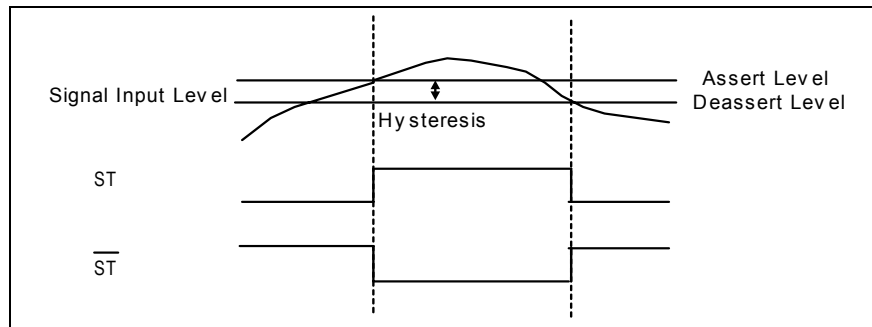


Fig. 3a



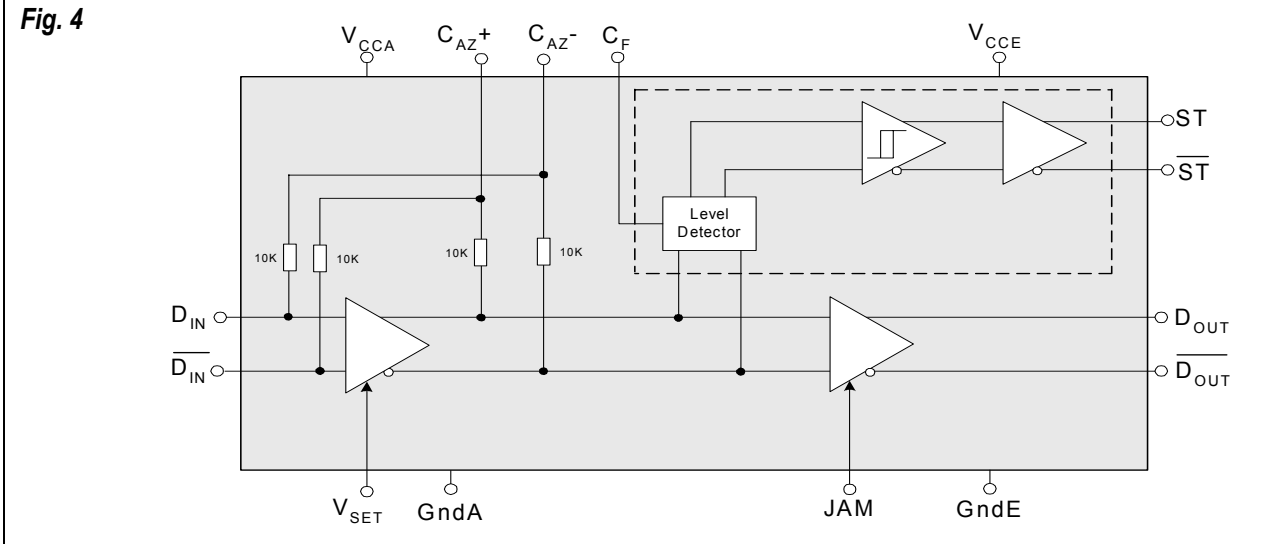
ASSERT DEASSERT LEVEL

The Fig. 3a shows the operation of the signal detect function as the signal level varies. The top line indicates the assert level, the bottom the deassert level. The difference between the two levels is the hysteresis. When the signal level goes above the assert level the ST output

switches high (\overline{ST} switches low). When the signal level falls below the deassert level, ST output switches low (\overline{ST} switches high).

Postamplifier/Quantizer for Applications to 200 Mbps

FUNCTIONAL BLOCK DIAGRAM



Preliminary Information

FUNCTIONAL DESCRIPTION

Data Input

The Data Input pins are internally DC-biased at approximately $V_{CC} - 1V$. The MC2045-2Y signals are AC coupled, using external capacitors. These capacitors must be large enough to pass the lowest frequencies of interest (consecutive '1's or '0's) considering the input resistance. For example, at 155 Mbps SONET, there can be up to a maximum of 72 consecutive '1' s, which is 465 ns.

To minimise the data dependant jitter, the low frequency cut-off needs to be lower by a factor of 10. However, it is better to set it a further decade lower, due to the interaction of the time constants for the input stage and the DC restore circuitry. For example setting C1, C2 (Fig. 5) to 10 nF will give a typical -3 dB point of approximately 3.5 KHz.

DC Offset Compensation

Internal feedback is included to remove the effects of DC offsets and acts as a DC auto zero circuit. An external capacitor (C_{AZ}) acting with the internal circuit feedback resistors (typ 10 k Ω) ensures that the feedback is effective only at frequencies below the lowest frequency of interest. C_{AZ} is normally set to 10 nF.

Signal Level Detector

The gain of the first stage is determined by R_{SET} . This amplification sets the level of input at which the status thresholds operate. The data is then rectified and low-pass filtered before being compared with a reference voltage. The low-pass filter is formed by C_F (Fig. 5) and R_F (on chip resistor).

With C_F equal to 10 nF the time constant is nominally 2 μ s, avoiding false triggering due to variation in edge density of data.

Setting Signal Detect Level

R_{SET} is chosen using the graphs in Fig. 3 to determine the input signal level at which ST goes high (Assert). The value is dependant on supply voltage and should be chosen for 3.3 V or 5 V operation. If 3.3 V and 5 V operation are to be supported inter-changeably set RSET based on the 3.3 V graphs.

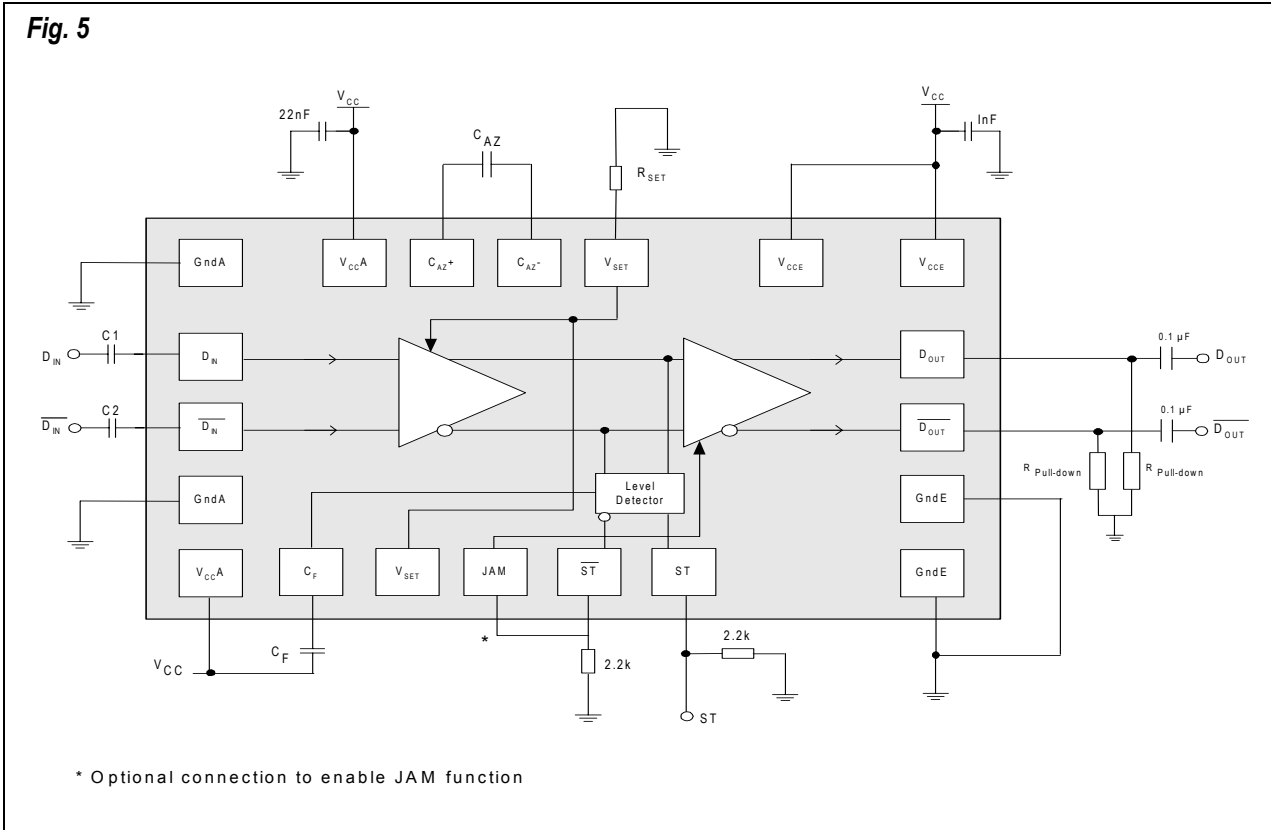
The comparator following the level detector has the equivalent of 2 dB (typ.) of optical hysteresis, and this determines the deassert level (ST goes LOW).

If the level detect function is not required connect V_{SET} to GndA (maximum gain).

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TYPICAL APPLICATIONS CIRCUIT

Preliminary Information



APPLICATIONS INFORMATION

JAM Function

The JAM function, sets the data output to a fixed state when no valid signal is present at the input. This is implemented by externally connecting the ST output to the JAM input.

This is normally used to allow data to propagate only when the signal is above the users' Bit-Error-Rate (BER) requirement. It therefore stops the data outputs toggling due to noise when no signal is present.

PECL Termination

The outputs of the MC2045-2Y are PECL compatible and any standard AC or DC-coupling termination technique can be used. Fig. 6 and 7 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption,

no susceptibility to DC drift and compatibility with non PECL interfaces. Pull-down resistors ($R_{pull-down}$) provide a DC path for the emitter follower outputs to Gnd, keeping the ECL output transistors in their active region. Values for $R_{pull-down}$, at different supply voltages, can be found in table 7.

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Fig. 7 shows the circuit configuration and table 7 the resistor values.

Alternatively, if available, terminating to $V_{CC} - 2V$ as shown in Fig. 8 (page 11) has the advantage that the resistance value is the same for 3.3 V and 5 V operation and it also has performance advantages at high data rates.

When calculating ZT the impedance of the transmission line (Z) must be taken into consideration.

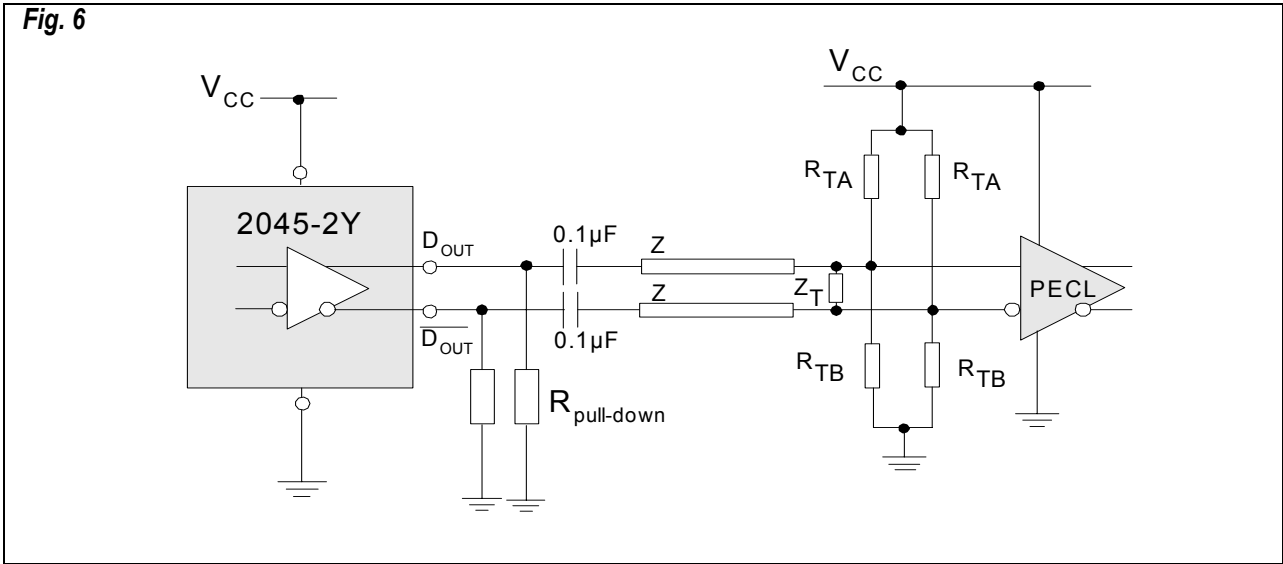
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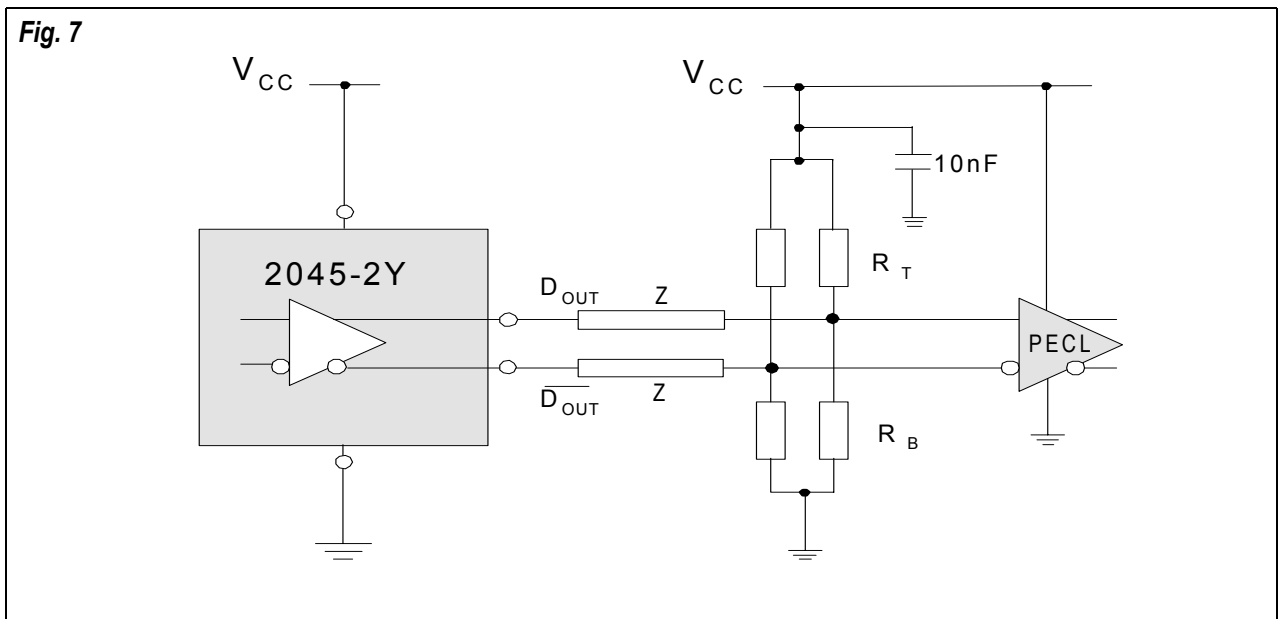
TABLE 7 TERMINATION RESISTOR VALUES

Supply	Output Impedance	R _{Pull-down}	Z _T	R _{TA} /R _{TB}	R _T /R _B
5 V	50 Ω	270 Ω	100 Ω	2k7 Ω/7k8 Ω	82 Ω/130 Ω
3.3 V	50 Ω	150 Ω	100 Ω	2k7 Ω/4k3 Ω	130 Ω/82 Ω

AC-COUPLED PECL TERMINATION

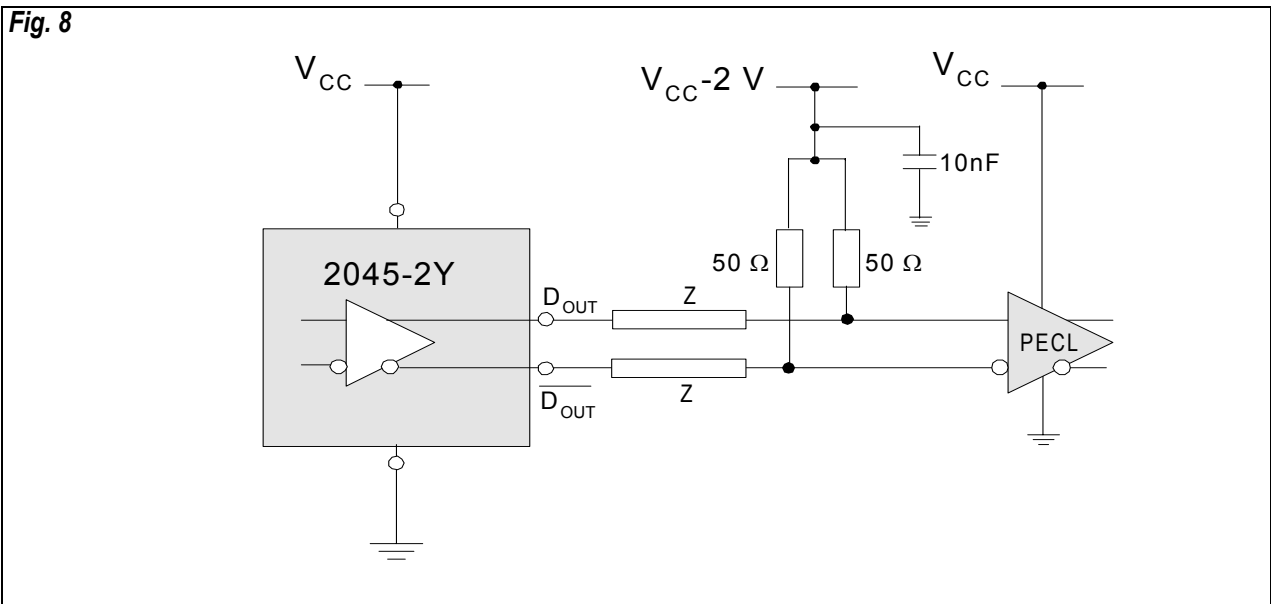


DC-COUPLED PECL TERMINATION



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Fig. 8



Preliminary Information

Power supply de-coupling & optimizing sensitivity

In most applications the MC2045-2Y will give adequate performance without ferrite beads. In applications where maximum sensitivity is required V_{CC}A and GNDA may be connected to their respective power rails via a ferrite suppressor, such as a Murata BLM31A601SPT.

Capacitors should be chosen with low effective series resistance, low dissipation factor and high Q. NPO or COG temperature characteristics are preferred because they provide more reliable performance over a wide range of environmental conditions.

Small surface mount packages are recommended since they exhibit less parasitic inductance which can lower the overall effectiveness of the bypass capacitor at high frequencies. Filter capacitors should be placed close to power and ground pins to minimise noise coupling.

Differences between die and packaged parts

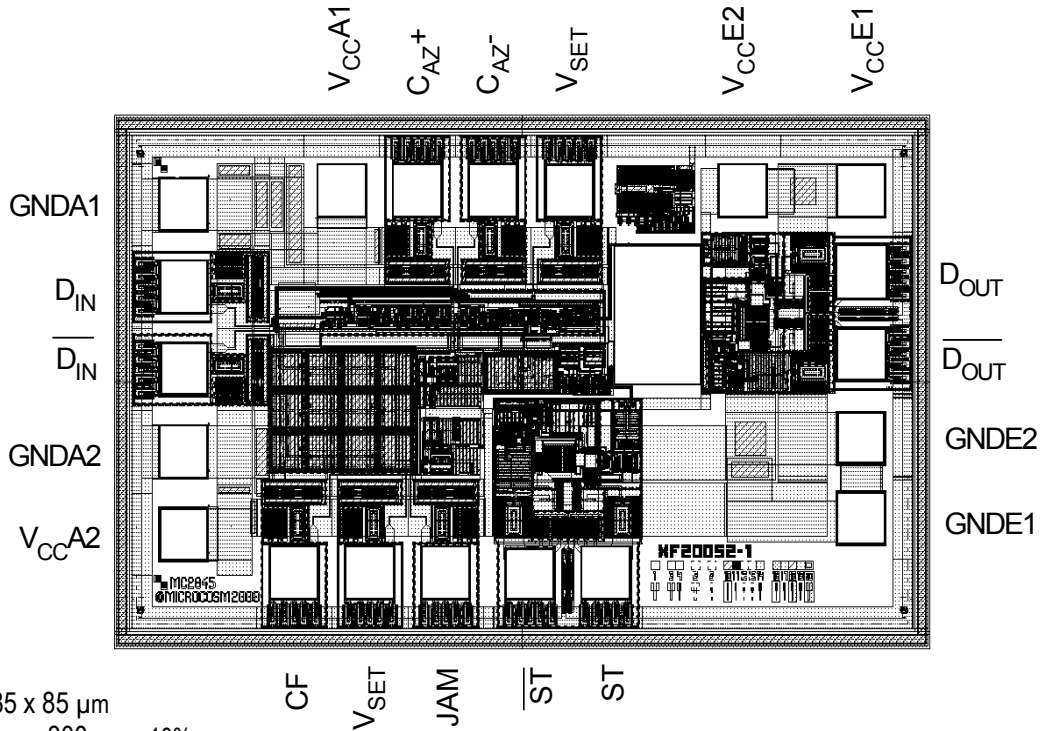
The die has two V_{SET} pads. Connect one or other, not both.

There are 2 sets of V_{CC}A and GNDA on the left of the die. Although two pairs are provided only one pair need be connected. On the TSSOP package, pairs of V_{CC}E and GNDE pins are connected.

Postamplifier/Quantizer for Applications to 200 Mbps

BARE DIE INFORMATION

Fig. 9



Pad size : 85 x 85 μm
Die thickness : 300 $\mu\text{m} \pm 10\%$

Preliminary Information

TABLE 8 PAD CENTERS

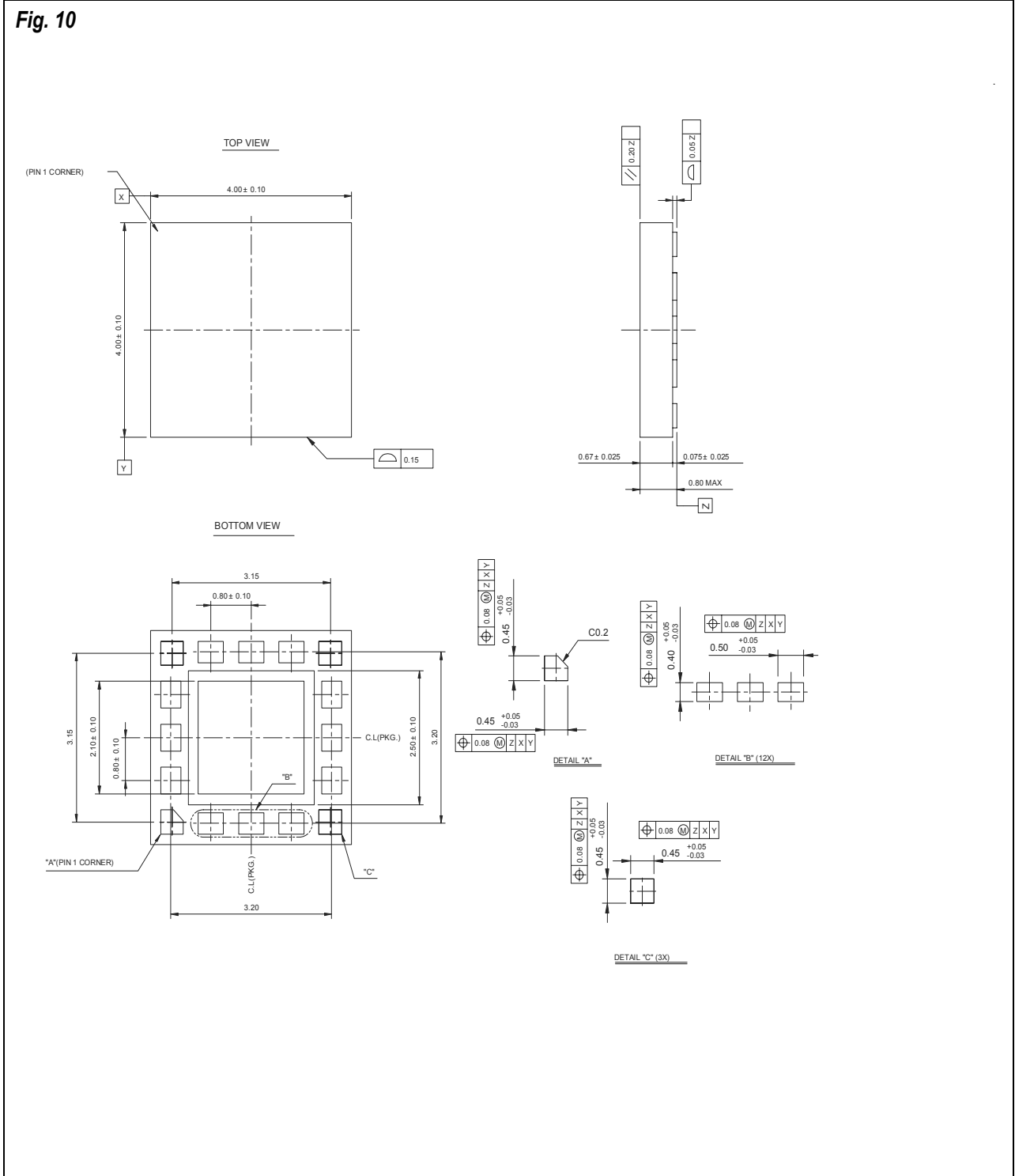
Description	X	Y	Description	X	Y
C_{AZ^-}	-56.8	347.5	JAM	-152.2	-347.5
C_{AZ^+}	-207	347.5	\overline{ST}	15.8	-347.5
$V_{CC A1}$	-356.9	347.5	ST	166	-347.5
GNDA1	-670	322.6	GNDE1	670	-248
D_{IN}	-670	172.6	GNDE2	670	-103
$\overline{D_{IN}}$	-670	22.4	$\overline{D_{OUT}}$	670	50.1
GNDA2	-670	-127.6	D_{OUT}	670	200.3
$V_{CC A2}$	-670	-277.5	$V_{CC E1}$	670	347.5
C_F	-451.4	-347.5	$V_{CC E2}$	436.9	347.5
V_{SET2}	-301.3	-347.5	V_{SET}	93.2	347.5

Note: Pad coordinates are in μm , and are measured from the center of the die to the center of the pad.

Postamplifier/Quantizer for Applications to 200 Mbps

BCC++16L PACKAGE OUTLINE

Fig. 10



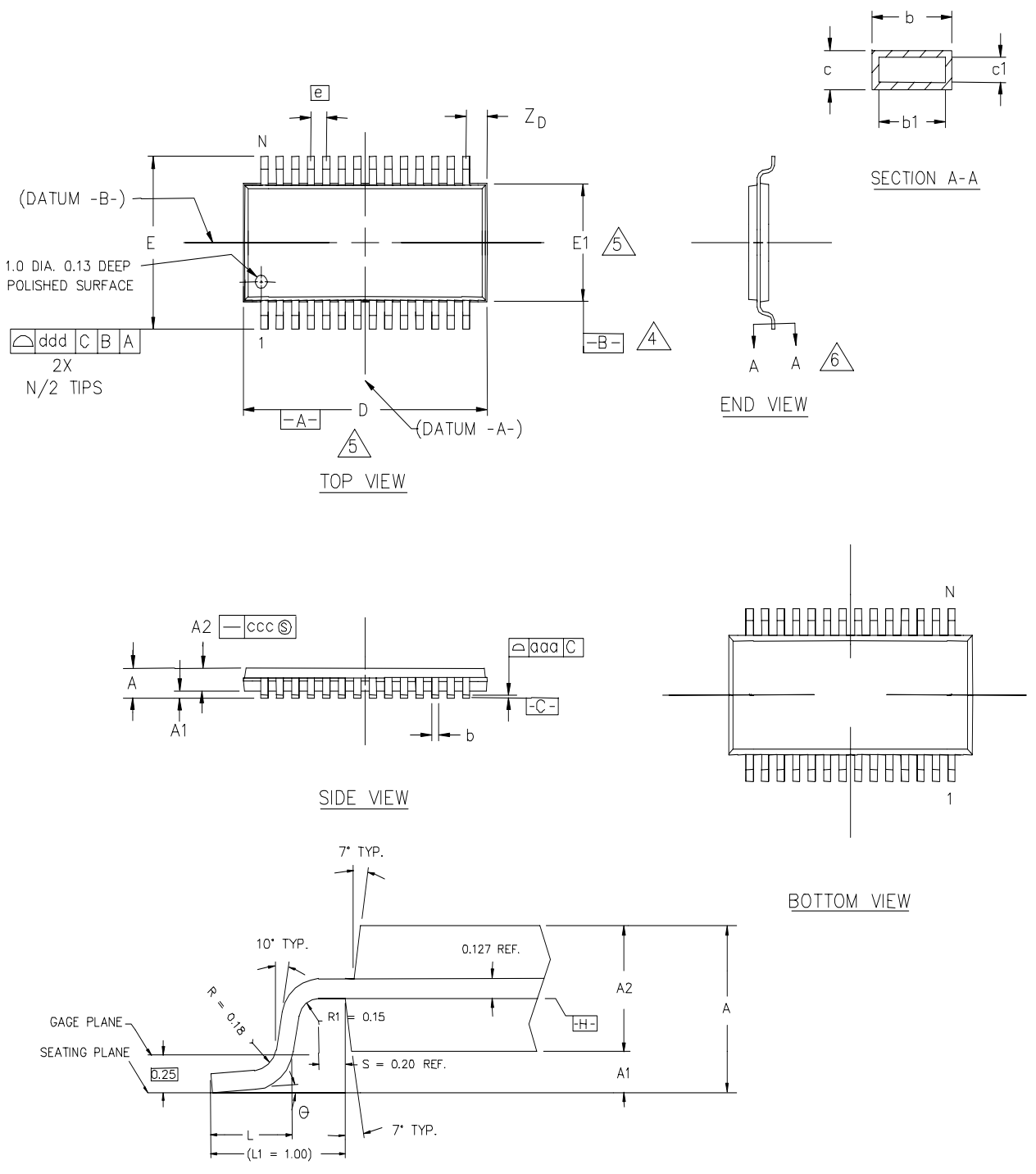
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TSSOP20 PACKAGE INFORMATION

Preliminary Information

Fig.11



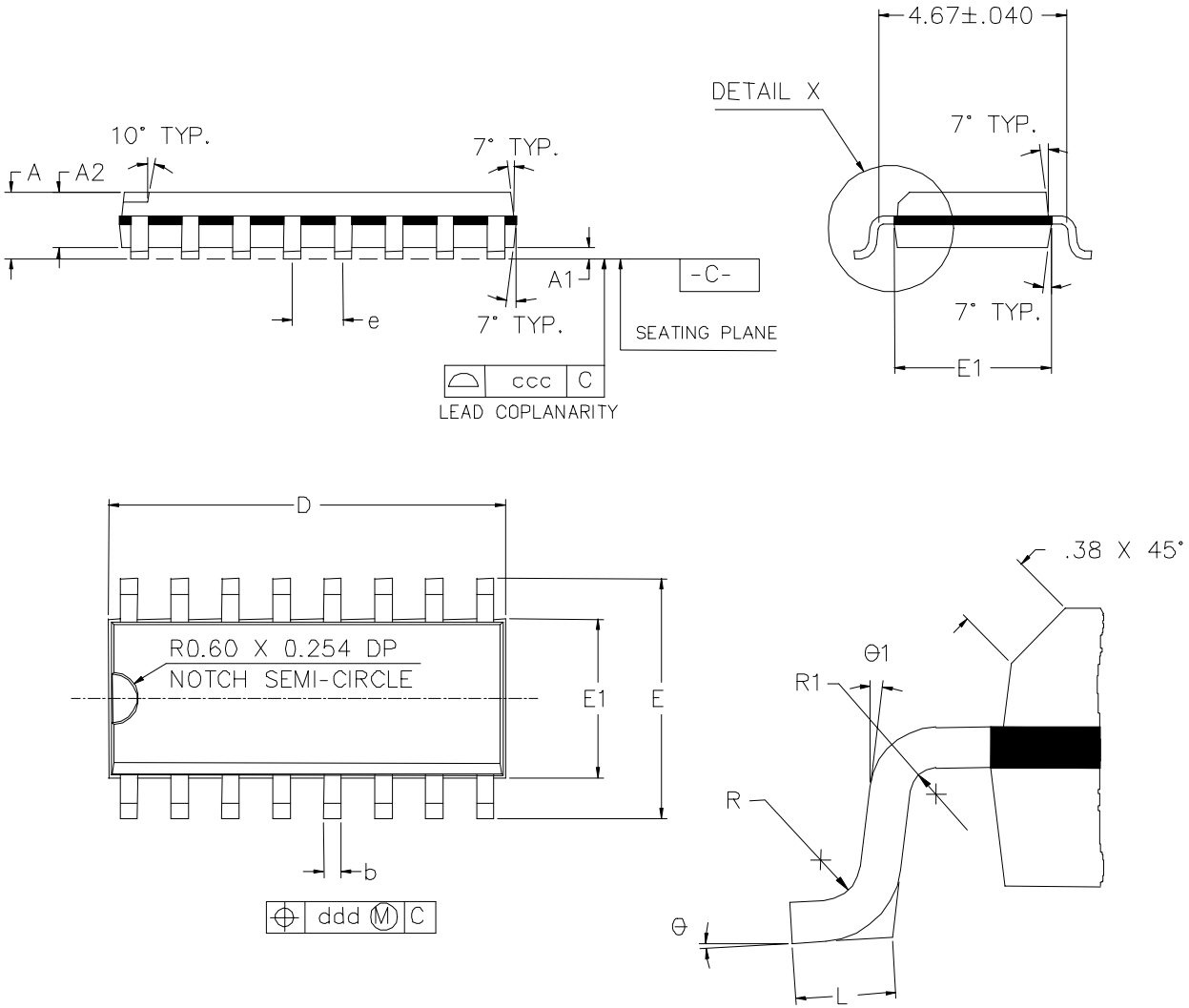
Note: Please see dimensions on page 17, table 9.

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SOIC16 PACKAGE INFORMATION

Preliminary Information

Fig. 12

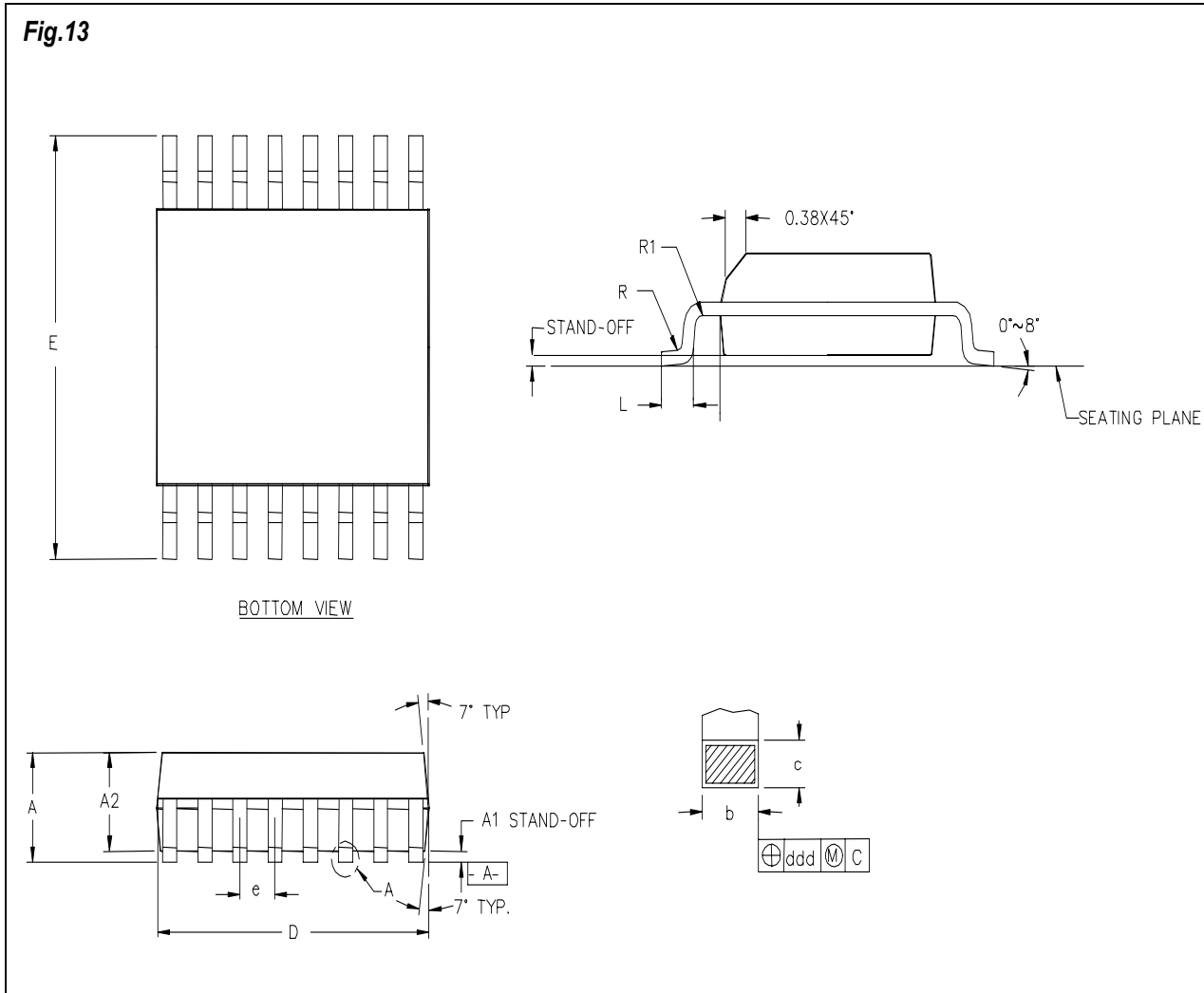


Note: Please see dimensions on page 17, table 10.

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QSOP16 PACKAGE INFORMATION

Preliminary Information



Note: Please see dimensions on page 17, table 11.

Postamplifier/Quantizer for Applications to 200 Mbps

PACKAGE DIMENSIONS

TABLE 9 TSSOP20 DIMENSIONS

Dims.	Tols/leads	TSSOP20L
A	MAX	1.20
A1		0.5MIN/.10MAX.
A2	NOM	.90
D	±.05	6.50
E	±.10	6.40
E1	±.10	4.40
L	+.15/-.10	.60
L1	REF.	1.00
Zp	REF.	.325
e	BASIC	.65
b	±.05	.22
c		.13MIN/.20MAX
e	±4°	4°
aaa	MAX.	.10
bbb	MAX.	.10
ccc	MAX	.05
ddd	MAX.	.20

TABLE 11 QSOP16 DIMENSIONS

Dims.	Tols/N	QSOP16
A	MAX.	1.60
A1	±.05	0.1
A2	±.10	1.40
D	±.10	4.9
E	±.20	6.00
E1	±.10	3.90
L	±.05	0.6
ccc	MAX.	0.10
ddd	MAX.	0.10
e	BASIC	0.65
b	±.05	0.25
c	±.05	.2 Min. .24 Max.
R	±.05	0.20
R1	Min.	0.20

TABLE 10 SOIC16 DIMENSIONS

Dims.	Tols/N	SOIC16
A	MAX.	1.70
A1	±.05	0.17
A2	±.10	1.38
D	±.10	9.9
E	±.20	6.00
E1	±.10	3.90
L	±.05	0.5
ccc	MAX.	0.10
ddd	MAX.	0.10
e	BASIC	1.27
b	±.05	0.43
O		0°~7°
01	±4°	7°
R	MAX	0.20
R1	TYP.	0.13

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