

512Mb DDR2 SDRAM

HY5PS12421C(L)FP

HY5PS12821C(L)FP

HY5PS121621C(L)FP

Revision History

| Rev. | History | Draft Date |
|------|--|------------|
| 0.1 | Preliminary | May 2006 |
| 0.2 | IDD Spec. Changed | July 2006 |
| 0.3 | Removed improper note in ODT spec. | July 2006 |
| 0.4 | Updated IDD3P-S value/OCD Default Characteristics | Aug. 2006 |
| 0.5 | Updated IDD spec for x8 org. on page 16 | Feb. 2007 |
| 0.6 | Removed Y4 Speed bin | July 2007 |
| 0.7 | Updated Timing Patterns (DDR2-800 5/5/5 and 6/6/6) | Sep. 2007 |
| 0.8 | Corrected Typo | Oct. 2007 |
| 0.9 | Editorial Correction | Sep. 2008 |

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1. Description

1.1 Device Features & Ordering Information

1.1.1 Key Features

- VDD,VDDQ =1.8 +/- 0.1V
- All inputs and outputs are compatible with SSTL_18 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous-data transaction aligned to bidirectional data strobe (DQS, \overline{DQS})
- Differential Data Strobe (DQS, \overline{DQS})
- Data outputs on DQS, \overline{DQS} edges when read (edged DQ)
- Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ, DQS and \overline{DQS} transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 3, 4, 5 and 6 supported
- Programmable additive latency 0, 1, 2, 3, 4 and 5 supported
- Programmable burst length 4 / 8 with both nibble sequential and interleave mode
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- tRAS lockout supported
- 8K refresh cycles /64ms
- JEDEC standard 60ball FBGA(x4/x8) & 84ball FBGA(x16)
- Full strength driver option controlled by EMRS
- On Die Termination supported
- Off Chip Driver Impedance Adjustment supported
- Read Data Strobe supported (x8 only)
- Self-Refresh High Temperature Entry
- Partial Array Self Refresh support

Ordering Information

| Part No. | Organization | Package |
|----------------------|--------------|-------------|
| HY5PS12421C(L)FP-X* | 128Mx4 | Lead free** |
| HY5PS12821C(L)FP-X* | 64Mx8 | |
| HY5PS121621C(L)FP-X* | 32Mx16 | |

Note:

1. -X* is the speed bin, refer to the Operation Frequency table for complete Part No.
2. Hynix Lead-free products are compliant to RoHS.

Operating Frequency

| Speed Bin | tCK (ns) | CL | tRCD | tRP | Unit |
|-----------|----------|----|------|-----|------|
| E3 | 5 | 3 | 3 | 3 | Clk |
| C4 | 3.75 | 4 | 4 | 4 | Clk |
| Y5 | 3 | 5 | 5 | 5 | Clk |
| S5 | 2.5 | 5 | 5 | 5 | Clk |
| S6 | 2.5 | 6 | 6 | 6 | Clk |

1.2 Pin Configuration & Address Table

128Mx4 DDR2 Pin Configuration (Top view: see balls through package)

| | | | | | | |
|------|------|-----------------|---|------------------|------------------|------|
| 1 | 2 | 3 | | 7 | 8 | 9 |
| VDD | NC | VSS | A | VSSQ | \overline{DQS} | VDDQ |
| NC | VSSQ | DM | B | DQS | VSSQ | NC |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| NC | VSSQ | DQ3 | D | DQ2 | VSSQ | NC |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | \overline{WE} | F | \overline{RAS} | \overline{CK} | ODT |
| NC | BA0 | BA1 | G | \overline{CAS} | \overline{CS} | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

ROW AND COLUMN ADDRESS TABLE

| ITEMS | 128Mx4 |
|---------------------|------------|
| # of Bank | 4 |
| Bank Address | BA0, BA1 |
| Auto Precharge Flag | A10/AP |
| Row Address | A0 - A13 |
| Column Address | A0-A9, A11 |
| Page size | 1 KB |

64Mx8 DDR2 PIN CONFIGURATION (Top view: see balls through package)

| 1 | 2 | 3 | | 7 | 8 | 9 |
|------|------------------------------|------------------------|---|-------------------------|-------------------------|------|
| VDD | NU, $\overline{\text{RDQS}}$ | VSS | A | VSSQ | $\overline{\text{DQS}}$ | VDDQ |
| DQ6 | VSSQ | DM, RDQS | B | DQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | D | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{\text{WE}}$ | F | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$ | ODT |
| NC | BA0 | BA1 | G | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$ | |
| | A10 | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

ROW AND COLUMN ADDRESS TABLE

| ITEMS | 64Mx8 |
|---------------------|----------|
| # of Bank | 4 |
| Bank Address | BA0, BA1 |
| Auto Precharge Flag | A10/AP |
| Row Address | A0 - A13 |
| Column Address | A0-A9 |
| Page size | 1 KB |

32Mx16 DDR2 PIN CONFIGURATION (Top view: see balls through package)

| 1 | 2 | 3 | | 7 | 8 | 9 |
|------|------|------------------------|---|-------------------------|--------------------------|------|
| VDD | NC | VSS | A | VSSQ | $\overline{\text{UDQS}}$ | VDDQ |
| DQ14 | VSSQ | UDM | B | UDQS | VSSQ | DQ15 |
| VDDQ | DQ9 | VDDQ | C | VDDQ | DQ8 | VDDQ |
| DQ12 | VSSQ | DQ11 | D | DQ10 | VSSQ | DQ13 |
| VDD | NC | VSS | E | VSSQ | $\overline{\text{LDQS}}$ | VDDQ |
| DQ6 | VSSQ | LDM | F | LDQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | G | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | H | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | J | VSSDL | CK | VDD |
| | CKE | $\overline{\text{WE}}$ | K | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$ | ODT |
| NC | BA0 | BA1 | L | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$ | |
| | A10 | A1 | M | A2 | A0 | VDD |
| VSS | A3 | A5 | N | A6 | A4 | |
| | A7 | A9 | P | A11 | A8 | VSS |
| VDD | A12 | NC | R | NC | NC | |

ROW AND COLUMN ADDRESS TABLE

| ITEMS | 32Mx16 |
|---------------------|----------|
| # of Bank | 4 |
| Bank Address | BA0, BA1 |
| Auto Precharge Flag | A10/AP |
| Row Address | A0 - A12 |
| Column Address | A0-A9 |
| Page size | 2 KB |

1.3 PIN DESCRIPTION

| PIN | TYPE | DESCRIPTION |
|---|------------------|---|
| CK, \overline{CK} | Input | Clock: CK and \overline{CK} are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of \overline{CK} . Output (read) data is referenced to the crossings of CK and \overline{CK} (both directions of crossing). |
| CKE | Input | Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, \overline{CK} and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. |
| \overline{CS} | Input | Chip Select: All commands are masked when \overline{CS} is registered HIGH. \overline{CS} provides for external bank selection on systems with multiple banks. \overline{CS} is considered part of the command code. |
| ODT | Input | On Die Termination Control: ODT (registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to DQ, DQS, \overline{DQS} , RDQS, \overline{RDQS} , and DM signal for x4,x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/ \overline{UDQS} .LDQS/ \overline{LDQS} , UDM and LDM signal. The ODT pin will be ignored if the Extended Mode Register(EMRS(1)) is programmed to disable ODT. |
| \overline{RAS} , \overline{CAS} , \overline{WE} | Input | Command Inputs: \overline{RAS} , \overline{CAS} and \overline{WE} (along with \overline{CS}) define the command being entered. |
| DM (LDM, UDM) | Input | Input Data Mask: DM is an input mask signal for write data. Input Data is masked when DM is sampled High coincident with that input data during a WRITE access. DM is sampled on both edges of DQS, Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/ \overline{RDQS} is enabled by EMRS command. |
| BA0 - BA2 | Input | Bank Address Inputs: BA0 - BA2 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied (For 256Mb and 512Mb, BA2 is not applied). Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle. |
| A0 -A15 | Input | Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0-BA2. The address inputs also provide the op code during MODE REGISTER SET commands. |
| DQ | Input/ Output | Data input / output: Bi-directional data bus |

| PIN | TYPE | DESCRIPTION |
|--|------------------|--|
| DQS, $\overline{\text{DQS}}$ (UDQS), $\overline{\text{UDQS}}$ (LDQS), $\overline{\text{LDQS}}$ (RDQS), $\overline{\text{RDQS}}$ | Input/ Output | <p>Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. For the x16, LDQS correspond to the data on DQ0~DQ7; UDQS corresponds to the data on DQ8~DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals DQS, LDQS, UDQS and RDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.</p> <p>In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1)</p> <p style="text-align: center;"> x4 DQS/$\overline{\text{DQS}}$ x8 DQS/$\overline{\text{DQS}}$ if EMRS(1)[A11] = 0 x8 DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, $\overline{\text{RDQS}}$ if EMRS(1)[A11] = 1 x16 LDQS/$\overline{\text{LDQS}}$ and UDQS/$\overline{\text{UDQS}}$ </p> <p>"single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1)</p> <p style="text-align: center;"> x4 DQS x8 DQS if EMRS(1)[A11] = 0 x8 DQS, RDQS, if EMRS(1)[A11] = 1 x16 LDQS and UDQS </p> |
| NC | | No Connect: No internal electrical connection is present. |
| VDDQ | Supply | DQ Power Supply: 1.8V +/- 0.1V |
| VSSQ | Supply | DQ Ground |
| VDDL | Supply | DLL Power Supply: 1.8V +/- 0.1V |
| VSSDL | Supply | DLL Ground |
| VDD | Supply | Power Supply: 1.8V +/- 0.1V |
| VSS | Supply | Ground |
| VREF | Supply | Reference voltage for inputs for SSTL interface. |

2. Maximum DC Ratings

2.1 Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|------------------------------------|---|-----------------|-------|-------|
| VDD | Voltage on VDD pin relative to Vss | - 1.0 V ~ 2.3 V | V | 1 |
| VDDQ | Voltage on VDDQ pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| VDDL | Voltage on VDDL pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| V _{IN} , V _{OUT} | Voltage on any pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| T _{STG} | Storage Temperature | -55 to +100 | | 1, 2 |
| I _I | Input leakage current; any input 0V V _{IN} VDD; all other balls not under test = 0V) | -2 uA ~ 2 uA | uA | |
| I _{OZ} | Output leakage current; 0V V _{OUT} VDDQ; DQ and ODT disabled | -5 uA ~ 5 uA | uA | |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions. Please refer to JESD51-2 standard.

2.2 Operating Temperature Condition

| Symbol | Parameter | Rating | Units | Notes |
|-------------------|-----------------------|---------|-------|-------|
| t _{OPER} | Operating Temperature | 0 to 95 | °C | 1,2 |

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At t_{OPER} 85~95 , Double refresh rate (tREFI: 3.9us) is required, and to enter the self refresh mode at this temperature range it must be required an EMRS command to change itself refresh rate.

3. AC & DC Operating Conditions

3.1 DC Operating Conditions

3.1.1 Recommended DC Operating Conditions (SSTL_1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|--------|---------------------------|-----------|-----------|-----------|-------|-------|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.7 | 1.8 | 1.9 | V | 1 |
| VDDL | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 1,2 |
| VDDQ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 1,2 |
| VREF | Input Reference Voltage | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | mV | 3,4 |
| VTT | Termination Voltage | VREF-0.04 | VREF | VREF+0.04 | V | 5 |

1. Min. Typ. and Max. values increase by 100mV for C3(DDR2-533 3-3-3) speed option.
2. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDD.
3. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ
4. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
5. VTT of transmitting device must track VREF of receiving device.

3.1.2 ODT DC electrical characteristics

| PARAMETER/CONDITION | SYMBOL | MIN | NOM | MAX | UNITS | NOTES |
|--|-----------|-----|-----|-----|-------|-------|
| Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm | Rtt1(eff) | 60 | 75 | 90 | ohm | 1 |
| Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm | Rtt2(eff) | 120 | 150 | 180 | ohm | 1 |
| Rtt effective impedance value for EMRS(A6,A2)=1,1; 50 ohm | Rtt3(eff) | 40 | 50 | 60 | ohm | 1 |
| Deviation of VM with respect to VDDQ/2 | delta VM | -6 | | +6 | % | 1 |

Note:

1. Test condition for Rtt measurements

Measurement Definition for Rtt (eff): Apply $V_{IH}(ac)$ and $V_{IL}(ac)$ to test pin separately, then measure current $I(V_{IH}(ac))$ and $I(V_{IL}(ac))$ respectively. $V_{IH}(ac)$, $V_{IL}(ac)$, and VDDQ values defined in SSTL_18

$$R_{tt} \text{ (eff)} = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement Definition for VM: Measurement Voltage at test pin (mid point) with no load.

$$\text{delta VM} = \frac{2 \times V_m}{V_{DDQ}} - 1 \times 100\%$$

3.2 DC & AC Logic Input Levels

3.2.1 Input DC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|--------------|---------------------|-------------------|-------------------|-------|-------|
| $V_{IH(dc)}$ | dc input logic high | $V_{REF} + 0.125$ | $V_{DDQ} + 0.3$ | V | |
| $V_{IL(dc)}$ | dc input logic low | - 0.3 | $V_{REF} - 0.125$ | V | |

3.2.2 Input AC Logic Level

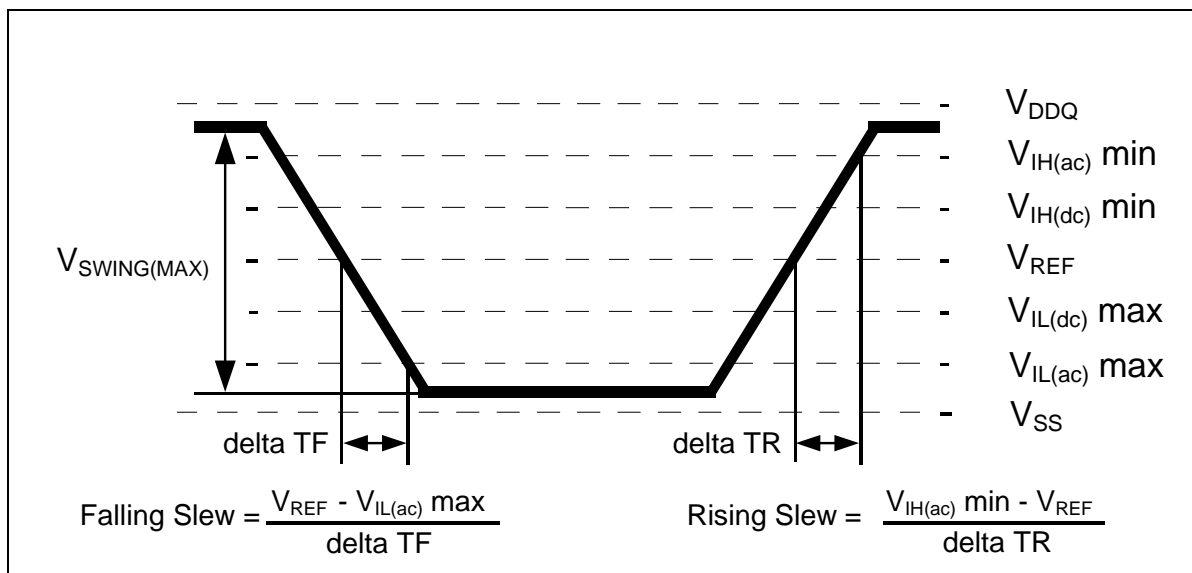
| Symbol | Parameter | DDR2 400,533 | | DDR2 667,800 | | Units | Notes |
|--------------|---------------------|-------------------|-------------------|-------------------|-------------------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| $V_{IH(ac)}$ | ac input logic high | $V_{REF} + 0.250$ | - | $V_{REF} + 0.200$ | - | V | |
| $V_{IL(ac)}$ | ac input logic low | - | $V_{REF} - 0.250$ | - | $V_{REF} - 0.200$ | V | |

3.2.3 AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|------------------|---|-----------------|-------|-------|
| V_{REF} | Input reference voltage | $0.5 * V_{DDQ}$ | V | 1 |
| $V_{SWING(MAX)}$ | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

Note:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

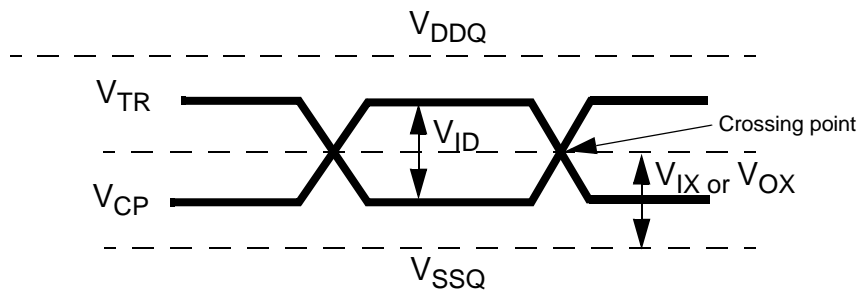


< Figure: AC Input Test Signal Waveform >

3.2.4 Differential Input AC logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|--------------|-------------------------------------|-------------------------|-------------------------|-------|-------|
| $V_{ID}(ac)$ | ac differential input voltage | 0.5 | $V_{DDQ} + 0.6$ | V | 1 |
| $V_{IX}(ac)$ | ac differential cross point voltage | $0.5 * V_{DDQ} - 0.175$ | $0.5 * V_{DDQ} + 0.175$ | V | 2 |

- $V_{IN}(DC)$ specifies the allowable DC execution of each input of differential pair such as \overline{CK} , \overline{DQS} , \overline{LDQS} , \overline{UDQS} and \overline{UDQS} .
- $V_{ID}(DC)$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as \overline{CK} , \overline{DQS} , \overline{LDQS} or \overline{UDQS}) level and V_{CP} is the complementary input (such as \overline{CK} , \overline{DQS} , \overline{LDQS} or \overline{UDQS}) level. The minimum value is equal to $V_{IH}(DC) - V_{IL}(DC)$.



< Differential signal levels >

Note:

- $V_{ID}(AC)$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as \overline{CK} , \overline{DQS} , \overline{LDQS} or \overline{UDQS}) and V_{CP} is the complementary input signal (such as \overline{CK} , \overline{DQS} , \overline{LDQS} or \overline{UDQS}). The minimum value is equal to $V_{IH}(AC) - V_{IL}(AC)$.
- The typical value of $V_{IX}(AC)$ is expected to be about $0.5 * V_{DDQ}$ of the transmitting device and $V_{IX}(AC)$ is expected to track variations in V_{DDQ} . $V_{IX}(AC)$ indicates the voltage at which differential input signals must cross.

3.2.5 Differential AC output parameters

| Symbol | Parameter | Min. | Max. | Units | Notes |
|--------------|-------------------------------------|-------------------------|-------------------------|-------|-------|
| $V_{OX}(ac)$ | ac differential cross point voltage | $0.5 * V_{DDQ} - 0.125$ | $0.5 * V_{DDQ} + 0.125$ | V | 1 |

Note:

- The typical value of $V_{OX}(AC)$ is expected to be about $0.5 * V_{DDQ}$ of the transmitting device and $V_{OX}(AC)$ is expected to track variations in V_{DDQ} . $V_{OX}(AC)$ indicates the voltage at which differential output signals must cross.

3.3 Output Buffer Characteristics

3.3.1 Output AC Test Conditions

| Symbol | Parameter | SSTL_18 Class II | Units | Notes |
|-----------|---|------------------|-------|-------|
| V_{OTR} | Output Timing Measurement Reference Level | $0.5 * V_{DDQ}$ | V | 1 |

1. The VDDQ of the device under test is referenced.

3.3.2 Output DC Current Drive

| Symbol | Parameter | SSTL_18 | Units | Notes |
|--------------|----------------------------------|---------|-------|---------|
| $I_{OH(dc)}$ | Output Minimum Source DC Current | - 13.4 | mA | 1, 3, 4 |
| $I_{OL(dc)}$ | Output Minimum Sink DC Current | 13.4 | mA | 2, 3, 4 |

1. $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = 1420\text{ mV}$. $(V_{OUT} - V_{DDQ})/I_{OH}$ must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and $V_{DDQ} - 280\text{ mV}$.
2. $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = 280\text{ mV}$. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT} .
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

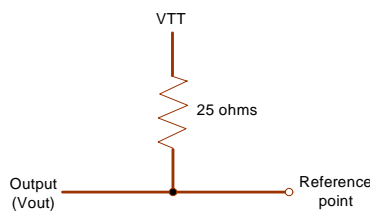
3.3.3 OCD default characteristics

| Description | Parameter | Min | Nom | Max | Unit | Notes |
|--|-----------|--|-----|-----|------|-------------|
| Output impedance | | See full strength default driver characteristics | | | ohms | 1 |
| Output impedance step size for OCD calibration | | 0 | | 1.5 | ohms | 6 |
| Pull-up and pull-down mismatch | | 0 | | 4 | ohms | 1,2,3 |
| Output slew rate | Sout | 1.5 | - | 5 | V/ns | 1,4,5,6,7,8 |

Note

- Absolute Specifications (Toper; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings. Please refer to the Device Operation & Timing Diagram of DDR2 for the Full Strength Default Driver Characteristics.
- Impedance measurement condition for output source dc current: VDDQ=1.7V; VOUT=1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
- Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
- Slew rate measured from vil(ac) to vih(ac).
- The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
- This represents the step size when the OCD is near 18 ohms at nominal conditions across all process corners/ variations and represents only the DRAM uncertainty. A 0 ohm value(no calibration) can only be achieved if the OCD impedance is 18 ohms +/- 0.75 ohms under nominal conditions.

Output Slew rate load:



- DRAM output slew rate specification applies to 400, 533 and 667 MT/s speed bins.
- Timing skew due to DRAM output slew rate mis-match between DQS / \overline{DQS} and associated DQs is included in tDQSQ and tQHS specification.

3.4 IDD Specifications & Test Conditions

IDD Specifications(max)

| Symbol | | DDR2 800 | | DDR2 667 | | DDR2 533 | | DDR2 400 | | Units |
|--------|--------------|----------|-----|----------|-----|----------|-----|----------|-----|-------|
| | | x4/x8 | x16 | x4/x8 | x16 | x4/x8 | x16 | x4/x8 | x16 | |
| IDD0 | | 100 | 120 | 90 | 110 | 80 | 100 | 80 | 100 | mA |
| IDD1 | | 100 | 130 | 90 | 120 | 90 | 110 | 80 | 110 | mA |
| IDD2P | | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | mA |
| IDD2Q | | 40 | 40 | 40 | 40 | 30 | 30 | 30 | 30 | mA |
| IDD2N | | 50 | 50 | 40 | 40 | 40 | 40 | 30 | 30 | mA |
| IDD3P | F | 35 | 35 | 30 | 30 | 30 | 30 | 30 | 30 | mA |
| | S | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | mA |
| IDD3N | | 60 | 60 | 50 | 50 | 50 | 50 | 40 | 40 | mA |
| IDD4W | | 160 | 240 | 140 | 200 | 120 | 170 | 90 | 130 | mA |
| IDD4R | | 140 | 200 | 120 | 170 | 100 | 150 | 80 | 110 | mA |
| IDD5B | | 160 | 165 | 160 | 160 | 150 | 150 | 150 | 150 | mA |
| IDD6 | Normal Power | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | mA |
| | Low Power* | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| IDD7 | | 230 | 340 | 220 | 320 | 210 | 320 | 210 | 320 | mA |

Note:

1. Low power parts have an extra suffix 'L' in part number; ex) HY5PS1216CLFP-C4

IDD Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1-5)

| Symbol | Conditions | Units |
|--------|---|---------------------------|
| IDD0 | Operating one bank active-precharge current; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RAS\ min}(IDD)$; CKE is HIGH, \overline{CS} is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA |
| IDD1 | Operating one bank active-read-precharge current; $I_{OUT} = 0mA$; $BL = 4$, $CL = CL(IDD)$, $AL = 0$; $t_{CK} = t_{CK}(IDD)$, $t_{RC} = t_{RC}(IDD)$, $t_{RAS} = t_{RAS\ min}(IDD)$, $t_{RCD} = t_{RCD}(IDD)$; CKE is HIGH, \overline{CS} is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | mA |
| IDD2P | Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | mA |
| IDD2Q | Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, \overline{CS} is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | mA |
| IDD2N | Precharge standby current; All banks idle; $t_{CK} = t_{CK}(IDD)$; CKE is HIGH, \overline{CS} is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA |
| IDD3P | Active power-down current; All banks open; $t_{CK} = t_{CK}(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0 |
| | | Slow PDN Exit MRS(12) = 1 |
| IDD3N | Active standby current; All banks open; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ max}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, \overline{CS} is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA |
| IDD4W | Operating burst write current; All banks open, Continuous burst writes; $BL = 4$, $CL = CL(IDD)$, $AL = 0$; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ max}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, \overline{CS} is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA |
| IDD4R | Operating burst read current; All banks open, Continuous burst reads, $I_{OUT} = 0mA$; $BL = 4$, $CL = CL(IDD)$, $AL = 0$; $t_{CK} = t_{CK}(IDD)$, $t_{RAS} = t_{RAS\ max}(IDD)$, $t_{RP} = t_{RP}(IDD)$; CKE is HIGH, \overline{CS} is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | mA |
| IDD5B | Burst refresh current; $t_{CK} = t_{CK}(IDD)$; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, \overline{CS} is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | mA |
| IDD6 | Self refresh current; CK and \overline{CK} at 0V; CKE $\leq 0.2V$; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | mA |

| | | |
|-------------|--|----|
| IDD7 | Operating bank interleave read current; All bank interleaving reads, IOU _T = 0mA; BL = 4, CL = CL(IDD), AL = t _{RCD} (IDD)-1*t _{CK} (IDD); t _{CK} = t _{CK} (IDD), t _{RC} = t _{RC} (IDD), t _{RRD} = t _{RRD} (IDD), t _{RCD} = 1*t _{CK} (IDD); CKE is HIGH, \overline{CS} is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions | mA |
|-------------|--|----|

Note:

1. VDDQ = 1.8 +/- 0.1V ; VDD = 1.8 +/- 0.1V
(exclusively VDDQ = 1.9 +/- 0.1V ; VDD = 1.9 +/- 0.1V for C3 speed grade)
2. IDD specifications are tested after the device is properly initialized
3. Input slew rate is specified by AC Parametric Test Condition
4. IDD parameters are specified with ODT disabled.
5. Data bus consists of DQ, DM, DQS, DQS, RDQS, RDQS, LDQS, LDQS, UDQS, and UDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.
6. Definitions for IDD
 - LOW is defined as $V_{in} \leq V_{ILAC}$ (max)
 - HIGH is defined as $V_{in} \geq V_{IHAC}$ (min)
 - STABLE is defined as inputs stable at a HIGH or LOW level
 - FLOATING is defined as inputs at $V_{REF} = VDDQ/2$
 - SWITCHING is defined as: inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

For purposes of IDD testing, the following parameters are to be utilized

| Speed Bin (CL-tRCD-tRP) | DDR2-800 | | DDR2-667 | DDR2-533 | DDR2-400 | Units |
|----------------------------|----------|-------|----------|----------|----------|-------|
| | 5-5-5 | 6-6-6 | 5-5-5 | 4-4-4 | 3-3-3 | |
| CL(IDD) | 5 | 6 | 5 | 4 | 3 | tCK |
| tRCD(IDD) | 12.5 | 15 | 15 | 15 | 15 | ns |
| tRC(IDD) | 57.25 | 60 | 60 | 60 | 55 | ns |
| tRRD(IDD)-x4/x8 | 7.5 | 7.5 | 7.5 | 7.5 | 7.5 | ns |
| tRRD(IDD)-x16 | 10 | 10 | 10 | 10 | 10 | ns |
| tCK(IDD) | 2.5 | 2.5 | 3 | 3.75 | 5 | ns |
| tRASmin (IDD) | 45 | 45 | 45 | 45 | 40 | ns |
| tRASmax (IDD) | 70000 | 70000 | 70000 | 70000 | 70000 | ns |
| tRP(IDD) | 12.5 | 15 | 15 | 15 | 15 | ns |
| tRFC(IDD)-256Mb | 75 | 75 | 75 | 75 | 75 | ns |
| tRFC(IDD)-512Mb | 105 | 105 | 105 | 105 | 105 | ns |
| tRFC(IDD)-1Gb | 127.5 | 127.5 | 127.5 | 127.5 | 127.5 | ns |

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum tRC(IDD) without violating tRRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOU_T = 0mA

Timing Patterns for 4 bank devices x4/ x8/ x16

- DDR2-400 3/3/3: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D (11 clocks)
- DDR2-533 3/3/3: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D (15 clocks)
- DDR2-533 4/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D (16 clocks)
- DDR2-667 4/4/4: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D (19 clocks)
- DDR2-667 5/5/5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D (20 clocks)
- DDR2-800 5/5/5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D (23 clocks)
- DDR2-800 6/6/6: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D (24 clocks)

3.5. Input/Output Capacitance

| Parameter | Symbol | DDR2- 400 DDR2- 533 | | DDR2 667 | | DDR2 800 | | Units |
|---|--------|------------------------|------|----------|------|----------|------|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Input capacitance, CK and \overline{CK} | CCK | 1.0 | 2.0 | 1.0 | 2.0 | 1.0 | 2.0 | pF |
| Input capacitance delta, CK and \overline{CK} | CDCK | x | 0.25 | x | 0.25 | x | 0.25 | pF |
| Input capacitance, all other input-only pins | CI | 1.0 | 2.0 | 1.0 | 2.0 | 1.0 | 1.75 | pF |
| Input capacitance delta, all other input-only pins | CDI | x | 0.25 | x | 0.25 | x | 0.25 | pF |
| Input/output capacitance, DQ, DM, DQS, \overline{DQS} | CIO | 2.5 | 4.0 | 2.5 | 3.5 | 2.5 | 3.5 | pF |
| Input/output capacitance delta, DQ, DM, DQS, \overline{DQS} | CDIO | x | 0.5 | x | 0.5 | x | 0.5 | pF |

4. Electrical Characteristics & AC Timing Specification

(0 T_{CASE} 95 ; $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$)

Refresh Parameters by Device Density

| Parameter | Symbol | 256Mb | 512Mb | 1Gb | 2Gb | 4Gb | Units |
|---|--------|--------------------|-------|-------|-----|-------|-------|
| Refresh to Active /Refresh command time | tRFC | 75 | 105 | 127.5 | 195 | 327.5 | ns |
| Average periodic refresh interval | tREFI | 0 T_{CASE} 85 | 7.8 | 7.8 | 7.8 | 7.8 | us |
| | | 85 < T_{CASE} 95 | 3.9 | 3.9 | 3.9 | 3.9 | us |

DDR2 SDRAM speed bins and tRCD, tRP and tRC for corresponding bin

| Speed | DDR2-800D | DDR2-800E | DDR2-667D | DDR2-533C | DDR2-400B | Units |
|-------------------|-----------|-----------|-----------|-----------|-----------|-------|
| Bin (CL-tRCD-tRP) | 5-5-5 | 6-6-6 | 5-5-5 | 4-4-4 | 3-3-3 | |
| Parameter | min | min | min | min | min | |
| CAS Latency | 5 | 6 | 5 | 4 | 5 | tCK |
| tRCD | 12.5 | 15 | 15 | 15 | 15 | ns |
| tRP | 12.5 | 15 | 15 | 15 | 15 | ns |
| tRAS | 45 | 45 | 45 | 45 | 40 | ns |
| tRC | 57.25 | 60 | 60 | 60 | 55 | ns |

Timing Parameters by Speed Grade

(Refer to notes for information related to this table at the following pages of this table)

| Parameter | Symbol | DDR2-400 | | DDR2-533 | | Unit | Note |
|--|---------------|------------------|---------|------------------|---------|------|--------------|
| | | min | max | min | max | | |
| DQ output access time from CK/ $\overline{\text{CK}}$ | tAC | -600 | +600 | -500 | +500 | ps | |
| DQS output access time from CK/ $\overline{\text{CK}}$ | tDQSCK | -500 | +500 | -450 | +450 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK half period | tHP | min (tCL,tCH) | - | min (tCL,tCH) | - | ps | 11,12 |
| Clock cycle time, CL=x | tCK | 5000 | 8000 | 3750 | 8000 | ps | 15 |
| DQ and DM input setup time (differential strobe) | tDS (base) | 150 | - | 100 | - | ps | 6,7,8, 20 |
| DQ and DM input hold time (differential strobe) | tDH (base) | 275 | - | 225 | - | ps | 6,7,8, 21 |
| DQ and DM input setup time (single ended strobe) | tDS | 25 | - | -25 | - | ps | 6,7,8, 20 |
| DQ and DM input hold time (single ended strobe) | tDH | 25 | - | -25 | - | ps | 6,7,8, 21 |
| Control & Address input pulse width for each input | tIPW | 0.6 | - | 0.6 | - | tCK | |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | - | 0.35 | - | tCK | |
| Data-out high-impedance time from CK/ $\overline{\text{CK}}$ | tHZ | - | tAC max | - | tAC max | ps | 18 |
| DQS low-impedance time from CK/ $\overline{\text{CK}}$ | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | ps | 18 |
| DQ low-impedance time from CK/ $\overline{\text{CK}}$ | tLZ(DQ) | 2*tAC min | tAC max | 2*tAC min | tAC max | ps | 18 |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | - | 350 | - | 300 | ps | 13 |
| DQ hold skew factor | tQHS | - | 450 | - | 400 | ps | 12 |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | - | tHP - tQHS | - | ps | |
| First DQS latching transition to associated clock edge | tDOSS | -0.25 | + 0.25 | -0.25 | + 0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | - | 0.35 | - | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | - | 0.35;; | - | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | 0.2 | - | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | - | 0.2 | - | tCK | |
| Mode register set command cycle time | tMRD | 2 | - | 2 | - | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 10 |
| Write preamble | tWPRE | 0.35 | - | 0.35 | - | tCK | |
| Address and control input setup time | tIS(base) | 350 | - | 250 | - | ps | 5,7,9, 23 |
| Address and control input hold time | tIH(base) | 475 | - | 375 | - | ps | 5,7,9, 23 |

(Refer to notes for information related to this table at the following pages of this table)

| Parameter | Symbol | DDR2-400 | | DDR2-533 | | Unit | Note |
|---|--------------------|--------------------|---------------------------|--------------------|---------------------------|------|------|
| | | min | max | min | max | | |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Active to active command period for 1KB page size products | tRRD | 7.5 | - | 7.5 | - | ns | 4 |
| Active to active command period for 2KB page size products | tRRD | 10 | - | 10 | - | ns | 4 |
| Four Active Window for 1KB page size products | tFAW | 37.5 | - | 37.5 | - | ns | |
| Four Active Window for 2KB page size products | tFAW | 50 | - | 50 | - | ns | |
| CAS to $\overline{\text{CAS}}$ command delay | tCCD | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | - | 15 | - | ns | |
| Auto precharge write recovery + precharge time | tDAL | WR+tRP | - | WR+tRP | - | tCK | 14 |
| Internal write to read command delay | tWTR | 10 | - | 7.5 | - | ns | 24 |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | ns | 3 |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | ns | |
| Exit self refresh to a read command | tXSRD | 200 | - | 200 | - | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | - | 2 | - | tCK | |
| Exit active power down to read command | tXARD | 2 | | 2 | | tCK | 1 |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 6 - AL | | 6 - AL | | tCK | 1, 2 |
| CKE minimum pulse width (high and low pulse width) | t _{CKE} | 3 | | 3 | | tCK | 27 |
| ODT turn-on delay | t _{AOND} | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | t _{AON} | tAC (min) | tAC(max) +1 | tAC (min) | tAC(max) +1 | ns | 16 |
| ODT turn-on (Power-Down mode) | t _{AONPD} | tAC(min)+ 2 | 2tCK+ tAC(max) +1 | tAC(min)+ 2 | 2tCK+ tAC(max) +1 | ns | |
| ODT turn-off delay | t _{AOFD} | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | t _{AOF} | tAC (min) | tAC (max)+ 0.6 | tAC (min) | tAC (max)+ 0.6 | ns | 17 |
| ODT turn-off (Power-Down mode) | t _{AOFPD} | tAC(min)+ 2 | 2.5tCK+ tAC(max) +1 | tAC(min)+ 2 | 2.5tCK+ tAC(max) +1 | ns | |
| ODT to power down entry latency | tANPD | 3 | | 3 | | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS + tCK + tIH | | tIS + tCK + tIH | | ns | 15 |

| Parameter | Symbol | DDR2-667 | | DDR2-800 | | Unit | Note |
|--|---------------|------------------|---------|------------------|---------|------|----------|
| | | min | max | min | max | | |
| DQ output access time from CK/ $\overline{\text{CK}}$ | tAC | -450 | +450 | -400 | +400 | ps | |
| DQS output access time from CK/ $\overline{\text{CK}}$ | tDQSCK | -400 | +400 | -350 | +350 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK half period | tHP | min(tCL, tCH) | - | min(tCL, tCH) | - | ps | 11,12 |
| Clock cycle time, CL=x | tCK | 3000 | 8000 | 2500 | | ps | 15 |
| DQ and DM input setup time | tDS(base) | 100 | - | 50 | - | ps | 6,7,8,20 |
| DQ and DM input hold time | tDH (base) | 175 | - | 125 | - | ps | 6,7,8,21 |
| Control & Address input pulse width for each input | tIPW | 0.6 | - | 0.6 | - | tCK | |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | - | 0.35 | - | tCK | |
| Data-out high-impedance time from CK/ $\overline{\text{CK}}$ | tHZ | - | tAC max | - | tAC max | ps | 18 |
| DQS low-impedance time from CK/ $\overline{\text{CK}}$ | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | ps | 18 |
| DQ low-impedance time from CK/ $\overline{\text{CK}}$ | tLZ(DQ) | 2*tAC min | tAC max | 2*tAC min | tAC max | ps | 18 |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | - | 240 | - | 200 | ps | 13 |
| DQ hold skew factor | tQHS | - | 340 | - | 300 | ps | 12 |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | - | tHP - tQHS | - | ps | |
| First DQS latching transition to associated clock edge | tDQSS | - 0.25 | + 0.25 | - 0.25 | + 0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | - | 0.35 | - | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | - | 0.35 | - | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | 0.2 | - | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | - | 0.2 | - | tCK | |
| Mode register set command cycle time | tMRD | 2 | - | 2 | - | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 10 |
| Write preamble | tWPRE | 0.35 | - | 0.35 | - | tCK | |
| Address and control input setup time | tIS(base) | 200 | - | 175 | - | ps | 5,7,9,22 |
| Address and control input hold time | tIH(base) | 275 | - | 250 | - | ps | 5,7,9,23 |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | tCK | 19 |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 19 |
| Activate to precharge command | tRAS | 45 | 70000 | 45 | 70000 | ns | 3 |
| Active to active command period for 1KB page size products | tRRD | 7.5 | - | 7.5 | - | ns | 4 |
| Active to active command period for 2KB page size products | tRRD | 10 | - | 10 | - | ns | 4 |

-Continue-

| Parameter | Symbol | DDR2-667 | | DDR2-800 | | Unit | Note |
|---|----------------------|-----------------|-------------------|-----------------|-------------------|------|------|
| | | min | max | min | max | | |
| Four Active Window for 1KB page size products | tFAW | 37.5 | - | 37.5 | - | ns | |
| Four Active Window for 2KB page size products | tFAW | 50 | - | 50 | - | ns | |
| CAS to CAS command delay | tCCD | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | - | 15 | - | ns | |
| Auto precharge write recovery + precharge time | tDAL | WR+tRP | - | WR+tRP | - | tCK | 14 |
| Internal write to read command delay | tWTR | 7.5 | - | 7.5 | - | ns | |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | ns | 3 |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | ns | |
| Exit self refresh to a read command | tXSRD | 200 | - | 200 | - | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | - | 2 | - | tCK | |
| Exit active power down to read command | tXARD | 2 | | 2 | | tCK | 1 |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 7 - AL | | 8 - AL | | tCK | 1, 2 |
| CKE minimum pulse width (high and low pulse width) | t ^o CKE | 3 | | 3 | | tCK | |
| ODT turn-on delay | t ^o AOND | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | t ^o AON | tAC (min) | tAC (max) + 0.7 | tAC (min) | tAC (max) + 0.7 | ns | 6,16 |
| ODT turn-on (Power-Down mode) | t ^o AONPD | tAC(min)+2 | 2tCK+tAC(max)+1 | tAC (min) + 2 | 2tCK+tAC(max)+1 | ns | |
| ODT turn-off delay | t ^o AOFD | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | t ^o AOF | tAC (min) | tAC (max) + 0.6 | tAC (min) | tAC (max) + 0.6 | ns | 17 |
| ODT turn-off (Power-Down mode) | t ^o AOFPD | tAC (min) + 2 | 2.5tCK+tAC(max)+1 | tAC (min) + 2 | 2.5tCK+tAC(max)+1 | ns | |
| ODT to power down entry latency | tANPD | 3 | | 3 | | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS + tCK + tIH | | tIS + tCK + tIH | | ns | 15 |

General notes, which may apply for all AC parameters

1. Slew Rate Measurement Levels

a. Output slew rate for falling and rising edges is measured between $V_{TT} - 250$ mV and $V_{TT} + 250$ mV for single ended signals.

For differential signals (e.g. $DQS - \overline{DQS}$) output slew rate is measured between $DQS - \overline{DQS} = -500$ mV and $DQS - \overline{DQS} = +500$ mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

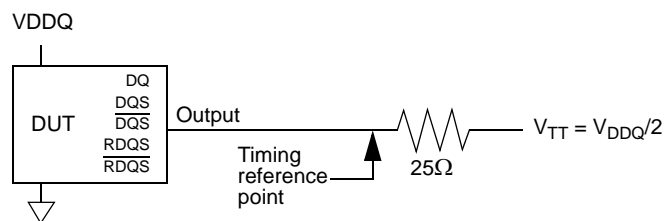
b. Input slew rate for single ended signals is measured from dc-level to ac-level: from V_{IL} (dc) to V_{IH} (ac) for rising edges and from V_{IH} (dc) and V_{IL} (ac) for falling edges.

For differential signals (e.g. $CK - \overline{CK}$) slew rate for rising edges is measured from $CK - \overline{CK} = -250$ mV to $CK - \overline{CK} = +500$ mV (250mV to -500 mV for falling edges).

c. VID is the magnitude of the difference between the input voltage on CK and the input voltage on \overline{CK} , or between DQS and \overline{DQS} for differential strobe.

2. DDR2 SDRAM AC timing reference load

The following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

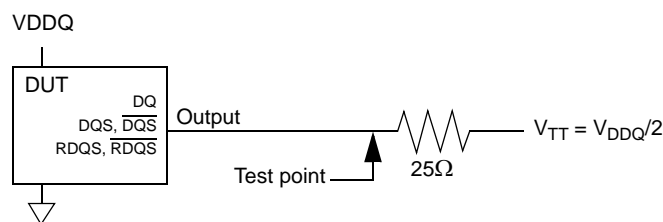


AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with V_{TT} . The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. \overline{DQS}) signal.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown below.



Slew Rate Test Load

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single

VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, \overline{DQS} . This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, \overline{DQS} , must be tied externally to VSS through a 20 ohm to 10 K ohm resistor to insure proper operation.

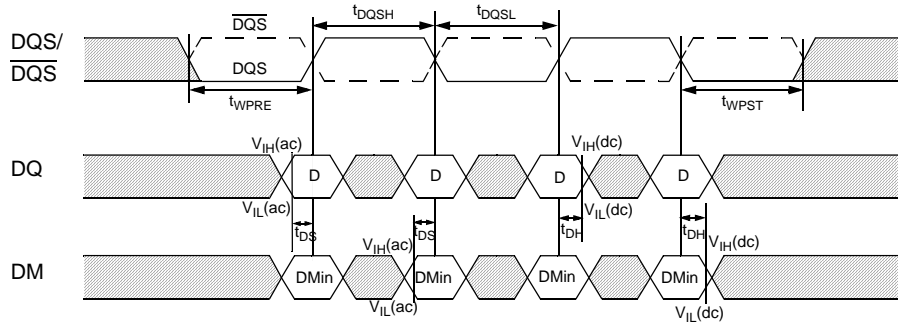


Figure -- Data input (write) timing

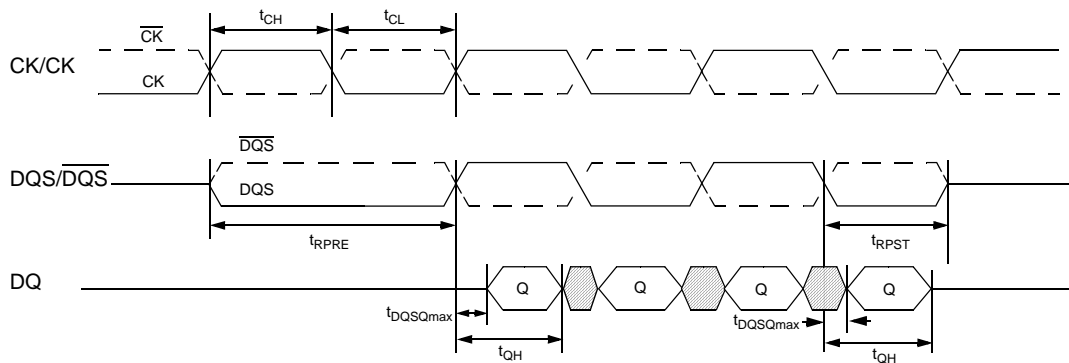


Figure -- Data output (read) timing

5. AC timings are for linear signal transitions. See System Derating for other signal transitions.
6. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
7. All voltages referenced to VSS.
8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/ supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for dedicated AC parameters

1. User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.
2. AL = Additive Latency
3. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS (min) have been satisfied.
4. A minimum of two clocks (2 * tCK) is required irrespective of operating frequency
5. Timings are guaranteed with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.
6. Timings are guaranteed with data, mask, and (DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

| tDS, tDH Derating Values(ALL units in 'ps', Note 1 applies to entire Table) | | | | | | | | | | | | | | | | | | | |
|---|-----|---------------------------------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|
| | | DQS, DQS Differential Slew Rate | | | | | | | | | | | | | | | | | |
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | | 0.8 V/ns | |
| | | tD S | tD H | tD S | tD H | tD S | tD H | tD S | tD H | tD S | tD H | tD S | tD H | tD S | tD H | tD S | tD H | tD S | tD H |
| DQ Slew rate V/ns | 2.0 | 125 | 45 | 125 | 45 | +125 | +45 | - | - | - | - | - | - | - | - | - | - | - | - |
| | 1.5 | 83 | 21 | 83 | 21 | +83 | +21 | 95 | 33 | - | - | - | - | - | - | - | - | - | - |
| | 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 12 | 12 | 24 | 24 | - | - | - | - | - | - | - | - |
| | 0.9 | - | - | -11 | -14 | -11 | -14 | 1 | -2 | 13 | 10 | 25 | 22 | - | - | - | - | - | - |
| | 0.8 | - | - | - | - | -25 | -31 | -13 | -19 | -1 | -7 | 11 | 5 | 23 | 17 | - | - | - | - |
| | 0.7 | - | - | - | - | - | - | -31 | -42 | -42 | -19 | -7 | -8 | 5 | -6 | 17 | 6 | - | - |
| | 0.6 | - | - | - | - | - | - | - | - | -43 | -59 | -31 | -47 | -19 | -35 | -7 | -23 | 5 | -11 |
| | 0.5 | - | - | - | - | - | - | - | - | - | - | -74 | -89 | -62 | -77 | -50 | -65 | -38 | -53 |
| | 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | -127 | -140 | -115 | -128 | -103 | -116 |

7. Timings are guaranteed with CK/CK differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.
8. tDS and tDH derating table (for DDR2- 400 / 533)
 - 1) For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the datasheet value to the derating value listed in above Table.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF (dc) and the first crossing of Vih (ac) min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF (dc) and the first crossing of Vil (ac) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF (dc) to ac region', use nominal slew rate for derating value (see Fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF (dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Fig b.)

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil (dc) max and the first crossing of VREF (dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih (dc) min and the first crossing of VREF (dc). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF (dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF (dc) level is used for derating value (see Fig d.)

Although for slow slew rates the total setup time might be negative(i.e. a valid input signal will not have reached VIH/IL (ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL (ac).

For slew rate in between the values listed in table x, the derating valued may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil (dc) max and the first crossing of VREF (dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih (dc) min and the first crossing of VREF (dc). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF (dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF (dc) level is used for derating value (see Fig d.)

Although for slow slew rates the total setup time might be negative(i.e. a valid input signal will not have reached VIH/IL (ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL (ac).

For slew rate in between the values listed in table x, the derating valued may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Fig. a Illustration of nominal slew rate for tIS, tDS

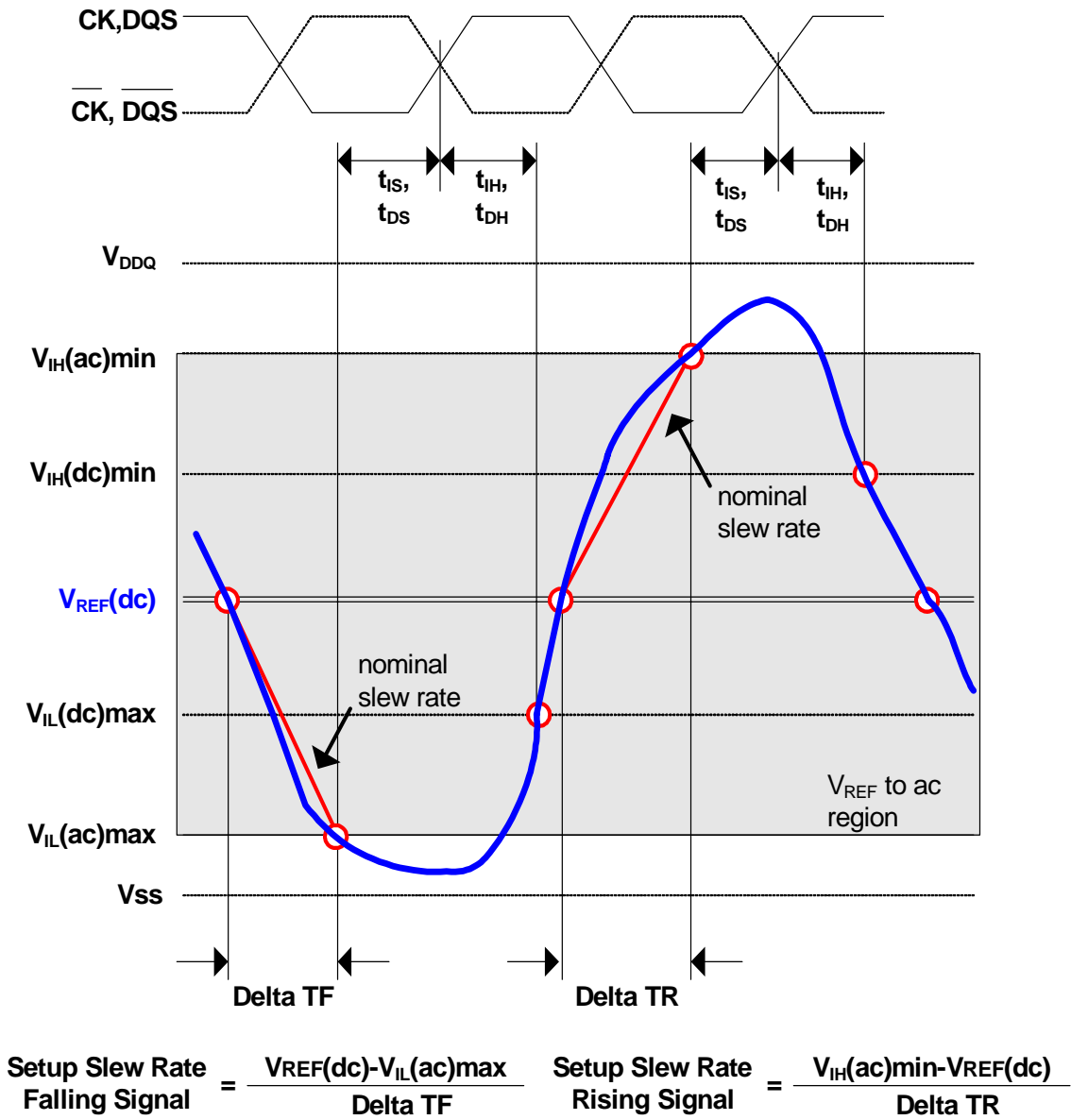
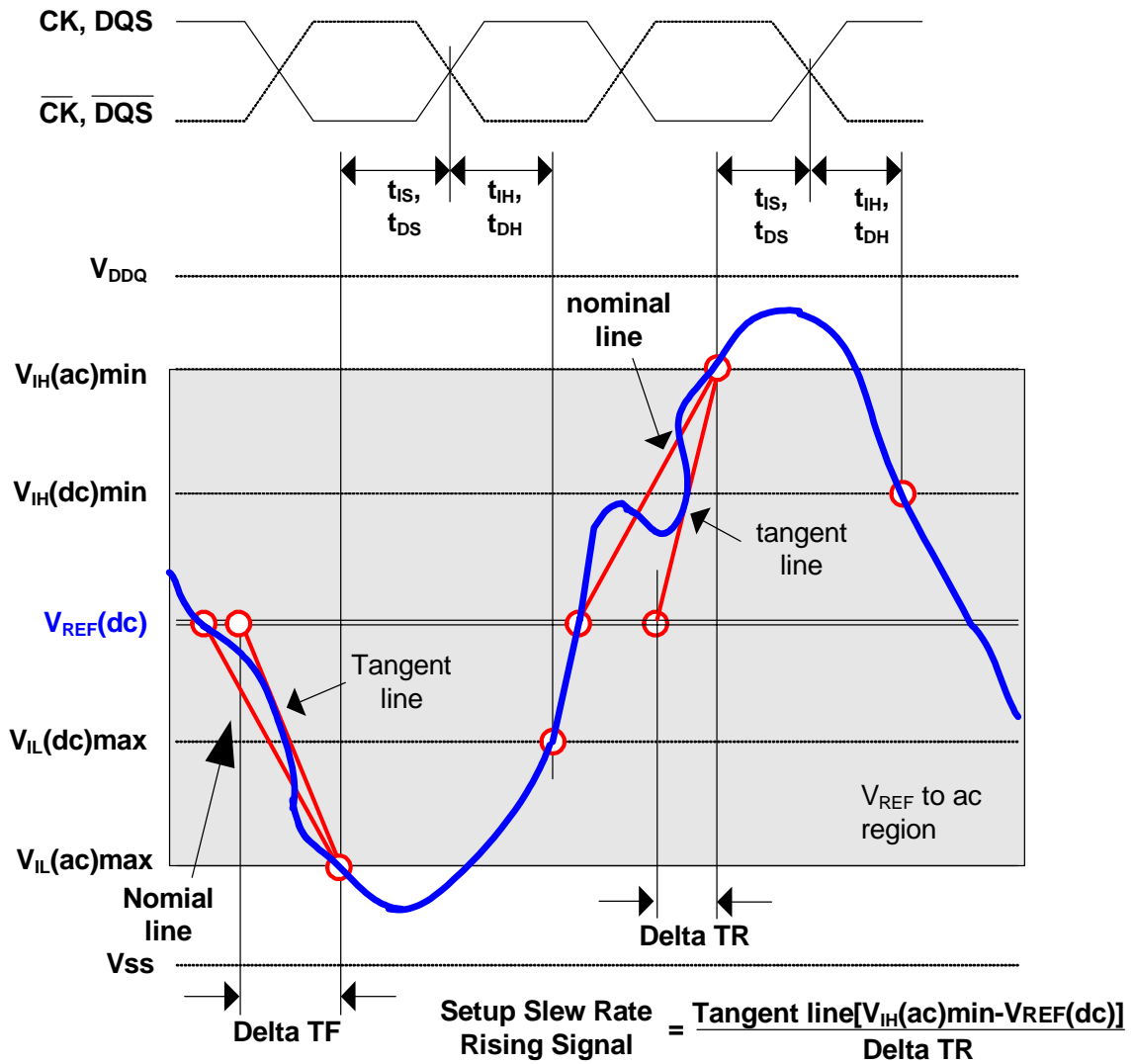


Fig. -B. Illustration of tangent line for tIS, tDS



$$\text{Setup Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{REF(dc)} - V_{IL(ac)max}]}{\Delta TF}$$

Fig. -C. Illustration of nominal line for t_{IH}, t_{DH}

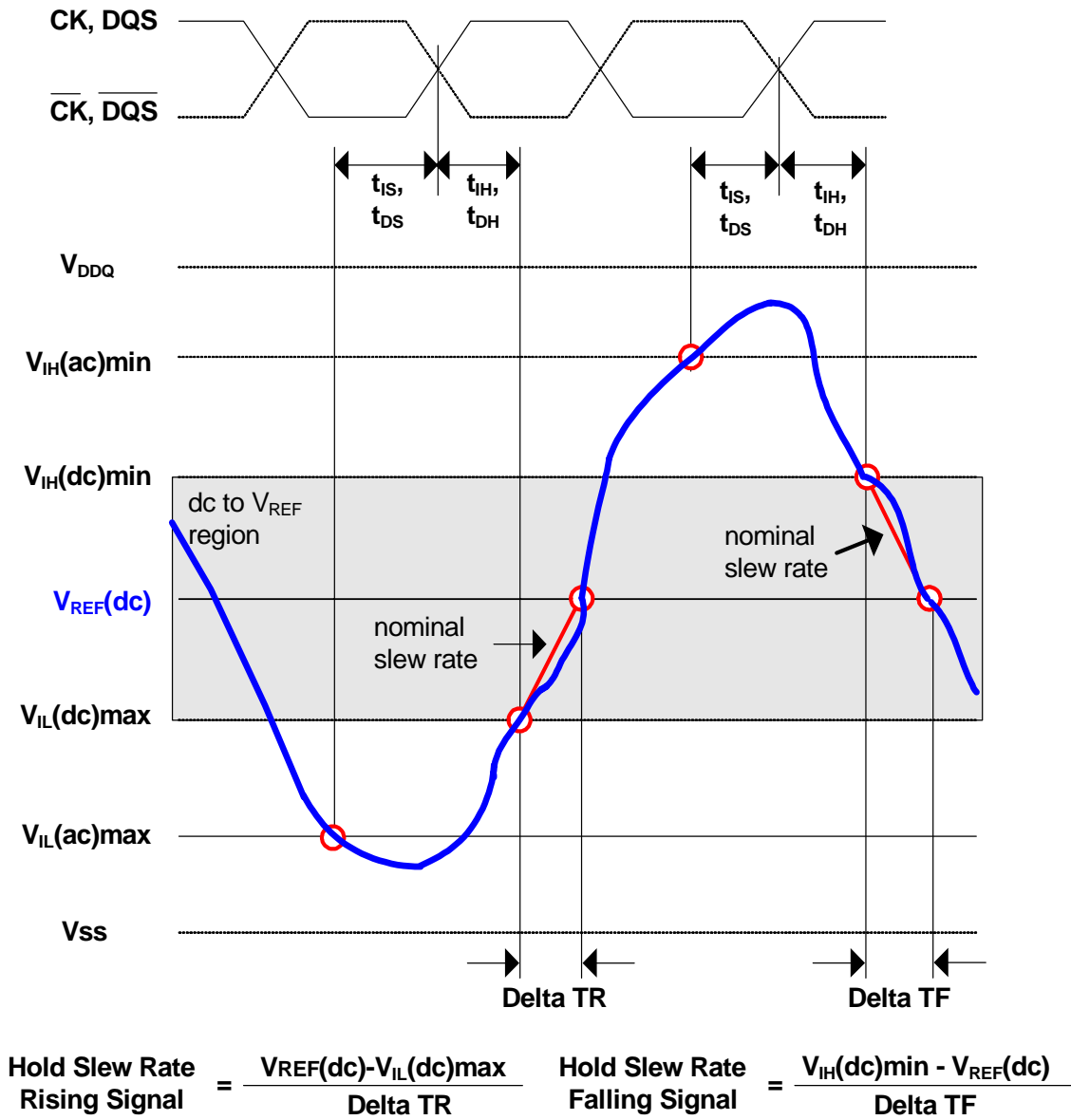
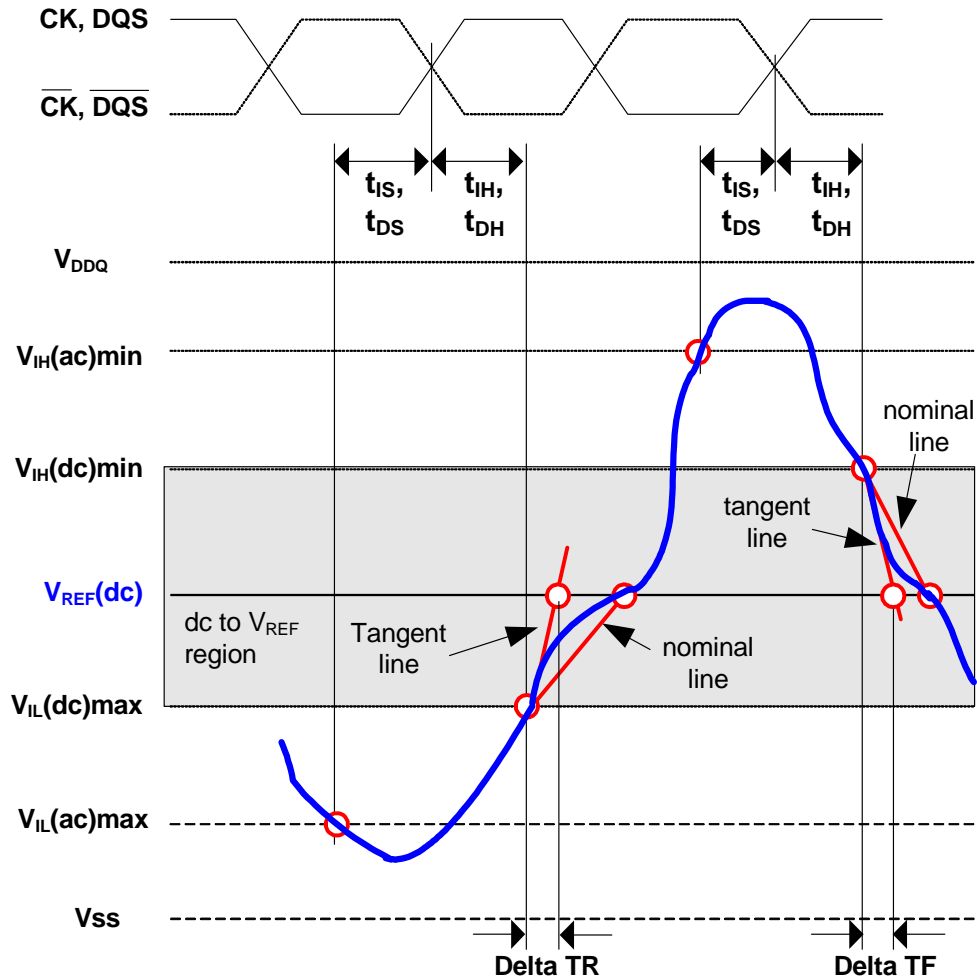


Fig. -d Illustration of tangent line for tIH, tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{REF}(dc) - V_{IL}(ac)max]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{IH}(ac)min - V_{REF}(dc)]}{\text{Delta TF}}$$

9. tIS and tIH (input setup and hold) derating

| tIS, tIH Derating Values for DDR2 400, DDR2 533 | | | | | | | | | | |
|---|-------|-------------------------------|-------|----------|-------|----------|------|-------|---|-------|
| | | CK, CK Differential Slew Rate | | | | | | Units | | Notes |
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | | | |
| | | tIS | tIH | tIS | tIH | tIS | tIH | | | |
| Command / Address Slew rate(V/ns) | 4.0 | +187 | +94 | +217 | +124 | +247 | +124 | ps | 1 | |
| | 3.5 | +179 | +89 | +209 | +119 | +239 | +149 | ps | 1 | |
| | 3.0 | +167 | +83 | +197 | +113 | +227 | +143 | ps | 1 | |
| | 2.5 | +150 | +75 | +180 | +105 | +210 | +135 | ps | 1 | |
| | 2.0 | +125 | +45 | +155 | +75 | +185 | +105 | ps | 1 | |
| | 1.5 | +83 | +21 | +113 | +51 | +143 | +81 | ps | 1 | |
| | 1.0 | +0 | 0 | +30 | +30 | +60 | 60 | ps | 1 | |
| | 0.9 | -11 | -14 | +19 | +16 | +49 | +46 | ps | 1 | |
| | 0.8 | -25 | -31 | +5 | -1 | +35 | +29 | ps | 1 | |
| | 0.7 | -43 | -54 | -37 | -53 | -7 | +6 | ps | 1 | |
| | 0.6 | -67 | -83 | -37 | -53 | -7 | -23 | ps | 1 | |
| | 0.5 | -100 | -125 | -80 | -95 | -50 | -65 | ps | 1 | |
| | 0.4 | -150 | -188 | -145 | -158 | -115 | -128 | ps | 1 | |
| | 0.3 | -223 | -292 | -255 | -262 | -225 | -232 | ps | 1 | |
| | 0.25 | -250 | -375 | -320 | -345 | -290 | -315 | ps | 1 | |
| | 0.2 | -500 | -500 | -495 | -470 | -465 | -440 | ps | 1 | |
| 0.15 | -750 | -708 | -770 | -678 | -740 | -648 | ps | 1 | | |
| 0.1 | -1250 | -1125 | -1420 | -1095 | -1065 | TBD | ps | 1 | | |

| tIS, tIH Derating Values for DDR2 667, DDR2 800 | | | | | | | | | | |
|---|-------|-------------------------------|------|----------|------|----------|------|-------|---|-------|
| | | CK, CK Differential Slew Rate | | | | | | Units | | Notes |
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | | | |
| | | tIS | tIH | tIS | tIH | tIS | tIH | | | |
| Command / Address Slew rate(V/ns) | 4.0 | +150 | +94 | +180 | +124 | +210 | +154 | ps | 1 | |
| | 3.5 | +143 | +89 | +173 | +119 | +203 | +149 | ps | 1 | |
| | 3.0 | +133 | +83 | +163 | +113 | +193 | +143 | ps | 1 | |
| | 2.5 | +120 | +75 | +150 | +105 | +180 | +135 | ps | 1 | |
| | 2.0 | +100 | +45 | +130 | +75 | +160 | +105 | ps | 1 | |
| | 1.5 | +67 | +21 | +97 | +51 | +127 | +81 | ps | 1 | |
| | 1.0 | 0 | 0 | +30 | +30 | +60 | 60 | ps | 1 | |
| | 0.9 | -5 | -14 | +25 | +16 | +55 | +46 | ps | 1 | |
| | 0.8 | -13 | -31 | +17 | -1 | +47 | +29 | ps | 1 | |
| | 0.7 | -22 | -54 | +8 | -24 | +38 | +6 | ps | 1 | |
| | 0.6 | -34 | -83 | -4 | -53 | -26 | -23 | ps | 1 | |
| | 0.5 | -60 | -125 | -30 | -95 | 0 | -65 | ps | 1 | |
| | 0.4 | -100 | -188 | -70 | -158 | -40 | -128 | ps | 1 | |
| | 0.3 | -168 | -292 | -138 | -262 | -108 | -232 | ps | 1 | |
| | 0.25 | -200 | -375 | -170 | -345 | -140 | -315 | ps | 1 | |
| | 0.2 | -325 | -500 | -295 | -470 | -265 | -440 | ps | 1 | |
| 0.15 | -517 | -708 | -487 | -678 | -457 | -648 | ps | 1 | | |
| 0.1 | -1000 | -1125 | -970 | -1095 | -940 | -1065 | ps | 1 | | |

1) For all input signals the total tIS (setup time) and tIH (hold) time) required is calculated by adding the datasheet value to the derating value listed in above Table.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}(dc)$ and the first crossing of $V_{IH}(ac)$ min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(dc)$ and the first crossing of $V_{IL}(ac)$ max. If the actual signal is always earlier than the nominal slew rate for line between shaded ' $V_{REF}(dc)$ to ac region', use nominal slew rate for derating value (see fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF}(dc)$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Fig b.)

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}(dc)$ max and the first crossing of $V_{REF}(dc)$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(dc)$. If the actual signal is always later than the nominal slew rate line between shaded ' dc to $V_{REF}(dc)$ region', use nominal slew rate for derating value (see Fig.c) If the actual signal is earlier than the nominal slew rate line anywhere between shaded ' dc to $V_{REF}(dc)$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF}(dc)$ level is used for derating value (see Fig d.)

Although for slow rates the total setup time might be negative(i.e. a valid input signal will not have reached $V_{IH/IL}(ac)$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}(ac)$.

For slew rates in between the values listed in table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

10. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

11. MIN (t CL, t CH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t CL and t CH). For example, t CL and t CH are = 50% of the period, less the half period jitter (t JIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT (crosstalk)) into the clock traces.

12. $T. QH = t HP - t QHS$, where: tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).

tQHS accounts for:

- 1) The pulse duration distortion of on-chip clock circuits; and
- 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS/\overline{DQS} and associated DQ in any given cycle.

14. $DAL = WR + RU \{tRP (ns)/tCK (ns)\}$, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer, round up to the next highest integer. tCK refers to the application clock period.

Example: For DDR533 at tCK = 3.75ns with tWR programmed to 4 clocks.

$$tDAL = 4 + (15ns/3.75ns) \text{ clocks} = 4+(4) \text{ clocks} = 8 \text{ clocks.}$$

15. The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in section 2.9.

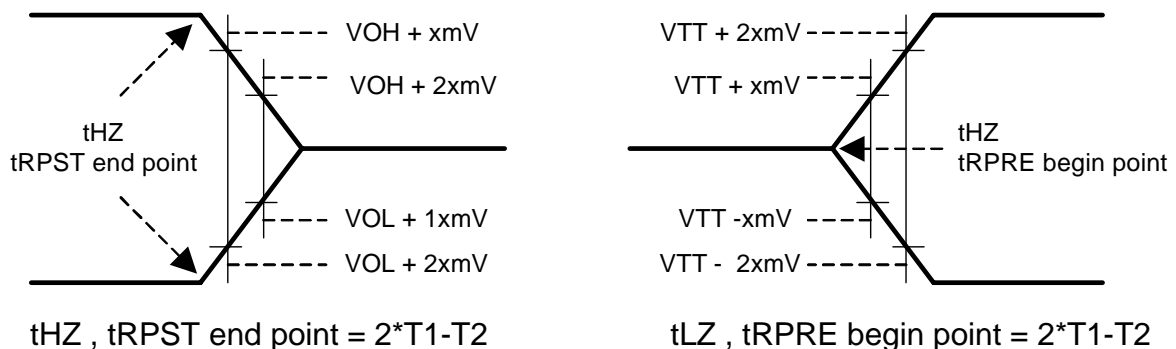
16. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
 ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

17. ODT turn off time min is when the device starts to turn off ODT resistance.

ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

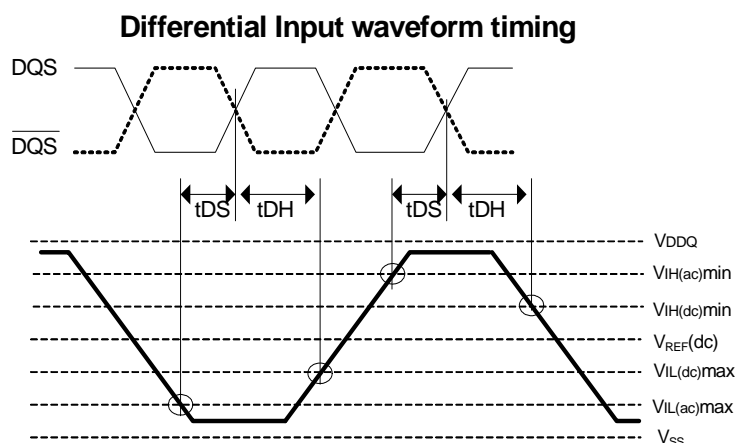
18. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Below figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

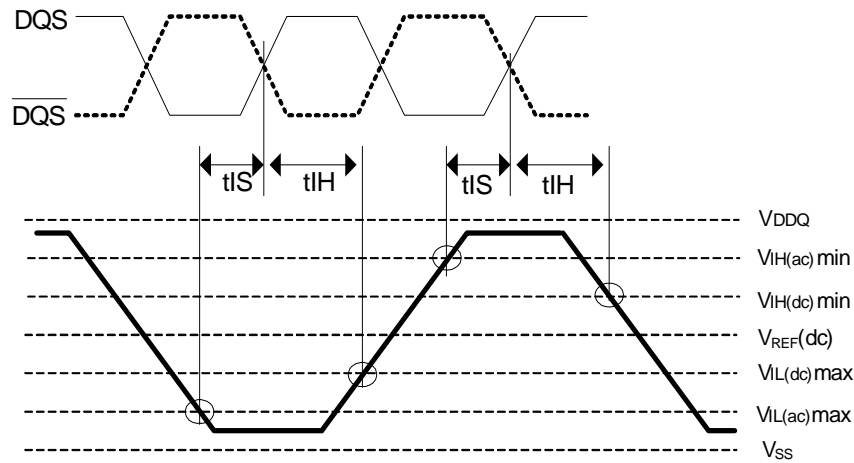
19. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Below figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE). Below Figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



20. Input waveform timing with differential data strobe enabled MR[bit10] =0, is referenced from the input signal crossing at the $V_{IH}(ac)$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL}(ac)$ level to the differential data strobe crosspoint for a falling signal applied to the device under test.

21. Input waveform timing with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH}(dc)$ level to the differential data strobe crosspoint for a rising signal and $V_{IL}(dc)$ to the differential data strobe crosspoint for a falling signal applied to the device under test.



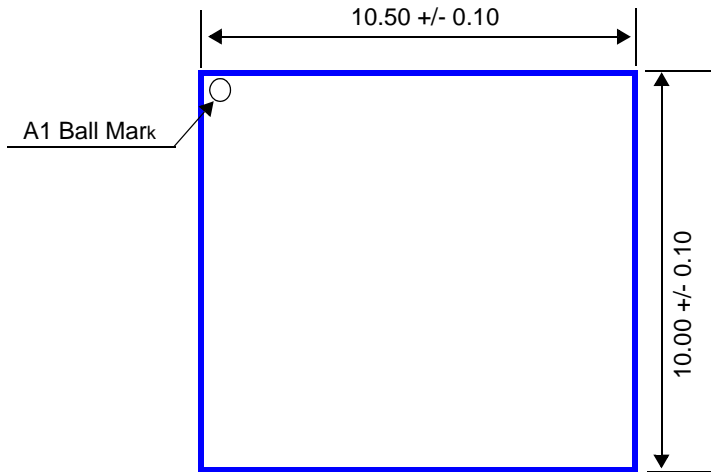


24. tWTR is at least two clocks ($2 \cdot tCK$) independent of operation frequency.
25. Input waveform timing with single-ended data strobe enabled $MR[\text{bit}10] = 1$, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between $V_{IL(dc)max}$ and $V_{IH(dc)min}$.
26. Input waveform timing with single-ended data strobe enabled $MR[\text{bit}10] = 1$, is referenced from the input signal crossing at the $V_{IH(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a rising signal, and from the input signal crossing at the $V_{IL(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between $V_{IL(dc)max}$ and $V_{IH(dc)min}$.
27. tCKE min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $tIS + 2 \cdot tCK + tIH$.

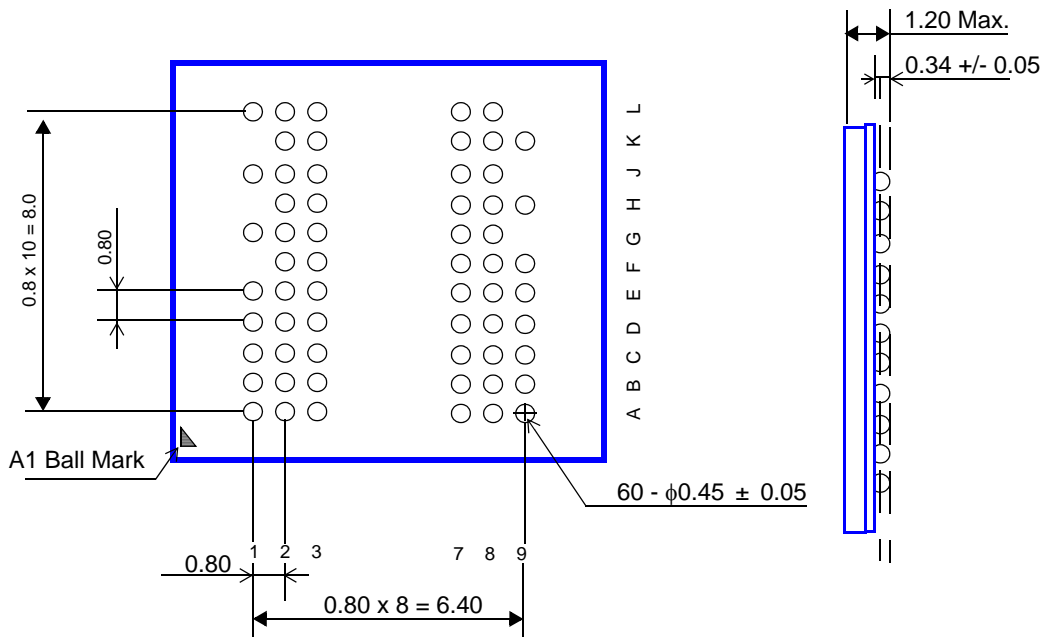
5. Package Dimensions

Package Dimension(x4,x8)

60Ball Fine Pitch Ball Grid Array Outline



<Top View>

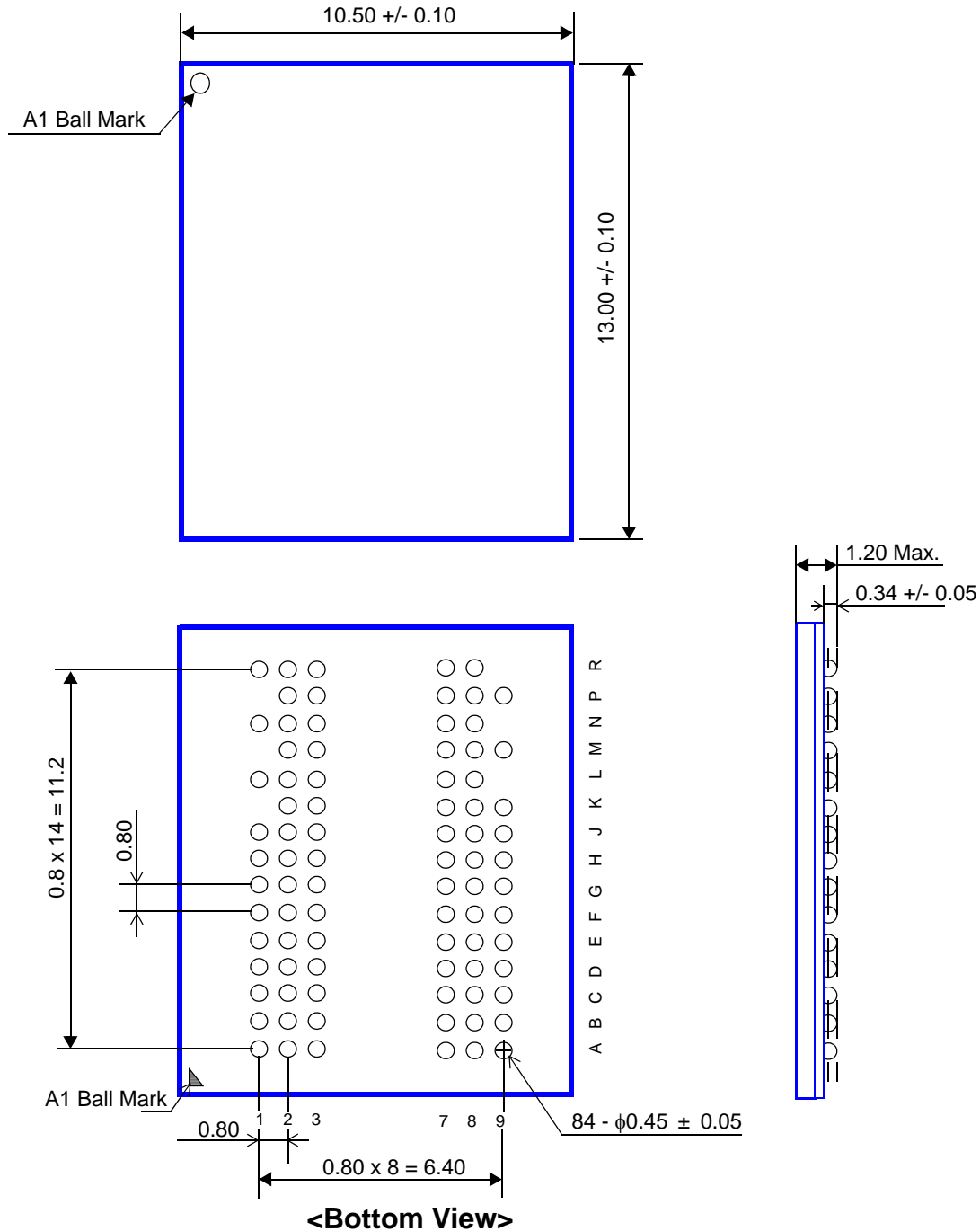


<Bottom View>

note: all dimension units are Millimeters.

Package Dimension(x16)

84Ball Fine Pitch Ball Grid Array Outline



note: all dimension units are Millimeters.