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**EM78P507N**

**8-Bit Microcontroller**

**Product  
Specification**

**DOC. VERSION 1.1**

**ELAN MICROELECTRONICS CORP.**

April 2016

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## APPENDIX

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## Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Official Release Version	2010/04/16
1.1	<ol style="list-style-type: none"> <li>Modified the Package Type and Name</li> <li>Added Ordering and Manufacturing Information</li> </ol>	2016/04/08

## 1 General Description

The EM78P507N is an 8-bit microprocessors designed and developed with low-power and high-speed CMOS technology. Integrated onto a single IC are on-chip Watchdog Timer (WDT), RAM, ROM, programmable real time clock counter (TCC), internal/external interrupt, power down mode, four 8-bit timers, SPI, I2C, UART, Current type DA Converter, 10 bits/24 channels AD, LVD, and tri-state I/O. It is equipped with a 6K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM).

With its enhanced OTP-ROM features, the EM78P507N provides a convenient way of developing and verifying user's programs. Moreover, this OTP-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development codes.

## 2 Features

- CPU Configuration
  - 6K×13 bits on-chip ROM
  - 272×8 bits on-chip registers
  - 8-level stacks for subroutine nesting
  - Dual clock operation mode
  - Four operation modes: Normal, Green, Idle, & Sleep
  - Two programmable Level Voltage Detector (LVD): 2.3V, 3.0V
  - Power-on reset Level Voltage: 1.9 reset level, 2.0 release
  - Less than 2.0 mA at 3.3V / 4 MHz
  - Typically 15  $\mu$ A, at 3V / 32kHz
  - Typically 2  $\mu$ A, during Sleep mode
- I/O Port Configuration
  - 6 bidirectional I/O ports: P7, P8, P9, PA, PB and PC
  - 45 I/O pins & 11 pin
  - 45 programmable pull-high I/O pins
  - 39 programmable open-drain I/O pins
  - External interrupt with Wake-up : P74~P77, P82~P83, PB0~PB3
- Operating Voltage
  - 2.2V~3.6V at -40°C~85°C (Industrial)
- Operating Frequency
  - Crystal/IRC/ERC oscillation circuit selected by code option for system clock
  - IRC oscillation circuit selected by code option or register
    - \* **Main Clock**
      - \* Crystal Mode:
        - DC~20 MHz/2clks@3.3V;
        - DC~100ns inst. cycle @ 3.3V;
        - DC~16 MHz/2 clks @ 2.2V;
        - DC~250ns inst. cycle @ 2.2V
      - \* ERC mode:
        - \* IRC mode: DC~16 MHz/2 clks @ 2.2V ;
        - DC~400ns inst. cycle @ 2.2V
    - \* **Sub Clock:**
      - IRC mode : 16kHz
- Special Features
  - Programmable free running watchdog timer
  - High ESD immunity
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Peripheral Configuration
  - One clock output pin can output the currently working frequency
  - 8-bit real time clock/counter (TCC)
  - 24-channel Analog-to-Digital Converter (ADC) with 12-bit resolution in Vref mode
  - Three 8-bit timers
  - 8-bit Timer 1, auto reload counter/timer which can be an interrupt source. Function modes: Timer, Toggle output, UART baud rate generator, Capture, & PWM
  - 8-bit Timer 2, auto reload timer which can be an interrupt source. Function modes: Timer, SPI baud rate generator, & PWM
  - Two sets of 8 bits auto reload counter/timer which can be cascaded to one 16-bit counter/timer
  - 8-bit Timer 3 with external clock source, can generate a 50% duty pulse output from T3OUT Pin.
  - Universal Asynchronous Receiver/Transmitter (UART) available (operates at 16 MHz/2Mbps, 2.2V)
  - I2C-bus function, including 7-bit/10-bit address 8-bit data transmit/ receive mode and 16 bytes buffer to save the data.
  - Serial Peripheral Interface (SPI)
  - Digital-to-Analog Converter (DAC) current type with 10-bit resolution
- Single instruction cycle commands
- 22 available interrupts: 10 external, 12 internal
  - TCC overflow interrupt
  - Ten external interrupts (wake-up from sleep mode)
  - Three timer interrupts
  - A/D converter interrupt
  - SPI interrupt
  - Two I2C interrupts
  - Three UART interrupts
  - Low voltage detect (LVD)

■ Package Type:

- 44 pin QFP/LQFP 10×10mm: EM78P507NQ/L44
- 48 pin LQFP 7×7mm: EM78P507NL48

**NOTE**

*These are Green products which do NOT contain hazardous substances.*

### 3 Pin Assignment

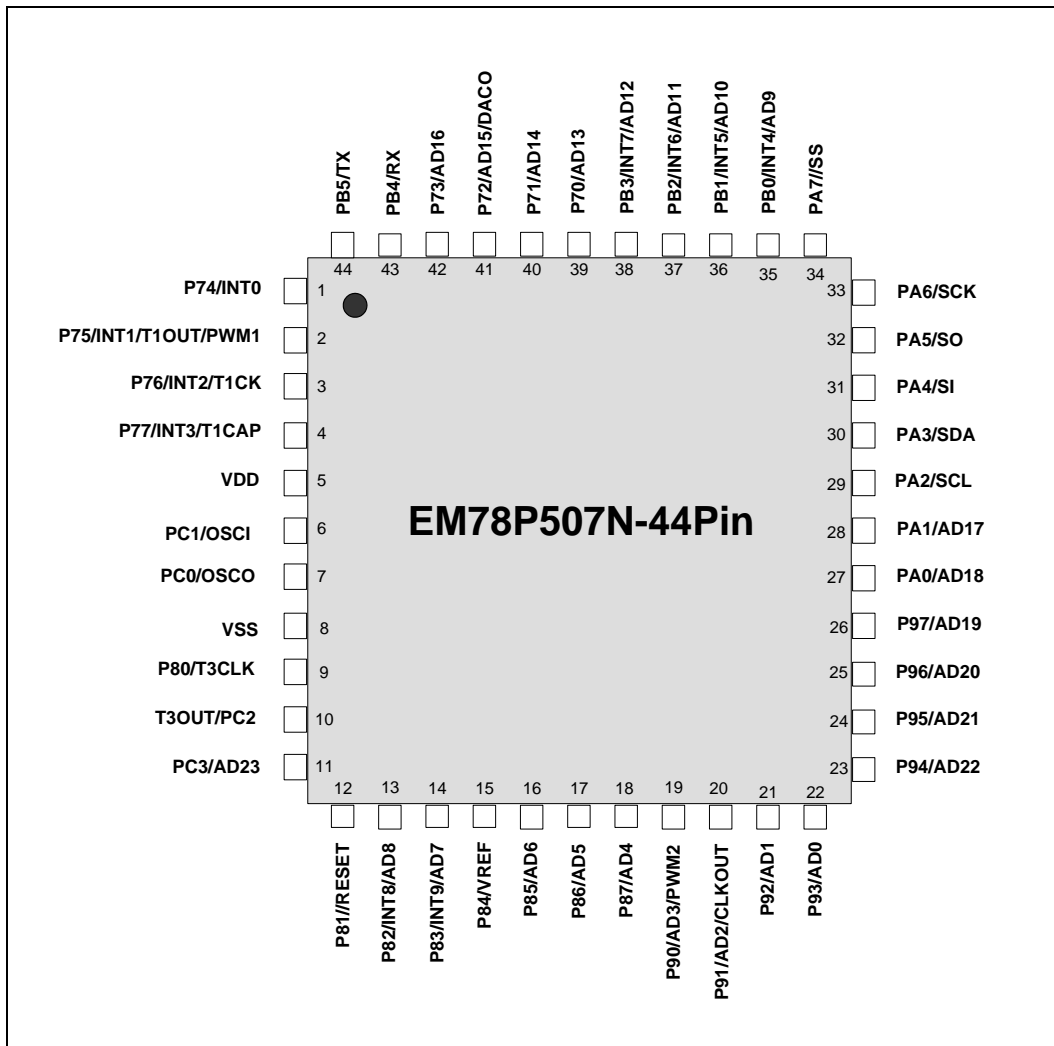


Figure 3-1a EM78P507N 44-pin QFP/LQFP Package



## 4 Pin Description

### 4.2 EM78P507N LQFP/QFP 44 pins

Symbol	Pin No.	Type	Function
OSCI	6	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	7	O	Crystal type: Output terminal for crystal oscillator or external clock input pin RC type: Clock output with a period of 1 instruction cycle time External clock signal input
P70 ~ P77	39~42 1~4	I/O	P70~P77 are bidirectional I/O pins P70 can be used as AD13 P71 can be used as AD14 P72 can be used as AD15, DACO P73 can be used as AD16 P74 can be used as INT0 P75 can be used as INT1, T1OUT, and PWM1 P76 can be used as INT2 and T1CK P77 can be used as INT3 and T1CAP
P80 ~ P87	9, 12 ~ 18	I/O	P80, P82~P87 are bidirectional I/O pins P81 only act as input pin P80 can be used as T3CLK P81 can be used as /RESET P82 can be used as INT8 and AD8 P83 can be used as INT9 and AD7 P84 can be used as Vref P85 can be used as AD6 P86 can be used as AD5 P87 can be used as AD4
P90 ~ P97	19 ~ 26	I/O	P90~P97 are bidirectional I/O pins P90 can be used as AD3 and PWM2 P91 can be used as AD2 and CLKOUT P92 can be used as AD1 P93 can be used as AD0 P94 can be used as AD22 P95 can be used as AD21 P96 can be used as AD20 P97 can be used as AD19

(Continuation)

Symbol	Pin No.	Type	Function
PA0 ~ PA7	27 ~ 34	I/O	PA0~PA7are bidirectional I/O pins PA0 can be used as AD18 PA1 can be used as AD17 PA2 can be used as SCL PA3 can be used as SDA PA4 can be used as SI PA5 can be used as SO PA6 can be used as SCK PA7 can be used as /SS
PB0 ~ PB5	35 ~ 38 43 ~ 44	I/O	PB0~PB5are bidirectional I/O pins PB0 can be used as INT4 and AD9 PB1 can be used as INT5 and AD10 PB2 can be used as INT6 and AD11 PB3 can be used as INT7 and AD12 PB4 can be used as RX PB5 can be used as TX
PC0 ~ PC3	7 ~ 6 10 ~ 11	I/O	PC0~PC3 are bidirectional I/O pins PC0 can be used as OSCO PC1 can be used as OSCI PC2 can be used as T3OUT PC3 can be used as AD23
/RESET	12	I	If it remains at logic low, the device will be reset. Wakes-up from Sleep mode when pins status changes. Voltage on /RESET must not be over VDD during Normal mode.
VDD	5	-	Power supply for IC emulation. Can be adjusted as per customer requirement.
VSS	6	-	Ground

## 4.1 EM78P507N LQFP 48 Pins

Symbol	Pin No.	Type	Function
OSCI	6	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	7	O	Crystal type: Output terminal for crystal oscillator or external clock input pin RC type: Clock output with a period of 1 instruction cycle time External clock signal input
P70 ~ P77	39~42 1~4	I/O	P70~P77 are bidirectional I/O pins P70 can be used as AD13 P71 can be used as AD14 P72 can be used as AD15, DACO P73 can be used as AD16 P74 can be used as INT0 P75 can be used as INT1, T1OUT, and PWM1 P76 can be used as INT2 and T1CK P77 can be used as INT3 and T1CAP
P80 ~ P87	9 12 ~ 18	I/O	P80, P82~P87 are bidirectional I/O pins P81 only act as intupt pin P80 can be used as T3CLK P81 can be used as /RESET P82 can be used as INT8 and AD8 P83 can be used as INT9 and AD7 P84 can be used as Vref P85 can be used as AD6 P86 can be used as AD5 P87 can be used as AD4
P90 ~ P97	19 ~ 26	I/O	P90~P97 are bidirectional I/O pins P90 can be used as AD3 and PWM2 P91 can be used as AD2 and CLKOUT P92 can be used as AD1 P93 can be used as AD0 P94 can be used as AD22 P95 can be used as AD21 P96 can be used as AD20 P97 can be used as AD19

(Continuation)

Symbol	Pin No.	Type	Function
PA0 ~ PA7	27 ~ 34	I/O	PA0~PA7are bidirectional I/O pins PA0 can be used as AD18 PA1 can be used as AD17 PA2 can be used as SCL PA3 can be used as SDA PA4 can be used as SI PA5 can be used as SO PA6 can be used as SCK PA7 can be used as /SS
PB0 ~ PB7	35 ~ 38 43 ~ 46	I/O	PB0~PB7are bidirectional I/O pins PB0 can be used as INT4 and AD9 PB1 can be used as INT5 and AD10 PB2 can be used as INT6 and AD11 PB3 can be used as INT7 and AD12 PB4 can be used as RX PB5 can be used as TX
PC0 ~ PC5	7 ~ 6 10 ~ 11 47 ~ 48	I/O	PC0~PC5 are bidirectional I/O pins PC0 can be used as OSCO PC1 can be used as OSCI PC2 can be used as T3OUT PC3 can be used as AD23
/RESET	12	I	If it remains at logic low, the device will be reset. Wakes-up from Sleep mode when pin status changes Voltage on /RESET must not be over VDD during Normal mode
VDD	5	-	Power supply for IC emulation. Can be adjusted as per customer requirement.
VSS	8	-	Ground

## 5 Block Diagram

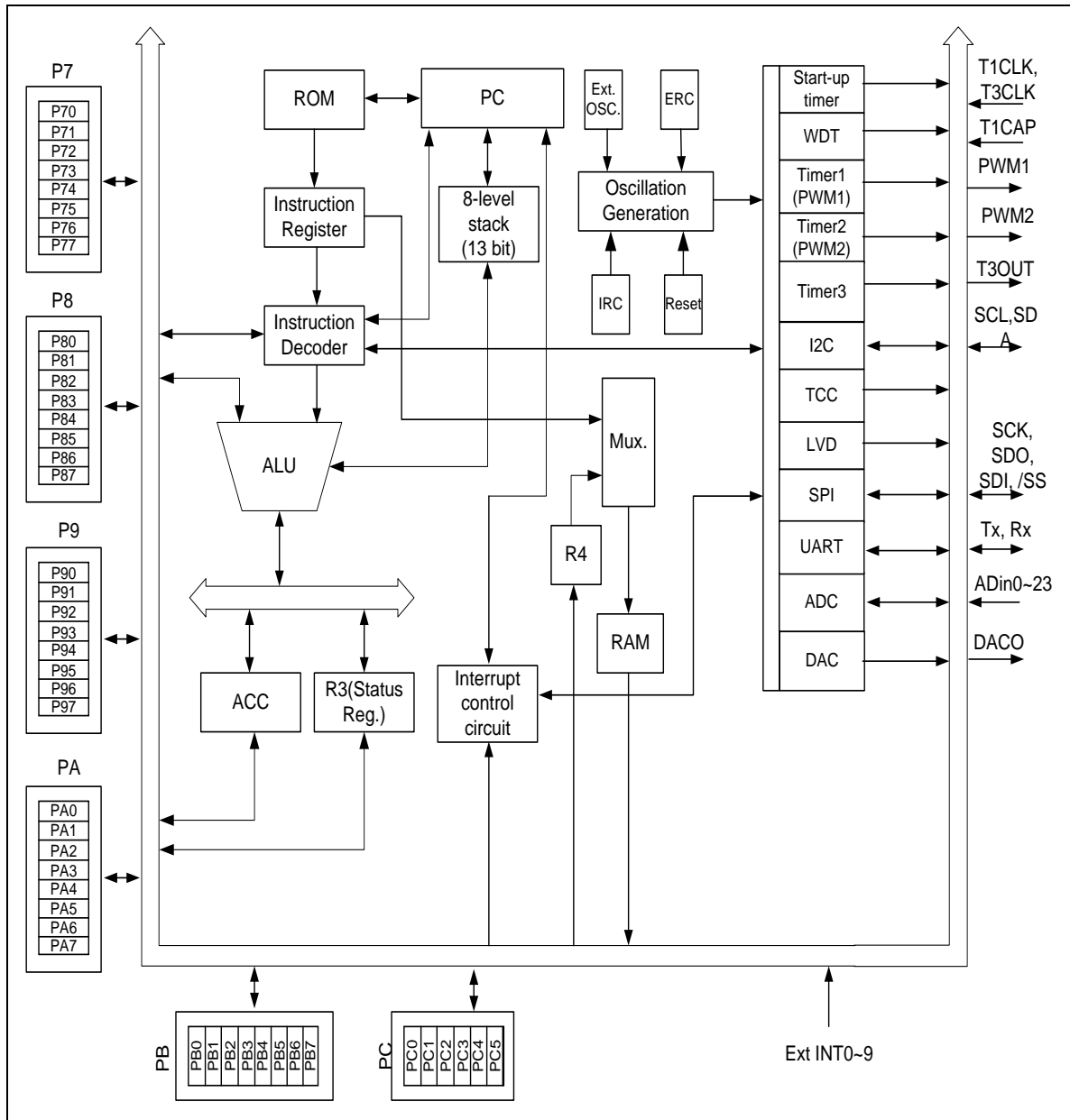


Figure 5-1 EM78P507N Functional Block Diagram

## 6 Function Description

### 6.1 Operational Registers

#### 6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

#### 6.1.2 R1 (ROM Page and RAM Bank Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PS2	PS1	PS0	0	BS2	BS1	BS0

**Bit 7:** Not used bits, fixed to "0" all the time.

**Bits 6~4 (PS2~PS0):** Page Select Registers used to select Pages 0~15. These are read only.

**Bit 3:** Not used bits, fixed to "0" all the time.

**Bits 2~0 (BS2~BS0):** RAM Bank Select Registers used to select Banks 0~7 for R20~R3F or Banks 0~7 for control register.

#### 6.1.3 R2 (Program Counter) and Stack

- R2 and hardware stacks are 10-bit wide. The structure is depicted in Figure 6-1.
- Generates 6K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are set to all "0"s upon a RESET condition.
- "JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 12 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 6K (212).
- "LCALL" instruction loads the lower 12 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 6K (212).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.

- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8~A9) of the PC remain unchanged.
- Any instruction except "ADD R2,A" that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth and the tenth bits (A8~A9) of the PC to remain unchanged.
- In the case of EM78P507N, the most significant bits (A12~A10) will be loaded with the contents of PS2~PS0 in the status register (R1) upon the execution of a "JMP", "CALL", or any other instruction set which are written to R2.
- **Program Counter Organization**

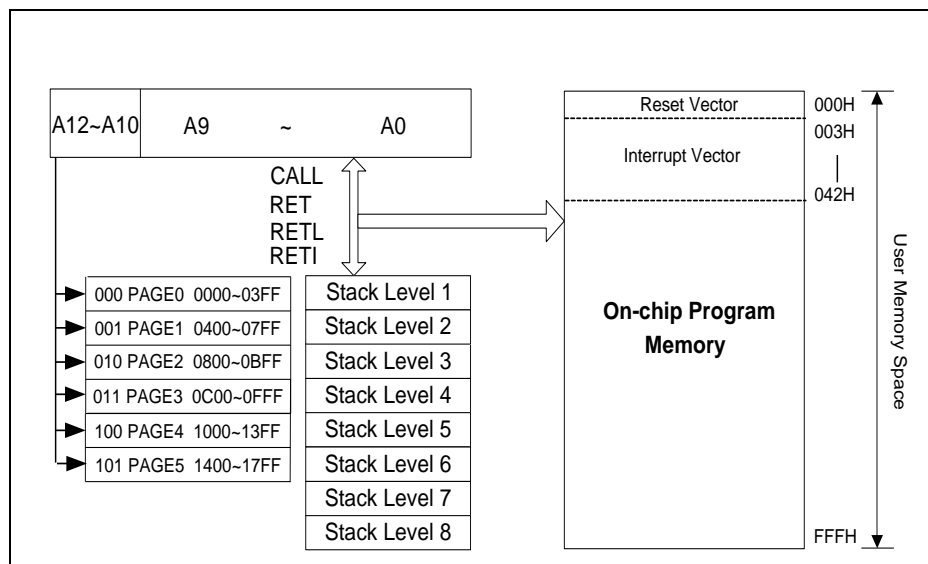


Figure 6-1 Program Counter Organization

**■ Data Memory Configuration**

Addr.	Bank 0 Registers	Bank 1 Registers	Bank 2 Registers	Bank 3 Registers	Bank 4 Registers	Bank 5 Registers	Bank 6 Registers	Bank 7 Registers
00	<b>R0</b> (Indirect Addressing Register, IAR)							
01	<b>R1</b> (ROM Page and RAM Bank Select Register, RPBSR)							
02	<b>R2</b> (Program Counter, PC)							
03	<b>R3</b> (Status Register, SR)							
04	<b>R4</b> (Select Indirect Address Register, RSR)							
05	<b>R5</b> (TBLP)	<b>R5</b> (ADCR1)	<b>R5</b> (T1CR)	<b>R5</b> (URC)	Reserve	Reserve	Reserve	<b>R5</b> (I2CCR1)
06	<b>R6</b> (TBHP)	<b>R6</b> (ADCR2)	<b>R6</b> (TSR)	<b>R6</b> (URS)	Reserve	Reserve	Reserve	<b>R6</b> (I2CCR2)
07	<b>R7</b> (Port 7)	<b>R7</b> (ADDL)	<b>R7</b> (T1PD)	<b>R7</b> (URRD)	<b>R7</b> (IOC7)	<b>R7</b> (P7PHCR)	<b>R7</b> (P7ODCR)	<b>R7</b> (I2CSA)
08	<b>R8</b> (Port 8)	<b>R8</b> (ADDH)	<b>R8</b> (T1TD)	<b>R8</b> (URTD)	<b>R8</b> (IOC8)	<b>R8</b> (P8PHCR)	<b>R8</b> (P8ODCR)	<b>R8</b> (I2CDA)
09	<b>R9</b> (Port 9)	<b>R9</b> (ADIC1)	<b>R9</b> (T2CR)	<b>R9</b> (URC2)	<b>R9</b> (IOC9)	<b>R9</b> (P9PHCR)	<b>R9</b> (P9ODCR)	<b>R9</b> (I2CA)
0A	<b>RA</b> (Port A)	<b>RA</b> (ADIC2)	<b>RA</b> (T2PD)	<b>RA</b> (SPIS)	<b>RA</b> (IOCA)	<b>RA</b> (PAPHCR)	<b>RA</b> (PAODCR)	<b>RA</b> (I2CDB)
0B	<b>RB</b> (Port B)	<b>RB</b> (ADIC3)	<b>RB</b> (T2TD)	<b>RB</b> (SPIC)	<b>RB</b> (IOCB)	<b>RB</b> (PBPHCR)	<b>RB</b> (PBODCR)	<b>RB</b> (DACDL)
0C	<b>RC</b> (SCCR)	<b>RC</b> (COCR)	<b>RC</b> (T3CR1)	<b>RC</b> (SPIR)	<b>RC</b> (IOCC)	<b>RC</b> (PCPHCR)	<b>RC</b> (Port C)	<b>RC</b> (DACDH)
0D	<b>RD</b> (TWTCCR)	Reserve	<b>RD</b> (T3CR2)	<b>RD</b> (SPIW)	Reserve	Reserve	Reserve	<b>RD</b> (DACC)
0E	<b>RE</b> (IMR)	<b>RE</b> (EIMR)	<b>RE</b> (T3PD)	<b>RE</b> (EIESH)	Reserve	Reserve	Reserve	Reserve
0F	<b>RF</b> (ISR)	<b>RF</b> (EISR)	<b>RF</b> (TCC)	<b>RF</b> (EIESL)	<b>RF</b> (WKCR)	Reserve	Reserve	<b>RF</b> (I2CCR3)
10 : 1F	General Registers (16x8 bits)							
20 : 3F	General Registers (32x8 bits)	General Registers (32x8 bits)	General Registers (32x8 bits)	General Registers (32x8 bits)	General Registers (32x8 bits)	General Registers (32x8 bits)	General Registers (32x8 bits)	General Registers (32x8 bits)

*Figure 6-2 Data Memory Configuration*

### 6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VDB	LVDEN	LVDS	T	P	Z	DC	C

**Bit 7 (VDB):** Voltage Detector. This bit is read only. When VDD pin voltage is lower than Vdet (selected by LVDS), this bit will be cleared.

**0:** Low voltage is detected

**1:** Low voltage is not detected or LVD function is disabled.

**Bit 6 (LVDEN):** Voltage Detect Enable bit

**0:** No action

**1:** Voltage detect enabled

**Bit 5 (LVDS):** Detect Voltage select bits

LVDS	Detect Voltage
0	2.3V
1	3.0V

**Bit 4 (T):** Time-out bit. Set to "1" by the "SLEP" and "WDTC" commands or during power-on and reset to "0" by WDT time-out. This bit is read only.

Event	T	P	Remark
WDT wake-up from Sleep mode	0	0	–
WDT time out (not Sleep mode)	0	1	–
/RESET wake-up from Sleep	1	0	–
Power up	1	1	–
Low pulse on /RESET	×	×	×: d'on't care

**Bit 3 (P):** Power-down bit. Set to "1" during power-on or by a "WDTC" command and reset to "0" by a "SLEP" command. This bit is read only.

**Bit 2 (Z):** Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

**Bit 1 (DC):** Auxiliary carry flag

**Bit 0 (C):** Carry flag

### 6.1.5 R4 (RAM Select Register)

**Bits 7 ~ 6:** Used to select Bank 0 ~ Bank 3

**Bits 5~0:** Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2 above for details.

### 6.1.6 Bank 0 R5 TBLP (Low Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit 7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0

**Bits 7 ~ 0 (RBit 7 ~ RBit 0):** Table Pointer Address Bits 0 ~7

### 6.1.7 Bank 0 R6 TBHP (High Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBSHL	0	0	RBit 12	RBit 11	RBit 10	RBit 9	RBit 8

**Bit 7 (TBSHL):** Table address high and low bit selection

**0:** Take the low 8 bits of machine code to the “TBLP” register.

**1:** Take the high 5 bits of machine code to the “TBHP” register.

**Bits 4 ~ 0 (RBit 12 ~ RBit 8):** Table Pointer Address Bits 12 ~ 8.

### 6.1.8 Bank 0 R7 ~ RB (Port 7 ~ Port B)

**R7 ~ RB:** These are all I/O registers.

### 6.1.9 Bank 0 RC SOCR (System Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	IDLE	0	0	CPUS

**Bits 7~4:** Not used bits, fixed to “0” all the time.

**Bit 3 (IDLE):** Idle Mode Enable bit. This bit will determine as to which mode to enter after SLEP instruction.

IDLE=“0”+SLEP instruction → Sleep mode.

IDLE=“1”+SLEP instruction → Idle mode.

**Bits 2 ~ 1:** Not used bits, fixed to “0” all the time.

**Bit 0 (CPUS):** CPU Oscillator Source select

**0:** sub-oscillator (Fs)

**1:** main oscillator (Fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator while the main oscillator is stopped.

■ CPU Operation Mode

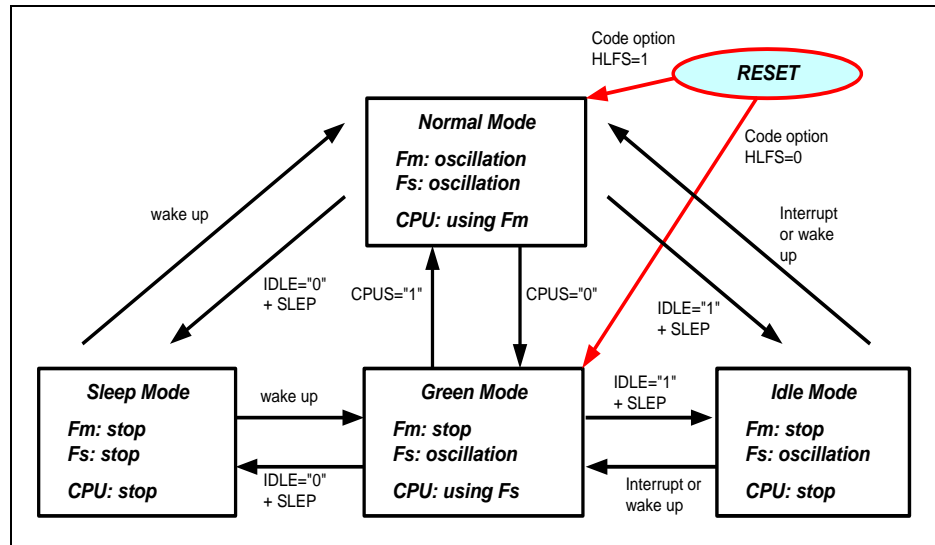


Figure 6-3 CPU Operation Mode

6.1.10 Bank 0 RD TWTCR (TCC and WDT Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	WPSR2	WPSR1	WPSR0	TCCS	TPSR2	TPSR1	TPSR0

**Bit 7 (WDTE):** Watchdog Timer Enable bit. This control bit is used to enable the watchdog timer.

**0:** Disable WDT function

**1:** Enable WDT function

**Bits 6 ~ 4 (WPSR2 ~ WPSR0):** WDT Prescaler bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:1 (Default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

**Bit 3 (TCCS):** TCC Clock Source select bit

**0:** Fm (main clock)

**1:** Fs (sub clock)

**Bits 2 ~ 0 (TPSR2 ~ TPSR0): TCC Prescaler bits**

TPSR2	TPSR1	TPSR0	TCC Rate
110	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

### 6.1.11 Bank 0 RE IMR (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1IE	LVDIE	ADIE	SPIE	URTIE	EXIE9	EXIE8	TCIE

**NOTE**

- "1" means with interrupt request; "0" means no interrupt occurs.
- Banks 0 ~ 1-RF can be cleared by instruction but cannot be set.
- Banks 0 ~ 1-RE are the interrupt mask registers.
- Reading Banks 0 ~ 1-RF will result to "logic AND" of Banks 0 ~ 1-RE and Banks 0 ~ 1-RF.

**Bits 7~0 (TCIE ~ T1IE) :** Interrupt Enable bit. Enable interrupt source respectively.

**0:** Disable interrupt

**1:** Enable interrupt

### 6.1.12 Bank 0 RF ISR (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1IF	LVDIF	ADIF	SPIIF	URTIF	EXIF9	EXIF8	TCIF

**NOTE**

- "1" means with interrupt request; "0" means no interrupt occurs.
- Bank 0-RF can be cleared by instruction but cannot be set.
- Bank 0-RE is the interrupt mask register.
- Reading Bank 0-RF will result to "logic AND" of Bank 0-RE and Bank 0-RF.

**Bit 7 (T1IF):** Timer 1 Interrupt Flag

**Bit 6 (LVDIF):** Low Voltage Detector Interrupt Flag

**Bit 5 (ADIF):** A/D Conversion Complete Interrupt Flag

**Bit 4 (SPIIF):** SPI Transfer Complete Interrupt Flag

**Bit 3 (URTIF):** UART Transmit Interrupt Flag

**Bit 2 (EXIF9):** External Interrupt 9 Occur Flag

**Bit 1 (EXIF8):** External Interrupt 8 Occur Flag

**Bit 0 (TCIF):** TCC Overflow Interrupt Flag

### 6.1.13 Bank 1 R5 ADCR1 (A/D Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADRUN	ADP	ADCK1	ADCK0	-	-	-	-

**Bit 7 (ADRUN):** Start AD Conversion

**0:** Reset on conversion completion by hardware. This bit cannot be reset by software.

**1:** Start Conversion

**Bit 6 (ADP):** A/D Power Control

**Bits 5 ~ 4 (ADCK1~ADCK0):** AD Conversion Time Select bits

ADCK1	ADCK0	Clock Source	Max. Operating Frequency (Fc)
0	0	Fc/4	1 MHz
0	1	Fc/16	4 MHz
1	0	Fc/32	8 MHz
1	1	Fc/64	16 MHz

**Bit 3 ~ Bit 0:** Not used bits, fixed to "0" all the time.

### 6.1.14 Bank 1 R6 ADCR2 (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADREF	0	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0

**Bit 7:** Not used bit, fixed to "0" all the time.

**Bit 6 (ADREF):** A/D Reference Voltage Input select.

**0:** Internal VDD, P84 is used as I/O

**1:** External reference pin, P84 is used as reference input pin.

**Bit 5:** Not used bit, fixed to "0" all the time.

**Bits 4~0 (ADIS4~ADIS0):** A/D Input select bits

ADIS4	ADIS3	ADIS2	ADIS1	ADIS0	Analog Input Pin
0	0	0	0	0	AD0
0	0	0	0	1	AD1
0	0	0	1	0	AD2
0	0	0	1	1	AD3
0	0	1	0	0	AD4
0	0	1	0	1	AD5
0	0	1	1	0	AD6
0	0	1	1	1	AD7
0	1	0	0	0	AD8
0	1	0	0	1	AD9
0	1	0	1	0	AD10
0	1	0	1	1	AD11
0	1	1	0	0	AD12
0	1	1	0	1	AD13
0	1	1	1	0	AD14
0	1	1	1	1	AD15
1	0	0	0	0	AD16
1	0	0	0	1	AD17
1	0	0	1	0	AD18
1	0	0	1	1	AD19
1	0	1	0	0	AD20
1	0	1	0	1	AD21
1	0	1	1	0	AD22
1	0	1	1	1	AD23

#### 6.1.15 Bank 1 R7 ADDL (A/D Low 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

**Bits 7~0 (ADD7~ADD0):** AD Low 8-bit Data Buffer

#### 6.1.16 Bank 1 R8 ADDH (A/D High 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	ADD11	ADD10	ADD9	ADD8

**Bits 7~4:** Not used bits, fixed to "0" all the time

**Bits 3~0 (ADD11~ADD8):** AD High 4-bit Data Buffer

### 6.1.17 Bank 1 R9 ADIC1 (A/D Input Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bits 7~0 (ADE7~ADE0): AD Input pin enable control.

- 0: AD acts as I/O pin
- 1: AD acts as analog input pin

### 6.1.18 Bank 1 RA ADIC2 (A/D Input Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE15	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8

Bits 7~0 (ADE15~ADE8): AD Input pin enable control.

- 0: Act as I/O pin
- 1: Act as analog input pin

### 6.1.19 Bank 1 RB ADIC3 (A/D Input Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE23	ADE22	ADE21	ADE20	ADE19	ADE18	ADE17	ADE16

Bits 7~0 (ADE23~ADE16): AD Input pin enable control.

- 0: Act as I/O pin
- 1: Act as analog input pin

### 6.1.20 Bank 1 RC COCR (Clock Output Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	RCM1	RCM0	CLKOE	CLKB1	CLKB0

Bits 7~5: Not used bits, fixed to "0" all the time.

Bits 4~3 (RCM1~0): IRC Mode select bits

RCM1	RCM0	Frequency
0	0	1 MHz
0	1	8 MHz
1	0	16 MHz
1	1	4 MHz

Bit 2 (CLKOE): Port 9.1 used as CLK Output Pin

- 1: No action
- 0: Enable CLK output

**Bits 1~0 (CLKB1~0):** Clock Output Rate select bits.

CLKB1	CLKB0	CLK Rate
0	0	1:1
0	1	1:2
1	0	1:4
1	1	1:8

### 6.1.21 Bank 1 RE EIMR (External Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXIE7	EXIE6	EXIE5	EXIE4	EXIE3	EXIE2	EXIE1	EXIE0

**Bits 7~0 (EXIE7~EXIE0):** Interrupt Enable bits. Enable interrupt source respectively.

### 6.1.22 Bank 1 RF EISR (External Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXIF7	EXIF6	EXIF5	EXIF4	EXIF3	EXIF2	EXIF1	EXIF0

**Bits 7~0 (EXIE7~EXIE0):** Interrupt Flag of External Interrupts 0~7 occur

### 6.1.23 Bank 2 R5 T1CR (Timer 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIS1	TIS0	T1MS2	T1MS1	T1MS0	T1P2	T1P1	T1P0

**Bits 7~6 (TIS1~0):** Timer 1 and Timer 2 Interrupt Type select bits. These two bits are used when the Timer operates in PWM mode.

TIS1	TIS0	Timer 1 and Timer 2 Interrupt Type Select
0	0	TXPD underflow
0	1	TXTD underflow
1	×	TXPD and TXTD underflow

**Bit 5~ (T1MS2~T1MS0):** Timer 1 Operation Mode select bits

T1MS2	T1MS1	T1MS0	Timer 1 Mode Select
0	0	0	Timer 1
0	0	1	T1OUT mode
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode falling Edge
1	0	0	UART Baud Rate Generator
1	0	1	PWM1
1	1	0	
1	1	1	

**Bits 2~0 (T1CSS1~T1CSS0):** Timer 1 Clock Source select bits

T1P2	T1P1	T1P0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

#### 6.1.24 Bank 2 R6 TSR (Timer 1 Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1MOD	TRCB	T1CSS1	T1CSS0	T2CSS	T1EN	0	T1OC

**Bit 7 (T1MOD):** Timer Operating Mode select bit

**0:** Two 8-bit Timers

**1:** Timer 1 and Timer 2 cascade to one 16-bit Timer

#### NOTE

*By setting T1MOD to "1", the Timer can cascade to one 16-bit Timer. This 16-bit Timer is controlled by Timer 1, including enable clock source and prescaler. Timer 1 is MSB and Timer 2 is LSB in period and duty values.*

**Bit 6 (TRCB):** Timers 1, 2, & 3 Read Control bit

**0:** When this bit is set to "0", read data from T1PD, T2PD or T3PD.

**1:** When this bit is set to "1", read data from T1PD, T2PD or T3PD, but the value is timer counter read value.

**Bits 5~4 (T1CSS1~0):** Timer 1 Clock Source select bits.

T1CSS1	T1CSS0	Timer 1 Clock Source Select
0	0	Fm
0	1	Fs
1	×	T1CK

**Bit 3 (T2CSS):** Timer 2 Clock Source select bit

**0:** Main clock with prescaler

**1:** Sub clock with prescaler

**Bit 2 (T1EN):** Timer 1 Start Bit

**0:** Timer 1 stop

**1:** Timer 1 start

**Bit 1:** Not used bits, fixed to “0” all the time.

**Bit 0 (T1OC):** Timer 1 Output Flip-Flop Control bit

**0:** T-FF is low

**1:** T-FF is high

### 6.1.25 Bank 2 R7 T1PD (Timer 1 Period Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]

**Bits 7~0 (PRD1[7]~PRD1[0]):** The content of this register is a period of Timer 1.

### 6.1.26 Bank 2 R8 T1TD (Timer 1 Duty Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TD1[7]	TD1[6]	TD1[5]	TD1[4]	TD1[3]	TD1[2]	TD1[1]	TD1[0]

**Bits 7~0 (TD1[7]~TD1[0]):** The content of this register is a period of Timer 1

### 6.1.27 Bank 2 R9 T2CR (Timer 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2IF	T2IE	T2EN	T2MS1	T2MS0	T2P2	T2P1	T2P0

**Bit 7(T2IF):** Interrupt Flag of Timer 2 Interrupt

**Bit 6(T2IE):** Timer 2 Interrupt Mask bit

**0:** Disable Timer 2 interrupt

**1:** Enable Timer 2 interrupt

**Bit 5 (T2EN):** Timer 2 Start Bit

**0:** Timer 2 stop

**1:** Timer 2 start

**Bits 4~3 (T2MS1~T2MS0):** Timer 2 Operation Mode select bits

T2MS1	T2MS0	Timer 2 Mode Select
0	0	Timer 2
0	1	SPI Baud Rate Generator
1	0	PWM2
1	1	

**Bits 2~0 (T2P2~T2P0):** Timer 2 Prescaler bits

T2P2	T2P1	T2P0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1 :32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

### 6.1.28 Bank 2 RA T2PD (Timer 2 Period Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]

**Bits 7~0 (PRD2[7] ~ PRD2[0]):** The content of this register is a period of Timer 2.

### 6.1.29 Bank 2 RB T2TD (Timer 2 Duty Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TD2[7]	TD2[6]	TD2[5]	TD2[4]	TD2[3]	TD2[2]	TD2[1]	TD2[0]

**Bits 7~0 (TD2[7] ~ TD2[0]):** The content of this register is a duty of Timer 2.

### 6.1.30 Bank 2 RC T3CR1 (Timer 3 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3IF	T3IE	T3EN	T3CSS1	T3CSS0	T3P2	T3P1	T3P0

**Bit 7 (T3IF):** Interrupt Flag of Timer 3 Interrupt

**Bit 6 (T3IE):** Timer 3 Interrupt Mask bit

**0:** Disable Timer 3 interrupt

**1:** Enable Timer 3 interrupt

**Bit 5 (T3EN):** Timer 3 Start Bit

**0:** Timer 3 stop

**1:** Timer 3 start

**Bits 4~3 (T3CSS1~T3CSS0):** Timer 3 Clock Source selects bits

T3CSS1	T3CSS0	Timer 3 Clock Source Select
0	0	Fm
0	1	Fs
1	x	T3CK

**Bits 2~0 (T3P2~T3P0):** Timer 3 Pre-scaler Bits

T3P2	T3P1	T3P0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1 : 4
0	1	0	1 : 8
0	1	1	1 : 16
1	0	0	1 : 32
1	0	1	1 : 64
1	1	0	1 : 128
1	1	1	1 : 256

### 6.1.31 Bank 2 RD T3CR2 (Timer 3 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	T3MS1	T3MS0

**Bits 7~2:** Not used bits, fixed to "0" all the time.

**Bits 1~0 (T3MS1~T3MS0):** Timer 3 Operation Mode select bits

T3MS1	T3MS0	Timer 3 Mode Select
0	0	Timer 3
0	1	T3OUT Mode
1	0	Reserved
1	1	Reserved

### 6.1.32 Bank 2 RE T3PD (Timer 2 Period Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]

**Bits 7~0 (PRD2[7] ~ PRD2[0]):** The content of this register is a period of Timer 2

### 6.1.33 Bank 2 RF TCC (Timer Clock/Counter)

Increased by the main oscillator clock (Fm), or sub oscillator clock (Fs). Controlled by TWTCR register.

### 6.1.34 Bank 3 R5 URC (UART Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

**Bit 7 (URTD8):** Transmission Data Bit 8

**Bits 6~5 (UMODE1~UMODE0):** UART Transmission Mode select bits.

UMODE1	UMODE0	UART Mode
0	0	Mode 1 : 7 bits
0	1	Mode 2 : 8 bits
1	0	Mode 3 : 9 bits
1	1	Reserved

**Bits 4~2 (BRATE2~BRATE0):** Transmit Baud Rate select ( $T_{uart} = F_c/16$ )

BRATE2	BRATE1	RRATE0	Baud Rate	e.g. $F_c = 8 \text{ MHz}$
0	0	0	$T_{uart}/13$	38400
0	0	1	$T_{uart}/26$	19200
0	1	0	$T_{uart}/52$	9600
0	1	1	$T_{uart}/104$	4800
1	0	0	$T_{uart}/208$	2400
1	0	1	$T_{uart}/416$	1200
1	1	0	Timer 1	
1	1	1	2M	

**Bit 1 (UTBE):** UART transfer buffer empty flag. Set to "1" when transfer buffer is empty. Reset to "0" automatically when in URTD register. The UTBE bit should be cleared by hardware when transmission is enabled. The UTBE bit is read-only. Therefore, writing to the URTD register is necessary when you want to start transmit shifting.

**Bit 0 (TXE):** Enable transmission  
**0:** Disable transmission  
**1:** Enable transmission

### 6.1.35 Bank 3 R6 URS (UART Status)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

**Bit 7(URRD8):** Receive Data Bit 8

**Bit 6 (EVEN):** Select Parity Check  
**0:** Odd parity  
**1:** EVEN parity

**Bits 5 (PRE):** Enable Parity Addition

**0:** Disable

**1:** Enable

**Bit 4 (PRERR):** Parity Error Flag

Set to “1” when parity error occurs and clear to “0” by software.

**Bit 3 (OVERR):** Overrun Error flag

Set to “1” when overrun error occurs and clear to “0” by software.

**Bit 2 (FMERR):** Framing Error Flag.

Set to “1” when framing error occurs and clear to “0” by software.

**Bit 1 (URBF):** UART Read Buffer Full Flag

Set to “1” when one character is received. Resets to “0” automatically when read from URS register. URBF will be cleared by hardware when Receive is enabled, and that URBF bit is read-only. Therefore, read URS register is necessary to avoid overrun error.

**Bit 0 (RXE):** Enable Receive

**0:** Disable Receive

**1:** Enable Receive

#### **6.1.36 Bank 3 R7 URRD (UART\_RD Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

**Bits 7~0 (URRD7~URRD0):** UART Receive Data Buffer. Read only.

#### **6.1.37 Bank 3 R8 URTD (UART\_TD Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

**Bits 7~0 (URTD7~URTD0):** UART Transmit Data Buffer. Write only.

#### **6.1.38 Bank 3 R9 URC1 (UART Status)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	UARTE	0	UINVEN	0	0	URRIF

**Bits 7~6:** Not used bits, fixed to “0” all the time.

**Bit 5 (UARTE):** UART Function Enable.

**0:** UART function disabled, PB4, PB5 act as general I/O.

**1:** UART function enabled, PB4, PB5 act as UART Rx & Tx pins respectively.

**Bit 4:** Not used bit, fixed to “0” all the time.

**Bit 3 (UINVEN):** Enable UART Tx and Rx Port Inverse Output

**0:** Disable Tx and Rx port inverse output.

**1:** Enable Tx and Rx port inverse output.

**Bits 2~1:** Not used bits, fixed to “0” all the time.

**Bit 0 (URRIF):** Interrupt flag of UART receive completed. Reset to “0” by software.

### 6.1.39 Bank 3 RA SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	0	OD3	OD4	0	RBF

**Bit 7 (DORD):** Data Shift Control bit

**0:** Shift left (MSB first)

**1:** Shift right (LSB first)

**Bits 5~6 (TD0~TD1):** SDO Status Output Delay Times Options

TD1	TD0	Delay Time
0	0	8 clk
0	1	16 clk
1	0	24 clk
1	1	32 clk

**Bit 4:** Not used bit, fixed to “0” all the time.

**Bit 3 (OD3):** Open-drain Control bit

**0:** Open-drain disabled for SDO

**1:** Open-drain enabled for SDO

**Bit 2 (OD4):** Open-Drain Control bit

**0:** Open-drain disabled for SCK

**1:** Open-drain enabled for SCK

**Bit 1:** Not used bit, fixed to “0” all the time.

**Bit 0 (RBF):** Read Buffer Full Flag

**0:** Receive is not completed and SPIR has not fully exchanged data

**1:** Receive is completed and SPIR has fully exchanged data.

### 6.1.40 Bank 3 RB SPIC (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIEN	SRO	SSE	SDOC	SBR2	SBR1	SBR0

**Bit 7 (CES):** Clock Edge Select Bit

**0:** Data shift out on a rising edge, and shifts in on a falling edge. Data is on hold during low-level.

**1:** Data shift out on a falling edge, and shifts in on a rising edge. Data is on hold during high-level.

**Bit 6 (SPIEN):** SPI Enable bit

**0:** Disable SPI mode

**1:** Enable SPI mode

**Bit 5 (SRO):** SPI Read Overflow bit

**0:** No overflow

**1:** A new data is received while the previous data is still being held in the SPIR register. In this situation, the data in SPIS register is destroyed. To avoid setting this bit, you should read the SPIRB register although only transmission is implemented. This can only occur during Slave mode.

**Bit 4 (SSE):** SPI Shift Enable bit

**0:** Reset as soon as the shift is completed, and the next byte is read to shift.

**1:** Start to shift, and kept on "1" while the current byte is still being transmitted.

**Bit 3 (SDOC):** SDO Output Status Control Bit

**0:** After the serial data is output, the SDO remains high.

**1:** After the serial data is output, the SDO remains low.

**Bits 2~0 (SBR2~SBR0):** SPI Baud Rate<sup>1</sup> select bits

SBR2	SBR1	SBR0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Timer 2
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

<sup>1</sup> If EM78P507N acts as the Master or Slave device to transmit and receive data, be sure to operate at Baud Rate lower than 3MHz and ensure that the operating voltage is higher than 2.5V.

#### 6.1.41 Bank 3 RC SPIR (SPI Read Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bits 7~0 (SRB7 ~ SRB0): SPI Read Data Buffer

#### 6.1.42 Bank 3 RD SPIW (SPI Write Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bits 7~0 (SWB7 ~ SWB0): SPI Read Data Buffer

#### 6.1.43 Bank 3 RE EIESH (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIES7	EIES6	EIES5	EIES4	EIES3	EIES2	EIES1	EIES0

Bits 7~0 (EIES7 ~ EIES0): External Interrupts 0~7 Edge Select Bit

0: Falling edge interrupt

1: Rising edge interrupt

#### 6.1.44 Bank 3 RF EIESL (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDWE	I2CWE	SPIWE	ADWK	INTWK9	INTWK8	EIES9	EIES8

**Bit 7 (LVDWE):** LVD Wake-up Function Enable bit

0: Disable

1: Enable

**Bit 6 (I2CWE):** I2C Receive Wake-up Function Enable bit

0: Disable

1: Enable

**Bit 5 (SPIWE):** SPI Receive Wake-up Function Enable bit

0: Disable

1: Enable

**Bit 4 (ADWK):** AD Converter Wake-up Function Enable bit

0: Disable

1: Enable

**Bit 3 (INTWK9):** External Interrupts 9 Wake-up Function Enable bit

0: Disable

1: Enable

**Bit 2 (INTWK8):** External Interrupts 8 Wake-up Function Enable Bit

**0:** Disable

**1:** Enable

**Bits 1~0 (EIES9 ~ EIES8):** External Interrupts 9~8 Edge Select Bit

**0:** Falling edge interrupt

**1:** Rising edge interrupt

#### **6.1.45 Bank 4 R7 IOC7 (Port 7 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

**Bits 7~0 (IOC77~IOC70):** Port 7 8-Bit I/O Direction Control Register

**0:** Define Port 7 as output port

**1:** Define Port 7 as input port

#### **6.1.46 Bank 4 R8 IOC8 (Port 8 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

**Bits 7~0 (IOC87~IOC80):** Port 8 8-Bit I/O Direction Control Register. P8.1 only acts as input pin.

**0:** Define Port 8 as output port

**1:** Define Port 8 as input port

#### **6.1.47 Bank 4 R9 IOC9 (Port 9 I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90

**Bits 7~0 (IOC97~IOC90):** Port 9 8-Bit I/O Direction Control Register

**0:** Define Port 9 as output port

**1:** Define Port 9 as input port

#### **6.1.48 Bank 4 RA IOCA (Port A I/O Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCA7	IOCA6	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0

**Bits 7~0 (IOCA7~IOCA0):** Port A 8-Bit I/O Direction Control Register

**0:** Define Port A as output port

**1:** Define Port A as input port

#### 6.1.49 Bank 4 RB IOCB (Port B I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0

Bits 7~0 (IOCB7~IOCB0): Port B 8-Bit I/O Direction Control Register

0: Define Port B as output port

1: Define Port B as input port

#### 6.1.50 Bank 4 RC IOCC (Port C I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0

Bits 7~ 6: Not used fixed "0"

Bits 5~0 (IOCC5~IOCC0): Port C 6-Bit I/O Direction Control Register

0: Define Port C as output port

1: Define Port C as input port

#### 6.1.51 Bank 4 RF WKCR (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTWK7	INTWK6	INTWK5	INTWK4	INTWK3	INTWK2	INTWK1	INTWK0

Bits 7~ 0 (INTWK7 ~ INTWK0): External Interrupts 7~0 Wake-up Function Enable Bits

0: Disable

1: Enable

#### 6.1.52 Bank 5 R7 P7PHCR (Port 7 Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH67	PH73	PH72	PH71	PH70

Bits 7~0 (PH77~PH70): Port 7 8-bit I/O Pull-high Control Registers

0: Pull-high disabled

1: Pull-high enabled

#### 6.1.53 Bank 5 R8 P8PHCR (Port 8 Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH87	PH86	PH85	PH84	PH83	PH82	0	PH80

Bits 7~0 (PH87~PH80): Port 8 8-bit I/O Pull-high Control Registers

0: Pull-high disable

1: Pull-high enable

#### 6.1.54 Bank 5 R9 P9PHCR (Port 9 Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH97	PH96	PH95	PH94	PH93	PH92	PH91	PH90

**Bits 7~0 (PH97~PH90):** Port 9 8-bit I/O Pull-high Control Registers.

0: Pull-high disabled

1: Pull-high enabled

#### 6.1.55 Bank 5 RA PAPHCR (Port A Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PHA7	PHA6	PHA5	PHA4	PHA3	PHA2	PHA1	PHA0

**Bits 7~0 (PHA7~PHA0):** Port A 8-bit I/O Pull-high Control Registers.

0: Pull-high disable

1: Pull-high enable

#### 6.1.56 Bank 5 RB PBPHCR (Port B Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PHB7	PHB6	PHB5	PHB4	PHB3	PHB2	PHB1	PHB0

**Bits 7~0 (PHB7~PHB0):** Port B 8-bit I/O Pull high Control Registers.

0: Pull-high disabled

1: Pull-high enabled

#### 6.1.57 Bank 5 RC PCPHCR (Port C Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0

**Bits 7~0 (PHC7~PHC0):** Port C 8-bit I/O Pull-high Control Registers.

0: Pull-high disabled

1: Pull-high enabled

#### 6.1.58 Bank 6 R7 P7ODCR (Port 7 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70

**Bits 7~0 (OD77~OD70) :** Port 7 8-bit I/O Open-drain Control Registers.

0: Open Drain disable

1: Open Drain enable

### 6.1.59 Bank 6 R8 P8ODCR (Port 8 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD87	OD86	OD85	OD84	OD83	OD82	0	OD80

Bits 7~0 (OD87~OD80): Port 8 8-bit I/O Open Drain Control Registers

- 0: Open Drain disabled
- 1: Open Drain enabled

### 6.1.60 Bank 6 R9 P9ODCR (Port 9 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90

Bits 7~0 (OD97~OD90): Port 9 8-bit I/O Open-drain Control Registers

- 0: Open-drain disabled
- 1: Open-drain enabled

### 6.1.61 Bank 6 RA PAODCR (Port A Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ODA7	ODA6	ODA5	ODA4	ODA3	ODA2	ODA1	ODA0

Bits 7~0 (ODA7~ODA0) : Port A 8-bits I/O Open-drain Control Registers.

- 0: Open-drain disabled
- 1: Open-drain enabled

### 6.1.62 Bank 6 RB PBODCR (Port B Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0

Bits 7~0 (ODB7~ODB0): Port B 8-bit I/O Open-drain Control Registers.

- 0: Open-drain Disable
- 1: Open-drain Enable

### 6.1.63 Bank 6 RC (Port C)

RC is an I/O register

### 6.1.64 Bank 7 R5 I2CCR1 (I2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY

**Bit 7 (Strobe/Pend):** In Master mode, it is used as strobe signal to control the I2C circuit to send SCL clock. Reset automatically after receiving or transmitting handshake signal (ACK or nACK).

In Slave mode, it is used as pending signal. You should clear it after writing data into the Tx buffer or reading data from Rx buffer to inform Slave I2C circuit to release the SCL signal.

**Bit 6 (IMS):** I2C Master/Slave mode select bit.

**0:** Slave

**1:** Master

**Bit 5 (ISS):** I2C Fast/Standard mode select bit.

**0:** Standard mode (100K bit/s)

**1:** Fast mode (400K bit/s)

**Bit 4 (STOP):** In Master mode, if STOP=1 and R/nW=1, then EM78P507N must return a nACK signal to the Slave device before sending a STOP signal. If STOP=1 and R/nW=0 then EM78P507N sends a STOP signal after receiving an ACK signal. Reset when the EM78P507N sends a STOP signal to the Slave device.

In Slave mode, if STOP=1 and R/nW=0 then the EM78P507N must return a nACK signal to the master device.

**Bit 3 (SAR\_EMPTY):** Set when the EM78P507N transmits a 1-byte data from the I2C Slave Address Register and receive an ACK (or nACK) signal. Reset when the MCU writes a 1-byte data to the I2C Slave Address Register.

**Bit 2 (ACK):** The ACK condition bit is set to "1" by hardware when the device responds with an acknowledge (ACK). Resets when the device responds with a not-acknowledge (nACK) signal.

**Bit 1 (FULL):** Set by hardware when I2C Receive Buffer Register is full. Reset by hardware when the MCU reads data from I2C Receive Buffer Register.

**Bit 0 (EMPTY):** Set by hardware when the I2C Transmit Buffer Register is empty and receives an ACK (or nACK) signal. Reset by hardware when the MCU writes new data to the I2C Transmit Buffer Register.

### 6.1.65 Bank 7 R6 I2CCR2 (I2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CRIF	I2CRIE	I2CTIF	I2CTIE	I2CTS1	I2CTS0	I2CCS	I2CEN

**Bit 7 (I2CRIF):** I2C Receive Interrupt Flag. Set when the I2C receives a 1 byte data and responds with an ACK signal. Reset by firmware or I2C disabled.

**Bits 6 (I2CRIE):** I2C Interface Receive Interrupt Enable bit

**0:** Disable Interrupt

**1:** Enable Interrupt

**Bit 5 (I2CTIF):** I2C Transmit Interrupt Flag. Set when I2C transmits 1 byte data and responds with an ACK signal. Reset by firmware or I2C disabled.

**Bits 4 (I2CTIE):** I2C Interface Tx Interrupt Enable bit

**0:** Disable Interrupt

**1:** Enable Interrupt

**Bits 3~2 (I2CTS1~I2CTS0):** I2C Transmit Clock Source Select bits (When I2CCS=0). I2C source must be low 6 MHz.

I2CTS1	I2CTS0	Source	Max. Operating Fm(MHz)
0	0	Fm/1	4
0	1	Fm/2	8
1	×	Fm/4	16

**Bit 1 (I2CCS):** I2C Clock Source Select Bit

**0:** Fm (main clock)

**1:** Fs (sub clock)

**Bit 0 (I2CEN):** I2C Enable bit

**0:** Disable I2C mode

**1:** Enable I2C mode

### 6.1.66 Bank 7 R7 I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW

**Bits 7~1 (SA6~SA0):** When EM78P507N functions as Master device for I2C application, these bits are used as the Slave device address registers.

**Bit 0 (IRW):** When EM78P507N functions as Master device for I2C application, this bit is used as Read/Write transaction control bit.

**0:** Write

**1:** Read

### 6.1.67 Bank 7 R8 I2CDA (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

**Bits 7~0 (DA7~DA0):** When the EM78P507N is used as a Slave device for I2C application, these bits store the registers address of EM78P507N. The address register is used to identify the data on the I2C bus to extract the message delivered to the EM78P507N.

### 6.1.68 Bank 7 R9 I2CA (I2C Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	IBFULL	AMB	IBEN	I2CSPE	I2CSPF	DA9	DA8

**Bit 7:** Not used, fixed to "0" all the time.

**Bit 6 (IBFULL):** Set by hardware when the I2C 16-byte buffer is full. Reset by software when the MCU reads data from the I2C 16-byte buffer.

**Bit 5 (AMB):** Don't care MSB bit of Slave address. If this bit (in 7-bit and 10-bit Address mode) is enabled and the two Slave devices have the same address, i.e., Bit 1 ~ Bit 6 or Bit 1~ Bit 9 (excluding MSB); the data will be received by the two Slave devices.

**0:** Disable AMB bit

**1:** Enable AMB bit

**Bit 4 (IBEN):** I2C 16 bytes Buffer Enable bit. The EM78P507N I2C has a 16-byte buffer which is distributed in Bank 7 0x30 ~ 0x3F to save the received data. If this bit is disabled, the buffer will be a general purpose RAM

**0:** Disable the I2C Buffer

**1:** Enable the I2C Buffer

**Bit 3 (I2CSPE):** I2C Interface Stop Interrupt Enable bit

**Bit 2 (I2CSPF):** I2C Interface Interrupt Stop Flag. Set after the EM78P507N acting as Slave device, has received the STOP signal from the Master device and the I2CSPE bit has been enabled. Reset by software.

**Bits 1~0 (DA9~8):** Device Address bits

### 6.1.69 Bank 7 RA I2CDB (I2C Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

**Bits 7~0 (DB7~ DB0):** I2C Receive/Transmit Data Buffer

### 6.1.70 Bank 7 RB DACDL (DA Conversion Low Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DACD7	DACD6	DACD5	DACD4	DACD3	DACD2	DACD1	DACD0

Bits 7~0 (DACD7 ~ DACD0): DA Conversion Low Data Buffer

### 6.1.71 Bank 7 RC DACDH (DA Conversion High Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	DACD9	DACD8

Bits 7~2: Not used, fixed to "0" all the time.

Bits 1~0 (DACD9 ~ DACD8): DA Convert high Data Buffer

### 6.1.72 Bank 7 RD DACC (DA Conversion Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DARUN	0	0	SEMCL	COF[3]	COF[2]	COF[1]	COF[0]

Bit 7 (DARUN): DA Conversion Start.

Bits 6~5: Not used, fixed to "0" all the time.

Bit 4 (SEMCL): Set the maximum output current

0: Output maximum current set at 3mA

1: Output maximum current set at 4mA

Bits 3~0 (COF[3]~COF[0]): Control output maximum current levels:

COF[3]	COF[2]	COF[1]	COF[0]	DA Max Level ( $I_c = 3mA$ )
0	0	0	0	$I_c/16$
0	0	0	1	$I_c/15$
0	0	1	0	$I_c/14$
0	0	1	1	$I_c/13$
0	1	0	0	$I_c/12$
0	1	0	1	$I_c/11$
0	1	1	0	$I_c/10$
0	1	1	1	$I_c/9$
1	0	0	0	$I_c/8$
1	0	0	1	$I_c/7$
1	0	1	0	$I_c/6$
1	0	1	1	$I_c/5$
1	1	0	0	$I_c/4$
1	1	0	1	$I_c/3$
1	1	1	0	$I_c/2$
1	1	1	1	$I_c/1$

### 6.1.73 Bank 7 RF I2CCR3 (I2C Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	GCEN	I2CBF

**Bits 7~2:** Not used, fixed to “0” all the time.

**Bit 1 (GCEN):** I2C General Call Function Enable bit. If this bit is enabled and the Master device transmitted “0000000”, the connected Slave device will respond with an acknowledgment.

**0:** Disable

**1:** Enable

**Bit 0 (I2CBF):** I2C Busy Flag. If the Slave receives the address from the Master, this flag will be set. The flag is cleared after Slave receives the STOP signal from Master or I2C Slave address does not match.

**0:** I2C does not operate

**1:** I2C is in operation

## 6.2 TCC/WDT and Prescaler

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X0D	TWTCR	WDTE	WPSR2	WPSR1	WPSR0	TCCS	TPSR2	TPSR1	TPSR0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X0F	TCC	TCC[7]	TCC[6]	TCC[5]	TCC[4]	TCC[3]	TCC[2]	TCC[1]	TCC[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	IMR	T1IE	LVDIE	ADIE	SPIIE	URTIE	EXIE9	EXIE8	TCIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	ISR	T1IF	LVDIF	ADIF	SPIIF	URTIF	EXIF9	EXIF8	TCIF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the Bank 0 RD TWTCR register are used to determine the ratio of the TCC prescaler, and the PWR0~PWR2 bits of the Bank 0 RD register are used to determine the prescaler of WDT. The prescaler counter is cleared by instruction each time they are written into TCC. The WDT and prescaler are cleared by the “WDTC” and “SLEP” instructions. The following Figure 6-4 depicts the circuit diagram of TCC/WDT.

Bank 2 RF (TCC) is an 8-bit timer/counter. The TCC clock source can be internal clock or external signal input (edge selectable from the TCC pin). If the TCC signal source is from an internal clock, the TCC will be incremented by 1 at every oscillator cycle (without prescaler). If the TCC signal source is from an external clock input, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in high or low level) must be greater than 1CLK.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep running even if the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Normal mode through software programming. Refer to the WDTE bit of the TWTCR register in the above table. With no prescaler, the WDT time-out period is approximately 18 ms<sup>2</sup>.

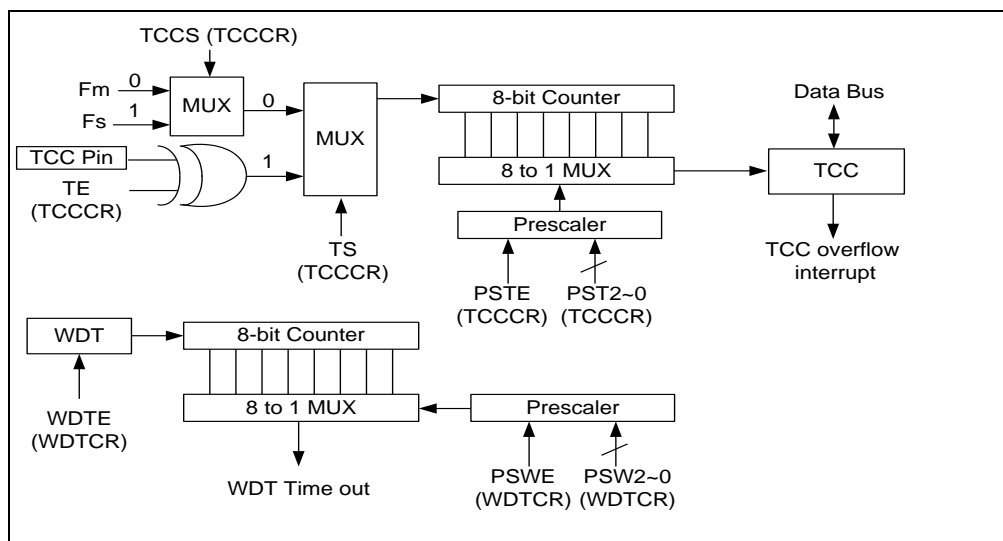


Figure 6-4 TCC and WDT Block Diagram

### 6.3 I/O Port

Port 7, Port 8, Port 9, Port A, Port B, and Port C the I/O registers are bidirectional tri-state I/O ports. The function of Pull-high and Open-drain can be set internally by Bank 5 R7, R8, R9, RA, RB, and RC, Bank 6 R7, R8, R9, RA, and RB respectively. Port 7 [4:7], Port 8 [2:3], and Port B [0:3] feature an input status (Rising or Falling edge) changed interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (Bank 4 R7~RD IOC7~IOCC). P81 cannot be defined as pull-high and open drain. The I/O registers and I/O control registers are both readable and writable.

The I/O interface circuits for Port 7, Port 8, Port 9, Port A, and Port C are illustrated in the following figures.

<sup>2</sup>  $V_{dd} = 3V$ , set up time period =  $18ms \pm 30\%$

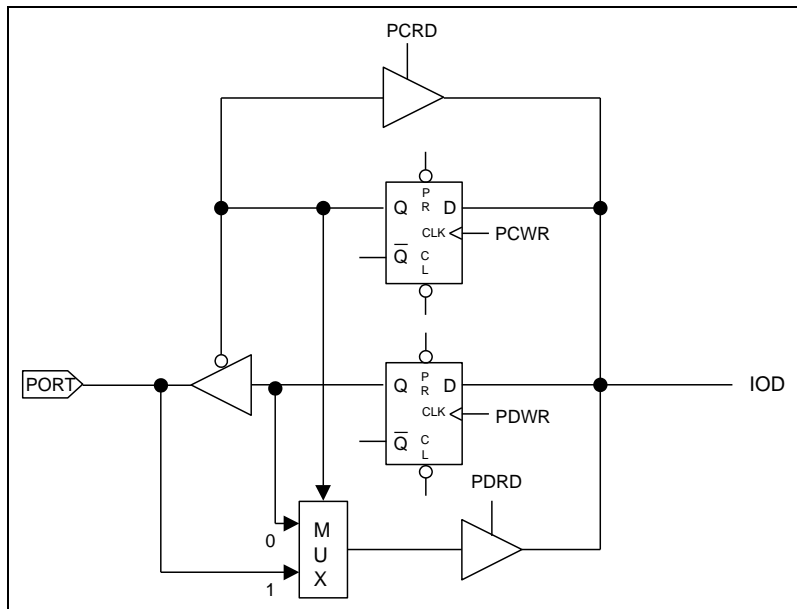


Figure 6-5a I/O Port and I/O Control Register Interface Circuit for Port 7-Port C

**NOTE**

*Pull-high and Open-drain are not shown in the figure.*

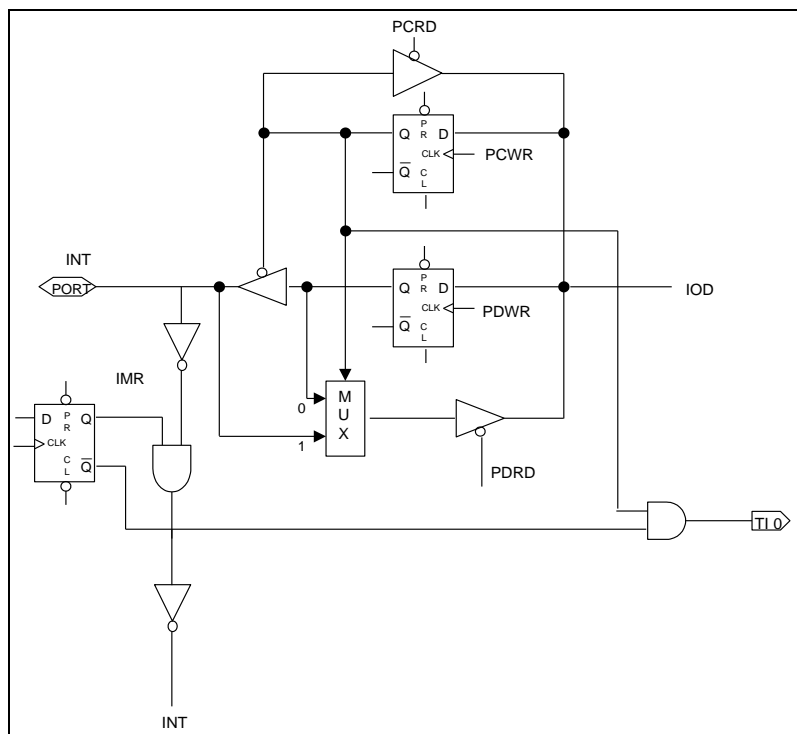


Figure 6-5b I/O Port and I/O Control Register for INT

**NOTE**

*Pull-high and Open-drain are not shown in the figure.*

## 6.4 Reset and Wake-up

### 6.4.1 Reset and Wake-up Function

A reset is initiated by one of the following events-

- (1) Power-on reset
- (2) /RESET pin input "low"
- (3) WDT time-out (if enabled)

#### NOTE

*The power-on reset circuit is always enabled. It will reset the CPU at 1.9V and consumed about 0.5 $\mu$ A or lower less.*

The device is kept in a reset condition for a period of approximately 18ms (one oscillator start-up timer period) after the Power-on reset is detected. If the /Reset pin goes "low" or WDT time-out is active, a reset is generated.

Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, R1 is cleared.
- The bits of the P7ODCR, P8ODCR, P9ODCR, PAODCR, PBODCR registers are set to all "0".
- The bits of the P7PHCR, P8PHCR, P9PHCR, PAPHCR, PBPHCR, PCPHCR registers are set to all "0".
- Bits 7~0 of Bank 0 RE, RF registers and Bank 1 RE, RF registers are cleared.

Executing the "SLEP" instruction will assert the Sleep (power down) mode. While going into Sleep mode, the Oscillator, TCC, and Timers 2~1 are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by one of the following events:

- 1) External reset input on /RESET pin
- 2) WDT time-out (if enabled)
- 3) External Interrupt status changes (if INTWE is enabled)
- 4) Low Voltage Detector initiated (if LVDWE is enabled)

The first two events will cause the EM78P507N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Events 3 and 4 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0x3~0x42 at each interrupt vector after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Only one of Events 2 to 4 can be enabled before entering into Sleep mode. That is:

- a) If WDT is enabled before SLEP, all of Bank 0, 1 RE bit is disabled. Hence, the EM78P507 can be awakened only by Event 1 or 2. Refer to the section (Section 5) on Interrupt for further details.
- b) If External interrupt status change is used to wake-up the EM78P507N and INTWK bit of Banks 3, 4 RF register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P507N can be awakened only by Event 3.
- c) If Low voltage detector is used to wake-up the EM78P507N and LVDWE bit of Bank 3-RF register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P507N can be awakened only with Event 4.

#### 6.4.2 Wake-up and Interrupt Modes Operation Summary

All categories under Wake-up and relative Interrupt modes are summarized below:

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
TCC time out	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
INT pin	Wake-up + interrupt (if interrupt is enabled) + next instruction	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt	Interrupt
Timer 1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Timer 2	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Timer 3	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
UART	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt	Interrupt

(Continuation)

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
LVD	Wake-up + interrupt (if interrupt is enabled) + next instruction	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt	Interrupt
I2C	Wake-up + interrupt (if interrupt is enabled) + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
SPI	Wake-up + interrupt (if interrupt is enabled) + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
A/D	Wake-up + interrupt (if interrupt is enabled) + next instruction	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt	Interrupt
WDT time out	RESET	RESET	RESET	RESET

**NOTE**

- User must set the wake up register (Bank 3 RF Bits 2~7 and Bank 4 RF Bits 0~7).
- Actions to be taken after Wake up through INT pin, A/D, UART, SPI, I2C, or LVD from Sleep and Idle modes:
  1. If interrupt is enabled → interrupt+ next instruction
  2. If interrupt is disabled → next instruction.

### 6.4.3 Status of T and P of the Status Register

A reset condition is initiated by one of the following events:

- 1) Power-on condition
- 2) High-low-high pulse on the /RESET pin
- 3) Watchdog Timer time-out

The values of T and P, as listed in the table below, are used to check how the processor wakes up.

■ **Values of RST, T, and P after Reset**

Reset Type	T	P
Power-on	1	1
/RESET during Operation mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operation mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

\*P: Previous status before reset

The following table shows the events which may affect the status of T and P.

■ **Status of RST, T, and P affected by Events**

Events	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

\*P: Previous value before reset

■ **Controller Reset Block Diagram**

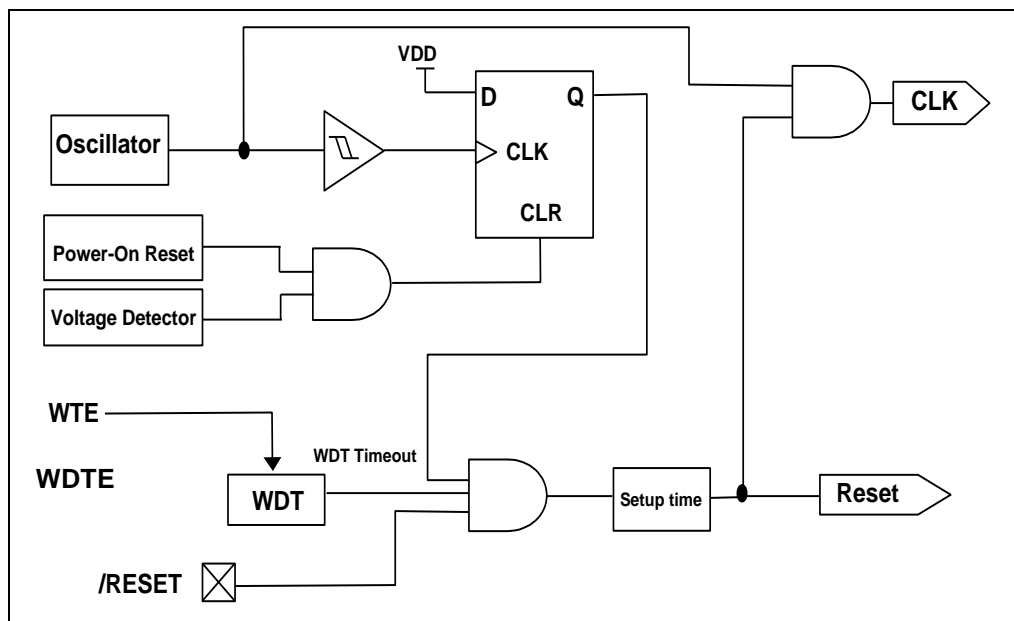


Figure 6-6 Controller Reset Functional Block Diagram

## 6.5 Interrupt

The EM78P507N has 21 interrupts as listed below:

1. Low Voltage Detector Interrupt
2. TCC Overflow Interrupt
3. External Interrupt (INT0~INT9) Pin
4. Timers 1~3 Underflow Interrupt
5. A/D Conversion Completed Interrupt
6. SPI Transmit/Receive Interrupt
7. UART Transmit/Receive/Error Completed Interrupt
8. I2C Transmit/Receive Interrupt

External interrupt can select the detector edge in Banks 3 RE and RF (EIESH, EIESL). During a power source unsteady situation, such as external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. While VDD is still erratic, the voltage supply may be below the required operational voltage. When this condition occurs, the IC kernel must automatically keep all the register status.

ISR is the Interrupt Status Register that records the interrupt requests in the relative flags/bits. IMR is an Interrupt Mask Register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (if enabled) occurs, the next instruction will be fetched from its address. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in ISR. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag in the Interrupt Status Register is set regardless of the status of its mask bit or ENI execution. Note that the outcome of ISR will be the logic AND of ISR and IMR. The RETI instruction ends the interrupt routine and enables the global interrupt (ENI execution).

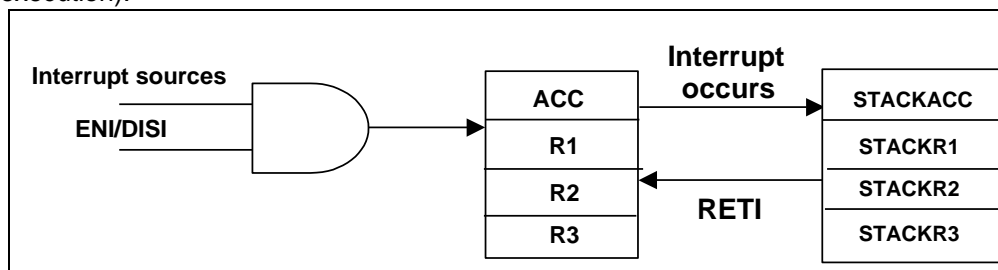


Figure 6-7a Interrupt Backup Diagram

With EM78P507N, each individual interrupt source has its own interrupt vector as depicted in the following table.

Interrupt Vector	Interrupt Status
0003H	Low voltage detector interrupt
0006H	TCC overflow interrupt
0009H	External INT0 interrupt
000CH	External INT1 interrupt
000FH	External INT2 interrupt
0012H	External INT3 interrupt
0015H	External INT4 interrupt
0018H	External INT5 interrupt
001BH	External INT6 interrupt
001EH	External INT7 interrupt
0021H	External INT8 interrupt
0024H	External INT9 interrupt
0027H	Timer 1 overflow interrupt
002AH	Timer 2 overflow interrupt
002DH	Timer 3 overflow interrupt
0030H	A/D Converter complete interrupt
0033H	SPI transmti/receive complete interrupt
0036H	UART transmit complete interrupt
0039H	UART error complete interrupt
003CH	UART receive complete interrupt
003FH	I2C transmit/receive complete interrupt
0042H	I2C Slave stop interrupt

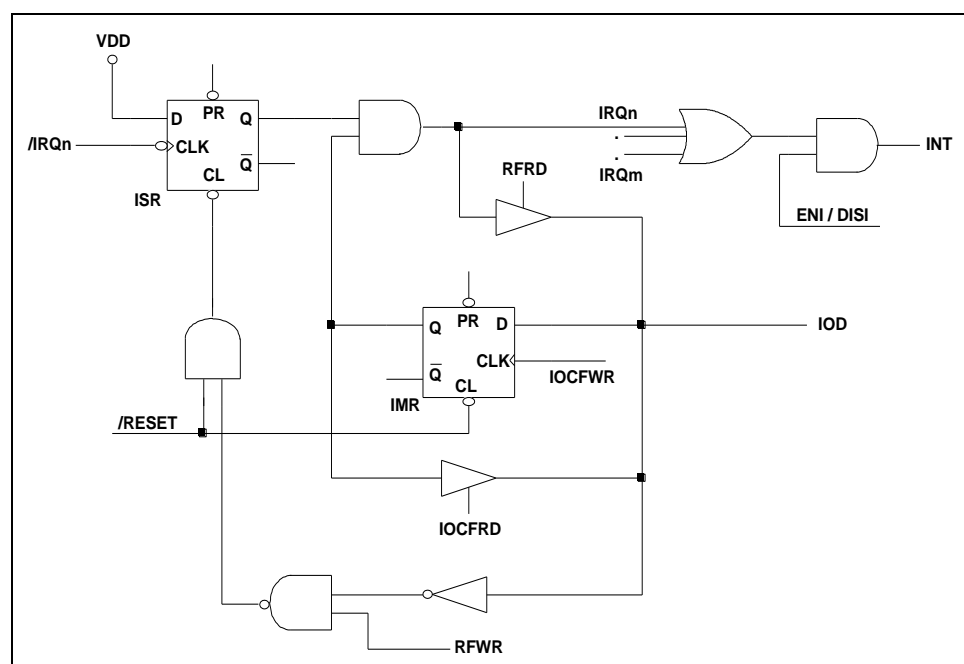


Figure 6-7b Interrupt Input Circuit

## 6.6 Analog-to-Digital Converter (ADC)

### 6.6.1 Registers for ADC Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0x05	ADCR1	ADRUN	ADP	ADCK1	ADCK0	-	-	-	-
			R/W	R/W	R/W	R/W	-	-	-	-
Bank 1	0x06	ADCR2	-	ADREF		ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
			-	R/W		R/W	R/W	R/W	R/W	R/W
Bank 1	0x07	ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
			R	R	R	R	R	R	R	R
Bank 1	0x08	ADDH					ADD11	ADD10	ADD9	ADD8
							R/W	R/W	R/W	R/W
Bank 1	0x09	ADIC1	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x0A	ADIC2	ADE15	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x0B	ADIC3	ADE23	ADE22	ADE21	ADE20	ADE19	ADE18	ADE17	ADE16
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	IMR			ADIE					
					R/W					
Bank 0	0x0F	ISR			ADIF					
					R/W					

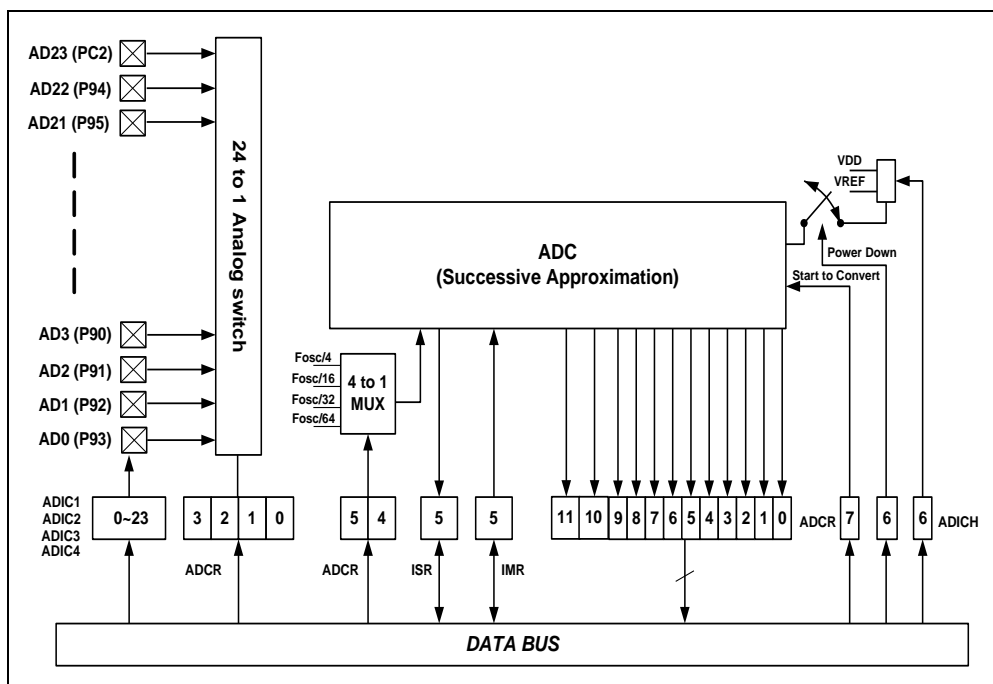


Figure 6-8 ADC Functional Block Diagram

It is a 12-bit successive approximation type AD converter. The upper side of analog reference voltage can select either internal VDD or external input pin P84 (VREF) by setting the ADREF bit in ADCR2.

### 6.6.2 ADC Data Register

When the A/D conversion is complete, the result is loaded to the ADDH (4-bit) and ADDL (8-bit). The START/END bit is cleared, and the ADIF is set.

### 6.6.3 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation by A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sampling time to meet the specified accuracy. Generally speaking, the program should wait for 2  $\mu$ s for each K $\Omega$  of the analog source impedance and at least 2  $\mu$ s for the low-impedance source. The maximum recommended impedance for the analog source is 10K $\Omega$  at Vdd = 3.3V. After the analog input channel is selected, this acquisition time must be done before A/D conversion can be started.

### 6.6.4 A/D Conversion Time

ADCK0 and ADCK1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of A/D conversion. For the EM78P507N, the conversion time per bit is about 4 $\mu$ s. The table below shows the relationship between Tct and the maximum operating frequencies.

ADCK1:0	Operation Mode	Maximum Frequency (Fc)	Maximum Conversion Rate per Bit	Maximum Conversion Rate
0 0	Fc/4	1 MHz	250kHz (4 $\mu$ s)	48 $\mu$ s (20.83kHz)
0 1	Fc/16	4 MHz	250kHz (4 $\mu$ s)	48 $\mu$ s (20.83kHz)
1 0	Fc/32	8 MHz	250kHz (4 $\mu$ s)	48 $\mu$ s (20.83kHz)
1 1	Fc/64	16 MHz	250kHz (4 $\mu$ s)	48 $\mu$ s (20.83kHz)

## 6.7 SPI (Serial Peripheral Interface)

### 6.7.1 Registers for SPI Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 3	0X0A	SPIS	DORD	TD1	TD0	-	OD3	OD4	-	RBF
			R/W	R/W	R/W		R/W	R/W		R
Bank 3	0X0B	SPIC	CES	SPIE	SRO	SSE	SDOC	SBR2	SBR1	SBR0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 3	0X0C	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 3	0X0D	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	IMR				SPIE				
						R/W				
Bank 0	0x0F	ISR				SPIF				
						R/W				

### 6.7.2 Overview and Features

#### ■ Overview:

Figures 7-9a and 7-9b below show how the EM78P507N communicates with other devices through the SPI module. If the EM78P507N is a Master controller, it sends a clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the EM78P507N is defined as a Slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. You can also set the SPIS Bit 7 (DORD) to determine the SPI transmission order, the SPIC Bit 3 (SDOC) to control the SO pin after serial data output status, and the SPIS Bit 6 (TD1) & Bit 5 (TD0) to determine the SO status output delay times.

#### ■ Features:

- Operation in either Master mode or Slave mode
- Full duplex, 3-wire synchronous communication
- Programmable baud rates of communication
- Programming clock polarity (RD Bit 7)
- Interrupt flag available for the read buffer full
- SPI transmission order
- After serial data output SDO status select
- SDO status output delay time
- Up to 8 MHz bit frequency (maximum)

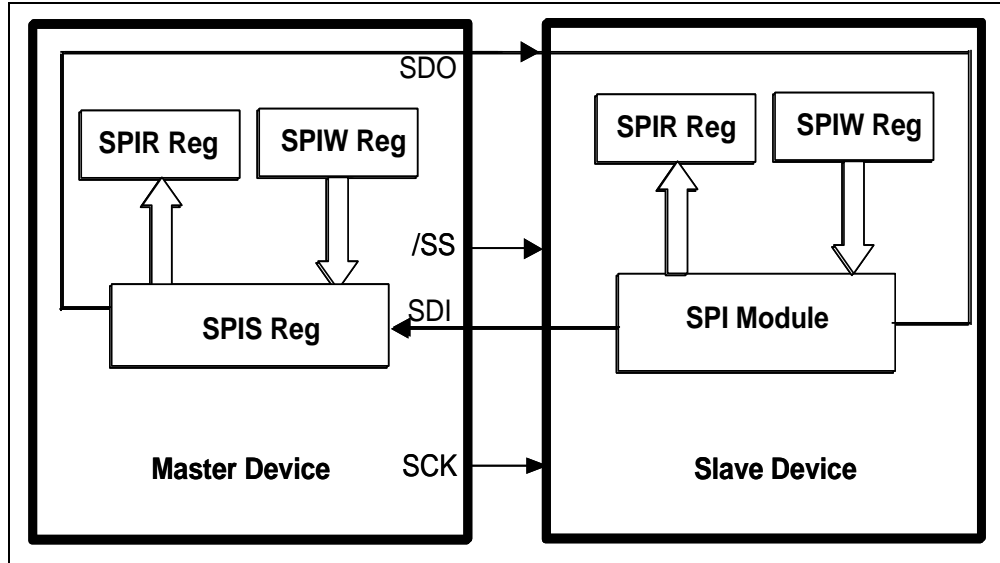


Figure 6-9a SPI Master/Slave Communication

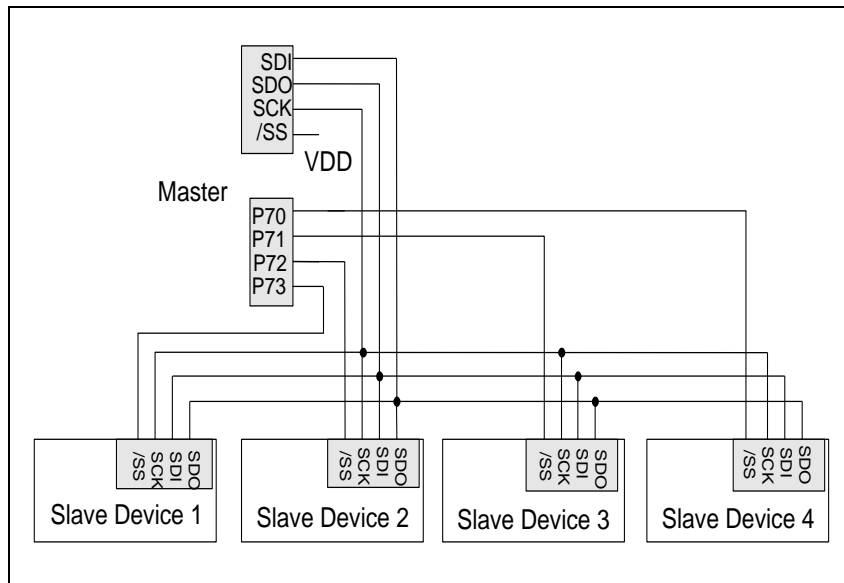


Figure 6-9b SPI Single-Master and Multi-Slave Configurations



Listed below are the function descriptions of each block depicted in Figures 6-9c and 6-9d above. It also explains how to carry out the SPI communication with the relevant signals.

- **PA4/SDI:** Serial Data In
- **PA5/SDO:** Serial Data Out
- **PA6/SCK:** Serial Clock
- **PA7//SS:** /Slave Select (Option). This pin (/SS) may be required in Slave mode
- **RBF:** Set by Buffer Full Detector
- **Buffer Full Detector:** Set to “1” when an 8-bit shifting is completed.
- **SSE:** Loads the data in SPIS register, and begin to shift. The SSE bit will be kept at “1” if communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.
- **SPIS reg.:** Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data are written, SPIS starts transmission/reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPIIF (SPI transmit/receive completed Interrupt flag) are then set.
- **SPIR reg.:** Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- **SPIW reg.:** Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.
- **SBRS2~SBRS0<sup>3</sup>:** Programming the clock frequency/rates and sources.
- **Clock Select:** Selects either the internal or the external clock as the shifting clock.
- **Edge Select:** Selects the appropriate clock edges by programming the CES bit.

#### **6.7.4 SPI Signal and Pin Description**

The detailed functions of the four pins, SDI, SDO, SCK, and /SS are as follows:

- **PA4/SDI:**
  - Serial Data In
  - Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
  - Defined as high-impedance, if not selected.

<sup>3</sup> If EM78P507N acts as the Master or Slave device to transmit and receive data, be sure to operate at lower Baud rate of less than 3MHz and ensure that the operating voltage higher than 2.5V.



- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
  - The received byte will update the transmitted byte.
  - The RBF will be set when the SPI operation is completed.
  - Timing is as shown in Figures 6-10a and 6-10b below.
- **PA5/SDO:**
- Serial Data Out
  - Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
  - Program the same clock rate and clock edge to latch on both the Master and Slave devices.
  - The received byte will update the transmitted byte.
  - The CES bit will be reset when the SPI operation is completed.
  - Timing is as shown in Figures 6-10a and 6-10b below.
- **PA6/SCK:**
- Serial Clock
  - Generated by a Master device
  - Synchronize the data communication on both the SDI and SDO pins.
  - The CES is used to select the edge to communicate.
  - The SBR0~SBR2 is used to determine the baud rate of communication.
  - The CES, SBR0, SBR1, and SBR2 bits have no effect in slave mode.
  - Timing is as shown in Figures 6-10a and 6-10b below.
- **PA7//SS:**
- Slave Select; negative logic
  - Generated by a Master device to indicate the Slave(s) has to receive data.
  - Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed.
  - Ignores the data on the SDI and SDO pins while /SS is high, because the SO is no longer driven
  - Timing is as shown in Figures 6-10a and 6-10b below.

**NOTE**

1. The Priority of PA4/SDO Pin:

PA4/SDO Pin Priority	
High	Low
SDO	PA4

2. The Priority of PA5/SCK Pin:

PA5/SCK Pin Priority	
High	Low
SCK	PA5

3. The Priority of PA6/SDI Pin:

PA6/SDI Pin Priority	
High	Low
SDI	PA6

4. The Priority of PA7 / /SS Pin :

PA7 / /SS Pin Priority	
High	Low
/SS	PA7

**6.7.5 SPI Mode Timing**

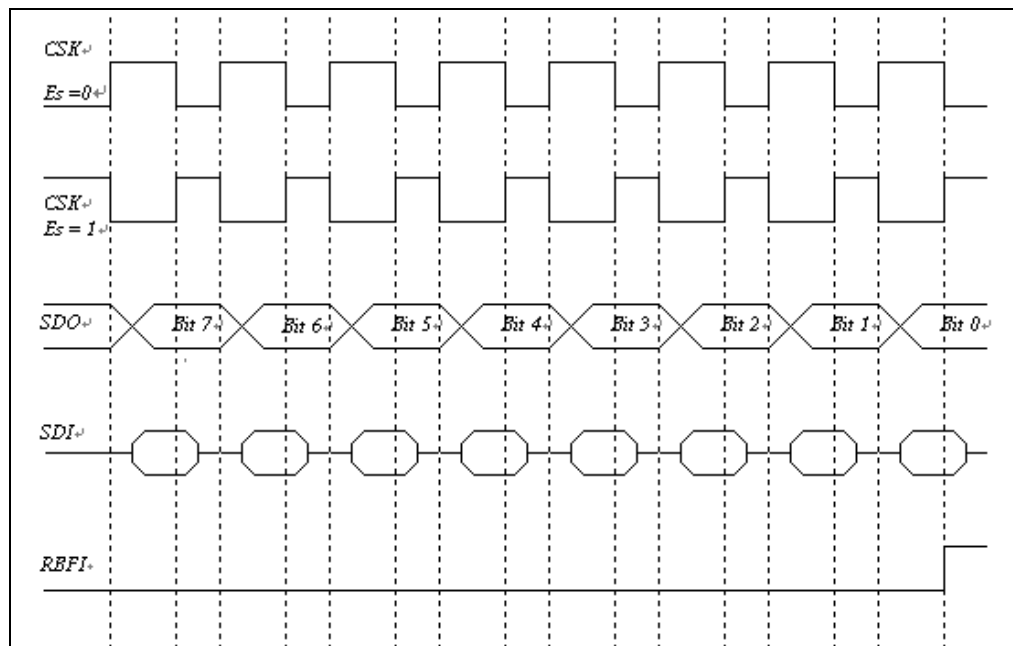


Figure 6-10a SPI Mode with /SS Disabled Timing Diagram

The SCK edge is selected by programming bit CES. The waveform shown in the above figure (Figure 6-10a) is applicable regardless whether the EM78P507N is in Master or Slave mode with /SS disabled. However, the waveform in the following Figure 6-10b can only be implemented in Slave mode with /SS enabled.

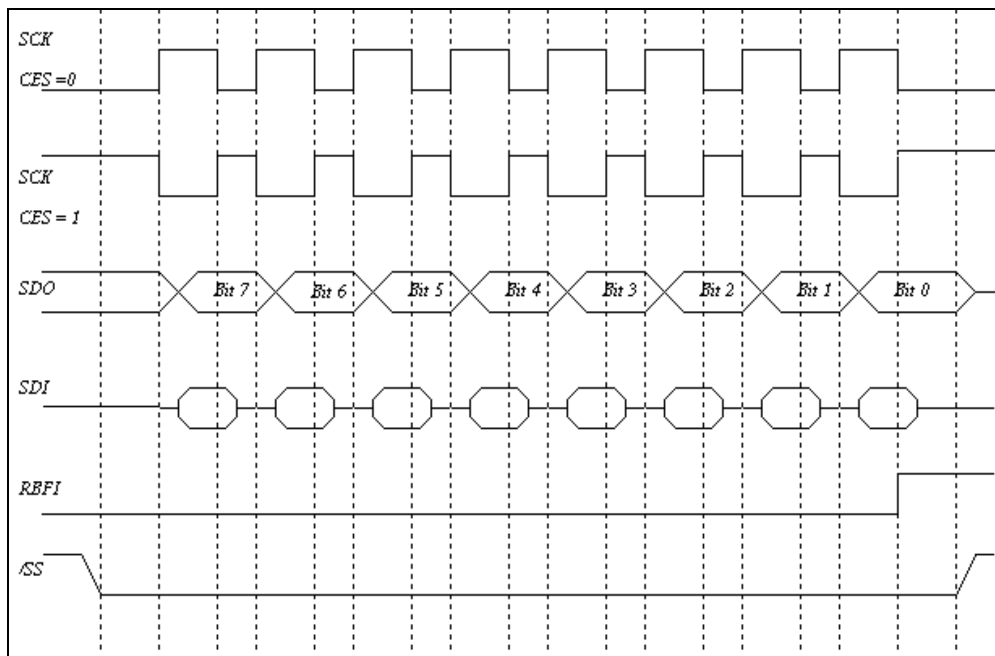


Figure 6-10b SPI Mode with /SS Enabled Timing Diagram

## 6.8 I<sup>2</sup>C Function

### ■ Registers for I2C Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 7	0X05	I2CCR1	Storbe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0X06	I2CCR2	I2CRIF	I2CRIE	I2CTIF	I2CTIE	I2CTS1	I2CT0	I2CCS	I2CEN
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0X07	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0X08	I2CDA	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0X09	I2CA	-	IBFULL	AMB	IBEN	I2CSPE	I2CSPF	DA9	DA8
			-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0x0A	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0x0F	I2CCR3	-	-	-	-	-	-	GCEN	I2CBF
			-	-	-	-	-	-	R/W	R/W

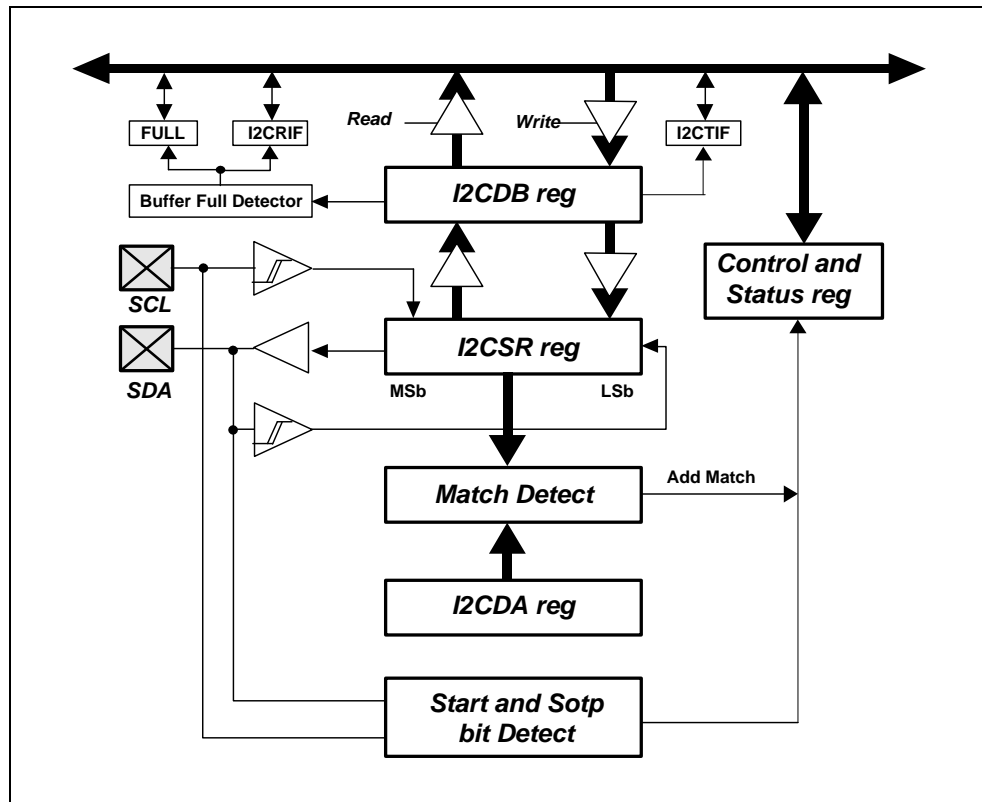


Figure 6-11a I<sup>2</sup>C Block Diagram

The EM78P507N supports a bidirectional, 2-wire bus, 7-bit/10-bit addressing and data transmission protocol, and has 16 provisional buffers to save the received data. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but only the Master device can determine which mode is activated.

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I<sup>2</sup>C bus can be transferred at the rates of up to 100kbit/s in the Standard-mode or up to 400kbit/s in the Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Within the procedure of the I<sup>2</sup>C bus, unique situations could arise, which are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH, is one of such unique cases. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH, defines a STOP condition.

The EM78P507N has a 16-byte buffer (BANK 7 0X30 ~ 0X3F) for the received data in I<sup>2</sup>C function. The 16-bit buffer characteristics requires that when you want to use this buffer, the IBEN bit in BANK 7 R9 needs to be enabled. For example, after the buffer has received data from one device and followed by another data received from another device, the previously received data will be overwritten by the recently received data. This is because the I<sup>2</sup>C receives the data from different devices address. However, if the first and subsequently received data are from the same device address, all the data will be saved in the 16-byte buffer. On the other hand, if the previously received data were transmitted in the I<sup>2</sup>C format (including the START and STOP signals), followed by subsequent data (from the same device) transmitted in other format (including START signal); the previously received data will also be overwritten by the recently received data. If the 16 bytes buffer is full, the IBFULL flag will be set by hardware and cleared by software.

The following will discuss the I<sup>2</sup>C interrupt procedure. When EM78P507N acts as the Master device and transmits the data to Slave device, the Slave device address will transmit first. After address transmission is completed, the transmit flag of the Master device will set automatically. Likewise, when EM78P507N acts as the Slave device, its receiver flag will also set automatically. In other circumstances where the Master device wants to read or receive the data from the Slave device after the Slave device has received the data transmitted by the Master device, the Master device transmit flag will automatically set. Likewise, the Slave device transmit flag will also automatically be set.

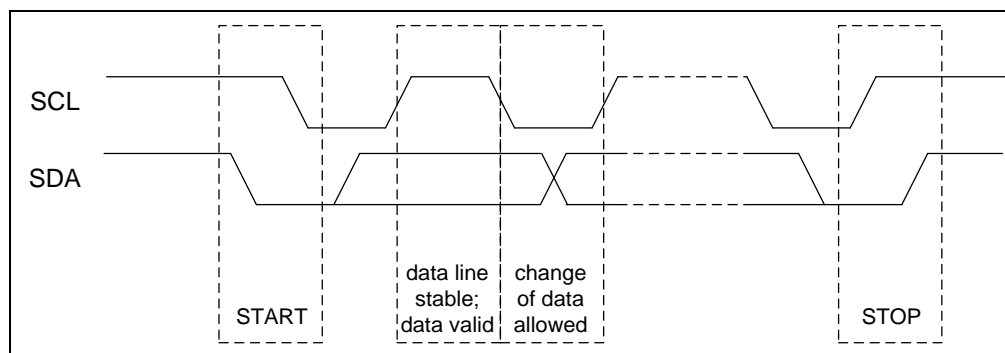


Figure 6-11b I<sup>2</sup>C Format Data Transfer Schematic

### 6.8.2 7-Bit Slave Address

The Master-transmitter transmits to Slave-receiver. The data transfer direction is not subject to change. The Master reads the Slave immediately after the first byte. At the moment of the first acknowledge, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledge is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a not-acknowledge (A). The difference between Master-transmitter with Master-receiver occurs only in R/W bit. If the R/W bit is "0", the Master device is a transmitter. Otherwise, the Master device would be a receiver (R/W bit is "1"). The Master-transmitter operation is further described in Figure 6-11c, and that of Master-receiver is described in Figure 6-11d below.

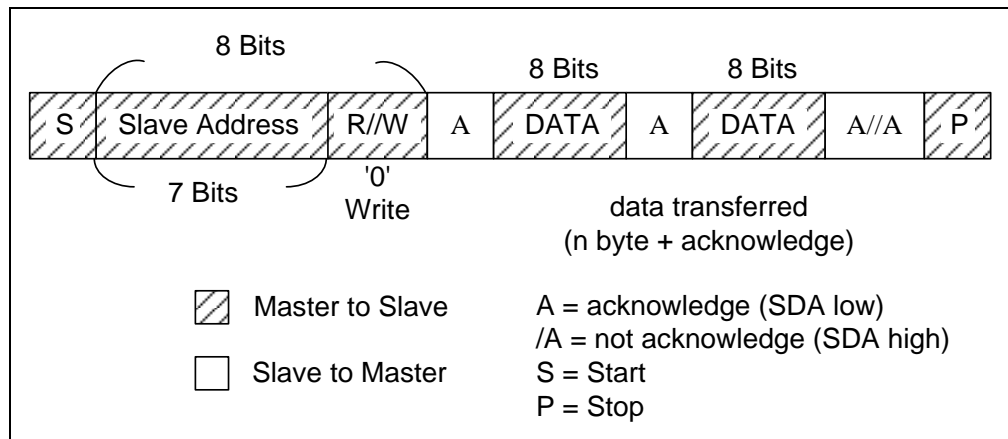


Figure 6-11c Master-Transmitter Transmits to Slave-Receiver with 7-Bit Slave Address

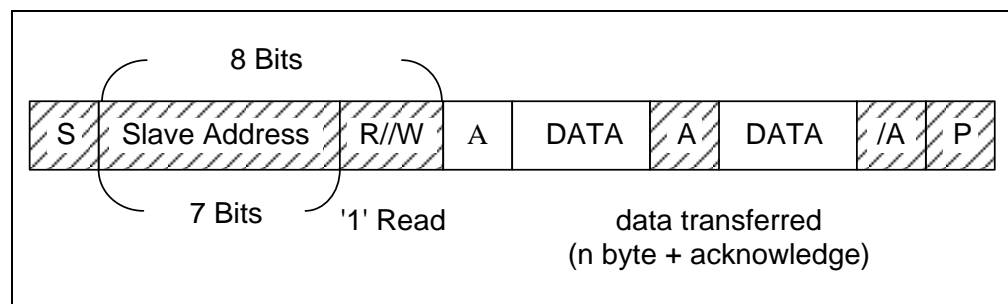


Figure 6-11d Master-Receiver Reads from Slave-Transmitter with 7-Bit Slave Address

### 6.8.2 10-Bit Slave Address

In 10-Bit Slave address mode, using 10-bit for addressing exploits the reserved combination 11110XX for the first 7 bits of the first byte following a START (S) or repeated START (Sr) condition. The first 7 bits of the first byte are the combination 11110XX of which the last 2 bits (XX) are the two most-significant bits of the 10-bit address. If the R/W bit were “0”, the second byte after acknowledge would be the 8 address bits of the 10-bit Slave address. Otherwise, the second byte would just be the next transmitted data from a Slave to Master device (R/W bit were “1”). The first bytes 11110XX are transmitted by using the Slave address register (I2CSA), and the second bytes XXXXXXXX would be transmitted by using the data buffer (I2CDB).

The possible data transfer formats for 10-bit Slave address mode are described in the following sub-sections:

#### ■ Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address

When the Slave has received the first byte after the START bit from the Master, each Slave device will compare the 7 bits of the first byte (11110XX) with their own address and with the 8th bit (R/W). If the R/W bit is “0”, the Slave will return acknowledge (A1) and it is possible that more than 1 Slave devices will return A1. The Slave devices will continue to compare the second address (XXXXXXXX). If a Slave device has found a match, that particular Slave device will be the only one to return the acknowledge (A1). The matched Slave device will remain addressed by the Master until it receives a STOP condition or a repeated START condition followed by a different Slave address.

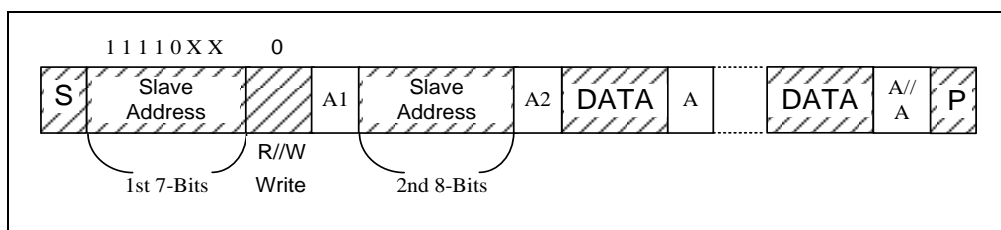


Figure 6-12a Master-Transmitter Transmits to Slave-Receiver with 10-Bit Slave Address

#### ■ Master-Receiver Read Slave-Transmitter with a 10-bit Slave Address

Up to, and including Acknowledge Bit A2; the procedure is the same as that of Master-transmitter addressing the Slave-receiver as described above. After the Acknowledge A2, a repeated START condition (Sr) takes place, followed by 7 bits Slave address (11110XX) but with the 8th bit R/W=1. The addressed Slave device will then return an Acknowledge A3. If the repeated START (Sr) condition occurs and the 7 bits of the first byte (11110XX) are received by the Slave device, all the Slave devices will compare with their own address and test the 8th R/W. However, none of the Slave devices can return an acknowledgement because R/W=1.

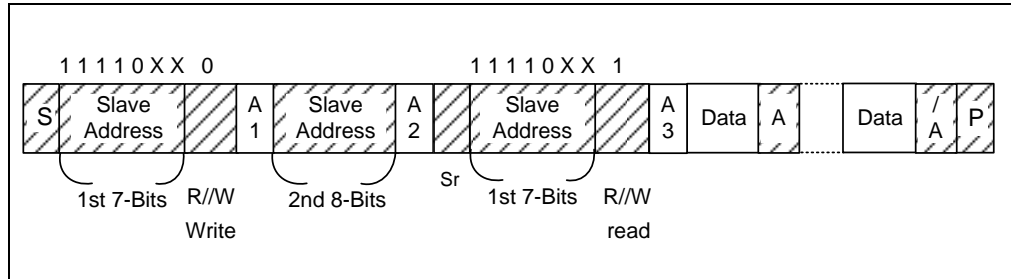


Figure 6-12b Master-Receiver Reads from Slave-Transmitter with 10-bit Slave Address

■ **Master Transmit and Receives Data to and from the Same Slave Device with 10-Bit Slave Address**

The Initial operation of this data transfer format is the same as explained in the above subsection on “Master- Transmitter Transmits to Slave-Receiver with 10-bit Slave Address”. Then the Master device starts to transmit the data to the Slave device. When the Slave device receives an Acknowledge or Not Acknowledge that is followed by repeat START (Sr), the operation “Master-Receiver Reads from Slave-Transmitter with 10-bit Slave Address” described in the preceding subsection, is then performed.

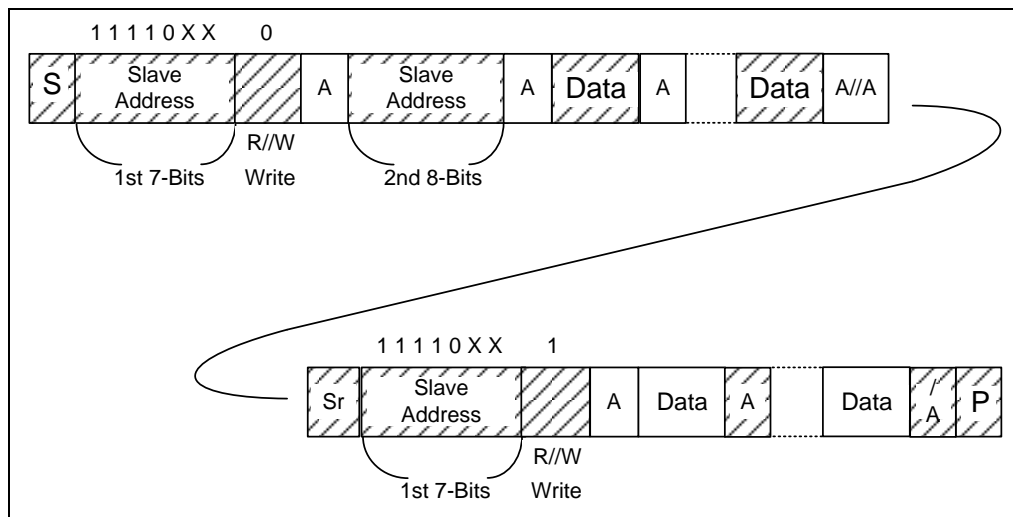


Figure 6-12c Master Transmit and Receives Data to and from the Same Slave Device with 10-bit Address

■ **Master Device Transmits Data to Two or More Slave Devices with 10 & 7 Bits Slave Address**

For 10-bit Slave address transmittal, the Initial operation of this data transmit format is the same as explained in the above subsection on “*Master-Transmitter Transmits to Slave-Receiver with 10-bit Slave Address*” which describes how to transmit the data to Slave device. After the Master device have finished the initial transmittal, and wants to transmit the data to other devices, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above.

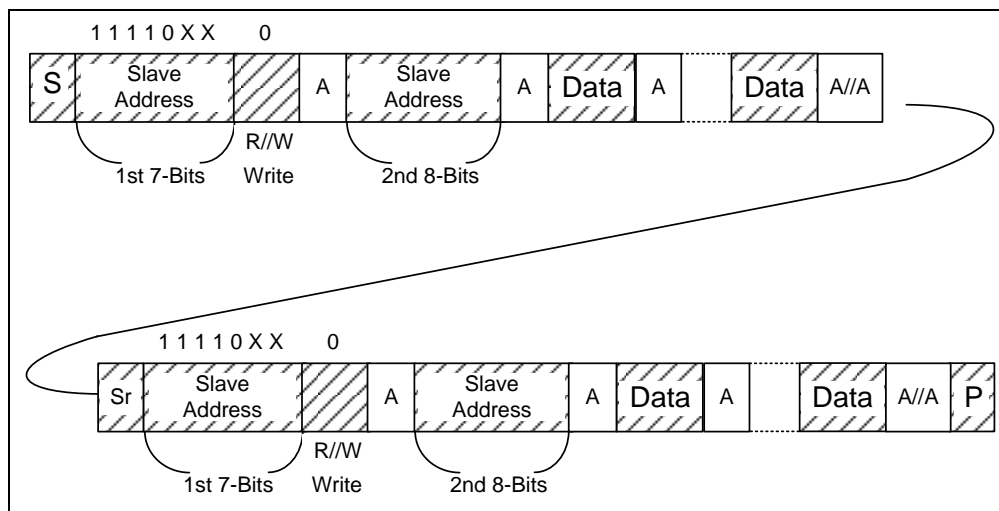


Figure 6-12d Master Transmitting to More than One Slaves with 10-Bit Slave Address

When the Master device wants to transmit data in 7-bit and 10-bit Slave address modes successively, this could be done after the START or repeat START conditions as illustrated in the following figure.

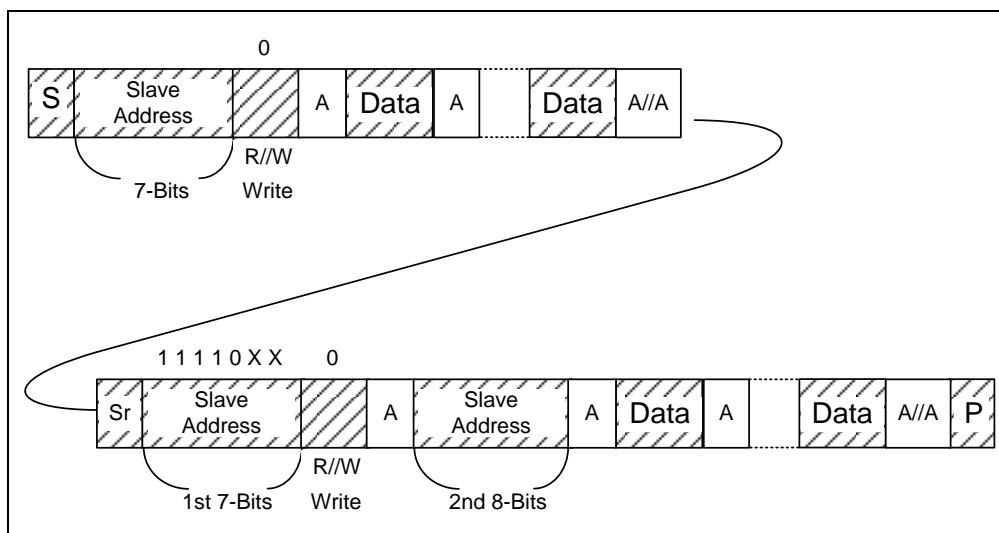


Figure 6-12e Master Successively Transmitting 7-Bit & 10-Bit Slave Addresses to Slave

### 6.8.3 Master Mode

In transmitting serial data, the I<sup>2</sup>C operates as follows:

1. Set I2CTS1~0, I2CCS, and ISS bits to select I2C transmit clock source.
2. Set I2CEN and IMS bits to enable I2C master function.
3. Write Slave address into the I2CSA register and IRW bit to select read or write.
4. Set strobe bit will start transmit and then Check SAR\_EMPTY bit.
5. Write 1<sup>st</sup> data into the I2CDB register, set strobe bit and Check EMPTY bit.
6. Write 2<sup>nd</sup> data into the I2CDB register, set strobe bit, STOP bit and Check EMPTY bit.

### 6.8.4 Slave Mode

In receiving, the I<sup>2</sup>C operates as follows:

1. Set I2CTS1~0, I2CCS and ISS bits to select I<sup>2</sup>C transmit clock source.
2. Set I2CEN and IMS bits to enable I<sup>2</sup>C slave function.
3. Write device address into the I2CDA register.
4. Read I2CDB register (address) and then clear Pend bit.
5. Check Full bit, read I2CDB register (1<sup>st</sup> data) and then clear Pend bit.
6. Check Full bit, read I2CDB register (2<sup>nd</sup> data) and then clear Pend bit.
7. If the I2CSPE bit is enabled and the slave device has received a stop signal from the master device, the flag of I2CSPF would be set automatic and the device be into interrupt address.

## 6.9 Timer/Counter 1

### ■ Registers for Timer/Counter 1 Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0X06	T1CR	TIS1	TIS0	T1MS2	T1MS1	T1MS0	T1P2	T1P1	T1P0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X07	TSR	T1MOD	TRCB	T1CSS1	T1CSS0	T2CSS	T1EN	-	T1OC
			R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Bank 2	0X08	T1PD	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X09	T1TD	TD1[7]	TD1[6]	TD1[5]	TD1[4]	TD1[3]	TD1[2]	TD1[1]	TD1[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x0E	IMR	T1IE	LVDIE	ADIE	SPIIE	URTIE	EXIE9	EXIE8	TCIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0F	ISR	T1IF	LVDIF	ADIF	SPIIF	URTIF	EXIF9	EXIF9	TCIF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

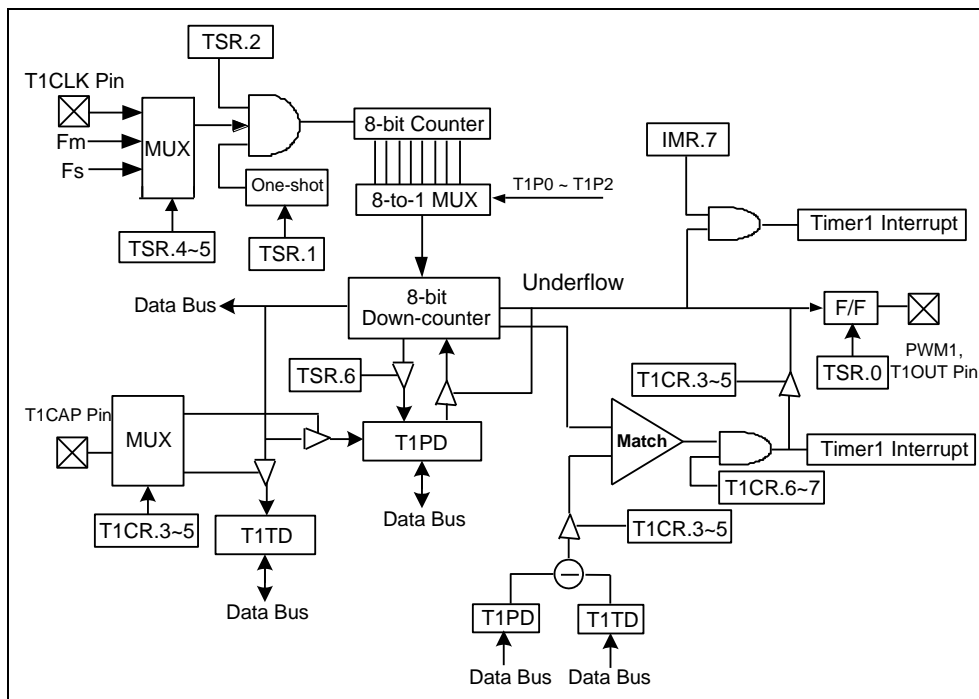


Figure 6-13 Timer/Counter 1 Configuration

### 6.9.1 Timer Mode

In Timer mode, count down is performed using the internal clock. The down-counter value auto reloads from T1PD. When the contents of the down-counter underflows, interrupt is the generated and the counter is cleared. Counting down resumes after the counter is cleared.

### 6.9.2 T1OUT Mode

In Timer 1 underflow Output mode, count down is performed using the internal clock with prescaler or External clock through T1CLK pin or Sub Frequency with prescaler. The counter value is loaded from T1PD when the counter underflows. The F/F output is toggled and the counter is auto-reloaded from T1PD each time an overflow is found. The F/F output is inverted and output to /T1OUT pin. This mode can generate 50% duty pulse output. The program can initialize the F/F and it is initialized to “0” during a reset. A T1OUT interrupt is generated each time the /T1OUT output is toggled.

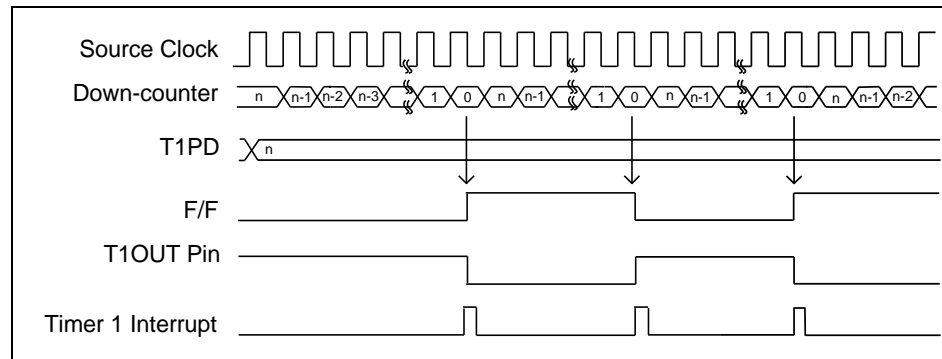


Figure 6-14 T1OUT Mode Timing Diagram

### 6.9.3 Capture Mode

In Capture mode, the pulse width, period, and duty of the T1CAP input pin are measured under this mode, which can be used in decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of T1CAP pin input, the contents of the counter is loaded into T1PD, then the counter is cleared and interrupt is generated. On the falling (rising) edge of T1CAP pin input, the contents of the counter are loaded into T1TD. The counter continues counting on the next rising edge of the T1CAP pin input and the contents of the counter are loaded into T1PD. Then, counter is cleared and interrupt is generated again. If an overflow occurs before the edge is detected, the 00H is loaded into T1PD and an underflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether the T1PD value is 00H. After an interrupt (capture to T1PD or overflow detection) is generated, capture and underflow detection are halted until T1PD is read out.

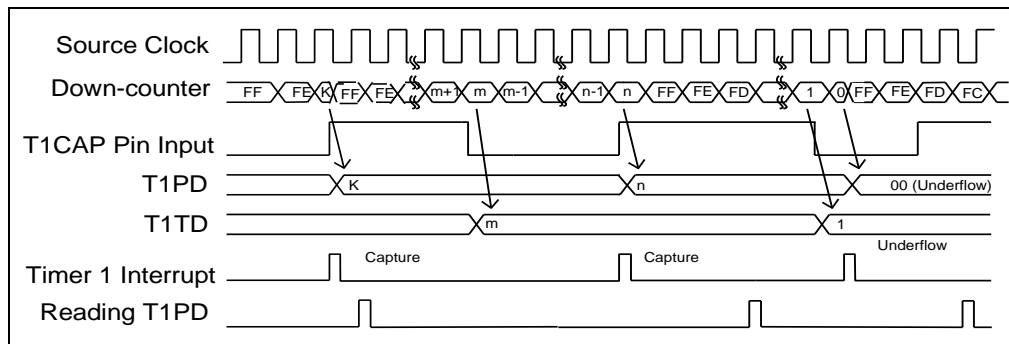


Figure 6-15 Capture Mode Timing Diagram

### 6.9.4 PWM Mode

In Pulse Width Modulation (PWM) Output mode, counting down is performed using the internal clock with prescaler or external clock through T1CLK Pin or Sub Frequency with prescaler. The PWM1 duty cycle is controlled by T1TD, and the PWM1 period is controlled by T1PD. The pulse at the PWM1 pin is held at high level as long as the counter value of T1TD is greater than or equal to zero, while the pulse is held at low level until the counter value of T1PD underflows. The F/F is toggled when counter underflows. While the counter is still counting, the F/F is toggled again when the counter underflows, then the counter is auto-reloaded from T1PD. The F/F output is inverted and output to the /PWM pin. A Timer1 interrupt is generated each time an underflow occurs. T1PD is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if T1PD is overwritten. Therefore, the output can be changed continuously. T1PD is also shifted for the first time by setting T1S to “1” after data is loaded to T1PD.

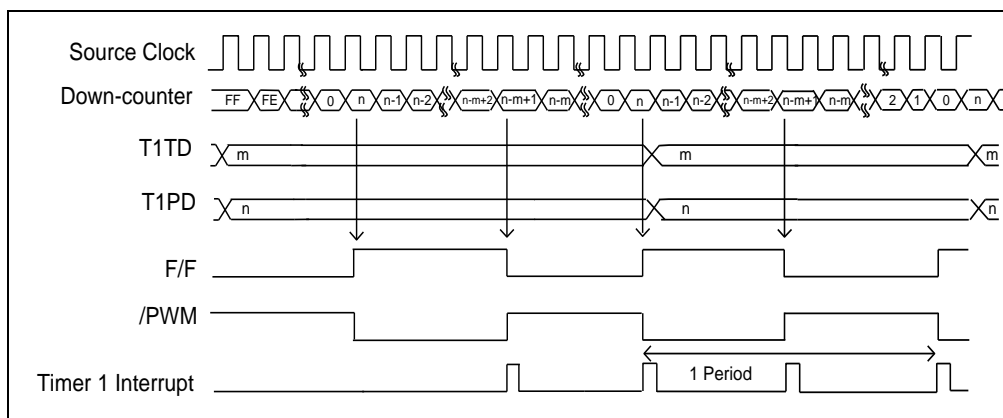


Figure 6-16 PWM Mode Timing Diagram

**NOTE**

Under 16-bit timer mode, all Timer 1 function resolution becomes 16 bits.

## 6.10 Timer 2

### ■ Registers for Timer/Counter 2 Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0X06	T1CR	TIS1	TIS0	T1MS2	T1MS1	T1MS0	T1P2	T1P1	T1P0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X07	TSR	T1MOD	TRCB	T1CSS1	T1CSS0	T2CSS	T1EN	0	T1OC
			R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Bank 2	0X0A	T2CR	T2IF	T2IE	T2S	T2MS1	T2MS0	T2P2	T2P1	T2P0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X0B	T2PD	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X0C	T2TD	TD2[7]	TD2[6]	TD2[5]	TD2[4]	TD2[3]	TD2[2]	TD2[1]	TD2[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

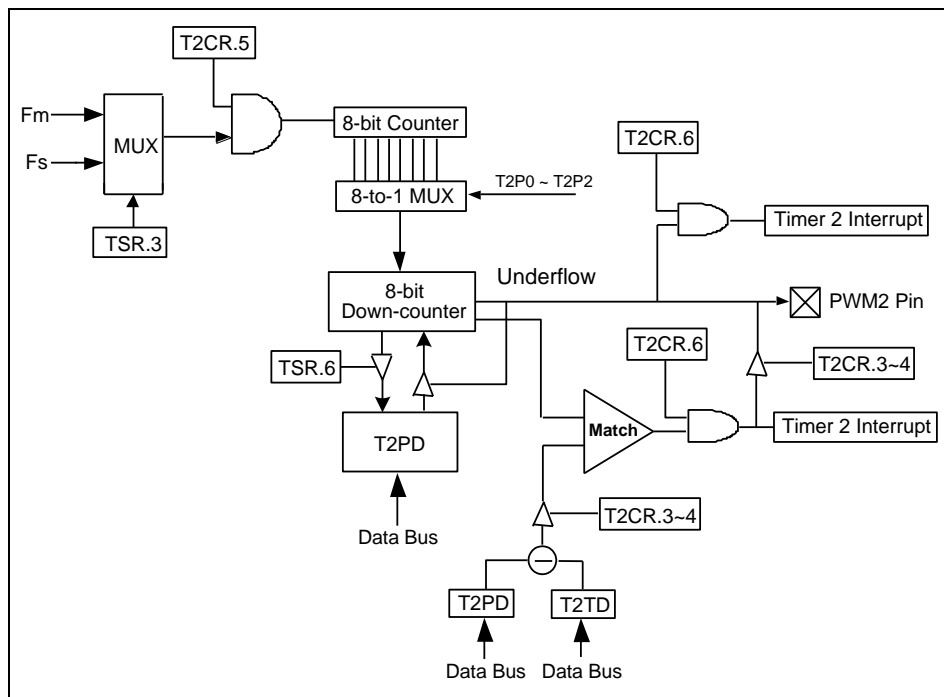


Figure 6-17 Timer 2 Configuration

### 6.10.1 Timer Mode

In Timer mode, count down is performed using the internal clock with prescaler. When the counter value from T2PD underflows, interrupt is generated and the counter is cleared. Count down resumes after the counter is cleared. The counter value will automatically reload from T2PD.

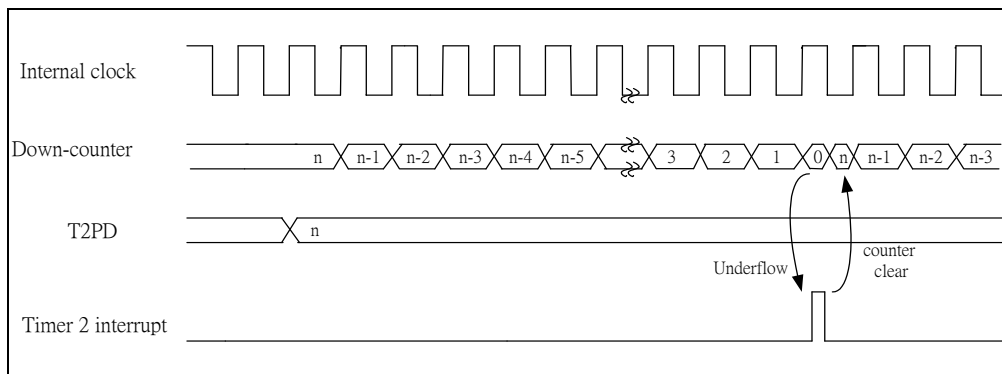


Figure 6-18 Timer Mode Timing Diagram

### 6.10.2 PWM Mode

In Pulse Width Modulation (PWM) Output mode, count down is performed using the internal clock with prescaler or  $F_{sub}$  with frequency. The PWM2 duty cycle is controlled by T2TD, and the PWM2 period is controlled by T2PD. The pulse at the PWM2 pin is held to high level as long as the T2TD counter value is greater than or equal to zero while the pulse is held to low level until the T2PD counter value underflows.

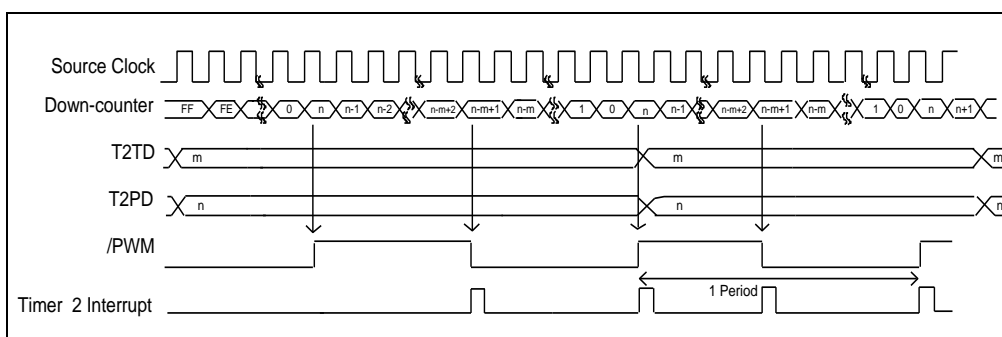


Figure 6-19 PWM Mode Timing Diagram

## 6.11 Timer 3

### ■ Registers for Timer/Counter 3 Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0X0C	T3CR1	T3IF	T3IE	T3EN	T3CSS1	T3CSS0	T1P2	T1P1	T1P0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 2	0X0D	T3CR2	-	-	-	-	-	-	T3MS1	T3MS0
			-	-	-	-	-	-	R/W	R/W
Bank 2	0X0E	T3PD	PRD3[7]	PRD3[6]	PRD3[5]	PRD3[4]	PRD3[3]	PRD3[2]	PRD3[1]	PRD[0]
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

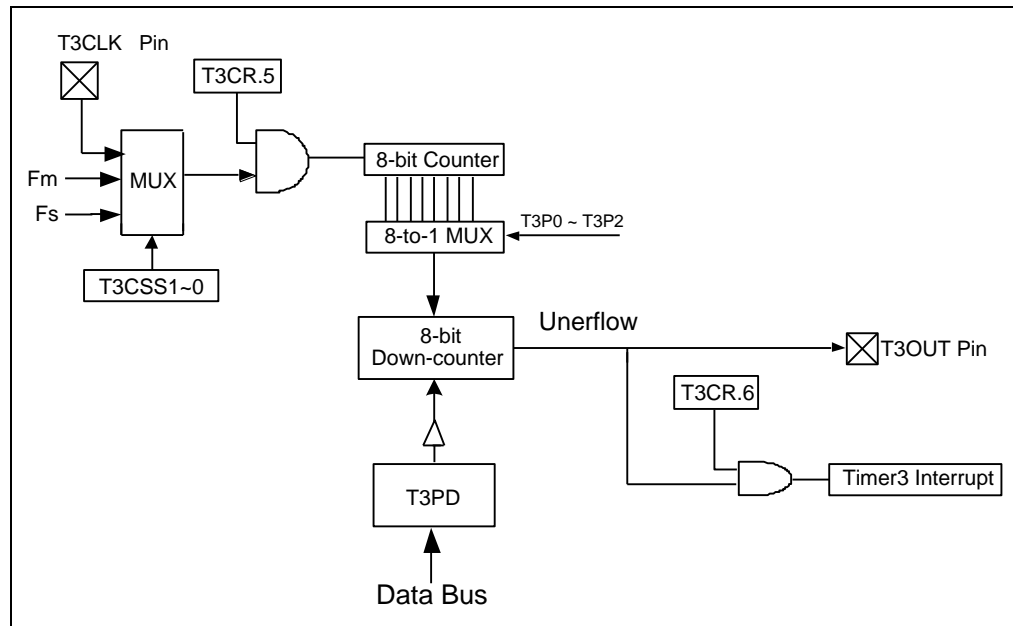


Figure 6-20 Timer 2 Configuration

### 6.11.1 Timer Mode

In Timer mode, count down is performed using the internal clock with prescaler. When the counter value from T3PD underflows, interrupt is then generated and the counter is cleared. Count down resumes after the counter is cleared. The counter value will automatically reload from T3PD.

### 6.11.2 T3OUT Mode

In Timer 3 Underflow Output mode, count down is performed using the internal clock with prescaler or external clock through T3CLK Pin or Sub Frequency with prescaler. The counter value is loaded from T3PD. When the counter underflows, this mode can generate 50% duty pulse output. A T3OUT interrupt is generated each time the /T3OUT output is toggled.

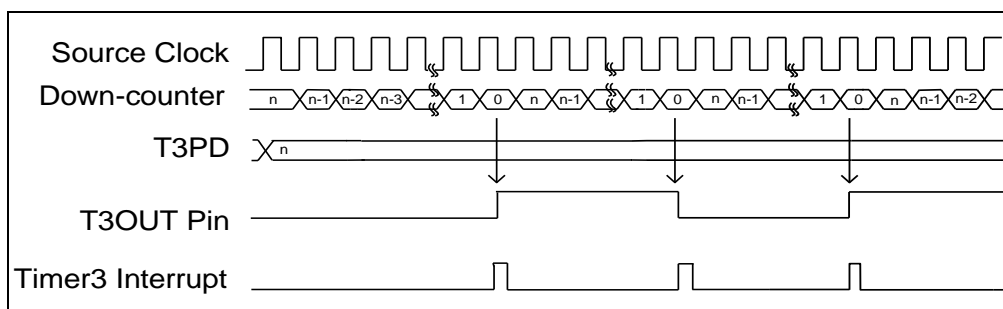


Figure 6-21 PWM Mode Timing Diagram

## 6.12 Universal Asynchronous Receiver Transmitter (UART)

### ■ Registers for UART Circuit

R BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK 3	0x05	URC1	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
			W	R/W	R/W	R/W	R/W	R/W	R	R/W
BANK 3	0x06	URS	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
			R	R/W	R/W	R	R	R	R	R/W
BANK 3	0x07	URRD	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
			R	R	R	R	R	R	R	R
BANK 3	0x08	URTD	URTD 7	URTD 6	URTD 5	URTD 4	URTD 3	URTD 2	URTD 1	URTD0
			W	W	W	W	W	W	W	W
BANK3	0x09	URC2			UARTE		UINVEN			URRIF
					R/W		R/W			R/W
BANK 0	0x0E	ISR	T1IE	LVDIE	ADIE	SPIE	URTIE	EXIE9	EXIE8	TCIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BANK 0	0x0F	IMR	T1IF	LVDIF	ADIF	SPIF	URTIF	EXIF9	EXIF8	TCIF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

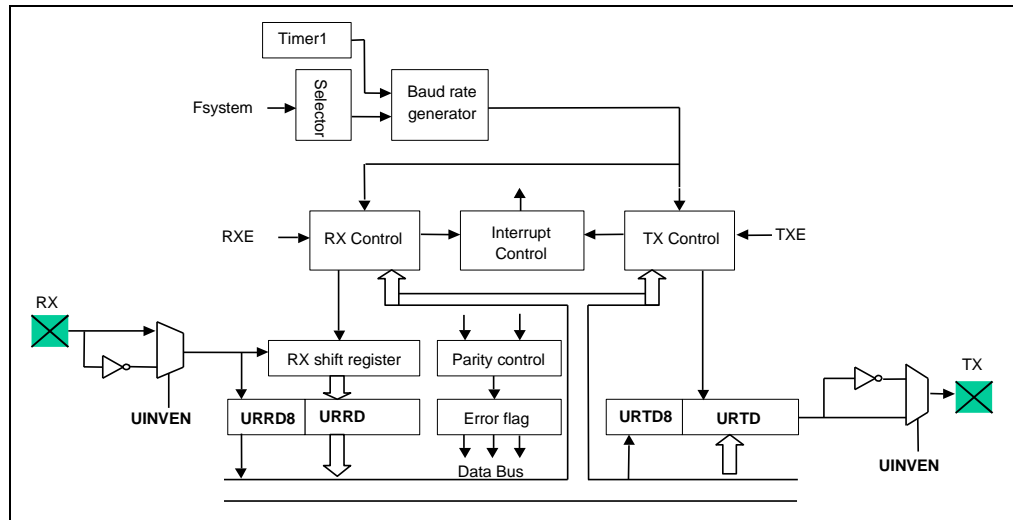


Figure 6-22a UART Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has an independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three "0" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

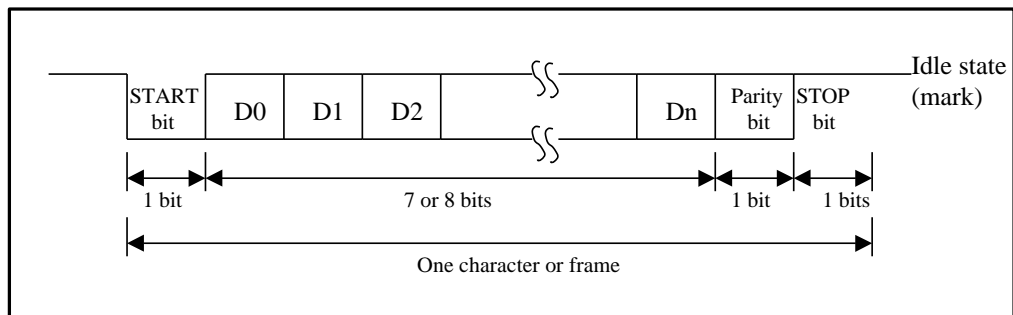


Figure 6-22b UART Data Format

### 6.12.1 UART MODE:

Three UART modes are available, i.e.; Mode 1 ~ Mode 3. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. The figure below shows the data format of each mode.

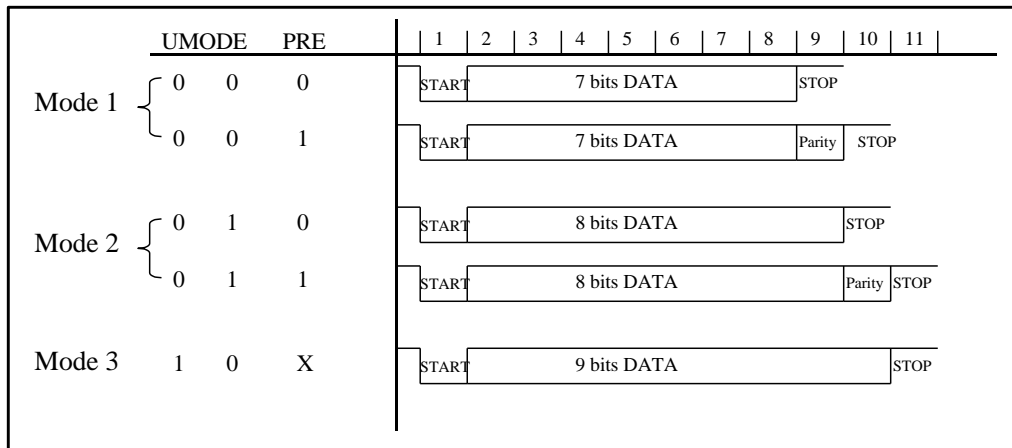


Figure 6-23 UART Modes 1, 2, & 3 Data Format

### 6.12.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URC register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URC register will be set by hardware.
3. Then start transmitting.
4. Serially transmit data in the following order from the TX pin:
  - a) **Start bit:** one "0" bit is output.
  - b) **Transmit data:** 7, 8 or 9 bits data are output from the LSB to the MSB.
  - c) **Parity bit:** one parity bit (odd or even selectable) is output.
  - d) **Stop bit:** one "1" bit (stop bit) is output.

Mark state: output "1" continues until the start bit of the next transmitted data. After transmitting the stop bit, UART generates a URTIF interrupt (if enabled).

### 6.12.3 Receiving

In receiving, the UART operates as follows:

1. Set RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Received data are shifted into the URRD register in LSB to MSB order.
3. The parity bit and the stop bit are received. After one character is received, UBIF bit of URC2 register is set to "1". This means the UART receive interrupt will occur.

4. The UART performs the following checks:
  - a) **Parity check:** The number of 1 of the received data must match the even or odd parity setting of the EVEN bit in the URS register.
  - b) **Frame check:** The start bit must be 0 and the stop bit must be 1.
  - c) **Overrun check:** The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

If any checked item failed, an ERROR interrupt will be generated (if enabled). If the UART has completely received data, the receive-complete interrupt is generated (if enabled). The error flag and receive complete flag should be cleared by software. The URTIE bit is the interrupt enable bit of ERROR, UBIF and URTIF.

5. Read the received data from URRD register and the URBF bit will be cleared by hardware.

#### 6.12.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

#### 6.12.5 UART Timing

##### ■ Transmission Counter Timing:

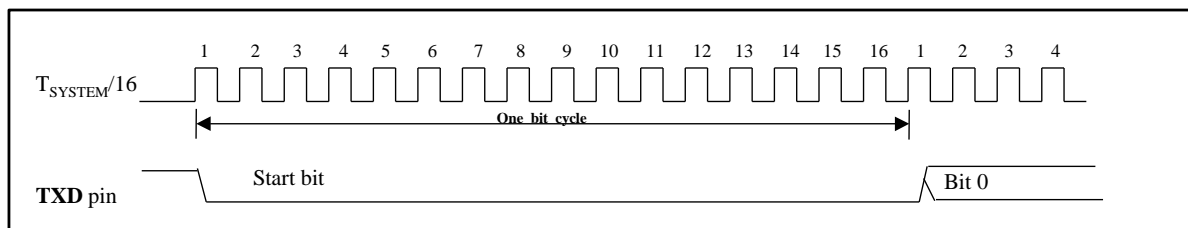


Figure 6-24a UART Transmission Counter Timing Diagram

##### ■ Receiving Counter Timing:

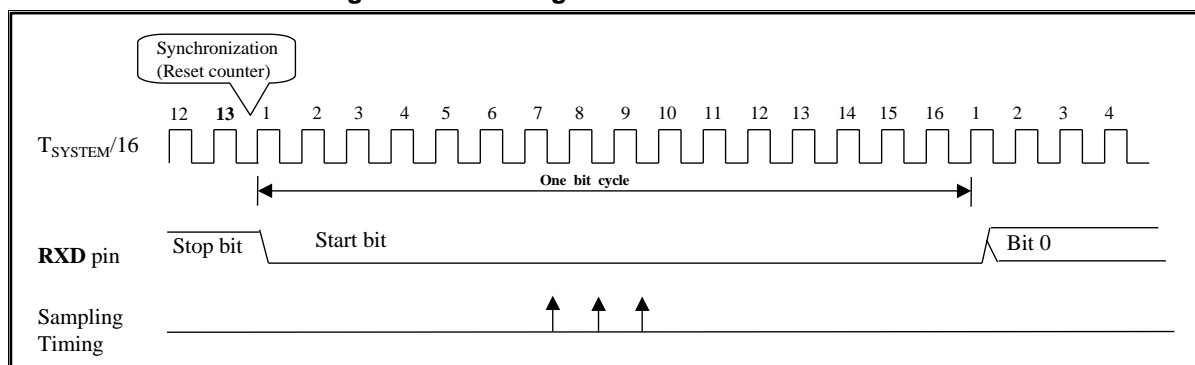


Figure 6-24b UART Receiving Counter Timing Diagram

■ UART Transmit Operation (8 bits data with parity bit):

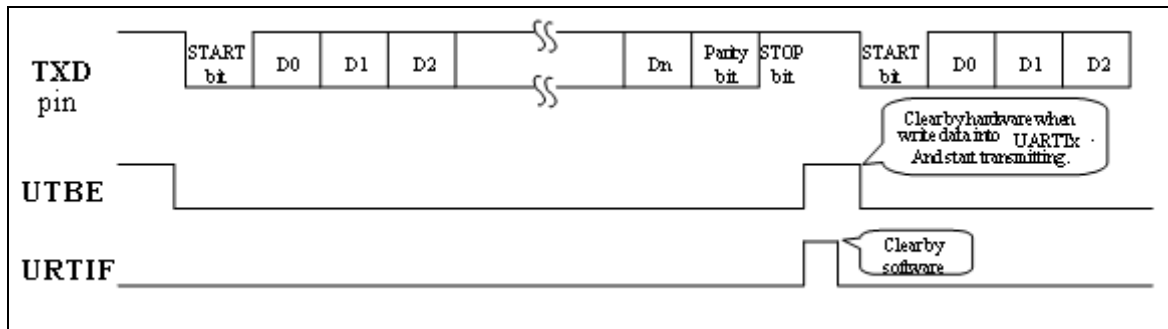


Figure 6-24c UART Transmit Operation Timing Diagram

## 6.13 DA Conversion

■ Registers for DAC Circuits

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 7	0X0B	DACDL	DACD7	DACD6	DACD5	DACD4	DACD3	DACD2	DACD1	DACD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 7	0X0C	DACDH	-	-	-	-	-	-	DACD9	DACD8
			-	-	-	-	-	-	R/W	R/W
Bank 7	0X0D	DACC	DARUN	-	-	SEMC	COF[3]	COF[2]	COF[1]	COF[0]
			R/W			R/W	R/W	R/W	R/W	R/W

Perform the Following steps to control the output current of DA:

1. Load the data to the DA buffer DACDL and DACDH.
2. Set the SEMC bit to determine the maximum level (3 or 4mA) of the output current.
3. Set the COF [3:0] to determine the range and resolution of the output current.
4. Set DARUN bit to "1" and clear by software.

The DA module is provided in the MCU internal circuit. When the register is set to enable the DA module, the output current of the DA pin DACO is 0~3 or 4mA.

The maximum level of the DA output current is determined by the SEMC bit. If the SEMCL is enabled, the maximum level of the DA output current is 4mA. The COF [3:0], COAC [3:0], and SEMC are used to control the DA Conversion output current.

**Examples:** If SEMC is disabled and COF [3:0] are all "1", the output current range of DA Conversion would be between 0 and 3mA. In this case, the output current of DA Conversion can be adjusted to  $3mA \times 1/16$ ,  $3mA \times 2/16$ ,  $3mA \times 3/16 \dots 3mA \times 16/16$ , by COF[3:0].

## 6.14 Registers Initialized Values after Reset

**Legend:** -: Not used    **U:** Unknown or don't care,    **P:** Previous value before wake-up,  
**T:** Check "Reset Type" in Section 6.4.2.

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
0x01	R1 (RPBSR)	Bit Name	0	PS2	PS1	PS0	0	BS2	BS1	BS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	0	0	P	P	0	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	Continue to execute next instruction							
0x03	R3 (SR)	Bit Name	VDB	LVDEN	LVDS	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Sleep & Idle mode	0	0	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Sleep & Idle mode	0	0	P	P	P	P	P	P
Bank 0 0x05	R5 (TBLP)	Bit Name	Rbit7	Rbit6	Rbit5	Rbit4	Rbit3	Rbit2	Rbit1	Rbit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	0	0	0	P	P	P	P	P
Bank 0 0x06	R6 (TBHP)	Bit Name	TBSHL	0	0	Rbit12	Rbit11	Rbit10	Rbit9	Rbit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 0 0x07	R7 (Port 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0 0x08	R8 (Port 8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 0 0x09	R9 (Port 9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 0 0x0A	RA (Port A)	Bit Name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 0 0x0B	RB (Port B)	Bit Name	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 0 0x0C	RC (SCCR)	Bit Name	0	0	0	0	IDLE	0	0	CPUS
		Power-on	0	0	0	0	1	0	0	1
		/RESET and WDT	0	0	0	0	1	0	0	1
		Wake-up from Sleep & Idle mode	0	0	P	P	P	0	P	P
Bank 0 0x0D	RD (TWTCR)	Bit Name	WDTE	WPSR2	WPSR1	WPSR0	TCCS	TPSR2	TPSR1	TPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 0 0x0E	RE (IMR)	Bit Name	T1IE	LVDIE	ADIE	SPIE	URTIE	EXIE9	EXIE8	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	0	0	0	P	P	P	P	P
Bank 0 0x0F	RF (ISR)	Bit Name	T1IF	LVDIF	ADIF	SPIF	URTIF	EXIF9	EXIF8	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P



(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10 ~ 0x3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x05	R5 (ADCR1)	Bit Name	ADRUN	ADP	ADCK1	ADCK0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x06	R6 (ADCR2)	Bit Name	0	ADREF	0	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x07	R7 (ADDL)	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x08	R8 (ADDH)	Bit Name	0	0	0	0	ADD11	ADD10	ADD9	ADD8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x09	R9 (ADIC1)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x0A	RA (ADIC2)	Bit Name	ADE15	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x0B	RB (ADIC3)	Bit Name	ADE23	ADE22	ADE21	ADE20	ADE19	ADE18	ADE17	ADE16
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1 0x0C	RC (COCR)	Bit Name	0	0	0	RCM1	RCM0	CLKOE	CLKB1	CLKB0
		Power-on	0	0	0	1	1	1	0	0
		/RESET and WDT	0	0	0	1	1	1	0	0
		Wake-up from Sleep & Idle mode	P	0	P	P	P	P	0	0
Bank 1 0x0E	RE (EIMR)	Bit Name	EXIE7	EXIE6	EXIE5	EXIE4	EXIE3	EXIE2	EXIE1	EXIE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 1 0x0F	RF (EISR)	Bit Name	EXIF7	EXIF6	EXIF5	EXIF4	EXIF3	EXIF2	EXIF1	EXIF0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	0	P	0	0	0
Bank 2 0x05	R5 (T1CR)	Bit Name	TIS1	TIS0	T1MS2	T1MS1	T1M0	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x06	R6 (TSR)	Bit Name	T1MOD	TRCB	T1CSS1	T1CSS0	T2CSS	T1EN	0	T1OC
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x07	R7 (T1PD)	Bit Name	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x08	R8 (T1TD)	Bit Name	TD1[7]	TD1[6]	TD1[5]	TD1[4]	TD1[3]	TD1[2]	TD1[1]	TD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x09	R9 (T2CR)	Bit Name	T2IF	T2IE	T2EN	T2MS1	T2MS0	T2P2	T2P1	T2P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P



(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2 0x0A	RA (T2PD)	Bit Name	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x0B	RB (T2TD)	Bit Name	TD2[7]	TD2[6]	TD2[5]	TD2[4]	TD2[3]	TD2[2]	TD2[1]	TD2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x0C	RC (T3CR1)	Bit Name	T3IF	T3IE	T3EN	T3CSS1	T3CSS0	T3P2	T3P1	T3P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x0D	RD (T3CR2)	Bit Name	0	0	0	0	0	0	T3MS1	T3MS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x0E	RE (T3PD)	Bit Name	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 2 0x0F	RF (TCC)	Bit Name	TCC[7]	TCC[6]	TCC[5]	TCC[4]	TCC[3]	TCC[2]	TCC[1]	TCC[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x05	R5 (URC)	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	U	0	0	0	0	0	1	0
		/RESET and WDT	P	0	0	0	0	0	1	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x06	R6 (URS)	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	P	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 3 0x07	R7 (URRD)	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x08	R8 (URTD)	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x09	R9 (URC2)	Bit Name	0	0	UARTE	0	UINVEN	0	0	URRIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x0A	RA (SPIS)	Bit Name	DORD	TD1	TD0	0	OD3	OD4	0	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x0B	RB (SPIC)	Bit Name	CES	SPIEN	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x0C	RC (SPIR)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x0D	RD (SPIW)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 3 0x0E	RE (IESH)	Bit Name	EIES7	EIES6	EIES5	EIES4	EIES3	EIES2	EIES1	EIES0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P



(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 3 0x0F	RF (EIESL)	Bit Name	LVDWE	I2CWE	SPIWE	ADWK	INTWK9	INTWK8	EIES9	EIES8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x07	R7 (IOC7)	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x08	R8 (IOC8)	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x09	R9 (IOC9)	Bit Name	IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x0A	R9 (IOCA)	Bit Name	IOCA7	IOCA6	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x0B	RB (IOCB)	Bit Name	IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x0C	RC (IOCC)	Bit Name	0	0	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 4 0x0F	RF (WKCR)	Bit Name	INTWK7	INTWK6	INTWK5	INTWK4	INTWK3	INTWK2	INTWK1	INTWK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 5 0x07	R7 (P7PHCR)	Bit Name	PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 5 0x08	R8 (P8PHCR)	Bit Name	PH87	PH86	PH85	PH84	PH83	PH82	0	PH80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 5 0x09	R9 (P9PHCR)	Bit Name	PH97	PH96	PH95	PH94	PH93	PH92	PH91	PH90
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 5 0x0A	RA (PAPHCR)	Bit Name	PHA7	PHA6	PHA5	PHA4	PHA3	PHA2	PHA1	PHA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 5 0x0B	RB (PBPHCR)	Bit Name	PHB7	PHB6	PHB5	PHB4	PHB3	PHB2	PHB1	PHB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 5 0x0C	RC (PCPHCR)	Bit Name	0	0	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 6 0x07	R7 (P7ODCR)	Bit Name	OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 6 0x08	R8 (P8ODCR)	Bit Name	OD87	OD86	OD85	OD84	OD83	OD82	0	OD80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P



(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 6 0x09	R9 (P9ODCR)	Bit Name	OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 6 0x0A	RA (PAODCR)	Bit Name	ODA7	ODA6	ODA5	ODA4	ODA3	ODA2	ODA1	ODA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 6 0x0B	RB (PBODCR)	Bit Name	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 6 0x0C	RC (Port C)	Bit Name	0	0	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 7 0x05	R5 (I2CCR1)	Bit Name	Strobe/ Pend	IMS	ISS	Stop	SAR_emptY	ACK	FULL	EMPTY
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-up from Sleep & Idle mode	0	P	P	P	P	P	P	P
Bank 7 0x06	R6 (I2CCR2)	Bit Name	I2CRIF	I2CRIE	I2CTIF	I2CTIE	I2CTS1	I2CTS0	I2CCS	I2CEN
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 7 0x07	R7 (I2CSA)	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 7 0x08	R8 (I2CDA)	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 7 0x09	R9 (I2CA)	Bit Name	0	IBFULL	AMB	IBEN	I2CSPE	I2CSPF	DA9	DA8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 7 0x0A	RA (I2CDB)	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 7 0x0B	RB (DACDL)	Bit Name	DACD7	DACD6	DACD5	DACD4	DACD3	DACD2	DACD1	DACD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	0	P	P	P	P	P	P
Bank 7 0x0C	RC (DACDH)	Bit Name	0	0	0	0	0	0	DACD9	DACD8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P
Bank 7 0x0D	RD (DACC)	Bit Name	DARUN	0	0	SEMC	COF[3]	COF[2]	COF[1]	COF[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	0	P	P	P	P	P
Bank 7 0x0F	RF (I2CCR3)	Bit Name	0	0	0	0	0	0	GCEN	I2CBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep & Idle mode	P	P	P	P	P	P	P	P

## 6.15 Oscillator

### 6.15.1 Oscillator Modes

The EM78P507N can be operated in five different oscillator modes, such as High Crystal oscillator mode (HXT), Crystal oscillator mode (XT), Low Crystal oscillator mode, External RC oscillator mode (ERC), and Internal RC oscillator mode (IRC). You can select one of the five modes by programming the Code Option. The up-limited operation frequency of crystal/resonator on the different VDD is listed in the following table.

#### ■ Summary of Maximum Operating Speeds

Conditions	VDD	Fxt Max. (MHz)
Two clocks	2.2	16
	3.3	20

### 6.15.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P507N can be driven by an external clock signal through the OSCI pin as shown in the following figure.

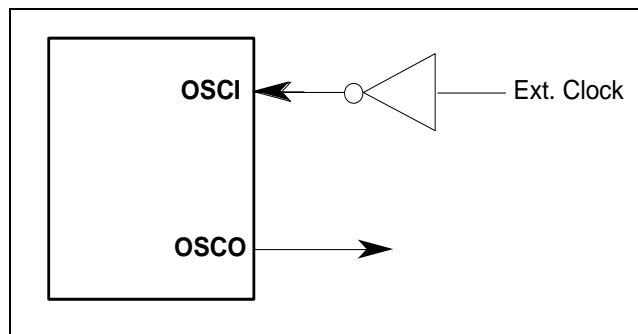


Figure 6-25a External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure below depicts such a circuit. The same applies to the HXT1, HXT2, XT, and LXT mode.

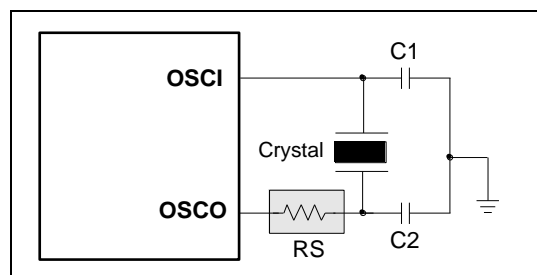


Figure 6-25b Crystal/Resonator Circuit

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, you should refer to their specifications for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
4.0 MHz		20pF	20pF	
Crystal Oscillator	LXT (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455Hz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MHz	30pF	30pF
	HXT1 (6M~12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	30pF	30pF
		12.0 MHz	30pF	30pF
	HXT2 (12M~20 MHz)	12.0 MHz	30pF	30pF
		16 MHz	20pF	20pF
		20 MHz	15pF	15pF

**6.15.3 External RC Oscillator Mode**

For some applications that do not require precise timing calculation, the RC oscillator (right figure) could offer users with an effective cost savings.

Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the resistor values (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

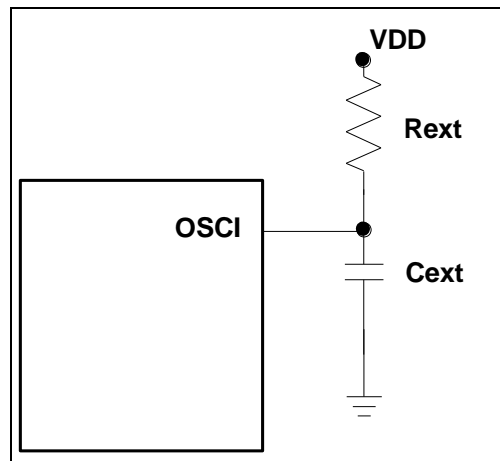


Figure 6-26 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept under this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, will have certain effects on the system frequency.

#### ■ ERC Oscillator Frequencies

Cext	Rext	Average Fosc 3.3V, 25°C	Average Fosc 2.4V, 25°C
20 pF	3.3k	2.9 MHz	2.855 MHz
	5.1k	2.1 MHz	1.92 MHz
	10k	1.1 MHz	1.1 MHz
	100k	135kHz	140kHz
100 pF	3.3k	1.08 MHz	1.05 MHz
	5.1k	727kHz	722kHz
	10k	387kHz	392kHz
	100k	43kHz	45kHz
300 pF	3.3k	457kHz	455kHz
	5.1k	307kHz	307kHz
	10k	162kHz	165kHz
	100k	17.7kHz	19kHz

#### NOTE

1. Data measured and obtained from DIP packages
2. The frequency drift is about  $\pm 30\%$
3. Data is provided design reference use only

#### 6.15.4 Internal RC Oscillator Mode

The EM78P507N offers a versatile internal RC mode with default frequency value of 4 MHz. In Internal RC oscillator mode, it has other frequencies (16 MHz, 8 MHz and 1 MHz) that can be set by Code Option (Word 1), RCM1 and RCM0, and Bank 1 RC. The following table describes the EM78P507N internal RC drift with variation of temperature, voltage, and process.

■ Internal RC Drift Rate ( $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=3.3\text{V}\pm 5\%$ ,  $V_{SS}=0\text{V}$ )

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.0V~3.6V)	Process	Total
4 MHz	±5%	±5%	±2.5%	±12.35%
1 MHz	±5%	±5%	±2.5%	±12.35%
16 MHz	±5%	±5%	±2.5%	±12.35%
8 MHz	±5%	±5%	±2.5%	±12.35%

**NOTE**

*These are theoretical values and are provided for reference only. Actual values may vary according to the actual process involved.*

All the four main frequencies can be calibrated by programming the Option bits, C4~C0. Table below describes a typical instance of the calibration.

■ Calibration Selection for Internal RC Mode

C4	C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	0	(1-28.6%) x F
0	0	0	0	1	(1-27.3%) x F
0	0	0	1	0	(1-25.9%) x F
0	0	0	1	1	(1-24.5%) x F
0	0	1	0	0	(1-23.1%) x F
0	0	1	0	1	(1-21.6%) x F
0	0	1	1	0	(1-20.0%) x F
0	0	1	1	1	(1-18.4%) x F
0	1	0	0	0	(1-16.7%) x F
0	1	0	0	1	(1-14.9%) x F
0	1	0	1	0	(1-13.0%) x F
0	1	0	1	1	(1-11.1%) x F
0	1	1	0	0	(1-9.09%) x F
0	1	1	0	1	(1-6.98%) x F
0	1	1	1	0	(1-4.76%) x F
0	1	1	1	1	(1-2.44%) x F
1	1	1	1	1	F (default)
1	1	1	1	0	(1+2.56%) x F
1	1	1	0	1	(1+5.26%) x F
1	1	1	0	0	(1+8.11%) x F
1	1	0	1	1	(1+11.1%) x F
1	1	0	1	0	(1+14.3%) x F
1	1	0	0	1	(1+17.6%) x F

(Continuation)

C4	C3	C2	C1	C0	Frequency (MHz)
1	1	0	0	0	$(1+21.2\%) \times F$
1	0	1	1	1	$(1+25.0\%) \times F$
1	0	1	1	0	$(1+29.0\%) \times F$
1	0	1	0	1	$(1+33.3\%) \times F$
1	0	1	0	0	$(1+37.9\%) \times F$
1	0	0	1	1	$(1+42.9\%) \times F$
1	0	0	1	0	$(1+48.2\%) \times F$
1	0	0	0	1	$(1+53.8\%) \times F$
1	0	0	0	0	$(1+60.0\%) \times F$

**NOTE**

*These are theoretical values and are provided for reference only. Actual values may vary according to the actual process involved.*

## 6.16 Power-On Considerations

Any microcontroller is not guaranteed to start operating properly before the power supply stabilizes in steady state. The EM78P507N is equipped with Power-on Voltage Detector (POVD) with detection level range of 1.8V to 1.9V. The circuitry eliminates any extra external reset circuit. It will work well if VDD rises fast enough. However, under critical applications, extra devices are still required to assist in solving power-on problems.

### 6.16.1 External Power-on Reset Circuit

The circuit shown at right figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow the VDD to achieve minimum operation voltage. Apply this circuit when the power supply has a slow rise time. As the current leakage from the /RESET pin is about

$\pm 5\mu\text{A}$ , it is recommended that R should not be greater than 40K in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor C will discharge rapidly and fully. The current-limited resistor Rin, prevents high current discharge or ESD (electrostatic discharge) from flowing into /RESET pin.

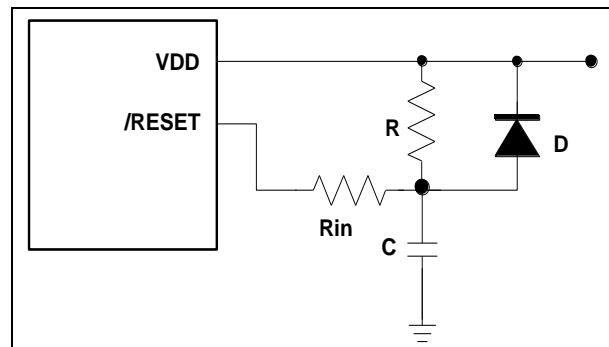


Figure 6-27a External Power on Reset Circuit

### 6.16.2 Residue-Voltage Protection

When battery is replaced, device power (VDD) takes off but residue-voltage remains. The residue-voltage may trips below VDD minimum, but not to zero. This condition may cause a poor power on reset. Figures 6-27b and 6-27c below illustrate how residue-voltage protection circuit is constructed.

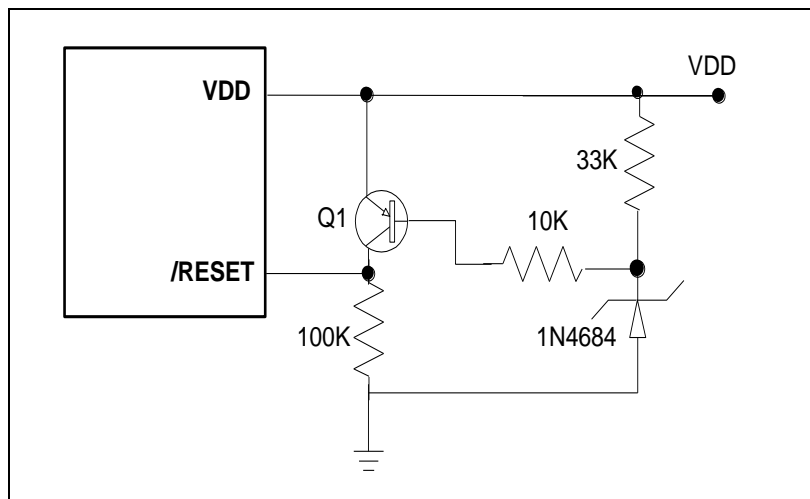


Figure 6-27b Residue Voltage Protection Circuit 1

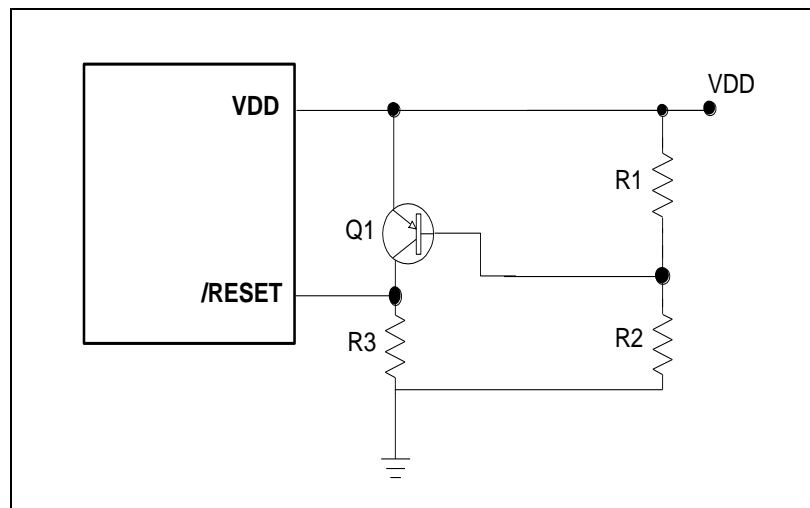


Figure 6-27c Residue Voltage Protection Circuit 2

### 6.17 Code Option

The EM78P507N has three Code Option words and one Customer ID word that are not a part of the normal program memory.

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

### 6.17.1 Code Option Register (Word 0)

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
COBS	-	TYPE	RESETB	ENWDTB	-	-	OSC2	OSC1	OSC0	PR2	PR1	PR0

**Bit 12 (COBS):** Code Option bit selection  
**0:** Select internal Bank 1 RC Bit 2 as code option input. The other code option depends on the H/W definition.  
**1:** Select H/W code option input (default)

**Bit 11:** Not used bit, fixed to "0" all the time.

**Bit 10 (TYPE):** TYPE bit selection for differential package

**EM78P507N TYPE:**

TYPE	Type Selection
0	44 Pins
1	48 Pins

**Bit 9 (RESETB):** Reset Pin Enable Bit  
**0:** Enabled, P81//RESET → RESET pin.  
**1:** Disabled, P81//RESET → P81 (default)

**Bit 8 (ENWDTB):** Watchdog Timer Enable Bit.  
**0:** Enabled  
**1:** Disabled (default)

**Bit 7:** Not used bit, fixed to "1" all the time.

**Bit 6:** Not used bit, fixed to "0" all the time.

**Bits 5~3 (OSC2~OSC0):** Oscillator Modes select bits

Mode	OSC2	OSC1	OSC0
ERC (External RC oscillator mode); PC0/OSCO acts as PC0	0	0	0
ERC (External RC oscillator mode); PC0/OSCO acts as OSC0	0	0	1
IRC (Internal RC oscillator mode); PC0/OSCO acts as PC0 (default)	0	1	0
IRC (Internal RC oscillator mode); PC0/OSCO acts as OSC0	0	1	1
LXT (Low Crystal oscillator mode)	1	0	0
HXT2 (High Crystal 2 oscillator mode)	1	0	1
HXT1 (High Crystal 1 oscillator mode)	1	1	0
XT (Crystal oscillator mode)	1	1	1

**NOTE**

1. Frequency range of HXT2 mode is 20MHz ~ 12MHz.
2. Frequency range of HXT1 mode is 12MHz ~ 6MHz.
3. Frequency range of XT mode is 6MHz ~ 1MHz.
4. Frequency range of LXT mode is 1MHz ~ 100kHz.

Bits 2~0 (PR2~PR0): Protect Bits

PR2~PR0 are protect bits, protect type are as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
0	0	1	Enable
0	1	0	Enable
0	1	1	Enable
1	0	0	Enable
1	0	1	Enable
1	1	0	Enable
1	1	1	Disable

### 6.17.2 Code Option Register (Word 1)

Word 1												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKOEB	RCOUT	EFTIM	-	C4	C3	C2	C1	C0	RCM1	RCM0	HLFS	-

**Bit 12 (CLKOEB):** P9.1 act as CLK output pin

**0:** P9.1 act as CLK output Pin

**1:** P9.1 act as General I/O Pin (default)

**Bit 11 (RCOUT):** System Clock Output Enable Bit in IRC or ERC mode

**0:** OSCO pin is open drain

**1:** OSCO output system clock (default)

**Bit 10 (EFTIM):** EFT Improvement

**0:** Low EFT improvement (default) (2.2V, 16 MHz)

**1:** High EFT improvement (1.8V, 4MHz)

**Bit 9:** Not used bit, fixed to "0" all the time.

**Bits 8~4 (C4~C0):** Calibrator of Internal RC Mode. For IRC calibration value, refer to table under Section 6.15.4, *Internal RC Oscillator Mode*.

**Bits 3~2 (RCM1~RCM0):** RC Mode Selection Bits

RCM 1	RCM 0	*Frequency (MHz)
0	0	1M
0	1	8M
1	0	16M
1	1	4M

**Bits 1 (HLFS):** Reset to Normal or Green Mode Select Bit

**0:** CPU is selected as Green mode when a reset occurs.

**1:** CPU is selected as Normal mode when a reset occurs (default).

**Bit 0:** Not used bit, fixed to "0" all the time.

### 6.17.3 Code Option Register (Word 2)

Word 2												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Customer ID												

## 6.18 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consisting of 2 oscillator periods), unless the program counter is changed by instructions "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BSI R2,6", "CLR R2", etc.). In this case, execution takes one or two instruction cycles as determined by Code Option Register CYES bit.

In addition, the instruction set has the following features:

- 1) Every bit of any register can be set, cleared, or tested directly.
- 2) The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

### ■ EM78P507N Instruction Set Table

In the following Instruction Set table, the following symbols are used:

"R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.

"b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation.

"k" represents an 8 or 10-bit constant or literal value.

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTTC	0 → WDT	T, P
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0001 10rr rrrr	01rr	DECA R	$R-1 \rightarrow A$	Z
0 0001 11rr rrrr	01rr	DEC R	$R-1 \rightarrow R$	Z
0 0010 00rr rrrr	02rr	OR A,R	$A \vee VR \rightarrow A$	Z
0 0010 01rr rrrr	02rr	OR R,A	$A \vee VR \rightarrow R$	Z
0 0010 10rr rrrr	02rr	AND A,R	$A \& R \rightarrow A$	Z
0 0010 11rr rrrr	02rr	AND R,A	$A \& R \rightarrow R$	Z
0 0011 00rr rrrr	03rr	XOR A,R	$A \oplus R \rightarrow A$	Z
0 0011 01rr rrrr	03rr	XOR R,A	$A \oplus R \rightarrow R$	Z
0 0011 10rr rrrr	03rr	ADD A,R	$A + R \rightarrow A$	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	$A + R \rightarrow R$	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	$R \rightarrow A$	Z
0 0100 01rr rrrr	04rr	MOV R,R	$R \rightarrow R$	Z
0 0100 10rr rrrr	04rr	COMA R	$/R \rightarrow A$	Z
0 0100 11rr rrrr	04rr	COM R	$/R \rightarrow R$	Z
0 0101 00rr rrrr	05rr	INCA R	$R+1 \rightarrow A$	Z
0 0101 01rr rrrr	05rr	INC R	$R+1 \rightarrow R$	Z
0 0101 10rr rrrr	05rr	DJZA R	$R-1 \rightarrow A$ , skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	$R-1 \rightarrow R$ , skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	$R(n) \rightarrow A(n-1), R(0) \rightarrow C,$ $C \rightarrow A(7)$	C
0 0110 01rr rrrr	06rr	RRC R	$R(n) \rightarrow R(n-1), R(0) \rightarrow C,$ $C \rightarrow R(7)$	C
0 0110 10rr rrrr	06rr	RLCA R	$R(n) \rightarrow A(n+1), R(7) \rightarrow C,$ $C \rightarrow A(0)$	C
0 0110 11rr rrrr	06rr	RLC R	$R(n) \rightarrow R(n+1), R(7) \rightarrow C,$ $C \rightarrow R(0)$	C
0 0111 00rr rrrr	07rr	SWAPA R	$R(0-3) \rightarrow A(4-7),$ $R(4-7) \rightarrow A(0-3)$	None
0 0111 01rr rrrr	07rr	SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None
0 0111 10rr rrrr	07rr	JZA R	$R+1 \rightarrow A$ , skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	$R+1 \rightarrow R$ , skip if zero	None
0 100b brrr rrrr	0xxx	BC R,b	$0 \rightarrow R(b)$	None
0 101b brrr rrrr	0xxx	BS R,b	$1 \rightarrow R(b)$	None <Note1>
0 110b brrr rrrr	0xxx	JBC R,b	if $R(b)=0$ , skip	None
0 111b brrr rrrr	0xxx	JBS R,b	if $R(b)=1$ , skip	None
1 00kk kkkk kkkk	1kkk	CALL k	$PC+1 \rightarrow [SP],$ $(Page, k) \rightarrow PC$	None

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	$A \vee k \rightarrow A$	Z
1 1010 kkkk kkkk	1Akk	AND A,k	$A \& k \rightarrow A$	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	$A \oplus k \rightarrow A$	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK K	K → R4(7:6)	None
1 1110 1010 kkkk	1EAK	LCALL	Next instruction: k kkkk kkkk kkkk; PC+1 → [SP], k → PC	None
1 1110 1011 kkkk	1EBK	LJMP	Next instruction: k kkkk kkkk kkkk; k → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 11rr rrrr	1Err	TBRD R	If R6, machine code(0:7) → R else R5 machine code (12:8) → R	None

**NOTE**

*These instructions cannot operate under interrupt status register.*

## 7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	V <sub>ss</sub> -0.3V	to	V <sub>dd</sub> +0.3V
Output voltage	V <sub>ss</sub> -0.3V	to	V <sub>dd</sub> +0.3V
Working Voltage	2.2V	to	3.6V
Working Frequency	DC	to	20 MHz

## 8 Electrical Characteristics

### 8.1 DC Electrical Characteristics

■ Ta= 25°C, VDD= 3.3V, VSS= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 3.6V	Two cycles with two clocks	0.1	-	20	MHz
ERC	ERC: VDD to 3.3V	R: 5.1KΩ, C: 100 pF	505	760	945	kHz
IRC1	IRC:VDD to 3.3V	RCM0:RCM1=1:1		4		MHz
IRCE	Internal RC oscillator error per stage	-		±2.5		%
IRC2	IRC:VDD to 3.3V	RCM0:RCM1=1:0		16		MHz
IRC3	IRC:VDD to 3.3V	RCM0:RCM1=0:1		8		MHz
IRC4	IRC:VDD to 3.3V	RCM0:RCM1=0:0		1		MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 7, 8, 9, A, B, C	0.7VDD	-	-	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 7, 8, 9, A, B, C	VSS	-	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7VDD	-	-	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	VSS	-	0.3VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	0.8VDD	-	-	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	-	-	0.3VDD	V
IOH	Output High Voltage (Ports 5, 6, 7, 8, 9, A)	VOH = VDD-0.1VDD	-	-3.6	-	mA
IOL	Output Low Voltage (Ports 5, 6, 7, 8, 9, A)	VOL = GND+0.1VDD	-	6	-	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-20	-25	-30	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	-	1		μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	-	5		μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type), output pin floating, WDT disabled	-	1.5		mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=16 MHz (Crystal type), output pin floating, WDT enabled	-	6		mA
ICC3	Operating supply current at two clocks	/RESET= 'High', In Green mode, output pin floating, WDT enabled	-	10		μA
ICC4	Operating supply current at two clocks	/RESET= 'High', in idle mode, output pin floating, WDT enabled	-	6		μA

## 8.2 AC Electrical Characteristics

■ Ta= -40°C ~ 85°C, VDD=3.3V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	125	-	DC	ns
		RC type	500	-	DC	ns
Tdrh	Device reset hold time	Ta = 25°C	9	18	30	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
Twdt	Watchdog timer period	Ta = 25°C	9	18	30	ms
Tset	Input pin setup time	-	-	0	-	ns
Thold	Input pin hold time	-	-	20	-	ns
Tdelay	Output pin delay time	Cload=20pF	-	50	-	ns

## 9 Timing Diagrams

### ■ AC Timing

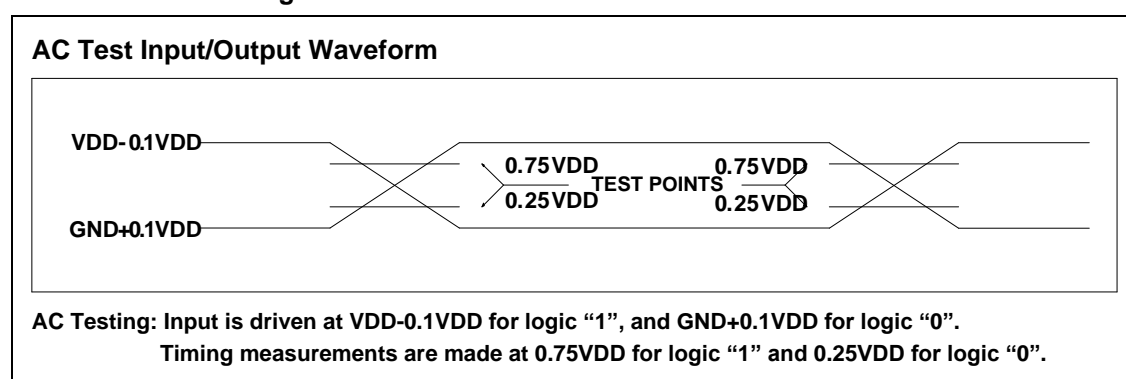


Figure 9-1a AC Timing Diagram

■ Reset Timing

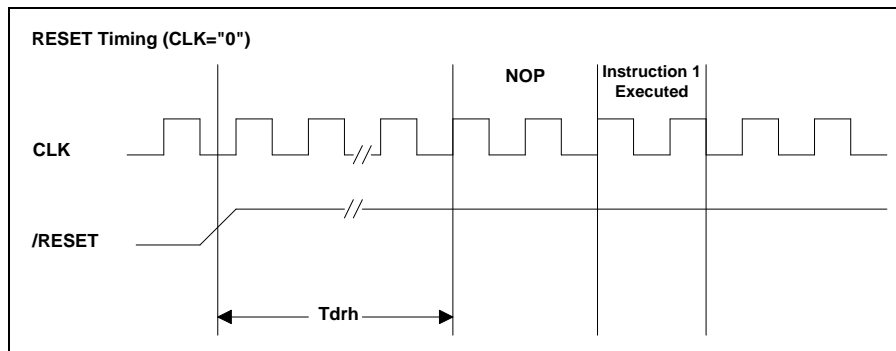


Figure 9-1b Reset Timing Diagram

■ TCC Input Timing

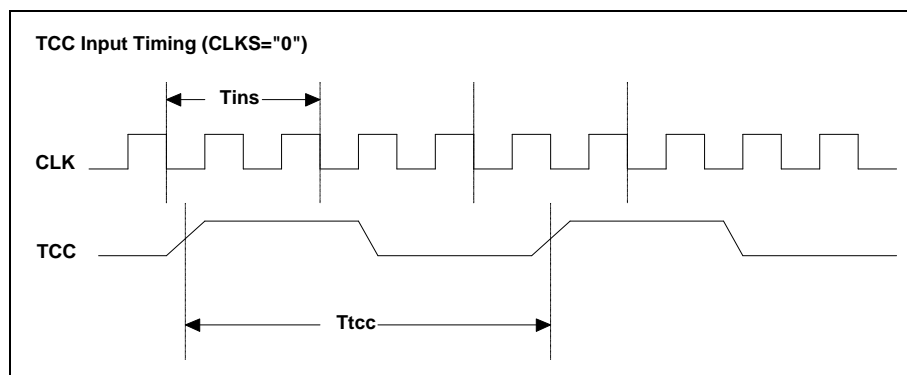
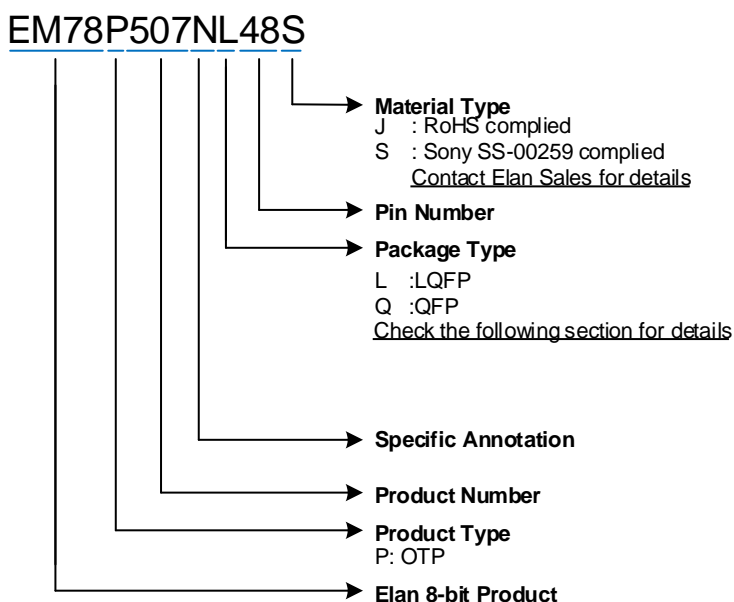


Figure 9-1c TCC Input Timing Diagram

## APPENDIX

### A Ordering and Manufacturing Information

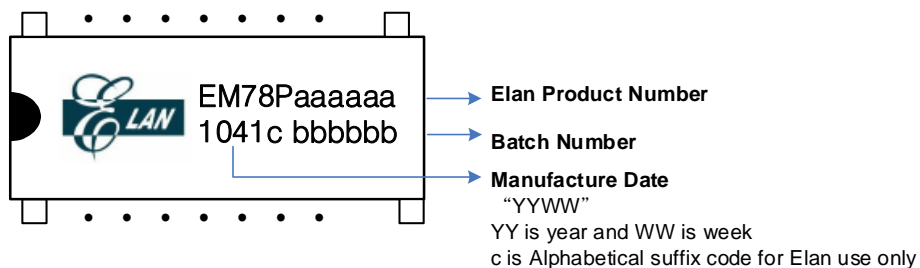


For example:

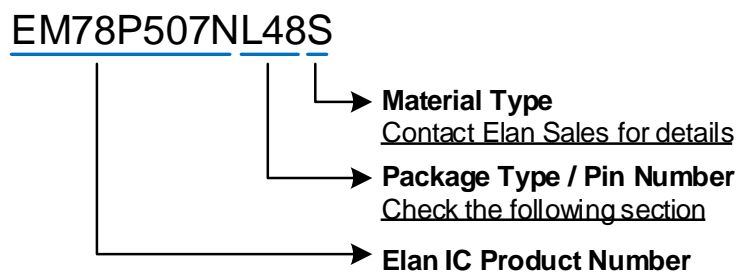
**EM78P507NL48S**

is EM78P507N with OTP program memory, industrial grade product, in 48-pin LQFP 7x7mm package with SONY SS-00259 complied

### IC Mark



## Ordering Code



## B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78P507NL44	LQFP	44	10*10 mm
EM78P507NQ44	QFP	44	10*10 mm
EM78P507NL48	LQFP	48	7*7 mm

### NOTE

- These are Green products which do not contain hazardous substances.
- These products comply with the 3<sup>rd</sup> edition of Sony SS-00259 Standard.
- Pb contents of these products are less than 100ppm and comply with Sony specifications.