HM62A9128/8128 Series

131072-word × 9 (8)-bit Synchronous Cache SRAM

Features

- For high speed cache memory applications
- Pipeline access capability with on-chip address, strobe and I/O resisters
- Organization: 128 kword × 9(8) bit
- SOJ - 32-pin
- TTL I/O

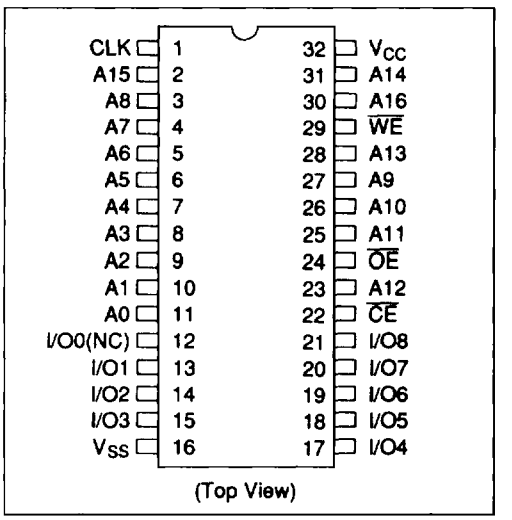
Main Characteristics

Item	Spec.	Remarks
Clock cycle time	20 ns (min)	
Clock to data valid	10 ns (max)	
Power dissipation	825 mW (max)	50 MHz

Ordering Information

Type No.	Clock cycle time	Package
HM62A9128JP–20	20 ns	32-pin SOJ (CP-32D)
HM62A8128JP–20	20 ns	

Pin Arrangement



(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O8	Input/output
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
CLK	Clock input
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection (for × 8)

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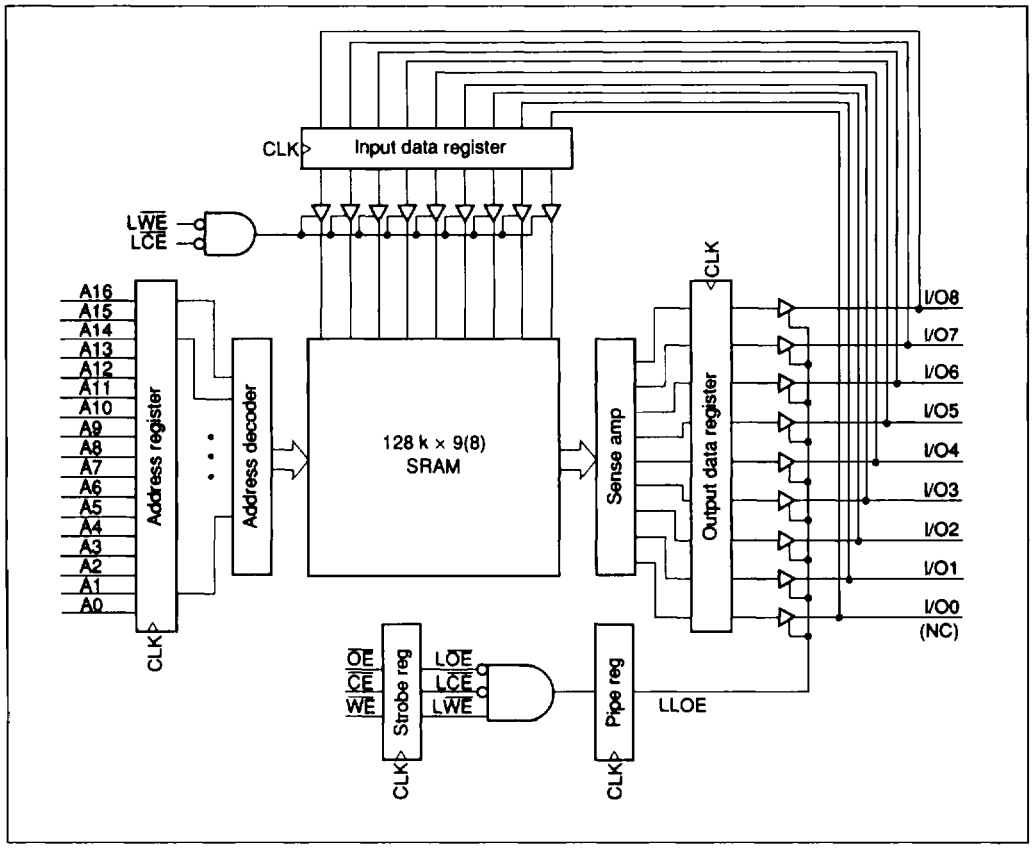
Block Diagram



Function Table

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Din	CLK	SRAM mode	Next cycle Dout	Ref. cycle
H	X	X	X	↗	Not selected	High-Z	Read cycle
L	H	H	X	↗	Not selected	High-Z	
L	L	H	X	↗	Read	Read data	Read cycle
L	H	L	Data	↗	Write	High-Z	Write cycle
L	L	L	Data	↗	Write	High-Z	

Note: 1. After power-on (V_{CC} in specification),CLK will be active for 10 cycles before any operation starts.
2. $\overline{CE}$,$\overline{OE}$ and $\overline{WE}$ will be in specification for at least 2 cycles before the first operation starts.
3. When the write after the read, the wait status more than 2cycles should be inserted due to the avoidance of data collision.

Registers

CLK	Mode	Register output
↗	Load	Register input
L or H	Hold	Not changed

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.2	—	6.0	V	
	V_{IL}	–0.5	—	0.8	V	1

Note: 1. –2.0 V for pulse width ≤ 10 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.5 V, Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	Dout High-Z state $V_{I/O}$ = V_{SS} to V_{CC}
Average operating current	I_{CC1}	—	—	150	mA	Min. cycle, $\overline{CE}$ = V_{IL} Duty: 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	110	mA	CLK ≤ V_{IL}, Min. cycle
	I_{SB1}	—	—	10	mA	Power standby, CLK ≤ 0.2 V, $\overline{CE} \geq V_{CC}$ – 0.2 V Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1.0 MHz)

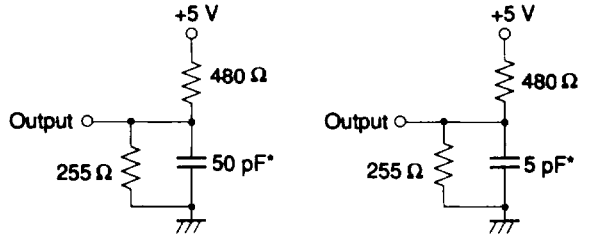
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 2 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figure



Output Load (A)

Output Load (B) (for t_{HZ}, t_{LZ})

*Including scope and jig capacitance

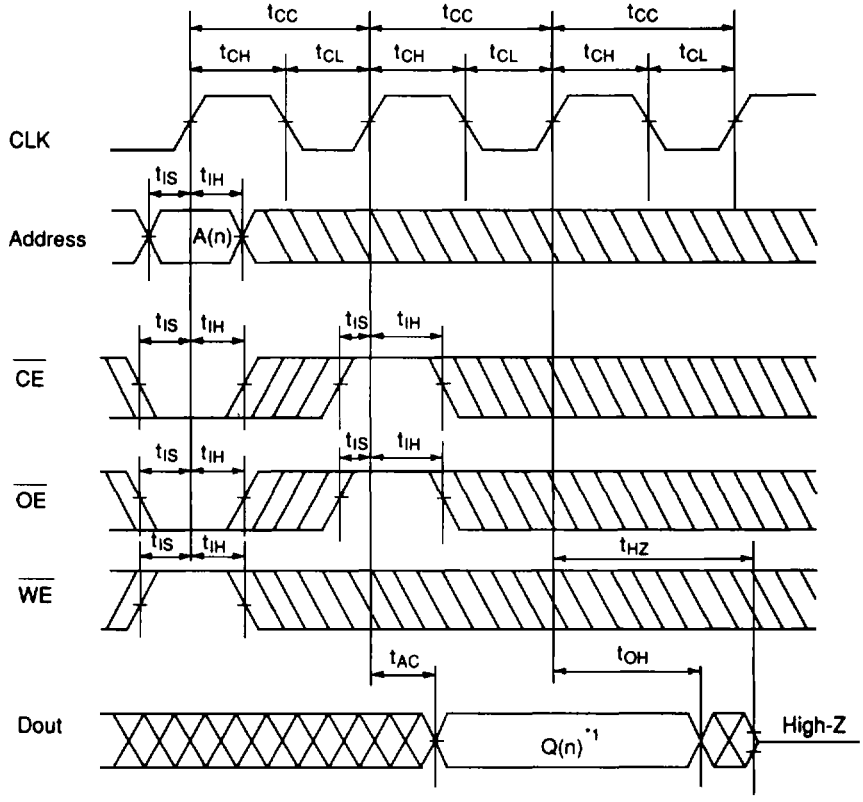
Read and Write Cycle

Parameter	Symbol	Min	Max	Unit	Notes
Clock cycle time	t_{CC}	20	—	ns	3
Clock high pulse width	t_{CH}	5	—	ns	
Clock low pulse width	t_{CL}	5	—	ns	
Input setup time (address, data, strobes)	t_{IS}	3	—	ns	
Input hold time (address, data, strobes)	t_{IH}	1	—	ns	
Clock to output data valid	t_{AC}	—	10	ns	
Output data hold from clock	t_{OH}	3	—	ns	
Clock to output in Low-Z	t_{LZ}	0	—	ns	1, 2
Clock to output in High-Z	t_{HZ}	—	10	ns	1, 2

Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
2. This parameter is sampled and not 100% tested.
3. The rise time and fall time of CLK: 10 ns(max.)

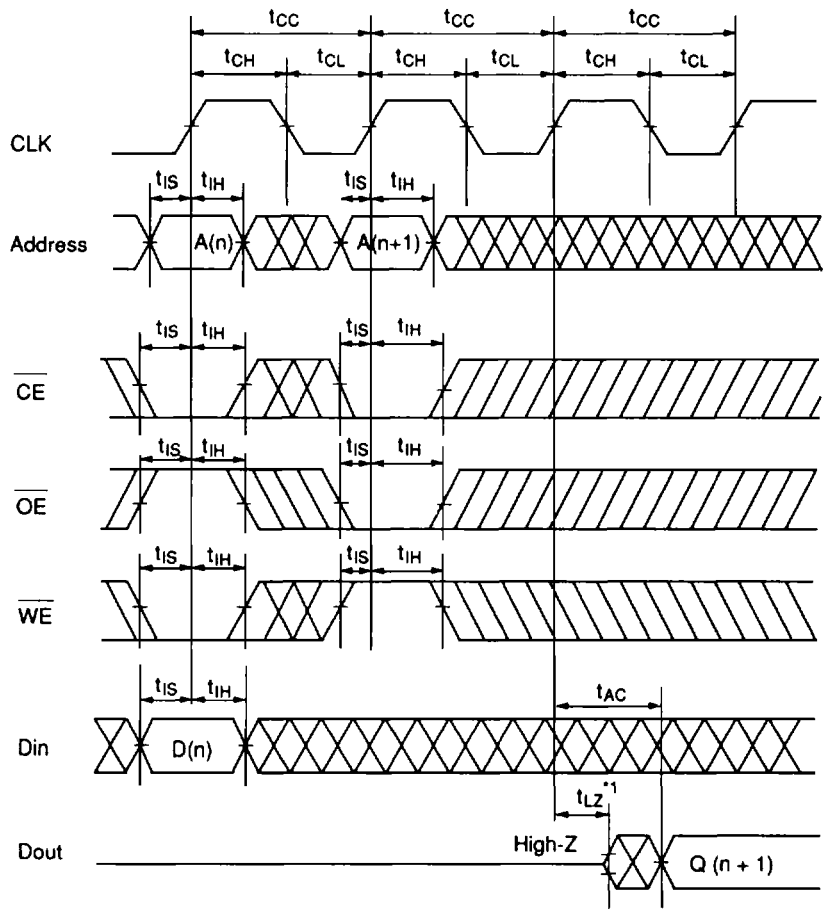
Timing Waveforms

Read Cycle



Notes: 1. Read data is valid on next cycle.
2. High impedance state is obtained on next cycle from $\overline{CE}$ = H, $\overline{OE}$ = H, or $\overline{WE}$ = L

Write/Read Cycle



Notes: 1. Low impedance state is obtained on next cycle from $\overline{OE}$ = L, $\overline{CE}$ = L, and $\overline{WE}$ = H.

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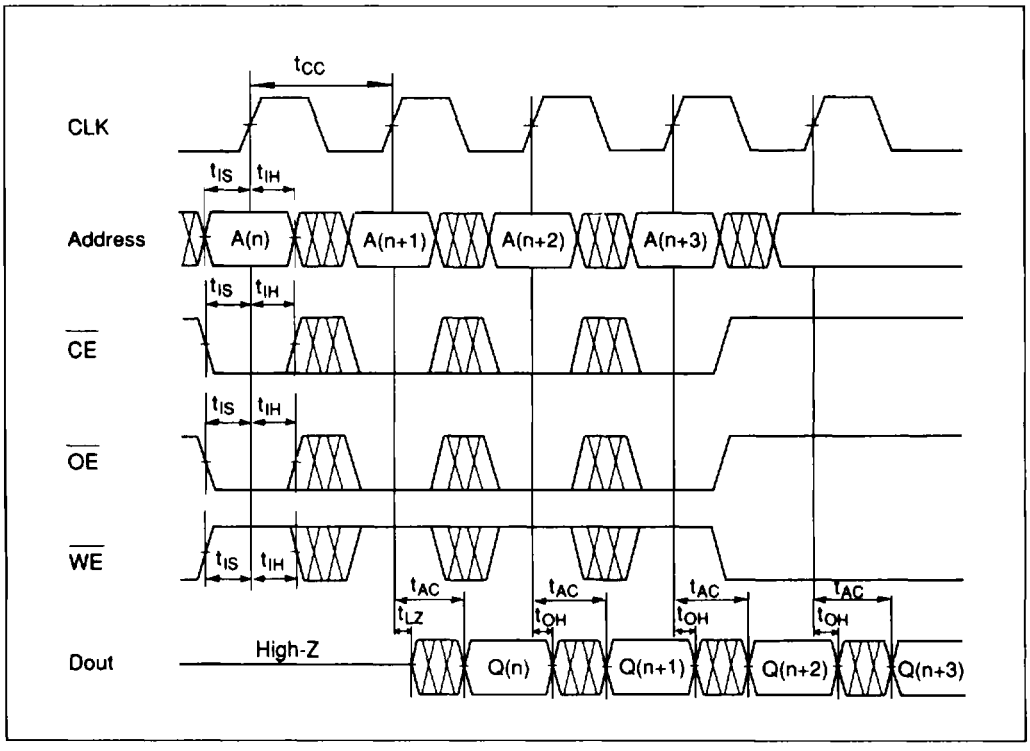
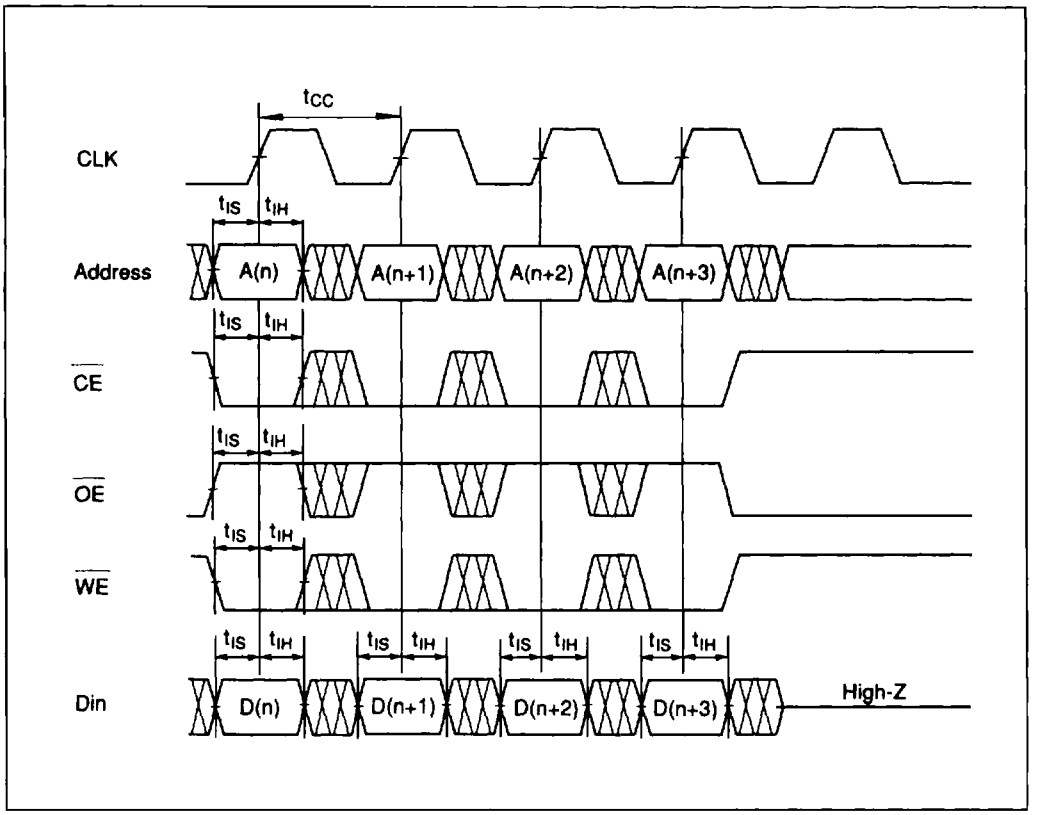
Pipelined Read Cycle



Pipelined Write Cycle



Alternate Read/Write/Read Cycle