19-0383; Rev 0; 7/05

Quad, Low-Power, 1200Mbps ATE Driver

General Description

The MAX9977 quad, low-power, high-speed, pin-electronics driver includes, for each channel, a three-level pin driver. The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings.

The MAX9977 provides high-speed, differential control inputs with internal 50Ω (100Ω LVDS) termination resistors that allow compatibility with 1.8V and 3.5V terminated 0.4VP-P CML, reducing the discrete component count required on the circuit board. The MAX9977AD has no internal termination.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage and tri-state/terminate operational configurations of the MAX9977.

The MAX9977's operating range is -1.5V to +6.5V (consult factory for other operating ranges), and features a maximum power dissipation of only 0.8W per channel. The device is available in a 100-pin, 14mm x 14mm x 0.1mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +60°C to +100°C, and features a die temperature monitor output.

Applications

Medium-Performance System-on-Chip ATE and Memory Applications

Features

- **Low Power Dissipation: 0.8W/Channel**
- **High Speed: 1200Mbps at 3VP-P and 1800Mbps at 1VP-P**
- **Low Timing Dispersion**
- **Wide -1.5V to +6.5V Operating Range**
- **Interfaces Easily with Most Logic Families**
- **Active Termination (3rd-Level Drive)**
- **Internal 50Ω Termination Resistors on Control Inputs**
- **Low Gain and Offset Errors**
- **Pin Compatible with the MAX9963 and MAX9965 Quad Drivers**

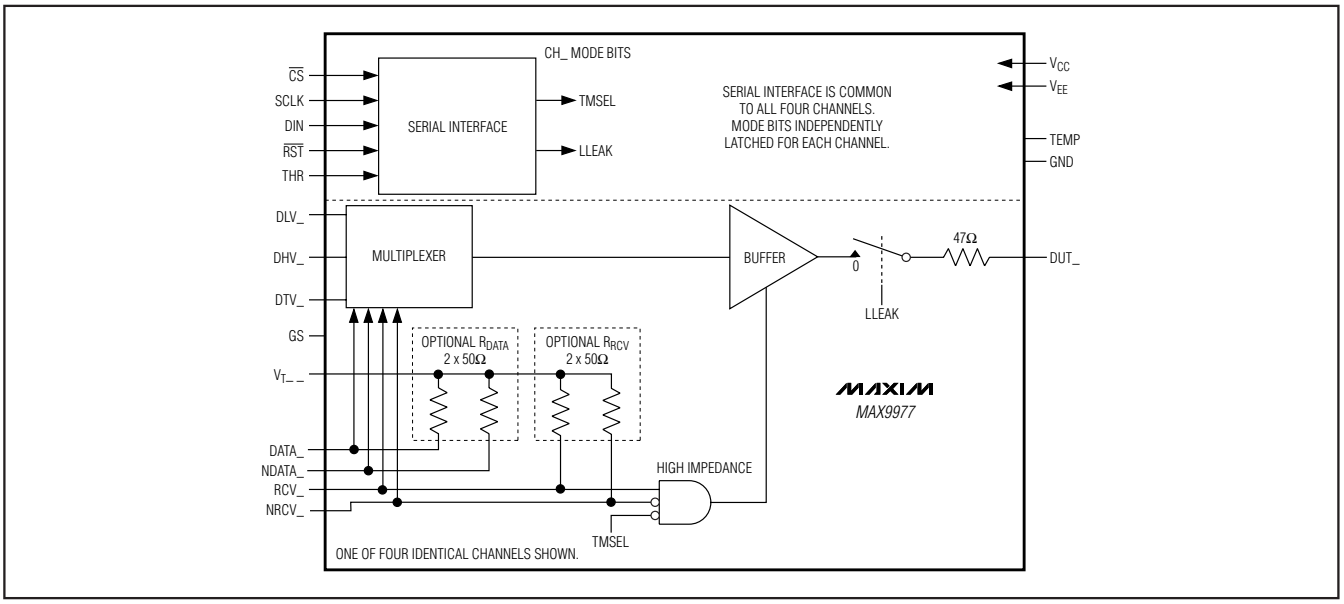
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	EXPOSED PAD VARIATION CODE
MAX9977AKCCQ	0°C to +70°C	100 TQFP-IDP**	C100E-8R
MAX9977AKCCQ+	0°C to +70°C	100 TQFP-IDP**	C100E-8R
MAX9977ADCCQ*	0°C to +70°C	100 TQFP-IDP**	C100E-8R
MAX9977ADCCQ+*	0°C to +70°C	100 TQFP-IDP**	C100E-8R

*Future product—contact factory for availability.
**IDP = Inverted die pad.
+Denotes lead-free package.

Pin Configuration and Selector Guide appear at end of data sheet.

Functional Diagram



Quad, Low-Power, 1200Mbps ATE Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11V
V_{EE} to GND .....-5.75V to +0.3V
V_{CC} - V_{EE} .....-0.3V to +16.75V
DUT_ to GND .....-2.75V to +7.5V
DATA_, NDATA_, RCV_, NRCV_ to GND .....-2.5V to +5V
DATA_ to NDATA_, RCV_ to NRCV_ .....±1.5V
V_T12, V_T34 to GND .....-2.5V to +5V
DATA_, NDATA_, RCV_, NRCV_ to V_T12 or V_T34 .....±2V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$ to GND .....-1V to +5V
DHV_, DLV_, DTV_ to GND .....-2.5V to +7.5V
DHV_ to DLV_ .....±10V
DHV_ to DTV_ .....±10V
DLV_ to DTV_ .....±10V
GS to GND .....±1V
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TEMP Current .....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V .....Continuous
Continuous Power Dissipation (T_A = +70°C)
100-Pin TQFP (derate 167mW/°C above +70°C) 13.3W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-5.25	-4.75	-4.50	V
Positive Supply Current (Note 2)	I_{CC}	Drivers active		192	215	mA
		Drivers in high impedance		175	196	
Negative Supply Current (Note 2)	I_{EE}	Drivers active		-224	-251	mA
		Drivers in high impedance		-207	-232	
Power Dissipation (Note 2)	P_D	Drivers active		3.0	3.3	W
		Drivers in high impedance		2.7	3.1	
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 3)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V			±3	µA
Leakage Current in Low-Leakage Mode		LLEAK = 1; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V		±5	±50	nA
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		2	5	pF
		Driver in high-impedance mode		4	6	
Low-Leakage Enable Time		(Notes 4, 5)		20		µs
Low-Leakage Disable Time		(Notes 5, 6)		0.1		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Notes 5, 6)		5		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL AND LEVELS INPUTS						
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling Time		To 0.1% of full-scale change		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)						
Input High Voltage	V_{IHD}		0		3.5	V
Input Low Voltage	V_{ILD}		-0.2		+3.2	V
Differential Input Voltage	V_{DIFF}	Between differential inputs	±0.15		±1.00	V
		Between a differential input and its termination voltage			±1.9	
Input Termination Voltage	$V_{T\_\_}$		0		+3.5	V
Input Termination Resistor		Between signal and corresponding termination voltage input	47.5	50	52.5	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 4)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		3.5			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		3.5			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}		20			ns
TEMPERATURE MONITOR (TEMP)						
Nominal Voltage		T_J = +70°C, R_L ≥ 10MΩ		3.33		V
Temperature Coefficient				+10		mV/°C
Output Resistance				20		kΩ

Quad, Low-Power, 1200Mbps ATE Driver

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVERS (Note 7)						
DC OUTPUT CHARACTERISTICS ($R_L \geq 10M\Omega$)						
DHV_, DLV_, DTV_ Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V			±15	mV
Output Offset Voltage Due to Ground Sense	V_{GSOS}	V_{GS} = +100mV, $V_{DHV\_}$ = 6.5V + 100mV		±2		mV
		V_{GS} = -100mV, $V_{DLV\_}$ = -1.5V - 100mV		±2		
DHV_, DLV_, DTV_ Output Offset Temperature Coefficient				+200		µV/°C
DHV_, DLV_, DTV_ Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V	0.997	1.00	1.003	V/V
DHV_, DLV_, DTV_ Gain Temperature Coefficient				-50		ppm/°C
Linearity Error		$V_{DUT\_}$ = 1.5V, 3V (Note 8)			±5	mV
		Full range (Notes 8, 9)			±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0; $V_{DHV\_}$ = 200mV, 6.5V			±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V; $V_{DLV\_}$ = -1.5V, +4.8V			±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0; $V_{DTV\_}$ = -1.5V, +6.5V			±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DLV\_}$ = 0; $V_{DHV\_}$ = 1.6V, 3V			±2	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0, 1.4V			±2	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 10)			±18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$		±40		±80	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 11)	46	47	48	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1mA, ±8mA		0.5	1	Ω
		$I_{DUT\_}$ = ±1mA, ±8mA, ±15mA, ±40mA		0.75	1.5	
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)						
AC Drive Current			±80			mA
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		15	22	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		110	130	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		210	370	
Drive-Mode Undershoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		4	11	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		20	65	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		30	185	
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0		180	250	mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V		180	250	
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0		100		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		100		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time to within 25mV		3V step (Note 12)		4		ns
Settling Time to within 5mV		3V step (Note 12)		40		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 13)						
Prop Delay, Data to Output	t_{PDD}		1.2	1.5	1.9	ns
Prop Delay Match, t_{LH} vs. t_{HL}		$3V_{P-P}$		±40	±100	ps
Prop Delay Match, Drivers within Package		(Note 14)		40		ps
Prop-Delay Temperature Coefficient				+1.6		ps/°C
Prop Delay Change vs. Pulse Width		$0.2V_{P-P}$, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width		±25	±50	ps
		$1V_{P-P}$, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width		±25	±50	
		$2V_{P-P}$, 40MHz, 0.75ns to 24.25ns pulse width, relative to 12.5ns pulse width		±30	±55	
		$3V_{P-P}$, 40MHz, 0.9ns to 24.1ns pulse width, relative to 12.5ns pulse width		±35	±60	
		$5V_{P-P}$, Z_L = 500Ω, 40MHz, 1.4ns to 23.6ns pulse width, relative to 12.5ns pulse width		±100		
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		50	75	ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	1.6	2.1	2.6	ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	2.6	3.2	3.9	ns
Prop Delay Match, t_{PDDZ} vs. t_{PDZD}			-1.5	-1.1	-0.7	ns
Prop Delay Match, t_{PDDZ} vs. t_{LH}			0.2	0.6	1.0	ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	1.3	1.8	2.3	ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	1.6	2.1	2.7	ns
Prop Delay Match, t_{PDDT} vs. t_{PDTD}			-0.7	-0.3	-0.1	ns
Prop Delay Match, t_{PDDT} vs. t_{LH}			-0.1	+0.3	+0.7	ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 10% to 90%	260	310	360	ps
		$1V_{P-P}$, 10% to 90%	330	390	450	
		$2V_{P-P}$, 10% to 90%	430	500	570	
		$3V_{P-P}$, 10% to 90%	500	650	750	
		$5V_{P-P}$, Z_L = 500Ω, 10% to 90%	800	1000	1200	
Rise and Fall Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±50		ps

Quad, Low-Power, 1200Mbps ATE Driver

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Pulse Width (Note 15)		$0.2V_{P-P}$		550		ps
		$1V_{P-P}$		550	630	
		$2V_{P-P}$		650	750	
		$3V_{P-P}$		850	1000	
		$5V_{P-P}$, Z_L = 500Ω		1300		
Data Rate (Note 16)		$0.2V_{P-P}$		1800		Mbps
		$1V_{P-P}$		1800		
		$2V_{P-P}$		1500		
		$3V_{P-P}$		1200		
		$5V_{P-P}$, Z_L = 500Ω		800		
Dynamic Crosstalk		(Note 17)		15		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 18)	0.6	1.0	1.3	ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 18)	0.6	1.0	1.3	ns
GROUND SENSE						
GS Voltage Range	V_{GS}		±250			mV
GS Input Bias Current		V_{GS} = 0			±25	µA

Note 1: Unless otherwise specified, all minimum and maximum DC and AC driver 3V rise and fall time test limits are 100% tested at production. All other test limits are guaranteed by design. All tests are performed at nominal supply voltages, unless otherwise noted.

Note 2: Total is for a quad device and is specified at the worst-case setting. The supply currents are measured with typical supply voltages.

Note 3: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

Note 4: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 5: Based on simulation results only.

Note 6: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 7: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 8: Specifications measured at the end points of the full range. Full range is -1.3V ≤ $V_{DHV\_}$ ≤ +6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ +6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ +6.5V.

Note 9: Relative to straight line between 0 and 4.5V.

Note 10: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 11: Nominal target value is 47Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 12: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 13: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs DATA_ and RCV_ are 250ps (10% to 90%).

Note 14: Rising edge to rising edge or falling edge to falling edge.

Note 15: Specified amplitude is programmed. At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 16: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 90% of its programmed amplitude may be generated at one-half of this frequency.

Note 17: Crosstalk from one driver to any other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 18: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_} < V_{DTV\_} < V_{DHV\_}$. If $V_{DTV\_} < V_{DLV\_}$ or $V_{DTV\_} > V_{DHV\_}$, switching speed is degraded by a factor of approximately 3.

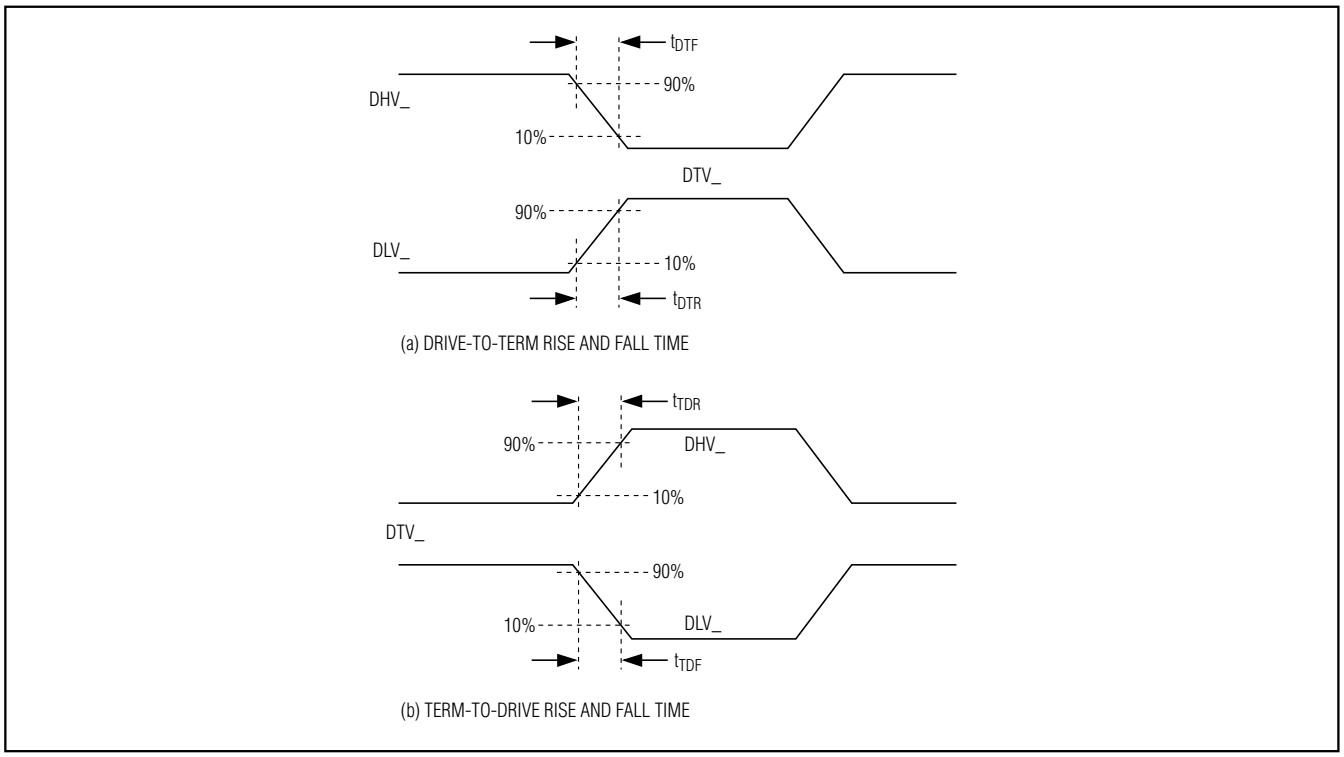
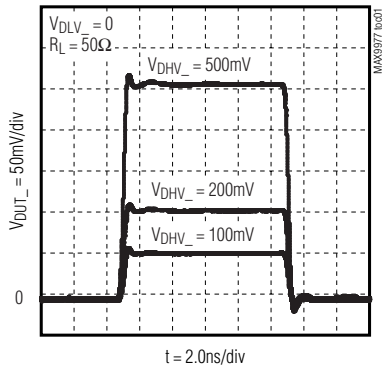


Figure 1. Drive-to-Term and Term-to-Drive Rise and Fall Times

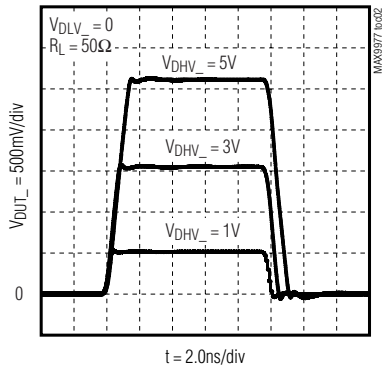
Typical Operating Characteristics

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

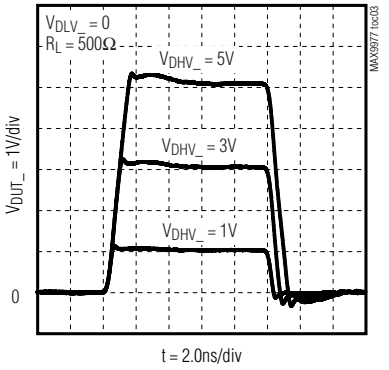
DRIVER SMALL-SIGNAL RESPONSE



DRIVER LARGE-SIGNAL RESPONSE



DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω

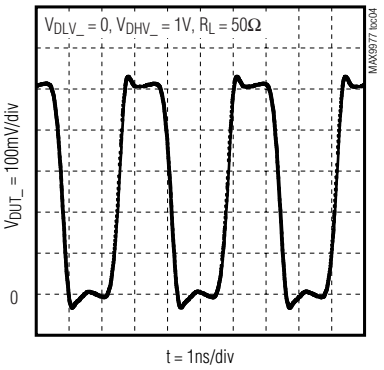


Quad, Low-Power, 1200Mbps ATE Driver

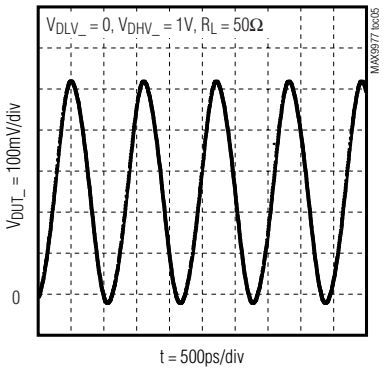
Typical Operating Characteristics (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

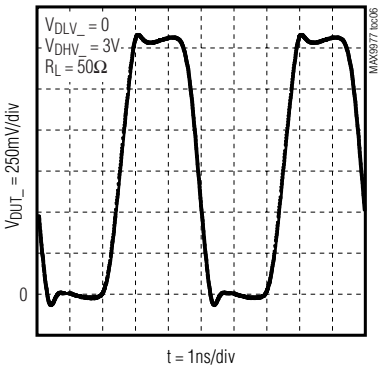
DRIVER 1V, 600Mbps SIGNAL RESPONSE



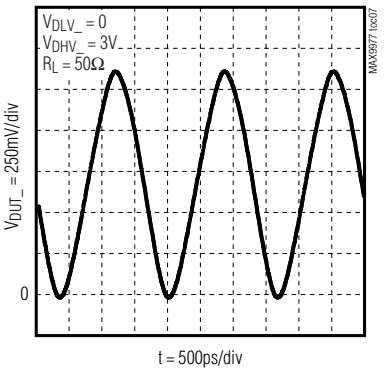
DRIVER 1V, 1800Mbps SIGNAL RESPONSE



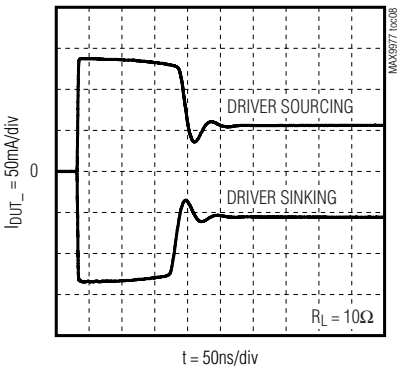
DRIVER 3V, 400Mbps SIGNAL RESPONSE



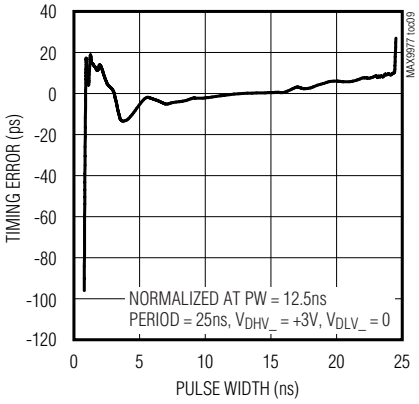
DRIVER 3V, 1200Mbps SIGNAL RESPONSE



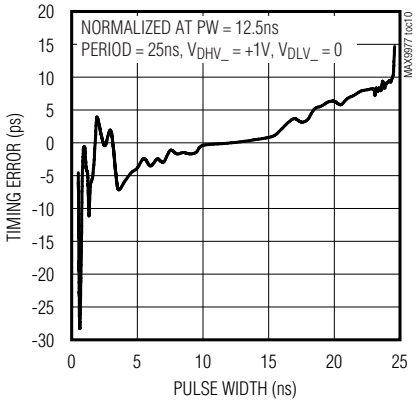
DRIVER DYNAMIC CURRENT-LIMIT RESPONSE



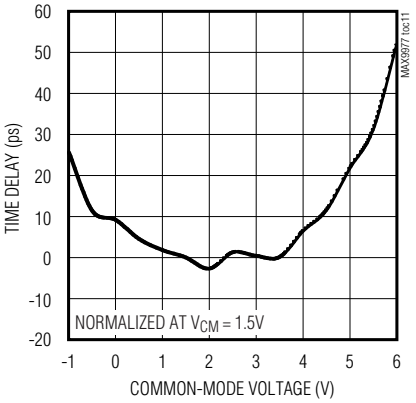
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



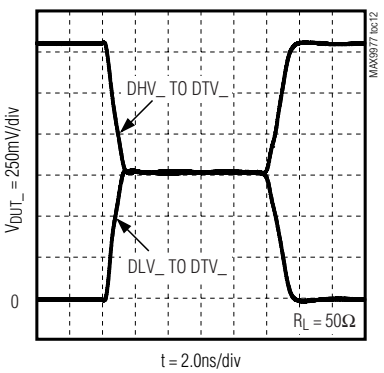
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



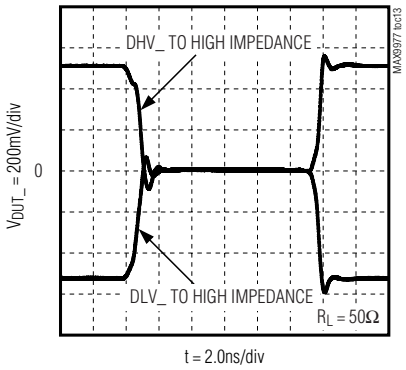
DRIVE TO TERM TRANSITION



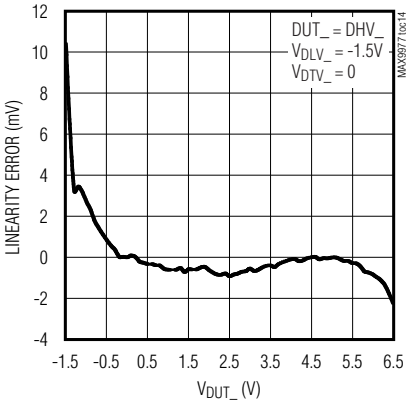
Typical Operating Characteristics (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

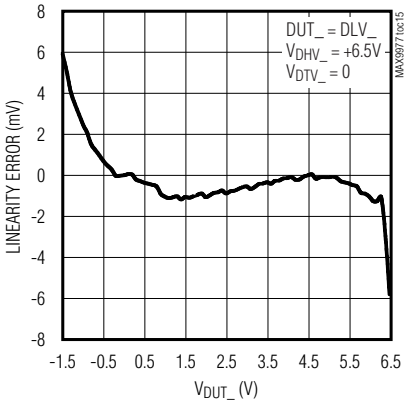
DRIVE TO HIGH-IMPEDANCE TRANSITION



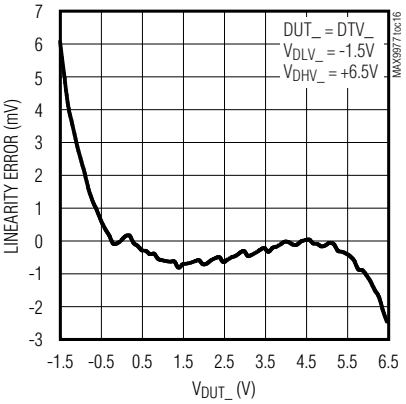
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



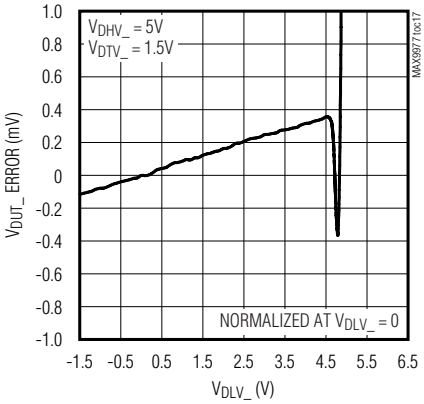
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



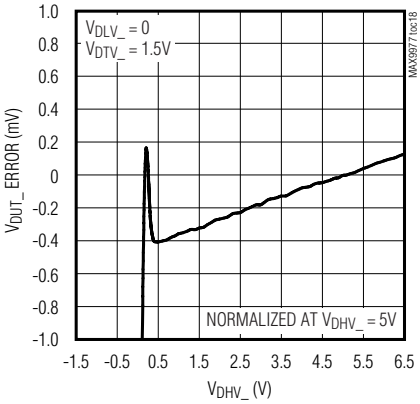
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



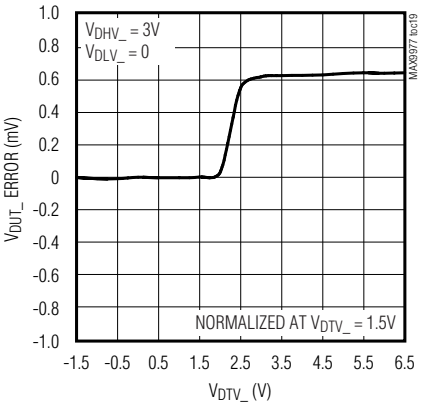
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



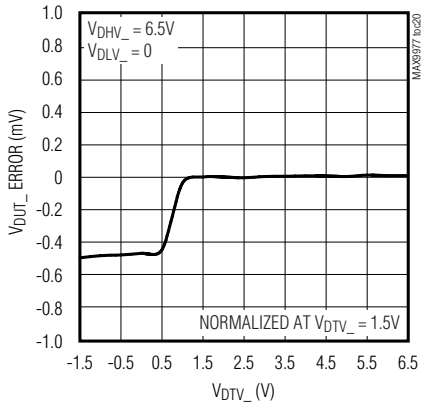
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



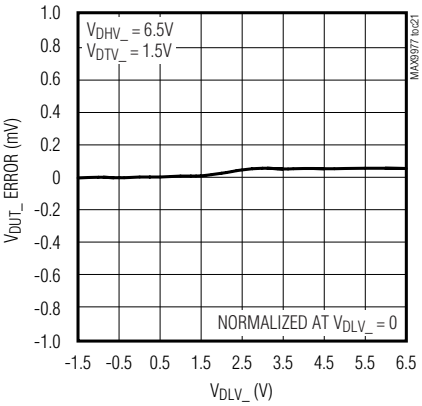
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_

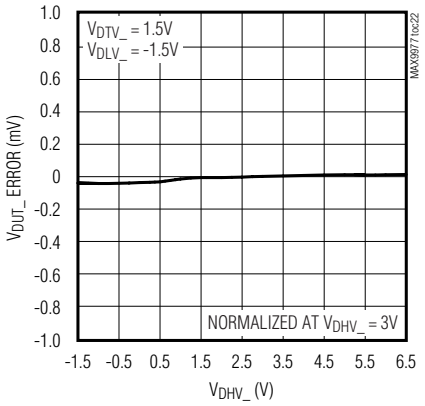


Quad, Low-Power, 1200Mbps ATE Driver

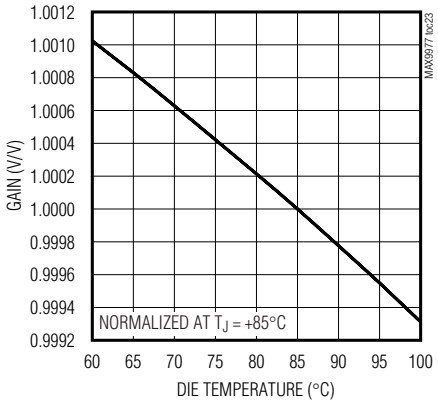
Typical Operating Characteristics (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

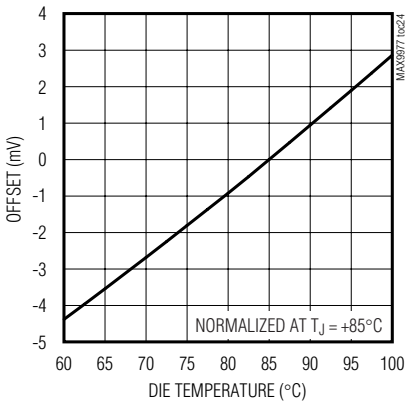
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



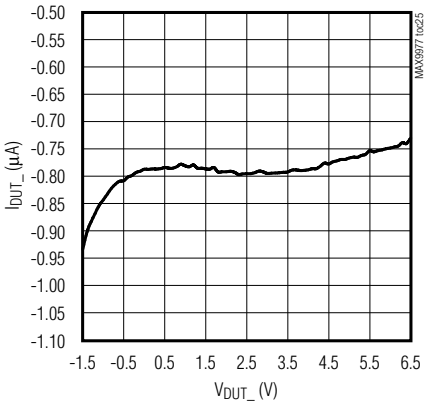
DRIVER GAIN vs. TEMPERATURE



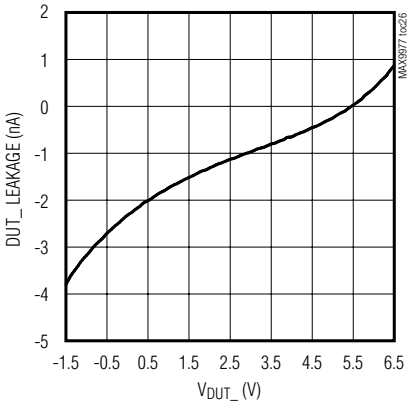
DRIVER OFFSET vs. TEMPERATURE



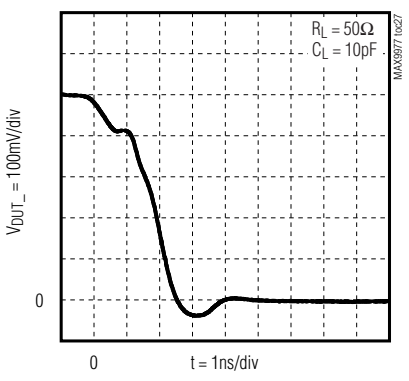
HIGH-IMPEDANCE CURRENT vs. DUT_ VOLTAGE



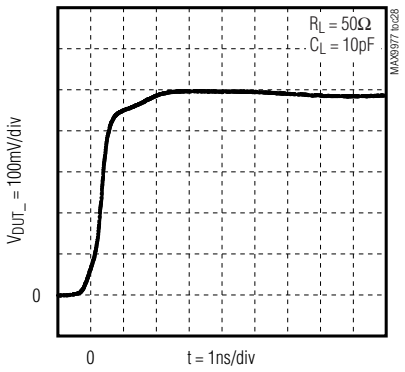
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



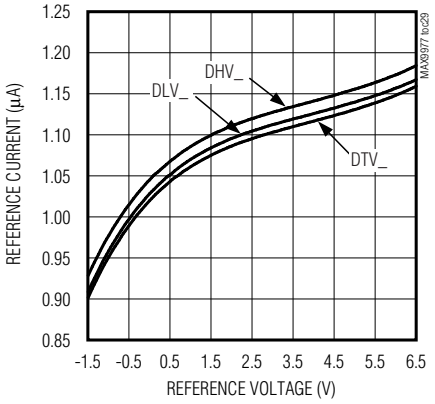
DRIVE 1V TO LOW-LEAKAGE TRANSITION



LOW-LEAKAGE TO DRIVE 1V TRANSITION



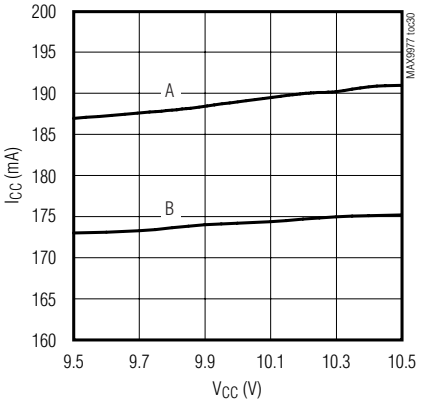
DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE



Typical Operating Characteristics (continued)

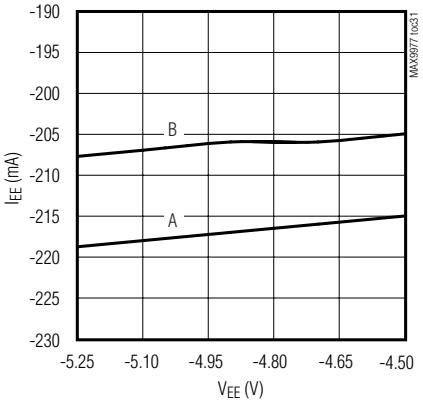
(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

SUPPLY CURRENT I_{CC} vs. VOLTAGE CURRENT V_{CC}



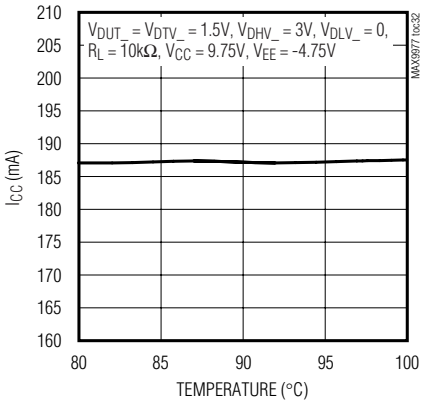
A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$, $R_L = 10k\Omega$, $V_{EE} = -4.75V$
B: SAME AS A EXCEPT DRIVER IN HIGH-IMPEDANCE MODE

SUPPLY CURRENT I_{EE} vs. VOLTAGE CURRENT V_{EE}

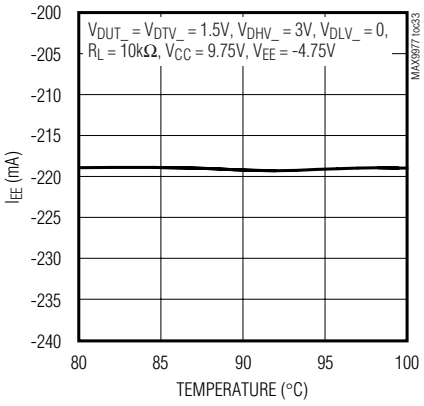


A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$, $R_L = 10k\Omega$, $V_{CC} = 9.75V$
B: SAME AS A EXCEPT DRIVER IN HIGH-IMPEDANCE MODE

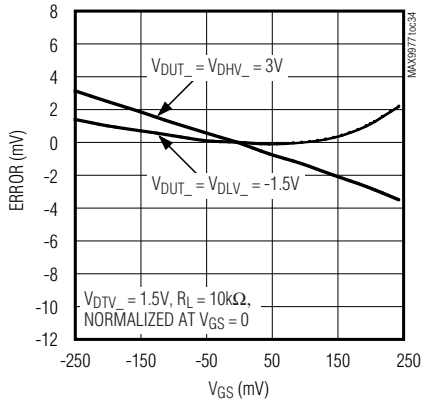
SUPPLY CURRENT I_{CC} vs. TEMPERATURE



SUPPLY CURRENT I_{EE} vs. TEMPERATURE



DRIVER OUTPUT-VOLTAGE ERROR vs. GROUND-SENSE VOLTAGE



Quad, Low-Power, 1200Mbps ATE Driver

Pin Description

PIN	NAME	FUNCTION
1	V_T34	Channel 3/4 Termination Voltage Input Differential Inputs, DATA3, NDATA3, RCV3, NRCV3, DATA4, NDATA4, RCV4, and NRCV4. See the *Functional Diagram*.
2	DATA4	Channel 4 Multiplexer Control Inputs. Differential controls DATA4 and NDATA4 select driver 4's input from DHV4 or DLV4. Drive DATA4 above NDATA4 to select DHV4. Drive NDATA4 above DATA4 to select DLV4. See Table 1.
3	NDATA4	
4	RCV4	Channel 4 Multiplexer Control Inputs. Differential controls RCV4 and NRCV4 place channel 4 into receive mode. Drive RCV4 above NRCV4 to place channel 4 into receive mode. Drive NRCV4 above RCV4 to place channel 4 into drive mode. See Table 1.
5	NRCV4	
6	DATA3	Channel 3 Multiplexer Control Inputs. Differential controls DATA3 and NDATA3 select driver 3's input from DHV3 or DLV3. Drive DATA3 above NDATA3 to select DHV3. Drive NDATA3 above DATA3 to select DLV3. See Table 1.
7	NDATA3	
8	RCV3	Channel 3 Multiplexer Control Inputs. Differential controls RCV3 and NRCV3 place channel 3 into receive mode. Drive RCV3 above NRCV3 to place channel 3 into receive mode. Drive NRCV3 above RCV3 to place channel 3 into drive mode. See Table 1.
9	NRCV3	
10, 27, 54, 55, 60, 61, 65, 66, 71, 72, 99	V_{EE}	Negative Power-Supply Input
11, 28, 51, 56, 62, 64, 70, 75, 98	GND	Ground Connection
12	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low. See Figure 3.
13	$\overline{CS}$	Chip-Select Input. Serial-port activation input. $\overline{CS}$ is active low.
14	SCLK	Serial-Clock Input. Clock for serial port.
15	DIN	Data Input. Serial-port data input.
16, 26, 52, 58, 68, 74, 100	V_{CC}	Positive Power-Supply Input
17	NRCV2	Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 into receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode. See Table 1.
18	RCV2	
19	NDATA2	Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2. See Table 1.
20	DATA2	
21	NRCV1	Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 into receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode. See Table 1.
22	RCV1	
23	NDATA1	Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1. See Table 1.
24	DATA1	
25	V_T12	Channel 1/2 Termination Voltage Input Differential Inputs, DATA1, NDATA1, RCV1, NRCV1, DATA2, NDATA2, RCV2, and NRCV2. See the *Functional Diagram*.
29–38, 43, 44, 45, 49, 50, 57, 69, 76, 77, 81, 82, 83, 88–97	N.C.	No Connection. Leave unconnected.

Pin Description (continued)

PIN	NAME	FUNCTION
39	DHV2	Channel 2 Driver High Voltage Input
40	DLV2	Channel 2 Driver Low Voltage Input
41	DTV2	Channel 2 Driver Termination Voltage Input
42	GS	Ground-Sense Voltage Input for All Channels
46	DHV1	Channel 1 Driver High Voltage Input
47	DLV1	Channel 1 Driver Low Voltage Input
48	DTV1	Channel 1 Driver Termination Voltage Input
53	DUT1	Channel 1 Device-Under-Test Input/Output
59	DUT2	Channel 2 Device-Under-Test Input/Output
63	TEMP	Temperature Monitor Output, One per Device
67	DUT3	Channel 3 Device-Under-Test Input/Output
73	DUT4	Channel 4 Device-Under-Test Input/Output
78	DTV4	Channel 4 Driver Termination Voltage Input
79	DLV4	Channel 4 Driver Low Voltage Input
80	DHV4	Channel 4 Driver High Voltage Input
84	THR	Single-Ended Logic Threshold Reference for All Channels
85	DTV3	Channel 3 Driver Termination Voltage Input
86	DLV3	Channel 3 Driver Low Voltage Input
87	DHV3	Channel 3 Driver High Voltage Input

Detailed Description

The MAX9977 low-power, high-speed, pin-electronics IC includes four three-level pin drivers. The drivers feature a -1.5V to +6.5V operating range and high-speed operation, include high-impedance and active-termination (3rd-level drive) modes, and are highly linear even at low voltage swings.

Optional internal resistors at the high-speed inputs provide compatibility with CML interfaces and reduce the discrete component count on the circuit board. Connect the termination voltage inputs, V_T12 and V_T34, to a voltage appropriate for the drive circuits to terminate the multiplexer control inputs (see the *Functional Diagram*).

A 3-wire, low-voltage CMOS-compatible serial interface programs the low-leakage and tri-state/terminate operational configurations of the MAX9977.

Compatibility with the MAX9963 and MAX9965

To upgrade from the MAX9963 or MAX9965 to the MAX9977 take these steps:

1) GS on the MAX9977 is in the position of CHV2 on the MAX9963/MAX9965. Program CHV2 to zero volts.
2) THR on the MAX9977 is in the position of CHV3 on the MAX9963/MAX9965. If CHV3 is being controlled by a DAC that is referenced to ground sense, reassign this input to a reference that is not affected by changes in ground sense.
3) MAX9977AK DRV_ and RCV_ inputs have center taps V_T12 and V_T34 for the internal termination resistors in the positions of V_{CCO12} and V_{CCO34} of the MAX9963/MAX9965, the comparator-output resistor termination points. Bias these termination points accordingly.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_ and mode-control bit TMSEL (Table 1).

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). High-speed input RCV_ and mode-control bits TMSEL and LLEAK control the switching. In high-impedance mode, the bias current at DUT_ is less than 3µA over the -1.5V to +6.5V range, while the node maintains its ability to track

Quad, Low-Power, 1200Mbps ATE Driver

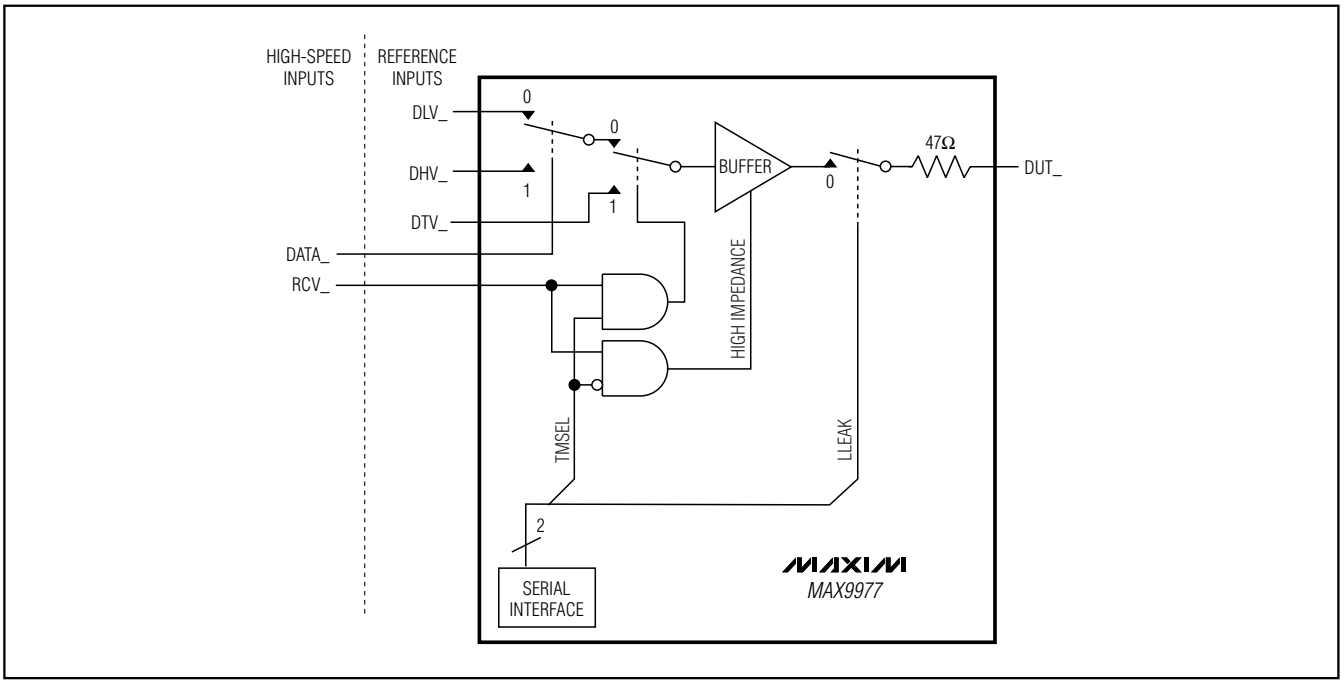


Figure 2. Simplified Driver Channel

Table 1. Driver Logic

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA	RCV	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-Z)
X	X	X	1	Low-leakage mode

high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 50nA, and signal tracking slows. See the *Low-Leakage Mode, LLEAK* section for more details.

The nominal driver output resistance is 47Ω. Contact the factory for custom resistance values within the 45Ω to 51Ω range.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9977 modes (Figure 3 and Table 2). Control data flow into an 8-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high, as shown in Figure 4. Latches contain 2 control bits for each channel of the MAX9977. Data from the shift register are then loaded to any or all of a group of four quad latches as determined by bits D4 and D7. The control bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel. $\overline{RST}$ sets LLEAK = 1 for all channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

Analog control input THR sets the threshold for the input logic, allowing operation with CMOS logic as low as 0.9V. Leaving THR unconnected results in a nominal threshold of 1.25V from an internal reference, providing compatibility with 2.5V to 3.3V logic.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with $\overline{RST}$ places the MAX9977 into a low-leakage state (see the *Electrical Characteristics* table). This mode is convenient

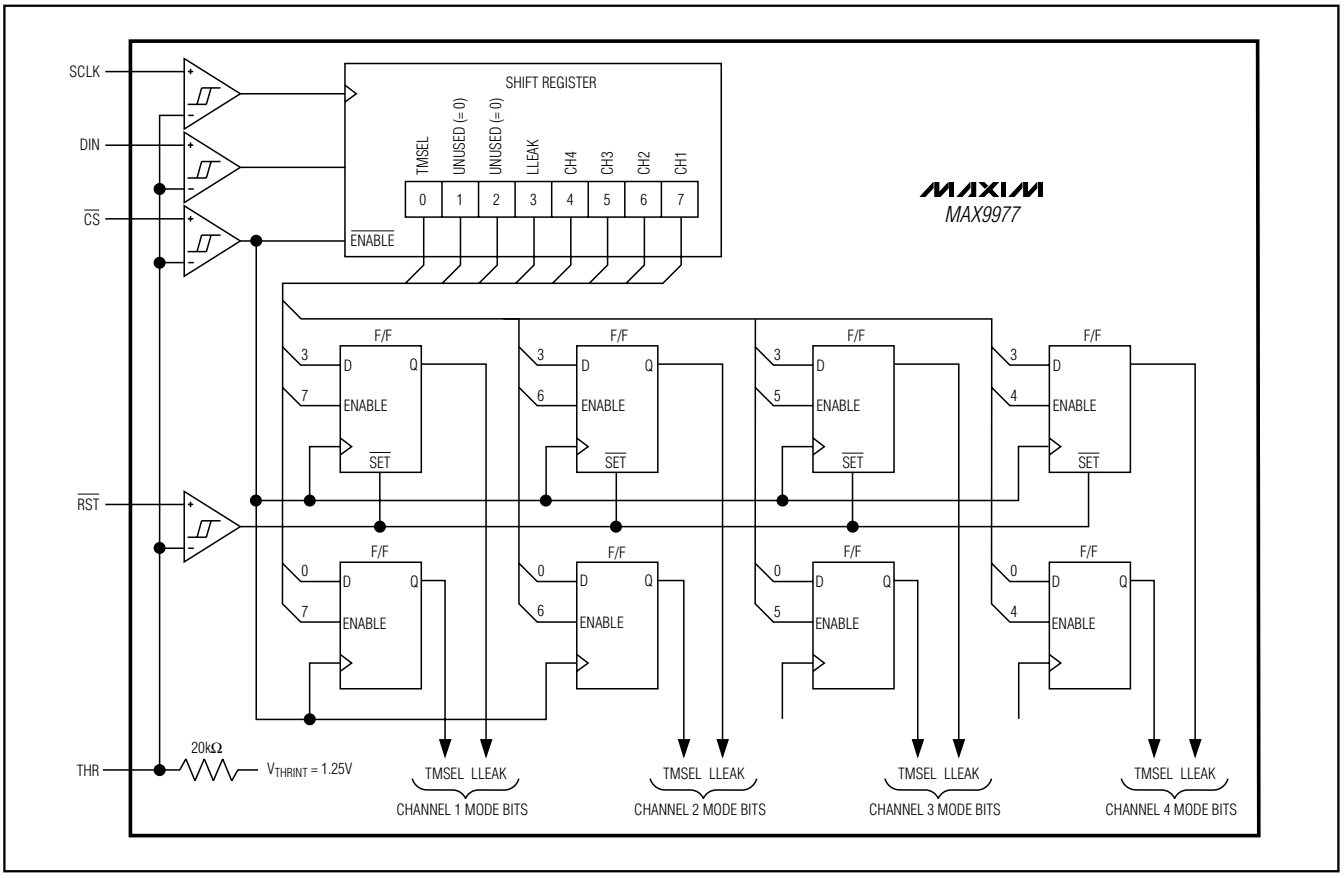


Figure 3. Serial Interface

Table 2. Serial Interface Bit Description

BIT	NAME	DESCRIPTION	BIT STATE AFTER RESET AND AT POWER-UP
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.	0
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.	0
D5	CH3	Channel 3 Write Enable. Set to 1 to update the control byte for channel 3. Set to 0 to make no changes to channel 3.	0
D4	CH4	Channel 4 Write Enable. Set to 1 to update the control byte for channel 4. Set to 0 to make no changes to channel 4.	0
D3	LLEAK	Low-Leakage Select. Set to 1 to put driver in low-leakage mode. Set to 0 for normal operation.	1
D2	UNUSED	These bits are not used. Their logic state has no effect.	X
D1	UNUSED		X
D0	TMSEL	Termination Select. Driver termination select bit.	0

Quad, Low-Power, 1200Mbps ATE Driver

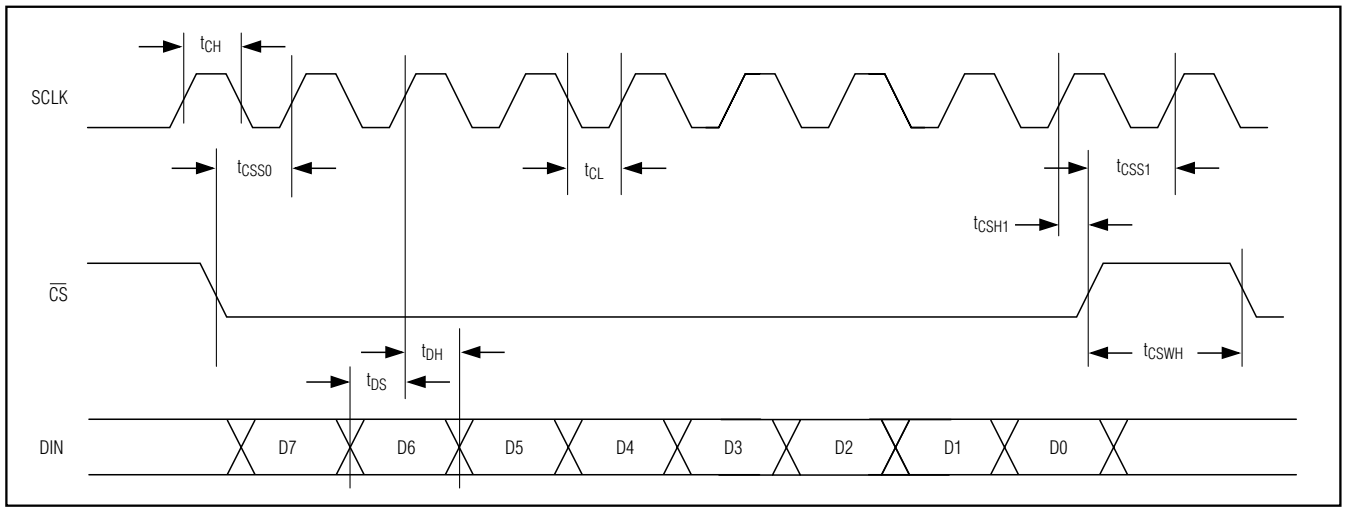


Figure 4. Serial-Interface Timing

for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

GS Input

The ground-sense input, GS, provides a ground reference for the mux inputs. Connect GS to the ground of the DAC circuits driving DHV_, DTV_, and DLV_.

To maintain an 8V range in the presence of GS variations, GS offsets DHV_, DLV_, and DTV_ ranges. Adequate supply headroom must be maintained in the presence of GS variations. Ensure:

$$V_{CC} \geq 9.5V + Max\ (V_{GS})$$

$$V_{EE} \leq -4.5V + Min\ (V_{GS})$$

Temperature Monitor

The MAX9977 supplies a temperature output signal, TEMP, that asserts a 3.33V nominal output voltage at a +70°C (343K) die temperature. The output voltage changes proportionally with temperature at 10mV/°C.

Heat Removal

Under normal circumstances, the MAX9977 requires heat removal through the exposed pad by use of an external heat sink. The exposed pad is electrically at V_{EE} potential, and must be either connected to V_{EE} or isolated.

θ_{JC} of the exposed-pad package is approximately 1°C/W to 2°C/W. Die temperature is thus highly dependent upon the heat removal techniques used in the application. Maximum total power dissipation occurs under the following conditions:

- V_{CC} = +10.5V
- V_{EE} = -5.25V
- $V_{DHV\_}$ = 6.5V, DATA = HIGH
- Short-circuit current = 60mA

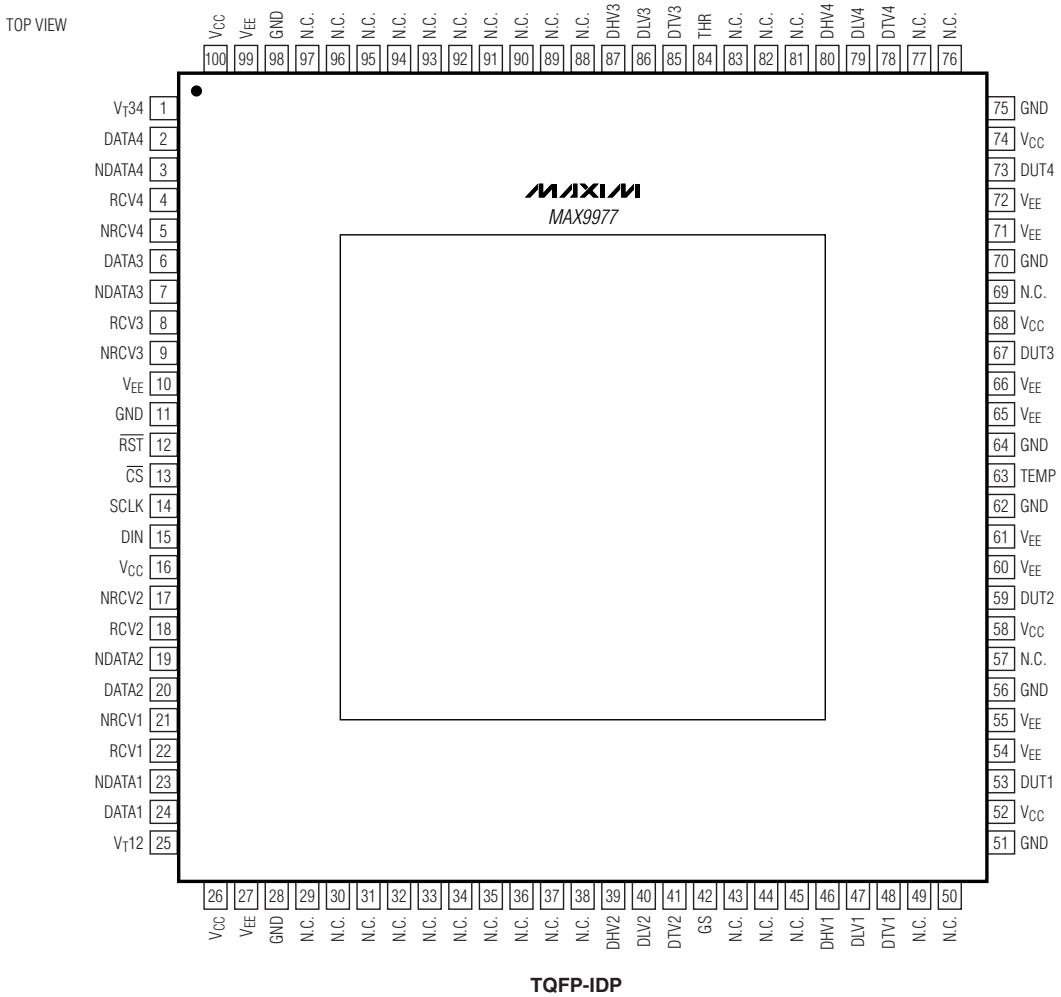
Under these extreme conditions, the total power dissipation is 5.8W. If the die temperature cannot be maintained at an acceptable level under these conditions, use software clamping to limit the load output currents to lower values and/or reduce the supply voltages.

Power-Supply Considerations

Bypass all V_{CC} and V_{EE} power input pins with 0.01µF capacitors, and use bulk bypassing of at least 10µF on each supply.

Quad, Low-Power, 1200Mbps ATE Driver

Pin Configuration



TQFP-IDP

Selector Guide

PART	INTERNAL DATA_ AND RCV_ TERMINATIONS	HEAT EXTRACTION
MAX9977AKCCQ	100Ω with center tap	Top
MAX9977ADCCQ*	None	Top

**Future product—contact factory for availability.*

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

MAX9977

Part Number Table

Notes:

1. See the MAX9977 QuickView Data Sheet for further information on this product family or download the MAX9977 full data sheet (PDF, 1.1MB).
2. Other options and links for purchasing parts are listed at: http://www.maxim-ic.com/sales.
3. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See full data sheet or Part Naming Conventions.
5. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX9977AKCCQ+TD				0C to +70C	RoHS/Lead-Free: Yes
MAX9977AKCCQ-TD				0C to +70C	RoHS/Lead-Free: No
MAX9977AKCCQ+D			TQFP;100 pin;14x14x1.0mm Dwg: 21-0148A (PDF) Use pkgcode/variation: C100E+8R*	0C to +70C	RoHS/Lead-Free: Yes Materials Analysis
MAX9977AKCCQ-D			TQFP;100 pin;14x14x1mm Dwg: 21-0148A (PDF) Use pkgcode/variation: C100E-8R*	0C to +70C	RoHS/Lead-Free: No Materials Analysis

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