PRELIMINARY

KM69B257

BiCMOS SRAM

T-46-23-14

32KX9 Bit BiCMOS Static RAM

FEATURES

- Ultra-Fast Access Times
  - —Commercial: 10ns, 12ns, 15ns, 20ns
  - —5ns & 6ns Output Enable times
- Low Power Dissipation
  - —Standby: 20mA
  - —Operating: 195mA, 175mA, 155mA, 130mA
- Single 5V±10% Power Supply
- Fully Static Operation
  - —No clock or refresh required
- Two Chip Select Input
  - —Memory expansion
- TTL-Level Three-State Output
- Standard Packaging
  - —32-pin 300 mil Plastic SOJ
  - —32-pin 300 mil Plastic DIP

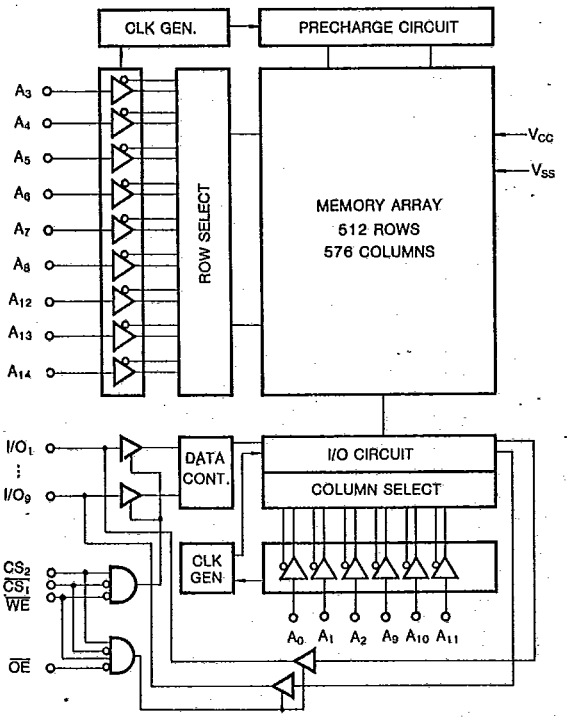
GENERAL DESCRIPTION

The KM69B257 is a 294,912 bit ultra high speed TTL-Level Static Random Access Memory organized as 32,768 words by 9 bits. The device is manufactured using Samsung's advanced BiCMOS process.

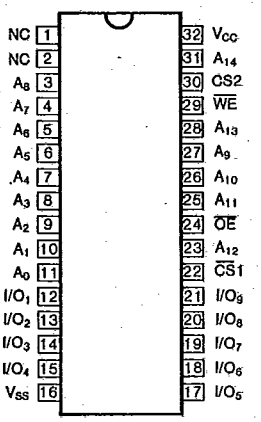
The KM69B257 has an Output Enable input for precise control of the data outputs. It also has tw chip select inputs for design flexibility.

The KM69B257 has been designed for high speed applications. It is particulary well suited for applications requiring high speed, local instruction cache large byte wide cache, or very fast data buffering in personal computers workstations, and communications. The parity (9th) bit makes the KM69B257 ideal for OLTP systems, and i486 based system.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$, CS_2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_9	Data Inputs/Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

* NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $T_A=0°C$ to $+70°C$)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Unput Leakage Current	$\|I_{LI}\|$	V_{CC}=Max, $V_{IN}=V_{SS}$ to V_{CC}				2	μA
Output Leakge Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}, $\overline{WE}=V_{IL}$ $V_{I/O}=V_{SS}$ to V_{CC}, V_{CC}=max.				10	μA
Operating Current	I_{CC1}	f_{MAX}=0, $I_{I/O}$=0mA, $\overline{CS1}=V_{IL}$, CS2=V_{IH}				85	mA
	I_{CC2}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, I_O=0mA, Min Cycle=100% Duty	−10			195	mA
			−12			175	
			−15			155	
			−20			130	
Standy Current	I_{SB}	$\overline{CS1}=V_{IH}$, or CS2=V_{IL}, $V_{IN}=V_{IL}$ or V_{IH}				20	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}-0.2V$, CS2≤0.2V $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$				8	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4			V
Input High Voltage	V_{IH}			2.2		V_{CC}+0.5	V
Input Low Voltage	V_{IL}	Min=−3.0V for <20ns pulse*		−0.5		0.8	V

* Note: This V_{IL} description is not a test condition. It is an Absolute Maximum Rating. V_{IL} condition greater than those described may cause improper functional operation of the device.

CAPACITANCE* ($0°C \leq T_A \leq 70°C$)

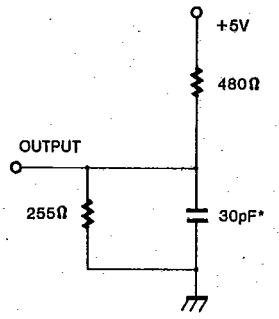
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

* Note: Sampled, not 100% tested.

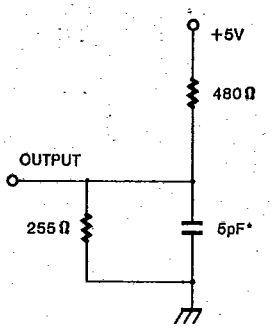
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{OHZ}, t_{LZ}, t_{OLZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE (V_{CC}=5V±10%, T_A=0°C to +70°C)

Parameter	Symbol	KM69B257-10		KM69B257-12		KM69B257-15		KM69B257-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10		12		15		20		ns
Address Access Time	t_{AA}		10		12		15		20	ns
Chip Select to Output	t_{ACS}		10		12		15		20	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Valid Output	t_{OE}		5		6		6		6	ns
Output Enable to Low-Z Output	t_{OLZ}	1		1		1		2		ns
Chip Disable to High-Z Output	t_{HZ}		4		5		6		8	ns
Output Disable to High-Z Output	t_{OHZ}		4		5		6		8	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns

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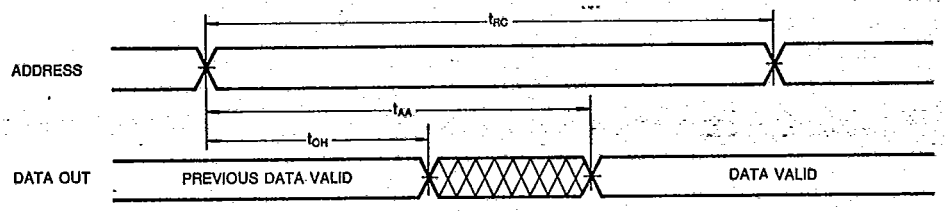
TIMING WAVEFORM OF READ CYCLE NO. 1 (Note 1, 2, 6)



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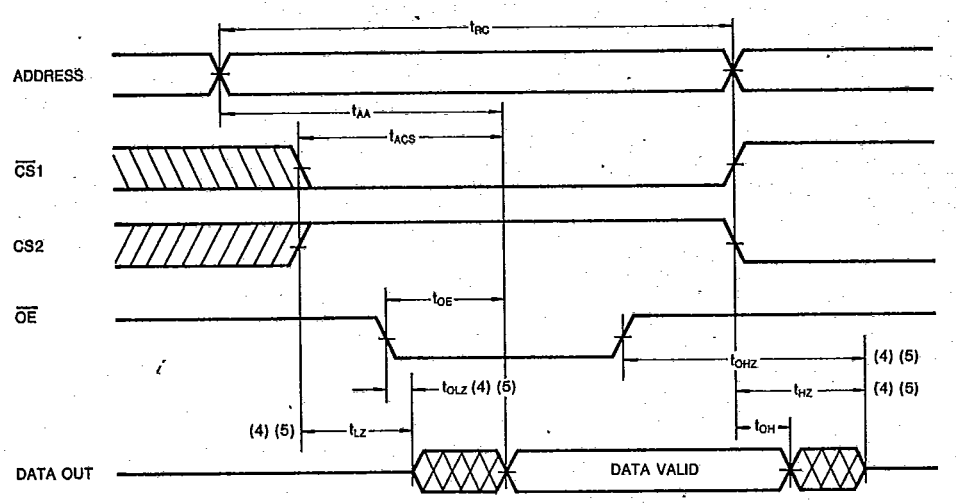
TIMING WAVEFORM OF READ CYCLE NO. 2 (Note 1, 3)



Notes (Read Cycle):

1. $\overline{WE}$ is high for ready cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(maximum) is less than t_{LZ} (minimum) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS1}=V_{IL}$, $CS2=V_{IH}$.

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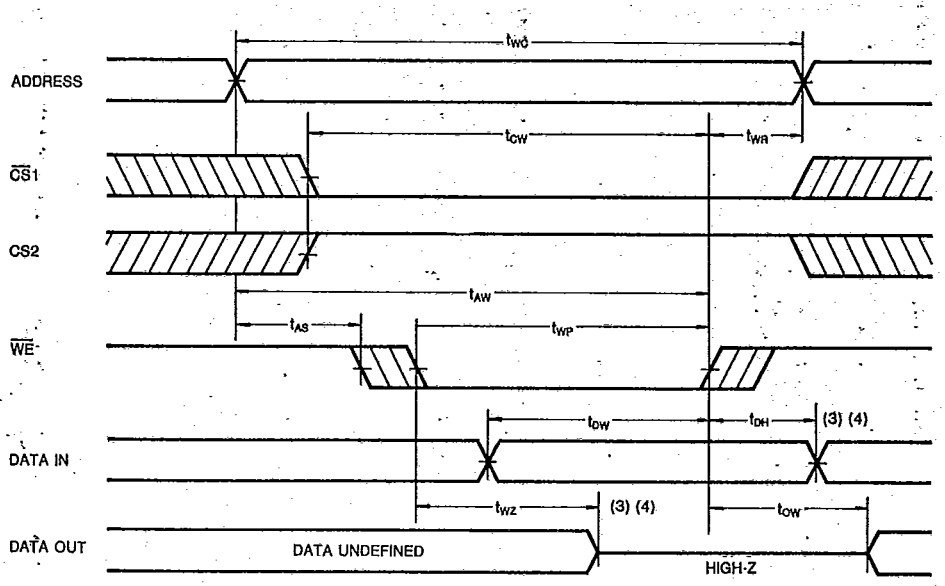
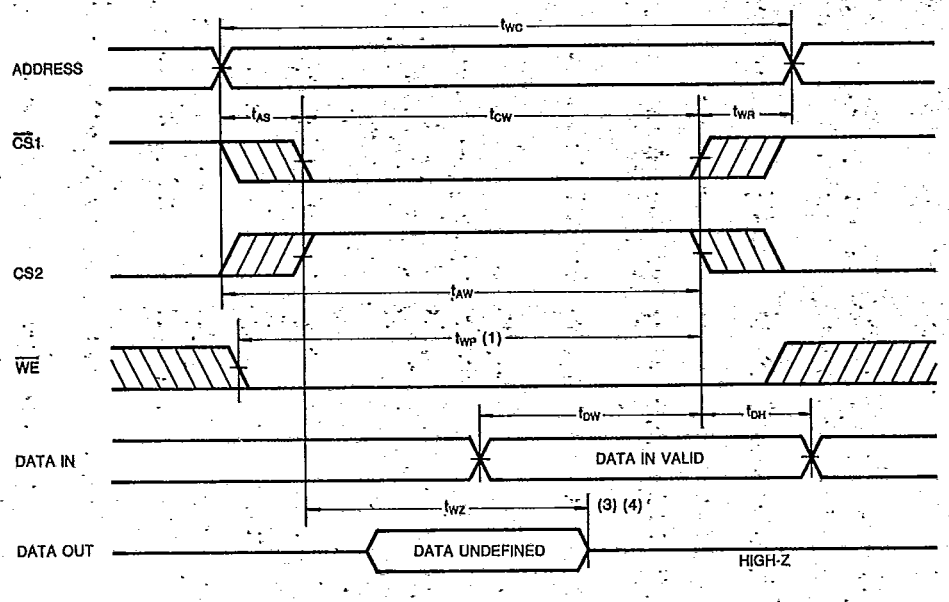
WRITE CYCLE (V_{CC}=5V±10%, T_A=0°C to +70°C)

Parameter	Symbol	KM69B257-10		KM69B257-12		KM69B257-15		KM69B257-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10		12		15		20		ns
Chip Select to End of Write	t_{CW}	6		8		10		13		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	6		8		10		13		ns
Write Pulse Width	t_{WP}	6		8		10		13		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}		4		6		6		8	ns
Data to Write Time Overlap	t_{DW}	6		6		8		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	3		3		3		3		ns

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled) (Notes 1, 2, 5, 6)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS1}$, CS2 Controlled) (Notes 1, 2, 5, 6)



Notes: (Write Cycle)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(maximum) is less that t_{OW}(minimum) both for a given device and from device to device.
6. $\overline{CS1}$ or $\overline{WE}$ must be high or CS2 must be low during address transition.

FUNCTIONAL DESCRIPTION

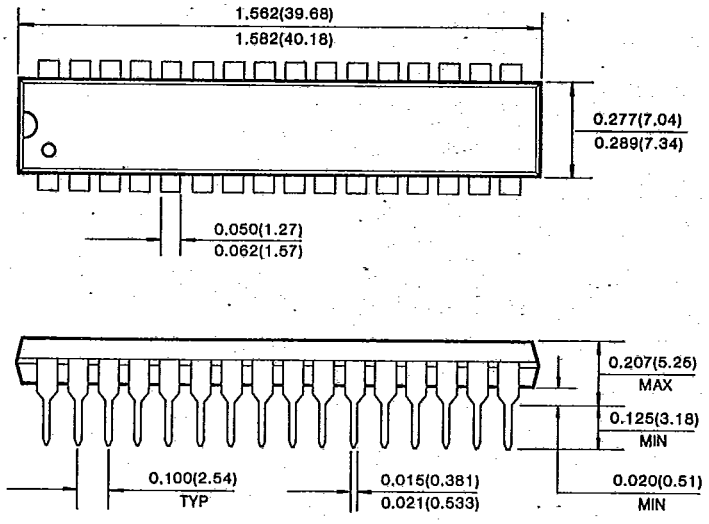
$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current	Mode
H	X	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
X	L	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
L	H	H	H	High-Z	I_{CC}	Output Disable
L	H	H	L	D_{OUT}	I_{CC}	Read
L	H	L	X	D_{IN}	I_{CC}	Write

* Note: X means Don't Care

PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



32 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE