



SANYO Semiconductors

## DATA SHEET

# STK415-140-E

Thick-Film Hybrid IC  
— 2-Channel Power Switching  
Audio Power IC, 120W+120W

## Overview

The STK415-140-E is a class H audio power amplifier hybrid IC that features a built-in power supply switching circuit. This IC provides high efficiency audio power amplification by controlling (switching) the supply voltage supplied to the power devices according to the detected level of the input audio signal.

## Applications

- Audio power amplifiers.

## Features

- Pin-to-pin compatible outputs ranging from 80W to 180W.
- Can be used to replace the STK416-100 series (3-channel models) and the class-AB series (2, 3-channel models) due to its pin compatibility.
- Pure complementary construction by new Darlington power transistors
- Output load impedance:  $R_L = 8\Omega$  to  $4\Omega$  supported
- Using insulated metal substrate that features superlative heat dissipation characteristics that are among the highest in the industry.

## Series Models

	STK415-090-E	STK415-100-E	STK415-120-E	STK415-130-E	STK415-140-E
Output 1 (10%/1kHz)	80W×2ch	90W×2ch	120W×2ch	150W×2ch	180W×2ch
Output 2 (0.8%/20Hz to 20kHz)	50W×2ch	60W×2ch	80W×2ch	100W×2ch	120W×2ch
Max. rated $V_H$ (quiescent)	±60V	±65V	±73V	±80V	±80V
Max. rated $V_L$ (quiescent)	±41V	±42V	±45V	±46V	±51V
Recommended operating $V_H$ ( $8\Omega$ )	±37V	±39V	±46V	±51V	±52V
Recommended operating $V_L$ ( $8\Omega$ )	±27V	±29V	±32V	±34V	±32V
Dimensions (excluding pin height)	64.0mm×31.1mm×9.0mm				

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## STK415-140-E

### Specifications

**Absolute maximum ratings** at  $T_a=25^\circ\text{C}$  (excluding rated temperature items),  $T_c=25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Conditions	Ratings	Unit
$V_H$ maximum quiescent supply voltage 1	$V_H$ max (1)	When no signal	$\pm 80$	V
$V_H$ maximum supply voltage 2	$V_H$ max (2)	$R_L \geq 6\Omega$	$\pm 78$	V
$V_H$ maximum supply voltage 3	$V_H$ max (3)	$R_L \geq 4\Omega$	$\pm 60$	V
$V_L$ maximum quiescent supply voltage 1	$V_L$ max (1)	When no signal	$\pm 51$	V
$V_L$ maximum supply voltage 2	$V_L$ max (2)	$R_L \geq 6\Omega$	$\pm 48$	V
$V_L$ maximum supply voltage 3	$V_L$ max (3)	$R_L \geq 4\Omega$	$\pm 36$	V
Maximum voltage between $V_H$ and $V_L$ *4	$V_H-V_L$ max	No loading	60	V
Standby pin maximum voltage	$V_{st}$ max		-0.3 to +5.5	V
Thermal resistance	$\theta_{j-c}$	Per power transistor	1.5	$^\circ\text{C/W}$
Junction temperature	$T_j$ max	Both the $T_j$ max and $T_c$ max conditions must be met.	150	$^\circ\text{C}$
IC substrate operating temperature	$T_c$ max		125	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-30 to +125	$^\circ\text{C}$
Allowable load shorted time *3	$t_s$	$V_H=\pm 52\text{V}$ , $V_L=\pm 32\text{V}$ , $R_L=6\Omega$ , $f=50\text{Hz}$ , $P_O=120\text{W}$ , 1-channel active	0.3	s

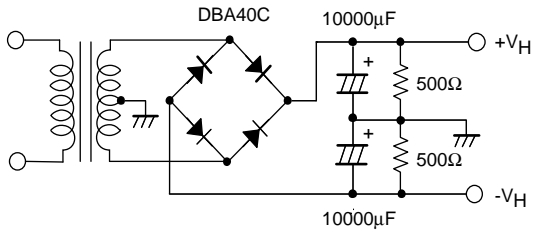
**Electrical Characteristics** at  $T_c=25^\circ\text{C}$ ,  $R_L=8\Omega$  (non-inductive load),  $R_g=600\Omega$ ,  $V_G=40\text{dB}$ ,  $V_Z=15\text{V}$

Parameter	Symbol	Conditions *1						Ratings			unit
		V (V)		f (Hz)	$P_O$ (W)	THD (%)		min	typ	max	
Output power	$P_O$ (1)	$V_H$ $V_L$	$\pm 52$ $\pm 32$	20 to 20k		0.8		120			W
	$P_O$ (2)	$V_H$ $V_L$	$\pm 42$ $\pm 28$	1k		0.8	$R_L=4\Omega$		120		
Total harmonic distortion	THD	$V_H$ $V_L$	$\pm 52$ $\pm 32$	20 to 20k	120				0.4		%
Frequency characteristics	$f_L, f_H$	$V_H$ $V_L$	$\pm 52$ $\pm 32$		1.0		+0 -3dB	20 to 50k			Hz
Input impedance	$r_i$	$V_H$ $V_L$	$\pm 52$ $\pm 32$	1k	1.0				55		$\text{k}\Omega$
Output noise voltage *2	$V_{NO}$	$V_H$ $V_L$	$\pm 58$ $\pm 38$				$R_g=2.2\text{k}\Omega$			1.0	mVrms
Quiescent current	$I_{CCO}$	$V_H$	$\pm 58$				$R_L=\infty$			30	mA
		$V_L$	$\pm 38$						100		
Output neutral voltage	$V_N$	$V_H$ $V_L$	$\pm 58$ $\pm 38$					-70	0	+70	mV
Pin 17 voltage when standby ON *7	VST ON	$V_H$ $V_L$	$\pm 52$ $\pm 32$				Standby		0	0.6	V
Pin 17 voltage when standby OFF *7	VST OFF	$V_H$ $V_L$	$\pm 52$ $\pm 32$				Operating	2.5	3.0		V

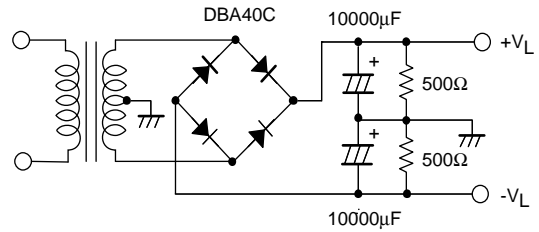
[Remarks]

- \*1: Unless otherwise specified, use a constant-voltage power supply to supply power when inspections are carried out.
- \*2: The output noise voltage values shown are peak values read with a VTVM. However, an AC stabilized (50Hz) power supply should be used to minimize the influence of AC primary side flicker noise on the reading.
- \*3: Use the designated transformer power supply circuit shown in the figure below for the measurements of allowable load shorted time and output noise voltage.
- \*4: Design circuits so that  $(|V_H|-|V_L|)$  is always less than 40V when switching the power supply with the load connected.
- \*5: Set up the  $V_L$  power supply with an offset voltage at power supply switching ( $V_L-V_O$ ) of about 8V as an initial target.
- \*6: Please connect -Pre  $V_{CC}$  pin (#5 pin) with the stable minimum voltage and connect so that current does not flow in by reverse bias.
- \*7: Use the standby pin (pin 17) so that the applied voltage never exceeds the maximum rating.  
The power amplifier is turned on by applying +2.5V to +5.5V to the standby pin (pin 17).
- \*8: Thermal design must be implemented based on the conditions under which the customer's end products are expected to operate on the market.
- \*9: A thermoplastic adhesive resin is used for this hybrid IC.

**STK415-140-E**



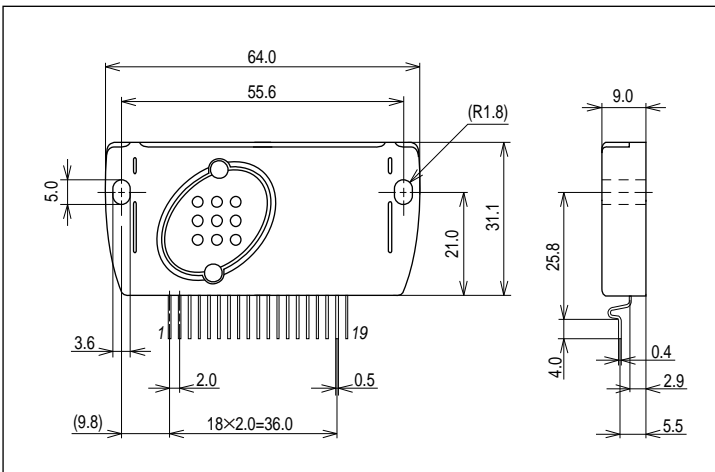
Designated transformer power supply  
(MG-250 equivalent)



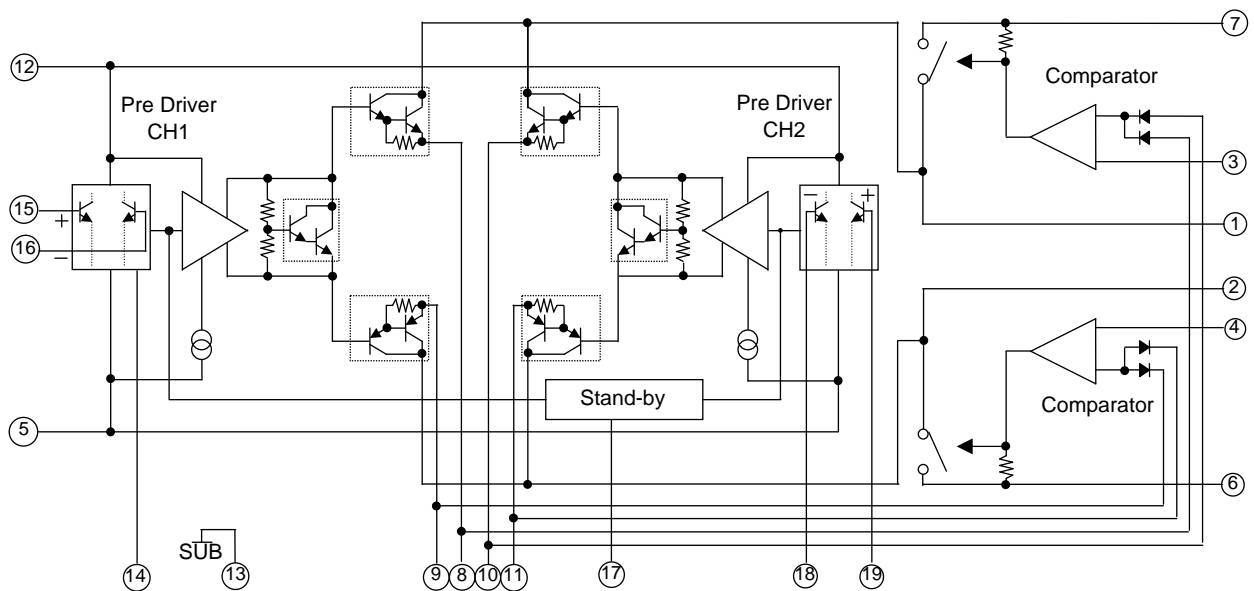
Designated transformer power supply  
(MG-200 equivalent)

**Package Dimensions**

unit:mm (typ)

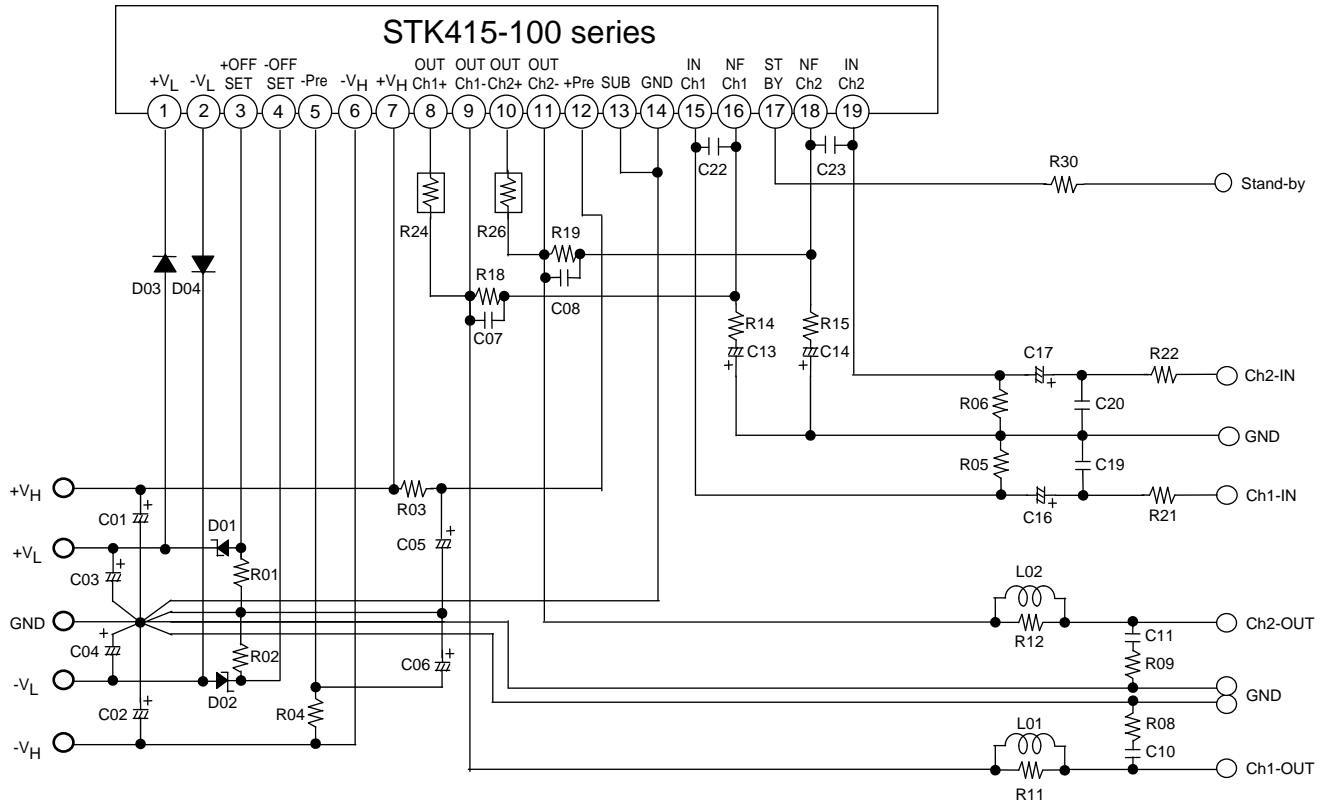


**Internal Equivalent Circuit**



**STK415-140-E**

**Application Circuit Example**



## STK415-140-E

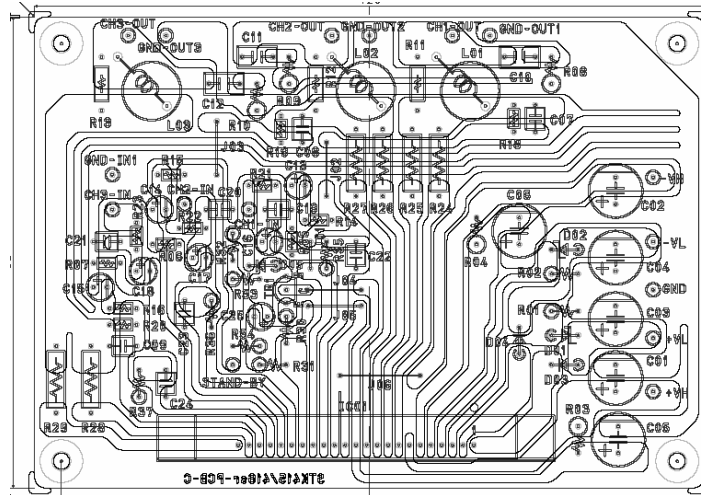
### Recommended Values for Application Parts (for the test circuit)

Symbol	Recommended Value	Description	Larger than Recommended Value	Smaller than Recommended Value
R01, R02	1.5kΩ	Determine the current flowing into the power switching circuit (comparator), (3mA to 10mA at $V_H$ power switching)	Power holding circuit remains active at lower frequencies.	Power switching circuit activates at higher frequencies.
R03, R04	100Ω/1W	Ripple filtering resistors (Used with C05 and C06 to form a ripple filter.)	Decreased pass-through current at high frequencies.	Increased pass-through current at high frequencies.
R05, R06	56kΩ	Input bias resistors (Virtually determine the input impedance.)	VN offset (Ensure R05=R18, R06=R19 when changing.)	
R08, R09	4.7Ω/1W	Oscillation prevention resistor	-	-
R11, R12	4.7Ω	Oscillation prevention resistor	-	-
R14, R15	560Ω	Used with R18 and R19 to determine the voltage gain VG. (VG should desirably be determined by the R14 and R15 value.)	Likely to oscillate (VG<40dB)	None
R18, R19	56kΩ	Used with R14 and R15 to determine the voltage gain VG.	-	-
R21, R22	1kΩ	Input filtering resistor	-	-
R24, R26	0.22Ω±10%, 5W	Output emitter resistors (Use of cement resistor is desirable)	Decrease in maximum output power	Likely to cause thermal-runaway.
R30	Remarks *7	Use a limiting resistor according to the voltage applied to the standby pin so that it remains within the rating.		
C01, C02	100μF/ 100V	Oscillation prevention capacitors. • Insert the capacitors as close to the IC as possible to decrease the power impedance for reliable IC operation (use of electrolytic capacitors are desirable).	-	-
C03, C04	100μF/ 50V	Oscillation prevention capacitors. • Insert the capacitors as close to the IC as possible to decrease the power impedance for reliable IC operation (use of electrolytic capacitors are desirable).	-	-
C05, C06	100μF/ 100V	Decoupling capacitors. Eliminate ripple components that pass into the input side from the power line. (Used with R03 and R04 to form a ripple filter.)	Increase in ripple components that pass into the input side from the power line.	
C07, C08	3pF	Oscillation prevention capacitor	Likely to oscillate	
C10, C11	0.1μF	Oscillation prevention capacitor (Mylar capacitors are recommended.)	Likely to oscillate	
C13, C14	22μF/ 10V	NF capacitor (Changes the low cutoff frequency; $ex/f_L=1/2\pi \bullet C13 \bullet R14$ )	Increase in low-frequency voltage gain, with higher pop noise at power-on.	Decrease in low-frequency voltage gain
C16, C17	2.2μF/ 50V	Input coupling capacitor (block DC current)	-	-
C19, C20	470pF	Input filter capacitor (Used with R21 and R22 to form a filter that suppresses high-frequency noises.)	-	-
C22, C23	100pF	Oscillation prevention capacitor	Likely to oscillate.	
D01, D02	18V	Determine the offset voltage at $V_L \leftrightarrow V_H$ power.	Decreased distortion at power switching time	Increased distortion at power switching time.
D03, D04	3A/60V	Reverse current prevention diodes (FRD is recommended.)	-	-
L01, L02	3μH	Oscillation prevention inductance	None	Likely to oscillate.

**STK415-140-E**

**Sample PCB Trace Pattern**

STK415-100-E-Sr/STK416-100-E-Sr PCB PARTS LIST



**Parts List**

STK415, 416-100Sr PCB Parts List

PCB No.	PARTS	RATING	STK415 (416) -090-E, -100-E, -120-E, 130-E	STK415-140-E
R01, R02	-	ERX1SJ***	1.5kΩ, 1W	1.5kΩ, 1W
R03, R04	100Ω, 1W	ERG1SJ101	enabled	enabled
R05, R06, (R07), R18, R19, (R20)	56kΩ, 1/6W	RN16S563FK	enabled	enabled
R08, R09, (R10)	4.7Ω, 1W	ERX1SJ4R7	enabled	enabled
R11, R12, (R13)	4.7Ω, 1/4W	RN14S4R7FK	enabled	enabled
R14, R15, (R16)	-	RN16S***FK	560Ω, 1/6W	560Ω, 1/6W
R21, R22, (R23)	1kΩ, 1/6W	RN16S102FK	enabled	enabled
R25, R27, (R29)	0.22Ω±10%, 5W	BPR56CFR22J	Short	Short
R24, R26, (R28)	0.22Ω±10%, 5W	BPR56CFR22J	enabled	enabled
R35, R36, R37	-	-	Short	Short
C01, C02, C05, C06	100μF, 100V	100MV100HC	enabled	enabled
C03, C04	100μF, 50V	50MV100HC	enabled	enabled
C07, C08, (C09)	3pF	DD104-63B3R0K50	enabled	enabled
C10, C11, (C12)	0.1μF, 100V	ECQ-V1H104JZ	enabled	enabled
C13, C14, (C15)	22μF, 10V	10MV220HC	enabled	enabled
C16, C17, (C18)	2.2μF, 50V	50MV2R2HC	enabled	enabled
C19, C20, (C21)	470pF	DD104-63B471K50	enabled	enabled
C22, C23, (C24)	100pF	DD104-63B101K50	enabled	enabled
D01, D02	-	-	GZA15X (SANYO)	GZA18X (SANYO)
D03, D04	IF (AV)=3A/60V		enabled	enabled
L01, L02, (L03)	3μH		enabled	enabled
Stand-By	R30	3.3kΩ, 1/6W	RN16S332FK	enabled
	R32	1kΩ, 1/6W	RN16S102FK	enabled
	R33	33kΩ, 1/6W	RN16S333FK	enabled
	R34	2kΩ, 1/6W	RN16S202FK	enabled
	C25	47μF, 10V	10MV47HC	enabled
	D05	-	GMB01 (Ref.)	enabled
	TR1	-	2SC2274 (Ref.)	enabled
J01	Jumper	20mm	enabled	enabled
J02, J03, J06	Jumper	10mm	enabled	enabled
J04, J05	Jumper	7mm	enabled	enabled

(\*1) STK416-100Sr (3ch AMP) doesn't mount parts of ( ).

**STK415-140-E**

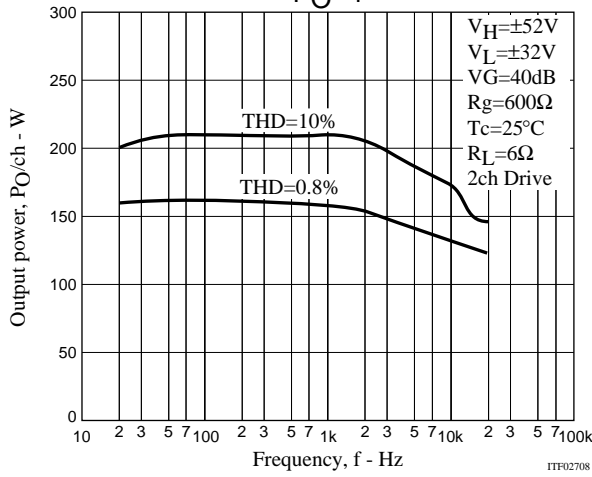
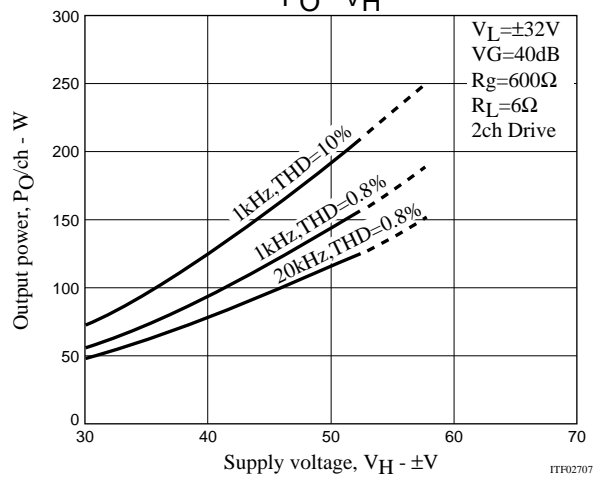
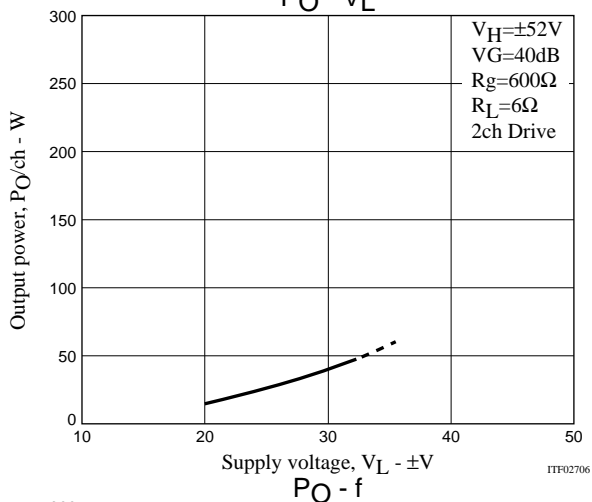
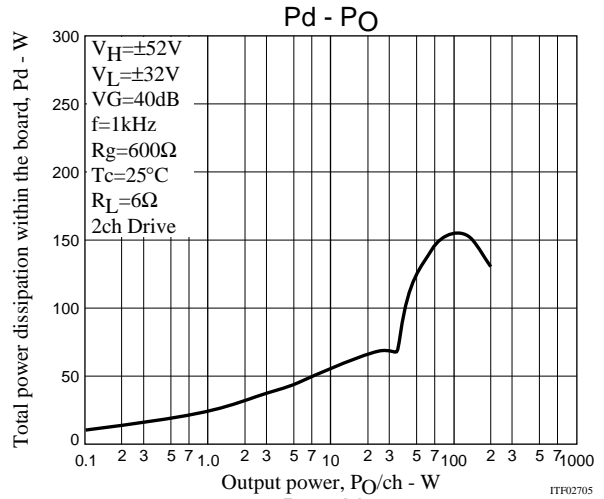
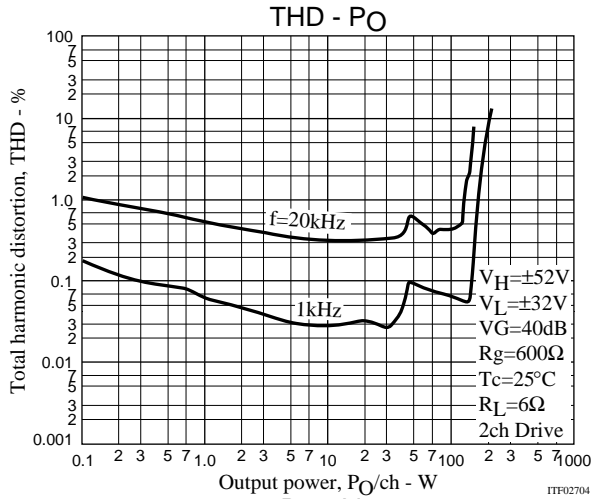
**Pin Assignments**

[STK433-000/-100/-200 Sr & STK415/416-100 Sr Pin Layout]

2ch class-AB		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15									
		2ch classAB/2.00mm																							
STK433-030-E 30W/JEITA		-	-	+	O	O	O	O	+		I	N	S	N	I										
STK433-040-E 40W/JEITA		P	V	V	U	U	U	U	P	S	G	N	F	T	F	N									
STK433-060-E 50W/JEITA		R	C	C	T	T	T	T	R	U	/	/	/	A	/	/									
STK433-070-E 60W/JEITA		E	C	C	/	/	/	/	E	B	D	C	C	N	C	C									
STK433-090-E 80W/JEITA					C	C	C	C	•		H	H	D	H	H										
STK433-100-E 100W/JEITA					H	H	H	H	G		1	1		2	2										
STK433-120-E 120W/JEITA					1	1	2	2	N				B												
STK433-130-E 150W/JEITA					+	-	+	-	D				Y												
3ch class-AB		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19					
		3ch classAB/2.00mm																							
STK433-230A-E 30W/JEITA		-	-	+	O	O	O	O	+		I	N	S	N	I	I	N	O	O						
STK433-240A-E 40W/JEITA		P	V	V	U	U	U	U	P	S	G	N	F	T	F	N	F	U	U						
STK433-260A-E 50W/JEITA		R	C	C	T	T	T	T	R	U	/	/	A	/	/	/	T	T							
STK433-270-E 60W/JEITA		E	C	C	/	/	/	/	E	B	D	C	C	N	C	C	/	/							
STK433-290-E 80W/JEITA					C	C	C	C	•		H	H	D	H	H	H	C	C							
STK433-300-E 100W/JEITA					H	H	H	H	G		1	1		2	2	3	3	H	H						
STK433-320-E 120W/JEITA					1	1	2	2	N				B				3	3							
STK433-330-E 150W/JEITA					+	-	+	-	D				Y				+	-							
2ch class-H		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19					
		2ch classH/2.00mm																							
STK415-090-E 80W/JEITA		+	-	+	-	-	+	O	O	O	O	+		I	N	S	N	I							
STK415-100-E 90W/JEITA		V	V	O	O	P	V	V	U	U	U	U	P	S	G	N	F	T	F	N					
STK415-120-E 120W/JEITA		L	L	F	F	R	H	H	T	T	T	T	R	U	/	/	A	/	/						
STK415-130-E 150W/JEITA				F	F	E			/	/	/	/	E	B	D	C	C	N	C	C					
<b>STK415-140-E 180W/JEITA</b>				S	S			C	C	C	C	•		H	H	D	H	H							
				E	E			H	H	H	H	G		1	1		2	2							
				T	T			1	1	2	2	N				B									
								+	-	+	-	D				Y									
3ch class-H		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
		3ch classH/2.00mm																							
STK416-090-E 80W/JEITA		+	-	+	-	-	+	O	O	O	O	+		I	N	S	N	I	I	N	O	O			
STK416-100-E 90W/JEITA		V	V	O	O	P	V	V	U	U	U	U	P	S	G	N	F	T	F	N	F	U	U		
STK416-120-E 120W/JEITA		L	L	F	F	R	H	H	T	T	T	T	R	U	/	/	A	/	/	/	T	T			
STK416-130-E 150W/JEITA				F	F	E			/	/	/	/	E	B	D	C	C	N	C	C	/	/			
				S	S			C	C	C	C	•		H	H	D	H	H	H	H	C	C			
				E	E			H	H	H	H	G		1	1		2	2	3	3	H	H			
				T	T			1	1	2	2	N				B				3	3	H	H		
								+	-	+	-	D				Y				+	-				

**STK415-140-E**

**Evaluation Board Characteristics**



**STK415-140-E**

[Thermal Design Example for STK415-140-E ( $R_L = 8\Omega$ )]

The thermal resistance,  $\theta_{c-a}$ , of the heat sink for total power dissipation,  $P_d$ , within the hybrid IC is determined as follows.

Condition 1: The hybrid IC substrate temperature,  $T_c$ , must not exceed  $125^\circ\text{C}$ .

$$P_d \times \theta_{c-a} + T_a < 125^\circ\text{C} \dots\dots\dots (1)$$

$T_a$ : Guaranteed ambient temperature for the end product

Condition 2: The junction temperature,  $T_j$ , of each power transistor must not exceed  $150^\circ\text{C}$ .

$$P_d \times \theta_{c-a} + P_d/N \times \theta_{j-c} + T_a < 150^\circ\text{C} \dots\dots\dots (2)$$

$N$ : Number of power transistors

$\theta_{j-c}$ : Thermal resistance per power transistor

However, the power dissipation,  $P_d$ , for the power transistors shall be allocated equally among the number of power transistors.

The following inequalities result from solving equations (1) and (2) for  $\theta_{c-a}$ .

$$\theta_{c-a} < (125 - T_a)/P_d \dots\dots\dots (1)'$$

$$\theta_{c-a} < (150 - T_a)/P_d - \theta_{j-c}/N \dots\dots\dots (2)'$$

Values that satisfy these two inequalities at the same time represent the required heat sink thermal resistance.

When the following specifications have been stipulated, the required heat sink thermal resistance can be determined from formulas (1)' and (2)'.

- Supply voltage  $V_H, V_L$
- Load resistance  $R_L$
- Guaranteed ambient temperature  $T_a$

[Example]

When the IC supply voltage,  $V_H = \pm 52\text{V}$ ,  $V_L = \pm 32\text{V}$  and  $R_L$  is  $6\Omega$ , the total power dissipation,  $P_d$ , within the hybrid IC, will be a maximum of  $156\text{W}$  at  $1\text{kHz}$  for a continuous sine wave signal according to the  $P_d$ - $P_O$  characteristics. For the music signals normally handled by audio amplifiers, a value of  $1/8P_O \text{ max}$  is generally used for  $P_d$  as an estimate of the power dissipation based on the type of continuous signal. (Note that the factor used may differ depending on the safety standard used.)

This is:

$$P_d \approx 63.0\text{W} \quad (\text{when } 1/8P_O \text{ max.} = 15\text{W}, P_O \text{ max.} = 120\text{W}).$$

The number of power transistors in audio amplifier block of these hybrid ICs,  $N$ , is 4, and the thermal resistance per transistor,  $\theta_{j-c}$ , is  $1.5^\circ\text{C/W}$ . Therefore, the required heat sink thermal resistance for a guaranteed ambient temperature,  $T_a$ , of  $50^\circ\text{C}$  will be as follows.

$$\begin{aligned} \text{From formula (1)'} \quad \theta_{c-a} &< (125 - 50)/63.0 \\ &< 1.19 \end{aligned}$$

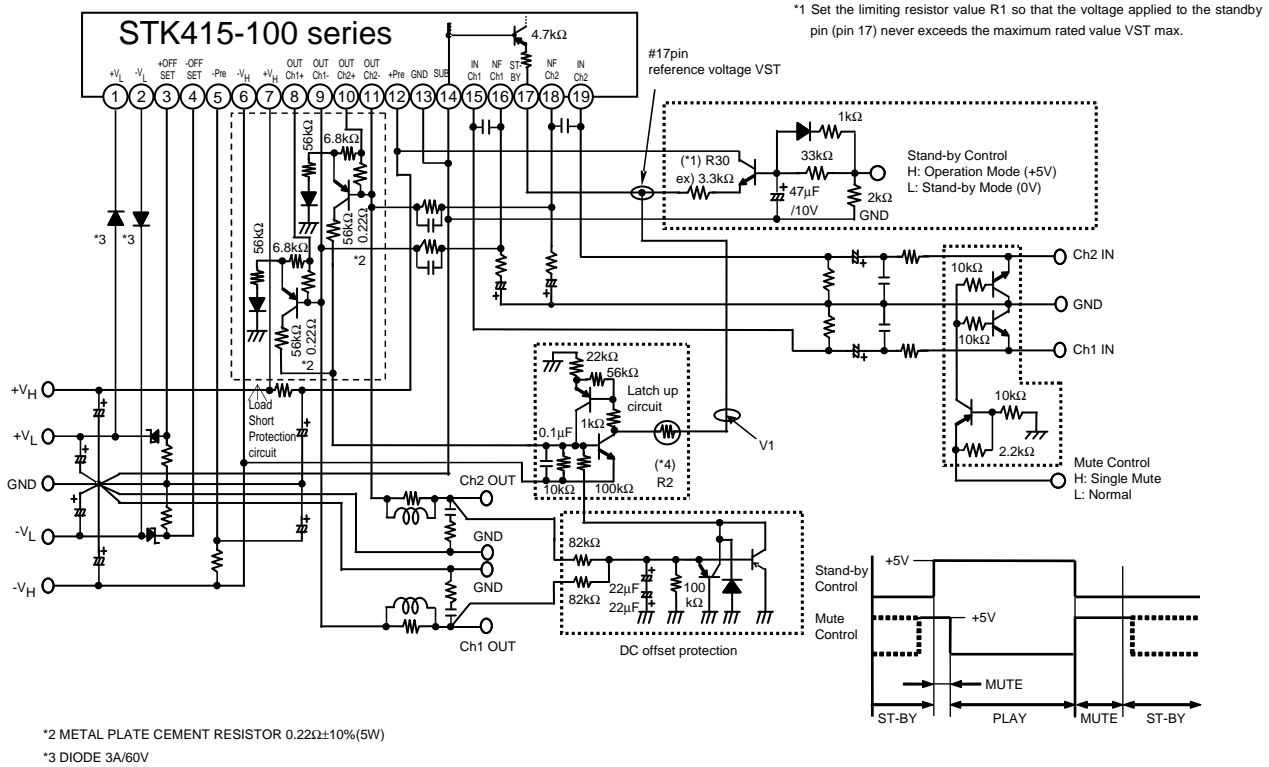
$$\begin{aligned} \text{From formula (2)'} \quad \theta_{c-a} &< (150 - 50)/63.0 - 1.5/4 \\ &< 1.21 \end{aligned}$$

Therefore, the value of  $1.19^\circ\text{C/W}$ , which satisfies both of these formulae, is the required thermal resistance of the heat sink.

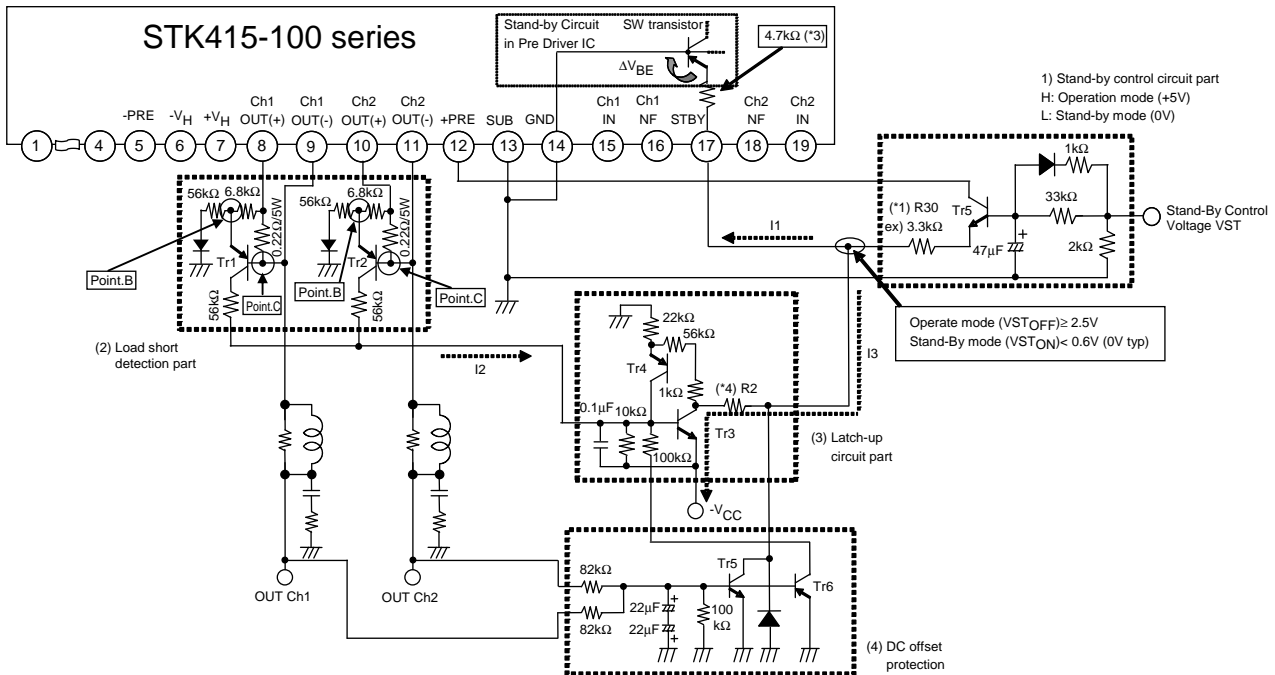
Note that this thermal design example assumes the use of a constant-voltage power supply, and is therefore not a verified design for any particular user's end product.

**STK415-140-E**

**STK415-100 Series Stand-by control, Mute control, Load-short protection & DC offset protection application**



**STK415-100 Series Application explanation**



## STK415-140-E

The protection circuit application for the STK415-100sr consists of the following blocks (blocks (1) to (4)).

- (1) Standby control circuit block
- (2) Load short-circuit detection block
- (3) Latch-up circuit block
- (4) DC voltage protection block

### 1) Standby control circuit block

Concerning pin 17 reference voltage VST

#### <1> Operation mode

The switching transistor of the predriver IC turns on when the pin 17 reference voltage, VST, becomes greater than or equal to 2.5V, placing the amplifier into the operation mode.

Example: When  $VST (\text{min.}) = 2.5\text{V}$

I1 is approximately equal to 0.40mA since  $VST = (*2) \times IST + 0.6\text{V} \rightarrow 2.5\text{V} = 4.7\text{k}\Omega \times IST + 0.6\text{V}$ .

#### <2> Standby mode

The switching transistor of the predriver IC turns off when the pin 17 reference voltage, VST, becomes lower than or equal to 0.6V (typ. 0V), placing the amplifier into the standby mode.

Example: When  $VST = 0.6\text{V}$

I1 is approximately equal to 0mA since  $VST = (*2) \times IST + 0.6\text{V} \rightarrow 0.6\text{V} = 4.7\text{k}\Omega \times IST + 0.6\text{V}$ .

#### (\*1) Limiting resistor

Determine the value of R1 so that the voltage VST applied to the standby pin (pin 17) falls within the rating (+2.5V to 5.5V (typ. 3.0V)).

(\*2) The standby control voltage must be supplied from the host including microcontrollers.

(\*3) A 4.7k $\Omega$  limiting resistor is also incorporated inside the hybrid IC (at pin 17).

### 2) Load short-circuit detection block

Since the voltage between point B and point C is less than 0.6V in normal operation mode ( $V_{BE} < 0.6\text{V}$ ) and TR1 (or TR2) is not activated, the load short-circuit detection block does not operate.

When a load short-circuit occurs, however, the voltage between point B and point C becomes larger than 0.6V, causing TR1 (or TR2) to turn on ( $V_{BE} > 0.6\text{V}$ ), and current I2 to flow.

### 3) Latch-up circuit block

TR3 is activated when I2 is supplied to the latch-up circuit.

When TR3 turns on and current I3 starts flowing, VST goes down to 0V (standby mode), protecting the power amplifier.

Since TR3 and TR4 configure a thyristor, once TR3 is activated, the IC is held in the standby mode.

To release the standby mode and reactivate the power amplifier, it is necessary to set the standby control voltage (\*2) temporarily low (0V). Subsequently, when the standby control is returned to high, the power amplifier will become active again.

(\*4) The I3 value varies depending on the supply voltage. Determine the value of R2 using the formula below, so that

I1 is equal to or less than I3.

$$I1 \leq I3 = V_{CC}/R2$$

### 4) DC offset protection block

The DC offset protection circuit is activated when  $\pm 0.5\text{V}$  (typ) voltage is applied to either "OUT CH1" or "OUT CH2," and the hybrid IC is shut down (standby mode).

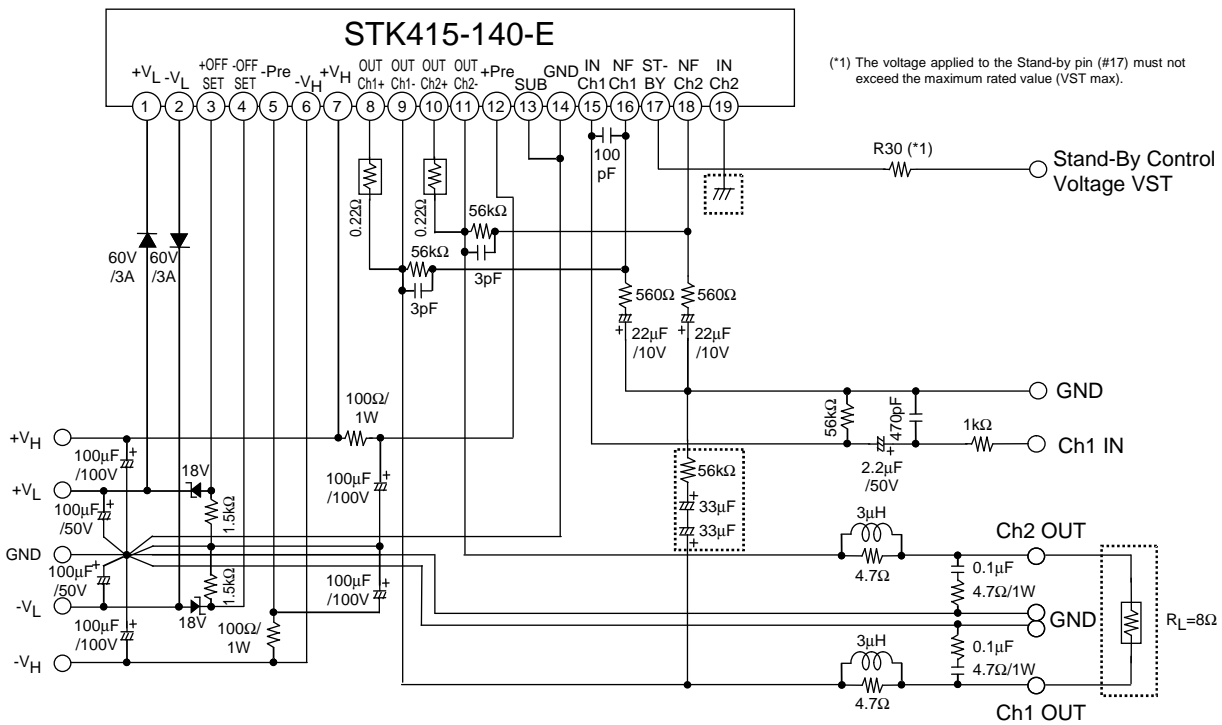
To release the IC from the standby mode and reactivate the power amplifier, it is necessary to set the standby control voltage temporarily low (0V).

Subsequently, when the standby control is returned to high (+5V, for example), the power amplifier will become active again.

The protection level must be set using the 82k $\Omega$  resistor. Furthermore, the time constant must be determined using 22 $\mu$ /22 $\mu$  capacitors to prevent the amplifier from malfunctioning due to the audio signal.

**STK415-140-E**

**STK415-140-E BTL Application**



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