AT&T Microelectronics

# 41LF2
# Quad Differential Line Receiver

## Features

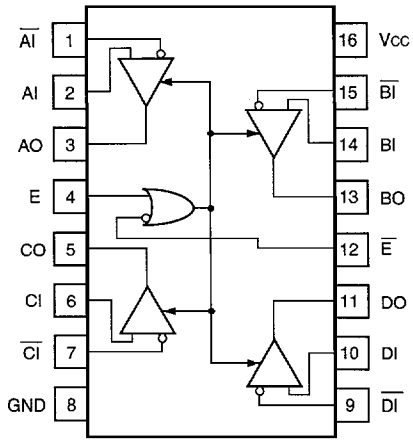
- 2000 V CDM and 2000 V HBM input ESD rating
- Pin-equivalent to the general-trade 26LS32 device, with improved speed and reduced power consumption
- High input impedance ≈ 8 kΩ
- Four line receivers per package
- Meets ESDI standards
- 9 ns maximum propagation delay
- Single 5.0 V supply
- Operating temperature range: 0 °C to 85 °C
- 160 Mbits/s maximum data rate when used with the 41LG or 41LP drivers
- 220 mW maximum power dissipation
- 0.20 V input sensitivity (typical)
- Common-mode rejection range of ±3.9 V
- −1.0 V to +7.2 V common-mode range

## Description

The 41LF2 Quad Differential Line Receiver integrated circuits receive digital data over balanced transmission lines. These receivers translate differential input logic levels to TTL output logic levels. The 41LF2 offers improved ESD performance over the 41LF device. These devices are pin equivalent to the general-trade 26LS32 device, but offer improved speed and reduced power consumption. These devices have four receivers with a common enable control. The 41LF2 devices are compatible with the AT&T 41 Series of line drivers and transceivers.

The packaging options that are available for the quad differential line receivers include a 16-pin DIP (41LF2), a 16-pin J-lead SOJ (1041LF2), a 16-pin gull-wing SOIC (1141LF2), and a 16-pin narrow-body gull-wing SOIC (1241LF2).

## Pin Information




41LF2
1041LF2
1141LF2
1241LF2

12-2248C

Note: The device is disabled when E = 0 and $\overline{E}$ = 1.

**Figure 4-3. 41LF2 Logic Diagram**

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | — | 7.0 | V |
| Ambient Operating Temperature | $T_A$ | 0 | 85 | °C |
| Storage Temperature | $T_{stg}$ | –40 | 125 | °C |

## Handling Precautions

**CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).**

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. 41 Series receiver differential inputs are not equipped with ESD protection. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltages presented here were obtained using this circuit.

| HBM ESD Threshold Voltage | |
|---|---|
| **Device** | **Rating** |
| 41 Series Receiver Inputs and Outputs | >2000 V |

## Electrical Characteristics

**Table 4-4. 41LF2 Power Supply Current Characteristics**

$T_A$ = 0 °C to 85 °C, $V_{CC}$ = 5 V ± 0.5 V.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Current: | | | | | |
| 41LF2: | | | | | |
| All Outputs Disabled | $I_{CC}$ | — | 35 | 50 | mA |
| All Outputs Enabled | $I_{CC}$ | — | 30 | 40 | mA |

**Table 4-5. 41LF2 Voltage and Current Characteristics**

$T_A$ = 0 °C to 85 °C.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltages, $V_{CC}$ = 4.5 V: | | | | | |
| Low, $I_{OL}$ = 8.0 mA | $V_{OL}$ | — | — | 0.5 | V |
| High, $I_{OH}$ = –400 µA | $V_{OH}$ | 2.5 | — | — | V |
| Enable Input Voltages: | | | | | |
| Low, $V_{CC}$ = 5.5 V | $V_{IL}$* | — | — | 0.7 | V |
| High, $V_{CC}$ = 4.5 V | $V_{IH}$* | 2.0 | — | — | V |
| Minimum Input Differential Voltage, $V_{IH} - V_{IL}$: | | | | | |
| –0.60 V < $V_{IH}$ < 7.2 V, –1.0 V < $V_{IL}$ < 6.8 V | $V_{TH}$* | — | 0.1 | 0.20 | V |
| Output Currents, $V_{CC}$ = 5.5 V: | | | | | |
| Off-state (high Z), $V_O$ = 0.4 V | $I_{OZL}$ | — | — | –20 | µA |
| Off-state (high Z), $V_O$ = 2.4 V | $I_{OZH}$ | — | — | 20 | µA |
| Short Circuit | $I_{OS}$† | –25.0 | — | –100 | mA |
| Enable Input Currents, $V_{CC}$ = 5.5 V: | | | | | |
| Low, $V_{IN}$ = –1.2 V | $I_{IL}$ | — | — | –400 | µA |
| High, $V_{IN}$ = 2.7 V | $I_{IH}$ | — | — | 20 | µA |
| Reverse, $V_{IN}$ = 5.5 V | $I_{IH}$ | — | — | 100 | µA |
| Differential Input Currents | | | | | |
| Low, $V_{IN}$ = –1.2 V | $I_{IL}$ | — | — | –1.0 | mA |
| High, $V_{IN}$ = 7.2 V | $I_{IH}$ | — | — | 1.0 | mA |

* The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.
† Test must be performed one lead at a time to prevent damage to the device.

Note: It is recommended that all unused positive inputs be tied to the positive power supply.

## Timing Characteristics

**Table 4-6. 41LF2 Timing Characteristics** (See Figures 6-3 and 6-4.)

Output propagation delay test circuit connected to output (see Figure 6-8).

$T_A$ = 25 °C, $V_{CC}$ = 5 V.

| Symbol | Parameter | Typ | Max | Unit |
|---|---|---|---|---|
| | Propagation Delay: | | | |
| $t_{PLH}$ | Input to Output High | 5.0 | 9.0 | ns |
| $t_{PHL}$ | Input to Output Low | 6.0 | 9.0 | ns |
| | Disable Time, $C_L$ = 5 pF: | | | |
| $t_{PHZ}$ | High to High Impedance | 10 | 15 | ns |
| $t_{PLZ}$ | Low to High Impedance | 10 | 15 | ns |
| | Enable Time, $C_L$ = 5 pF: | | | |
| $t_{PZH}$ | High Impedance to High | 10 | 15 | ns |
| $t_{PZL}$ | High Impedance to Low | 10 | 15 | ns |