

200V 40-Channel Vacuum-Fluorescent Display Driver

Ordering Information

Device	Package Options	
	60 Pin Plastic Gullwing	Die
HV701	HV701PG	HV701X
HV711	HV711PG	HV711X

Features

- 220V push-pull outputs
- 40 output lines
- 5V CMOS logic
- +2.5 / -10mA output sink/source
- Two 20-bit parallel shift registers
- 40-bit latch
- 60-pin 2-sided Gullwing
- 6MHz shift clock
- Processed with HVCMOS® technology

General Description

The HV701/711 are designed to drive vacuum fluorescent displays used in graphic applications. The 40 outputs are supplied by 40 output latches which are fed from two 20-bit shift registers that have been loaded in parallel from 2 data inputs. Data is shifted in on the HIGH-to-LOW clock transition. Logic control is provided by a latch enable (LE) and output clear (CL). When CL is HIGH, data is reflected at the output; when CL is LOW all outputs are LOW.

Pin assignments for the HV711 have pin reversed from the HV701 for ease in PC board layout.

Absolute Maximum Ratings

Supply voltage, ¹ V _{DD}	-0.5V to +7V
Supply voltage, ¹ V _{PP}	-0.5V to +250V
Logic input levels	-0.5V to V _{DD} +0.5V
Continuous total power dissipation ^{2, 3}	800mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10 seconds	260°C

Notes:

1. All voltages referenced to GND
2. Duty cycle is limited by the total power dissipated in the package
3. For operation above 25°C ambient, derate linearly to 614mW/°C @ 6.4mW/°C.



Electrical Characteristics ($V_{DD} = 5V$, $V_{PP} = 200V$, $T_A = -40^\circ C$ to $85^\circ C$ unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Logic supply current	I_{DD}	$V_{DD} = 5.5V$ No load $f_{CLK} = 6\text{ MHz}$	All outputs low			16.0	mA
			All outputs low $T_A = 25^\circ C$			12.0	mA
I_{DD} (quiescent)	I_{DDQ}	$V_{DD} = 5.5V$	All outputs high $T_A = 25^\circ C$			100	μA
High voltage supply current	I_{PP}	$V_{PP} = 200V$ No load	All outputs low			250	μA
			All outputs low $T_A = 25^\circ C$			250	μA
			All outputs high $T_A = 25^\circ C$			250	μA
High-level input voltage	V_{IH}		$V_{DD} = 4.5V$	3.6			V
			$V_{DD} = 5.5V$	4.4			V
Low-level input voltage	V_{IL}		$V_{DD} = 4.5V$			0.9	V
			$V_{DD} = 5.5V$			1.1	V
Input leak current	I_I	$T_A = 25^\circ C$				± 1	μA
Input capacitance	C_I	$T_A = 25^\circ C$				25	pF
High-level data output voltage	V_{OH}	$I_O = -0.1\text{ mA}$	$V_{DD} = 4.5V$	3.6			V
			$V_{DD} = 5.5V$	4.4			V
Low-level data output voltage	V_{OL}	$I_O = +0.1\text{ mA}$	$V_{DD} = 4.5V$			0.9	V
			$V_{DD} = 5.5V$			1.1	V
High-level output voltage	V_{HVOH}	$I_{HVO} = -1.0\text{ mA}$, $T_A = 25^\circ C$		198			V
Low-level output voltage	V_{HVOL}	$I_{HVO} = +0.5\text{ mA}$, $T_A = 25^\circ C$				2.0	V
High-level output current	I_{HVOH}	$V_{HVO} = 195V$, $T_A = 25^\circ C$		-10			mA
Low-level output current	I_{HVOL}	$V_{HVO} = 10V$, $T_A = 25^\circ C$		2.5			mA

Switching Characteristics ($V_{DD} = 5V$, $V_{PP} = 200V$, $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay time, clk to data out	t_{PD}	See Figure 1,2			150	ns
Delay time high voltage output, low to high	t_{DLH}	See Figure 1, 2, ¹ Each HVO ²			4.0	μs
Delay time high voltage output, high to low	t_{DHL}	See Figure 1, 2, ¹ Each HVO ²			0.3	μs
Transition time high voltage output, low to high	t_{TLH}	See Figure 1, 2, ¹ Each HVO ²			6.0	μs
Transition time high voltage output, high to low	t_{THL}	See Figure 1, 2, ¹ Each HVO ²			0.3	μs

Notes:

1. The values of t_{DLH} and t_{DHL} are the delay times from \overline{CL} .
2. High voltage output terminal.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage	V_{DD}	Logic Supply	4.5	5.5	V
Supply voltage	V_{PP}	High voltage supply	25	200	V
High-level input voltage	V_{IH}	Each input	$V_{DD} = 4.5V$	3.6	V
			$V_{DD} = 5.5V$	4.4	V
Low-level input voltage	V_{IL}	Each input	$V_{DD} = 4.5$	0.9	V
			$V_{DD} = 5.5$	1.1	V
High-level output current	I_{HVOH}	Each HVO*		-10	mA
Low-level output current	I_{HVOL}	Each HVO*		2.5	mA
Clock frequency	f_{CLK}	Cascade		6.0	MHz
Clock pulse width	$t_{w(CLK)}$	See Figure 1, 2	70		ns
Data setup time	t_{su}	See Figure 1, 2	20		ns
Data hold time	t_h	See Figure 1, 2	45		ns
Data pulse width	$t_{w(D)}$	See Figure 1, 2	145		ns
Latch enable pulse width	$t_{w(LE)}$	See Figure 1, 2	80		ns
Data setup time	CLK-LE	$t_{su(CLK-LE)}$	45		ns
Data setup time	LE-CLK	$t_{su(LE-CLK)}$	10		ns
Data setup time	LE-CL	$t_{su(LE-CL)}$	10		μs
Clear pulse width	$t_{w(\overline{CL})}$	See Figure 1, 2	2		μs
Operating free-air temperature range	T_{ope}		-40	+85	$^{\circ}C$

Note:

HVO*: High voltage output terminal

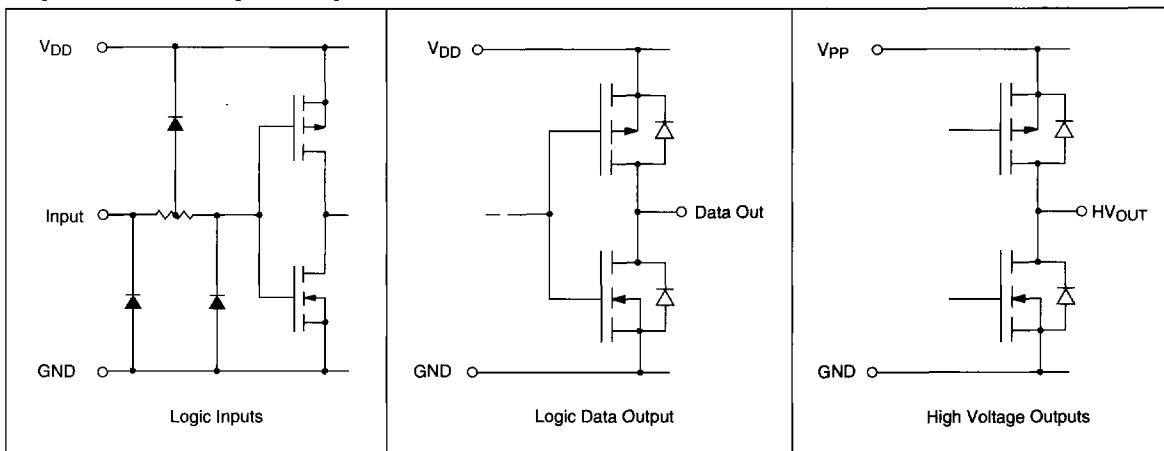
Power-up sequence should be the following:

1. Connect ground.
2. Apply VDD.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply VPP.

Power-down sequence should be the reverse of the above.



Input and Output Equivalent Circuits



Parameter Measurement Information

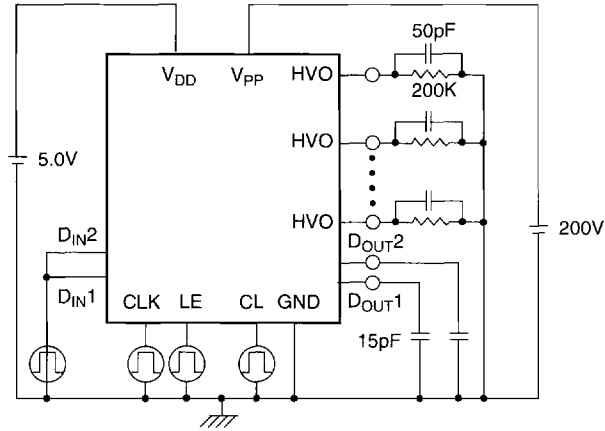


Figure 1: Test Circuit

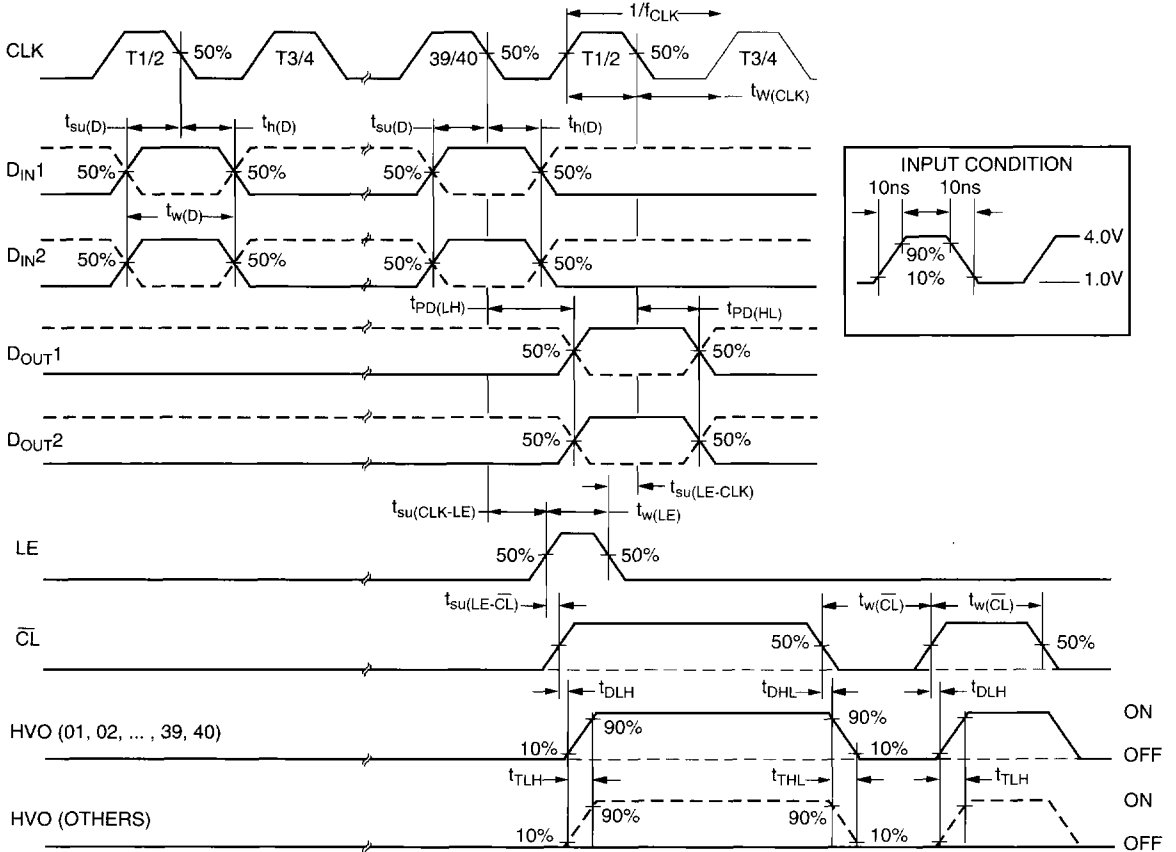
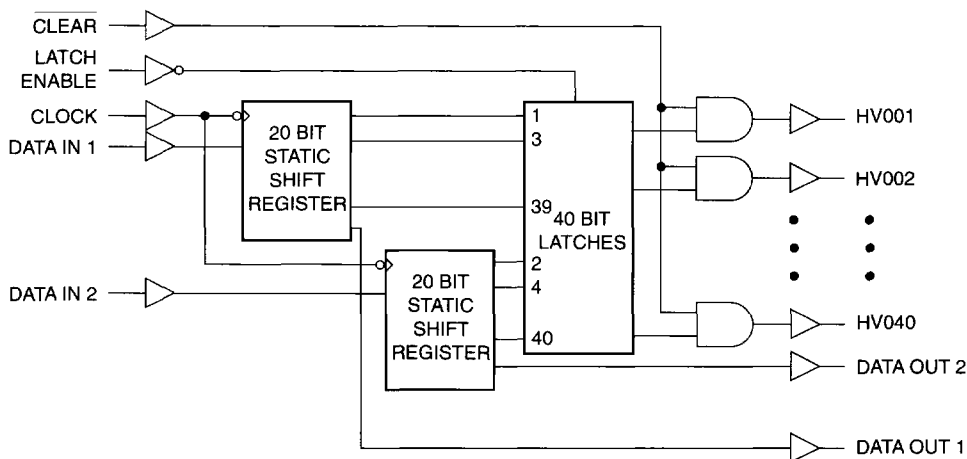


Figure 2: Timing Chart

Logic Diagram



Input Truth Table

CLK	Shift Register
	Data is Loaded
No Change	*

Output Truth Table

Data	LE	CLR	Output
X	X	L	All O/P Low
H	H	H	High
L	H	H	Low
X	L	H	Previous Latch Data

Note:

High = high level, L = low level, X = high or low level.

= high-to-low level transition

* Previous state



Pin Configurations

HV701

60 Pin FlatPackage

Pin	Function	Pin	Function
1	HV _{OUT} 36	31	D _{IN} 1
2	HV _{OUT} 35	32	D _{IN} 2
3	HV _{OUT} 34	33	NC
4	HV _{OUT} 33	34	CLK
5	HV _{OUT} 32	35	NC
6	HV _{OUT} 31	36	$\overline{\text{CLR}}$
7	HV _{OUT} 30	37	NC
8	HV _{OUT} 29	38	NC
9	HV _{OUT} 28	39	V _{PP}
10	HV _{OUT} 27	40	NC
11	HV _{OUT} 26	41	HV _{OUT} 1
12	HV _{OUT} 25	42	HV _{OUT} 2
13	HV _{OUT} 24	43	HV _{OUT} 3
14	HV _{OUT} 23	44	HV _{OUT} 4
15	HV _{OUT} 22	45	HV _{OUT} 20
16	HV _{OUT} 21	46	HV _{OUT} 19
17	HV _{OUT} 37	47	HV _{OUT} 18
18	HV _{OUT} 38	48	HV _{OUT} 17
19	HV _{OUT} 39	49	HV _{OUT} 16
20	HV _{OUT} 40	50	HV _{OUT} 15
21	NC	51	HV _{OUT} 14
22	V _{PP}	52	HV _{OUT} 13
23	NC	53	HV _{OUT} 12
24	GND	54	HV _{OUT} 11
25	NC	55	HV _{OUT} 10
26	LE	56	HV _{OUT} 9
27	NC	57	HV _{OUT} 8
28	V _{DD}	58	HV _{OUT} 7
29	D _{OUT} 2	59	HV _{OUT} 6
30	D _{OUT} 1	60	HV _{OUT} 5

HV711

60 Pin FlatPackage

Pin	Function	Pin	Function
1	HV _{OUT} 5	31	D _{OUT} 1
2	HV _{OUT} 6	32	D _{OUT} 2
3	HV _{OUT} 7	33	V _{DD}
4	HV _{OUT} 8	34	NC
5	HV _{OUT} 9	35	LE
6	HV _{OUT} 10	36	NC
7	HV _{OUT} 11	37	GND
8	HV _{OUT} 12	38	NC
9	HV _{OUT} 13	39	V _{PP}
10	HV _{OUT} 14	40	NC
11	HV _{OUT} 15	41	HV _{OUT} 40
12	HV _{OUT} 16	42	HV _{OUT} 39
13	HV _{OUT} 17	43	HV _{OUT} 38
14	HV _{OUT} 18	44	HV _{OUT} 37
15	HV _{OUT} 19	45	HV _{OUT} 21
16	HV _{OUT} 20	46	HV _{OUT} 22
17	HV _{OUT} 4	47	HV _{OUT} 23
18	HV _{OUT} 3	48	HV _{OUT} 24
19	HV _{OUT} 2	49	HV _{OUT} 25
20	HV _{OUT} 1	50	HV _{OUT} 26
21	NC	51	HV _{OUT} 27
22	V _{PP}	52	HV _{OUT} 28
23	NC	53	HV _{OUT} 29
24	NC	54	HV _{OUT} 30
25	$\overline{\text{CLR}}$	55	HV _{OUT} 31
26	NC	56	HV _{OUT} 32
27	CLK	57	HV _{OUT} 33
28	NC	58	HV _{OUT} 34
29	D _{IN} 2	59	HV _{OUT} 35
30	D _{IN} 1	60	HV _{OUT} 36

Package Outline

