IS6MC512L

512KB CMOS 3.1 *COASt* CACHE MODULE FOR THE INTEL PENTIUM™ CPU

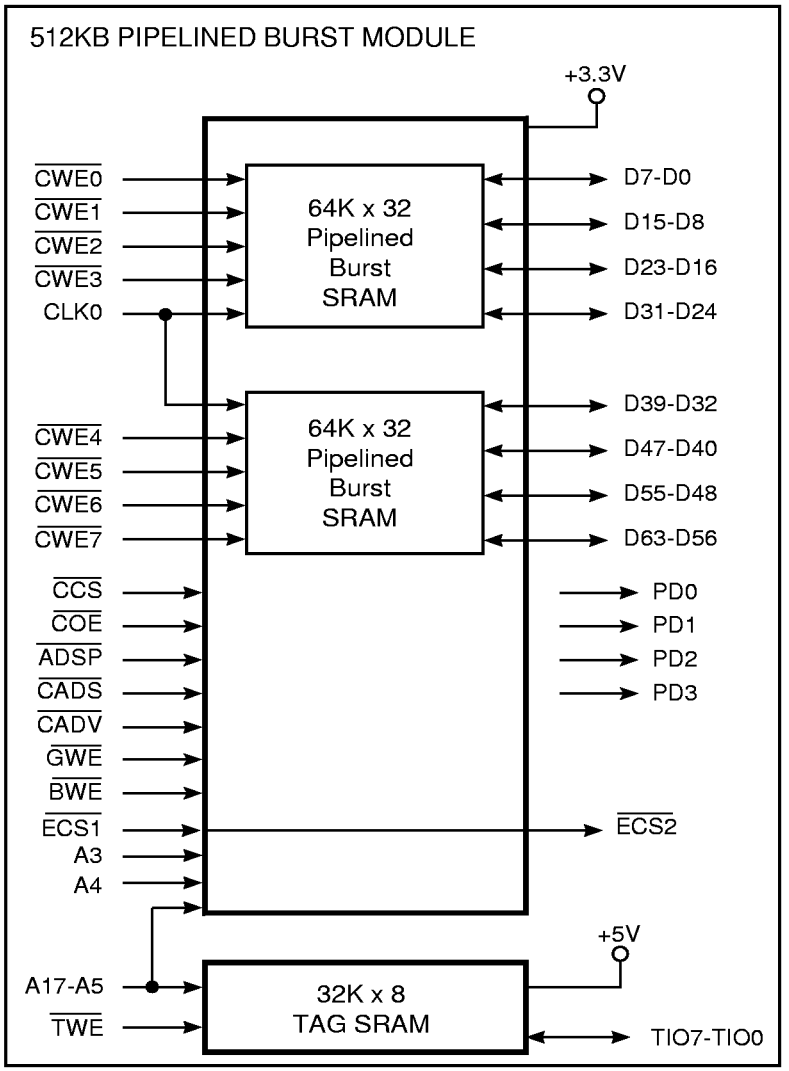
PRELIMINARY

MARCH 1997

FEATURES

- Low-cost, card-edge low-profile (CELP) module with 160 leads
- For Intel Pentium CPU-based systems
- Separate 5V and 3.3V power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- CMOS SRAMs for low power
- Conforms to Intel 3.1 COASt specification

IS6MC512L FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

ISSI's IS6MC512L is an L2 cache module designed for use with Intel Pentium CPU-based systems. This *ISSI* synchronous cache module uses IS61C6432 64K x 32 pipelined synchronous burst static RAMs which are mounted on a multilayer board. In addition, this module uses a single 5V 8-bit wide CMOS SRAM for the tag.

On-board logic, 3.3V data RAM, and a 5V tag RAM provide an exact interface between the module and the PC chipset. Four PD (presence detect) input pins allow the system to determine the particular cache configuration.

ISSI's CELP 160-lead module provides space savings that allows the customer to design additional functions into the system or to shrink the size of the motherboard.

All inputs and outputs are TTL-compatible. Multiple GND pins and on-board decoupling capacitors provide maximum protection from noise.

PRESENCE DETECT TABLE

PD3	PD2	PD1	PD0	MODULE
NC	NC	NC	NC	No Cache Present
GND	NC	NC	NC	IS6MC512L

PIN CONFIGURATION

TOP VIEW OF CONNECTOR (BURNDY CELP 2X80SC)

GND	81	1	GND
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
NC	86	6	NC
VCC5	87	7	VCC3
NC	88	8	$\overline{TWE}$
CADV	89	9	$\overline{CADS}$
GND	90	10	GND
$\overline{COE}$	91	11	$\overline{CWE4}$
$\overline{CWE5}$	92	12	$\overline{CWE6}$
$\overline{CWE7}$	93	13	$\overline{CWE0}$
$\overline{CWE1}$	94	14	$\overline{CWE2}$
VCC5	95	15	VCC3
$\overline{CWE3}$	96	16	$\overline{CCS}$
NC	97	17	$\overline{GWE}$
NC	98	18	$\overline{BWE}$
GND	99	19	GND
NC	100	20	A3
A4	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
VCC5	105	25	VCC3
A17	106	26	A18
GND	107	27	GND
A9	108	28	A12
A14	109	29	A13
A15	110	30	ADSP
NC	111	31	$\overline{ESC1}$
PD0	112	32	ESC2
PD2	113	33	PD1
PD4	114	34	PD3
GND	115	35	GND
CLK0	116	36	CLK1
GND	117	37	GND
D63	118	38	D62
VCC5	119	39	VCC3
D61	120	40	D60
D59	121	41	D58
D57	122	42	D56
GND	123	43	GND
D55	124	44	D54
D53	125	45	D52
D51	126	46	D50
D49	127	47	D48
GND	128	48	GND
D47	129	49	D46
D45	130	50	D44
D43	131	51	D42
VCC5	132	52	VCC3
D41	133	53	D40
D39	134	54	D38
D37	135	55	D36
GND	136	56	GND
D35	137	57	D34
D33	138	58	D32
D31	138	59	D30
VCC5	140	60	VCC3
D29	141	61	D28
D27	142	62	D26
D25	143	63	D24
GND	144	64	GND
D23	145	65	D22
D21	146	66	D20
D19	147	67	D18
VCC5	148	68	VCC3
D17	149	69	D16
D15	150	70	D14
D13	151	71	D12
GND	152	72	GND
D11	153	73	D10
D9	154	74	D8
D7	155	75	D6
VCC5	156	76	VCC3
D5	157	77	D4
D3	158	78	D2
D1	159	79	D0
GND	160	80	GND

PIN DESCRIPTIONS

A18-A3	Address Inputs
A18-A5	Tag Address Inputs
CLK0	Clock Input
CLK1	Clock Input
D63-D0	Cache Data Inputs/Outputs
TIO7-TIO0	Tag Inputs/Outputs
PD0-PD3	Presence Detect Pins
$\overline{COE}$	Cache Data Output Enable Input
$\overline{TWE}$	Tag Write Enable Input
$\overline{CWE7}$-$\overline{CWE0}$	Cache Data Write Enable Input
$\overline{CCS}$	Cache Data Chip Enable Input
$\overline{CADS}$	Cache Address Status Input
$\overline{ADSP}$	Processor Address Status Input
$\overline{CADV}$	Burst Address Advance
$\overline{GWE}$	Global Write Enable Input
$\overline{BWE}$	Byte Write Enable Input
$\overline{ECS1}$	Expansion Chip Select Input
$\overline{ECS2}$	Expansion Chip Select Output

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
$V_{CC}5$	Power Supply Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
$V_{CC}3$	Power Supply Voltage with Respect to GND	–0.5 to Vcc + 0.3	V
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
I_{OUT}	DC Output Current (LOW)	100	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (T_A = 0°C to +70°C)

Symbol	Parameter	Range
$V_{CC}3$	3.3V Supply Voltage	3.3V +10%, –5%
$V_{CC}5$	5.0V Supply Voltage	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

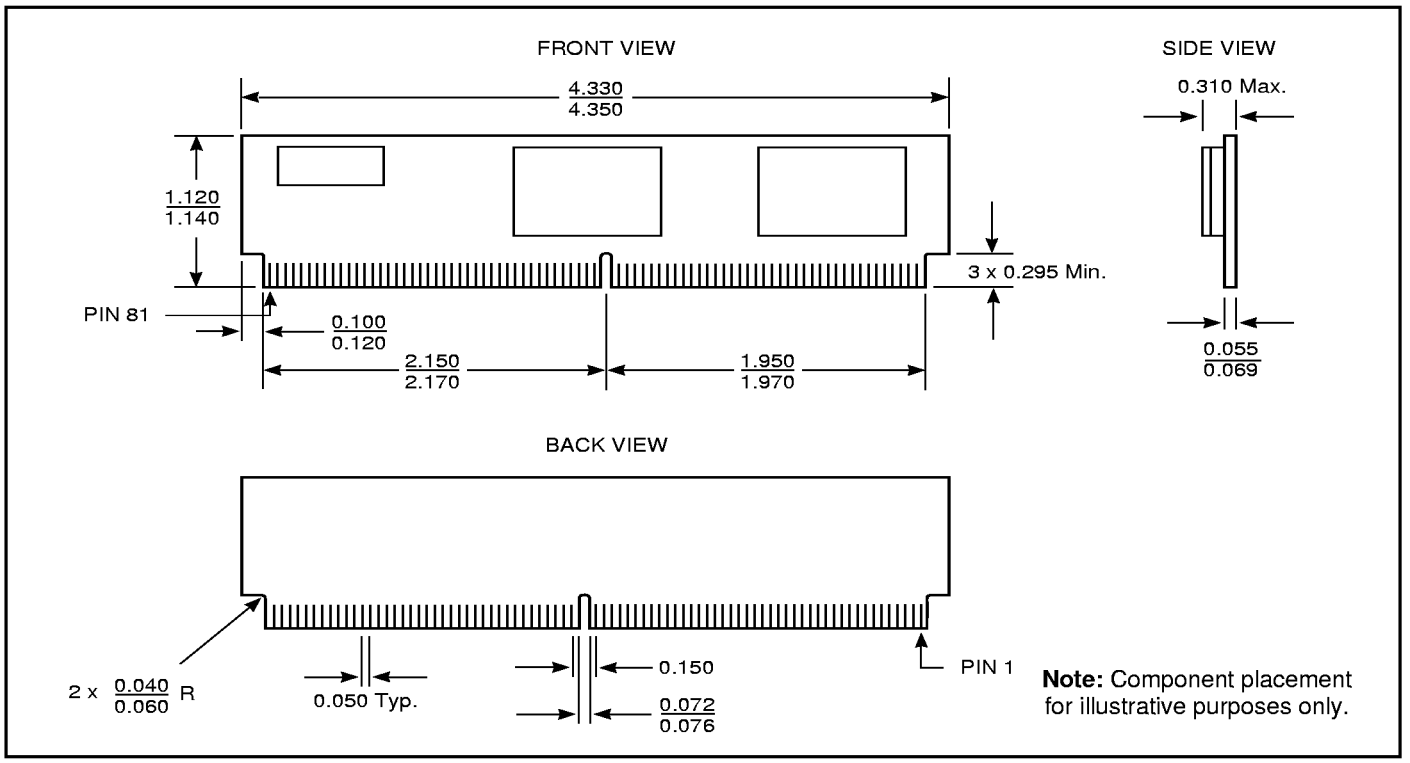
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –5.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 5.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–20	20	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{OE}$ = V_{IH}	–10	10	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$I_{CC}3$	3.3V Supply Current	$V_{CC}3$ = Max., $\overline{CCS}$ ≤ V_{IL} f = f_{MAX}, Outputs Open	—	400	mA
$I_{CC}5$	5.0V Supply Current	$V_{CC}5$ = Max., $\overline{CCS}$ ≤ V_{IL} f = f_{MAX}, Outputs Open	—	150	mA
$I_{SB}3$	Standby 3.3V Power Supply Current	$V_{CC}3$ = Max., $\overline{CCS}$ ≥ V_{CC} – 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} – 0.2V, f = 0, Outputs Open	—	120	mA
$I_{SB}5$	Standby 5.0V Power Supply Current	$V_{CC}5$ = Max., $\overline{CCS}$ ≥ V_{CC} – 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} – 0.2V, f = 0, Outputs Open	—	30	mA

MODULE DIMENSIONS

IS6MC512L PIPELINED BURST MODULE



ORDERING INFORMATION

Density (KBytes)	Speed (MHz)	Order Part Number
512	60	IS6MC512L-60
512	66	IS6MC512L-66

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Fax: (408) 588-0806
Toll Free: 1-800-379-4774
http://www.issiusa.com