

MH51216FRN-10,-12,-15

8388608-BIT(524288-WORD BY 16-BIT)CMOS FLASH MEMORY

DESCRIPTION

The Mitsubishi MH51216FRN are high-speed 8388608-bit CMOS Flash Memories. They are suitable for the applications with micro-processor or micro-controller where on-board reprogramming is required. The MH51216FRN are fabricated by N-channel double polysilicon gate for memory and CMOS technology for peripheral circuits.

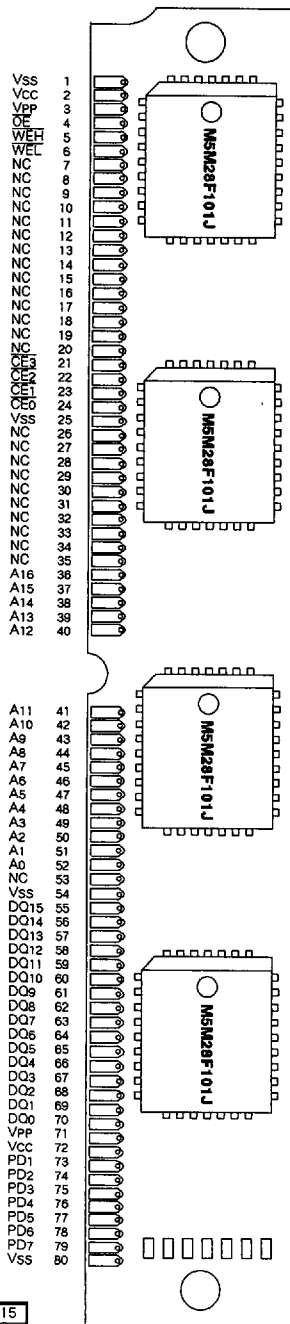
FEATURES

- 524288-word by 16-bit organization
- Access time
 MH51216FRN-10100ns (max)
 MH51216FRN-12120ns (max)
 MH51216FRN-15150ns (max)
- Low power consumption
 Active..... 363mW (max)
 Stand-by..... 44mW (max)
- Power supply voltage
 V_{CC} = 5V ± 0.5V
 V_{PP} = 12V ± 0.6V
- Byte program and Chip erase
- Program/erase operation controlled by software command
- Program/erase pulses controlled by an embedded timer
- 10000 program/erase cycles
- Tri-state output buffer
- TTL-compatible input and output in read and write mode
- Contained device-identifier code
- Incorporated data-protection
- 80-pin Single in-line module
- Gold plating contact

APPLICATION

Micro-computer systems and peripheral equipments

PIN CONFIGURATION (TOP VIEW) (Both side)



	-10	-12	-15
PD1	NC	NC	NC
PD2	Vss	Vss	Vss
PD3	NC	NC	NC
PD4	NC	Vss	Vss
PD5	Vss	NC	NC
PD6	Vss	NC	Vss
PD7	Vss	NC	NC

Outline 80N9A

NC : NO CONNECTION

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FUNCTION

MH51216FRN are set to the Read-only mode or Read-write mode by applying the voltage of $V_{PP,L}$ or $V_{PP,H}$, respectively, to V_{PP} pin. In Read-only mode, three operation modes, Read, Output disable and Stand by are accessible. While, in Read-Write mode, four operation modes, Read, Output disable, Stand by and Write are functional.

Read

Set \overline{CE} and \overline{OE} terminals to the read mode (low level). Low level input to \overline{CE} and \overline{OE} , and address signals to the address inputs ($A_0 \sim A_{15}$) make the data contents of the designated address location available at data input/output ($D_0 \sim D_{15}$).

Output Disable

When \overline{OE} is at high level, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

Stand by

When \overline{CE} is at high level, the devices is in the stand by mode and its power consumption is substantially reduced. Data input/output are in a high-impedance (High-Z) state.

Write

Software command accomplishes program and erase operations via the command latch in the device, when high voltage is supplied to V_{PP} . The contents of the latch serve as input to the internal controller. The controller output dictates the function of device. The command latch is written by bringing \overline{WE} to low level, while \overline{CE} is at low level and \overline{OE} is at high level. Addresses are latched on the falling edge of \overline{WE} , while data is latched on the rising edge of \overline{WE} . Standard micro-processor write timings are used.

DATA PROTECTION

1. Power Supply Voltage
When the power supply voltage (V_{CC}) is less than 3.0V, the device is set to the Read-only mode.
2. Write Inhibit
In the cases, as below, write mode is not set.
 - 1) When \overline{CE} and \overline{OE} are terminated to the low level.
 - 2) From 100ns through 5ms after 2nd rising edge of \overline{WE} for program.
 - 3) From 100ns through 5ms after 2nd rising edge of \overline{WE} for erase.
3. Over-erase Protection
Just after powering up, if erase command is inputted, erase operation is not executed. Once byte-program is performed or verified data is not FFH in the erase-verify mode, successive command input for erase will be accepted. Because of this, it is applicable to the case of multi-chip erasing simultaneously.

SOFTWARE COMMAND

When V_{PP} is low ($V_{PP} = V_{PP,L}$), the contents of the command latch are fixed to 00H, and the device is in read-only mode. When V_{PP} is high ($V_{PP} = V_{PP,H}$), the device enters read/write mode. The device operations are selected by writing specific software command into the command latch.

Read Command

The device is in read mode after writing Read Command (0000H) to the command latch. The device continues to be in read mode until the other commands are written. When

V_{PP} powers-up to high voltage ($V_{PP} = V_{PP,H}$), the default contents of the command latch is 0000H. So it is ensured that the false alteration of memory data does not occur during V_{PP} power transition.

Program Command

Program Command is the command for byte-program, and program is initiated by twice of write cycles. Program Command (4040H) is written to the command latch in first write cycle, and the address and data to be programmed are latched in second write cycle. Then the address and data are latched on the falling edge and the rising edge of \overline{WE} pulse, respectively. The byte-program operation is initiated at the rising edge of \overline{WE} in second write cycle, and terminates in 10ms, controlled by the internal timer.

Program Verify Command

Following byte program, the programmed byte must be verified. The program-verify is initiated by writing Program Verify Command (C0C0H) to the command latch. After writing Program Verify Command, programmed data is verified in read mode. Then the address information is not needed.

Erase Command

Erase Command is the command for chip-erase, and chip-erase is initiated by writing twice of the Erase Command (2020H) consecutively to the command latch. The erase operation is initiated with the rising edge of the \overline{WE} pulse and terminates in 9.5ms, controlled by the internal timer. This two-step sequence for chip-erase prevents from erasing accidentally.

Erase Verify Command

Following each erase, all bytes must be verified. The erase verify is initiated by writing Erase Verify Command (A0A0H) to the command latch, while the address to be verified is latched on the falling edge of the \overline{WE} pulse. The erase verify command must be written to the command latch and each address is latched before each byte is verified. The operation continues for each byte until a byte is not erased, or the last address is accessed.

Reset Command

Reset Command is the command to safely abort the erase or program sequences. Following erase or program command in first write cycle, the operation is aborted safely by writing the two consecutive Reset Commands (FFFFH). Then the device enters read mode without altering memory contents.

Read Device Identifier Code

Though PROM programmers can normally read device identifier codes by raising A_9 to high voltage, multiplexing high voltage onto address lines is not desired for micro-processor system. It is another means to read device identifier codes that Read Device Identifier Code Command (9090H) is written to the command latch. Following the command write, the manufacturer code (1C1CH) and the device code (D0D0H) can be read from address 00000H and 00001H, respectively.

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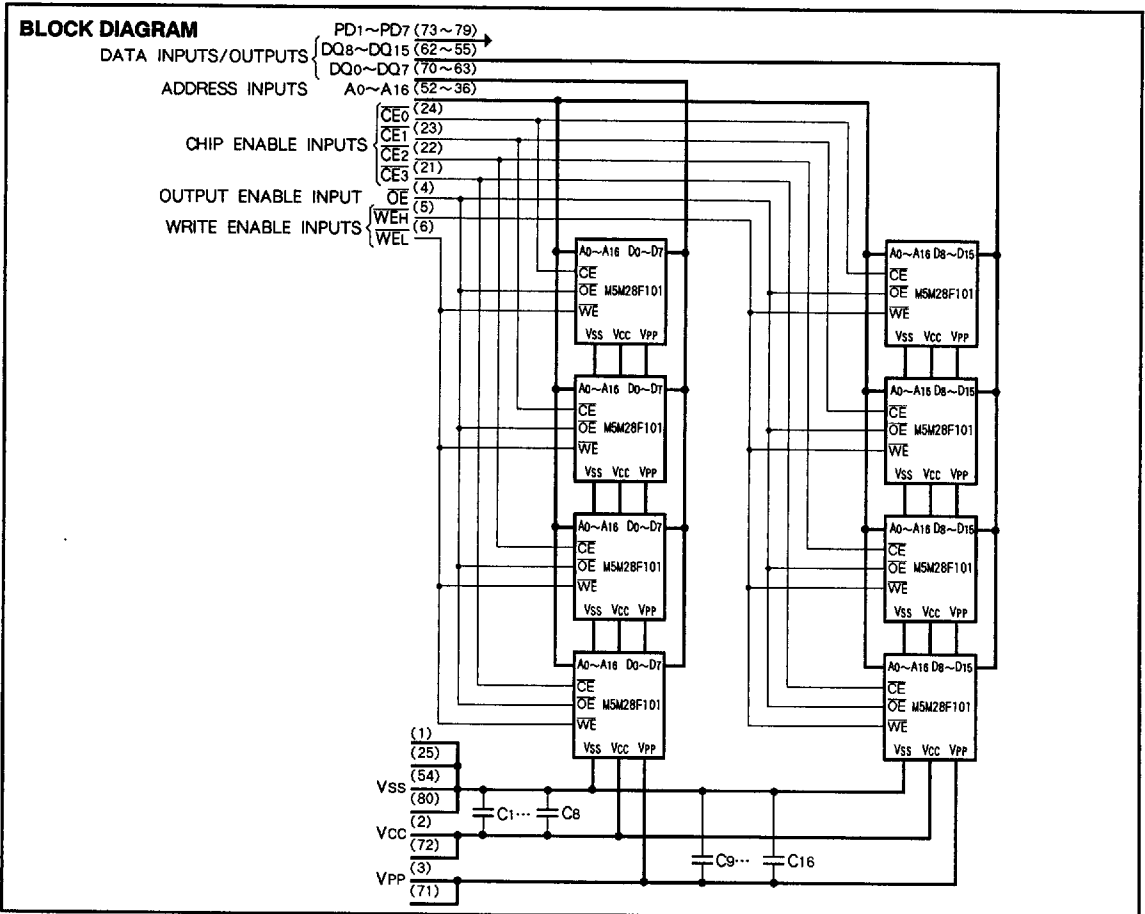
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MODE SELECTION

Mode	Pins	\overline{CE}	\overline{OE}	\overline{WE}	V_{PP}	Data I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	Hi-Z
	Stand by	V_{IH}	X	X	V_{PPL}	Hi-Z
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	Hi-Z
	Stand by	V_{IH}	X	X	V_{PPH}	Hi-Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	Data in

Note 1: X can be V_{IL} or V_{IH}



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Ratings	Unit
V_{I1}	All input or output voltage except V_{PP}/A_9	With respect to Ground	- 0.6~7	V
V_{I2}	V_{PP} supply voltage		- 0.6~14.0	V
V_{I3}	A_9 supply voltage		- 0.6~13.5	V
T_{opr}	Operating temperature		- 10~80	$^{\circ}C$
T_{stg}	Storage temperature		- 40~125	$^{\circ}C$

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SOFTWARE COMMAND DEFINITION

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data I/O	Mode	Address	Data I/O
Read	Write	X	0000H	—	—	—
Program (Byte Program)	Write	X	4040H	Write	Program Address	Program Data
Program verify	Write	X	C0C0H	Read	X	Verify Data
Erase (Chip Erase)	Write	X	2020H	Write	X	2020H
Erase verify	Write	Verify address	A0A0H	Read	X	Verify Data
Reset	Write	X	FFFFH	Write	X	FFFFH
Read device identifier code	Write	X	9090H	Read	ADI	DDI

Note 2: Write and read mode are defined in mode selection table.

ADI = Address of Device Identifier: 00000H for manufacturer code, 00001H for device code.

DDI = Data of Device Identifier: 1CH for manufacturer code, D0H for device code.

DEVICE IDENTIFIER CODE

Code	Pins	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Hex. Data
		Manufacturer Code	V _{IL}	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0
Device Code	V _{IH}	1	1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	D0D0H

Note 3: A₉ = 11.5V~13.0V

A₁~A₈, A₁₀~A₁₅, \overline{CE} , \overline{OE} = V_{IL}, \overline{WE} = V_{IH}

V_{CC} = V_{PP} = 5V ± 10%

The device identifier mode allows the reading of a binary code from the device that identifies the manufacturer and device type. The PROM programmers read the manufacturer code and device code by raising A₉ to high voltage, and automatically select the corresponding programming algorithm.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{IN}	Input capacitance (Address, \overline{CE} , \overline{OE} , \overline{WE})	T _a = 25 °C, f = 1MHz, V _{in} = V _{out} = 0V			65	pF
C _{OUT}	Output capacitance				55	pF

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DC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ILI	Input leakage current	$0 \leq V_{IN} \leq V_{CC}$			10	μA
ILO	Output leakage current	$0 \leq V_{OUT} \leq V_{CC}$			40	μA
ISB1	Vcc stand by current	$V_{CC} = 5.5V, \overline{CE} = V_{IH}$			8	mA
ISB2		$V_{CC} = 5.5V, \overline{CE} = V_{CC} \pm 0.2V$			0.8	mA
Icc1	Vcc active read current	$V_{CC} = 5.5V, \overline{CE} = V_{IL}, f = 10MHz, I_{OUT} = 0mA$			66	mA
Icc2	Vcc program current	$V_{PP} = V_{PPH}$			30	mA
Icc3	Vcc erase current	$V_{PP} = V_{PPH}$			36	mA
Ipp1	VPP read current	$0 \leq V_{PP} \leq V_{CC}$			80	μA
		$V_{CC} < V_{PP} \leq V_{CC} + 1.0V$			400	
		$V_{PP} = V_{PPH}$			80	
Ipp2	VPP program current	$V_{PP} = V_{PPH}$			61	mA
Ipp3	VPP erase current	$V_{PP} = V_{PPH}$			61	mA
VIL	Input low voltage		-0.5		0.8	V
VIH	Input high voltage		2.0		Vcc+0.5	V
Vol	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
VOH1	Output high voltage	$I_{OH} = -400 \mu A$	2.4			V
		$I_{OH} = -100 \mu A$		Vcc-0.4		V
Vppl	VPP during read-only mode		0		Vcc+1.0	V
Vpph	VPP during read/write mode		11.4	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 0.5V, unless otherwise noted)

Read-Only Mode

Symbol	Parameter	Limits						Unit
		MH51216FRN-10		MH51216FRN-12		MH51216FRN-15		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	100		120		150		ns
ta (AD)	Address access time		100		120		150	ns
ta (CE)	Chip enable access time		100		120		150	ns
ta (OE)	Output enable access time		50		50		55	ns
tCLZ	Chip enable to output in low Z	0		0		0		ns
tOLZ	Output enable to output in low Z	0		0		0		ns
tDF	Output enable high to output in high Z		25		30		35	ns
tOH	Output hold from $\overline{CE}, \overline{OE}$, addresses	0		0		0		ns
tWRR	Write recovery time before read	6		6		6		μs

Note 4: Vcc must be applied simultaneously or before VPP and removed simultaneously or after VPP.

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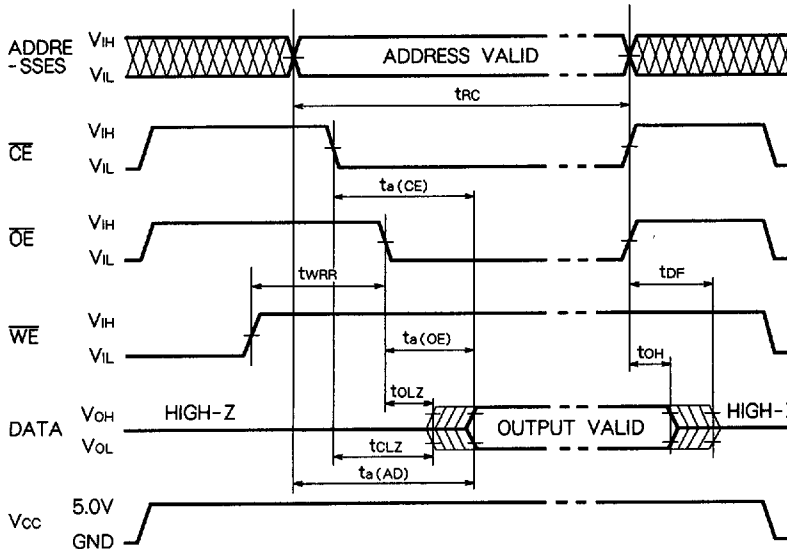
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Read/Write Mode

Symbol	Parameter	Limits						Unit
		MH51216FRN-10		MH51216FRN-12		MH51216FRN-15		
		Min	Max	Min	Max	Min	Max	
t _{wc}	Write cycle time	100		120		150		ns
t _{as}	Address set-up time	0		0		0		ns
t _{ah}	Address hold time	60		60		60		ns
t _{ds}	Data set-up time	50		50		50		ns
t _{dH}	Data hold time	10		10		10		ns
t _{wRR}	Write recovery time before read	6		6		6		μs
t _{rrw}	Read recovery time before write	0		0		0		μs
t _{cs}	Chip enable set-up time before write	20		20		20		ns
t _{ch}	Chip enable hold time	0		0		0		ns
t _{wP}	Write pulse width	60		60		60		ns
t _{owP}	Optional write pulse width	70		70		70		ns
t _{wPH}	Write pulse width high	20		20		20		ns
t _{DP}	Duration of programming operation	10		10		10		μs
t _{DE}	Duration of erase operation	9.5		9.5		9.5		ms
t _{vsc}	V _{PP} set-up time to chip enable low	1		1		1		μs

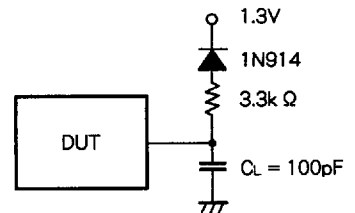
Note 5: Read timing parameters during read/write mode are the same as during read-only mode.
V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC WAVEFORMS FOR READ OPERATIONS



TEST CONDITIONS FOR AC CHARACTERISTICS

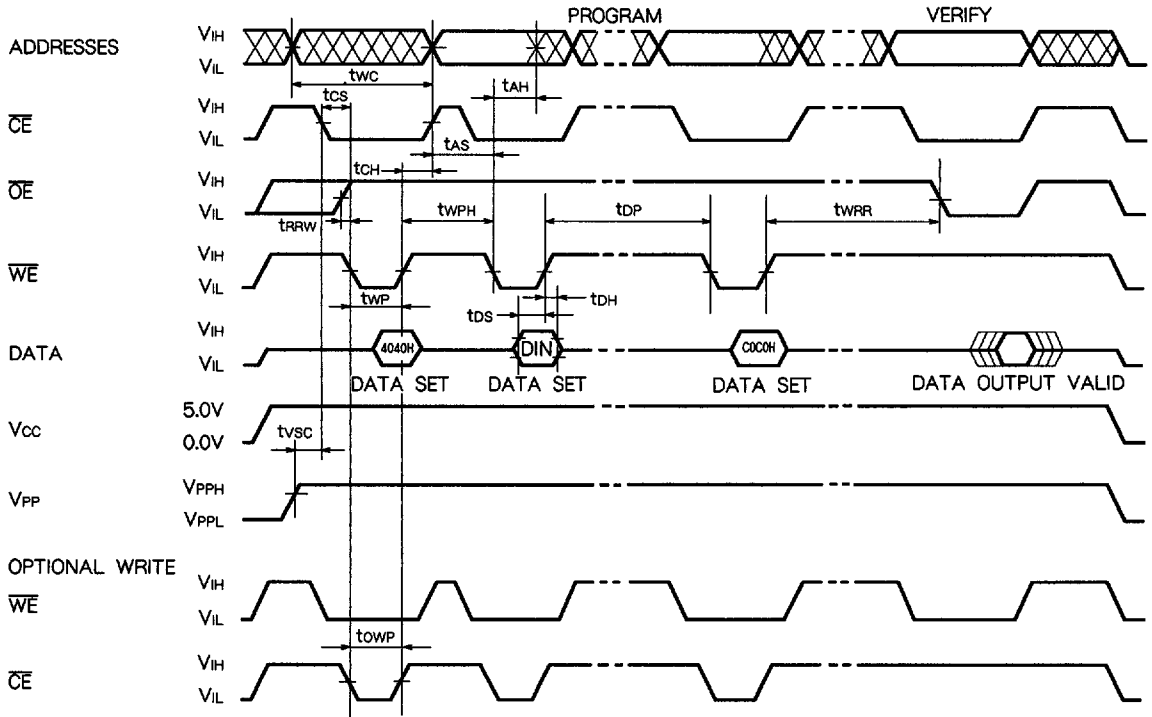
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
 Input rise and fall times: ≤ 10ns
 Reference voltage at timing measurement: 1.5V
 Output load: 1TTL gate + C_L (= 100pF)
 or



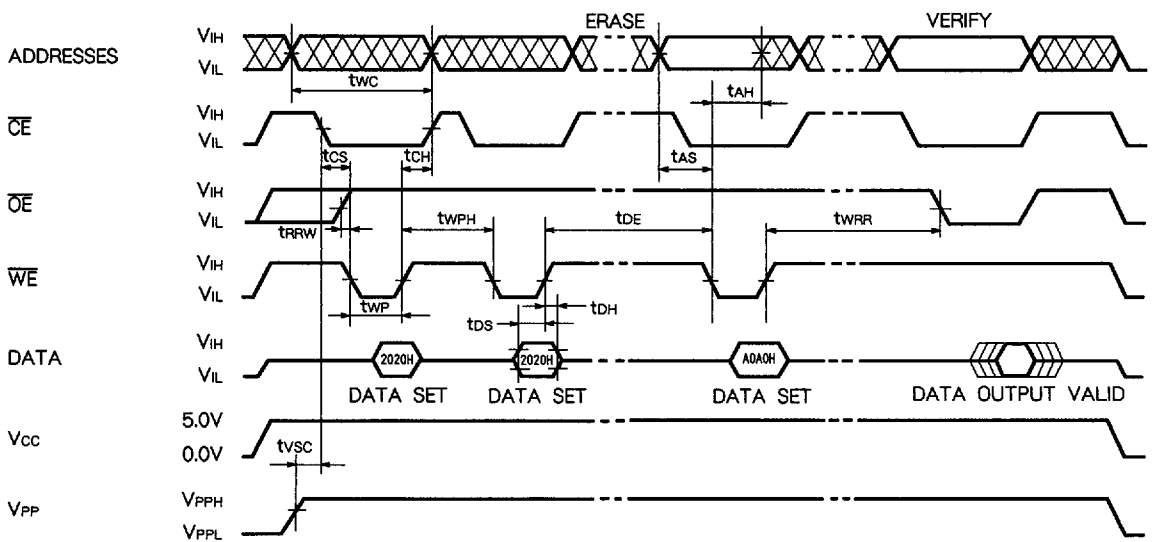
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AC WAVEFORMS FOR PROGRAM OPERATIONS



AC WAVEFORMS FOR ERASE OPERATIONS



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PROGRAMMING AND ERASE ALGORITHM FLOW CHART

PROGRAM :

ERASE :

