D2472, APRIL 1986 – REVISED DECEMBER 1989

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Stand-by Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN55501C, SN55501D**

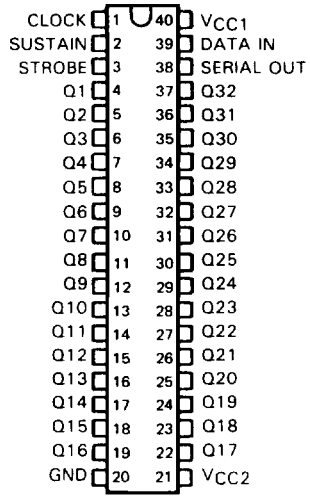
description

The SN55501E is a monolithic BIDFET† integrated circuit designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. This device has diode-clamped CMOS inputs.

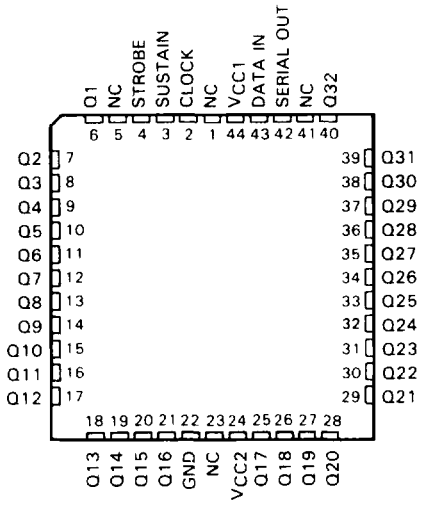
The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is switched low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the SUSTAIN pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low stand-by power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55501E is characterized for operation over the full military temperature range of −55°C to 125°C.

J PACKAGE
(TOP VIEW)



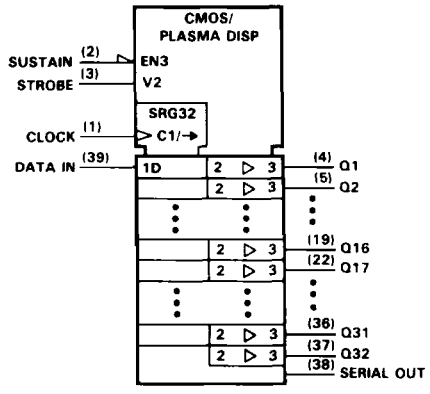
FD OR FJ PACKAGE
(TOP VIEW)



NC – No internal connection

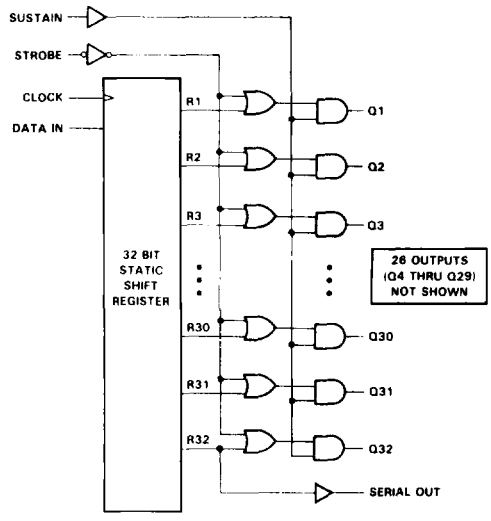
†BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

functional block diagram (positive logic)



FUNCTION TABLE

FUNCTION	INPUTS				OUTPUTS						
					SHIFT REGISTER			SERIAL			
	DATA	CLOCK	STROBE	SUSTAIN	R1	R2	R3...R32	DATA	Q1	Q2	Q3....Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$...$R31_n$	$R32_n$	H	H	H....H
	L	↑	H	H	L	$R1_n$	$R2_n$...$R31_n$	$R32_n$	H	H	H....H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	H	H	H....H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	R1	R2	R3....R32
SUSTAIN	X	X	X	L	$R1_n$	$R2_n$	$R3_n$...$R32_n$	$R32_n$	L	L	L....L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
R1...R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$...$R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the CLOCK input.

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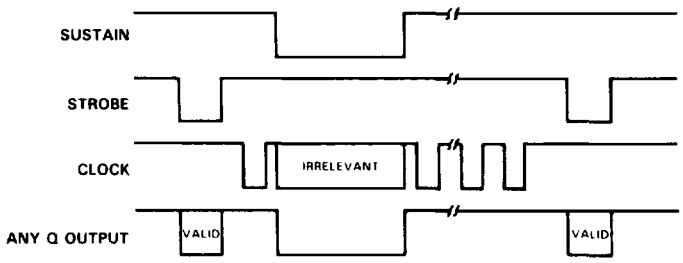
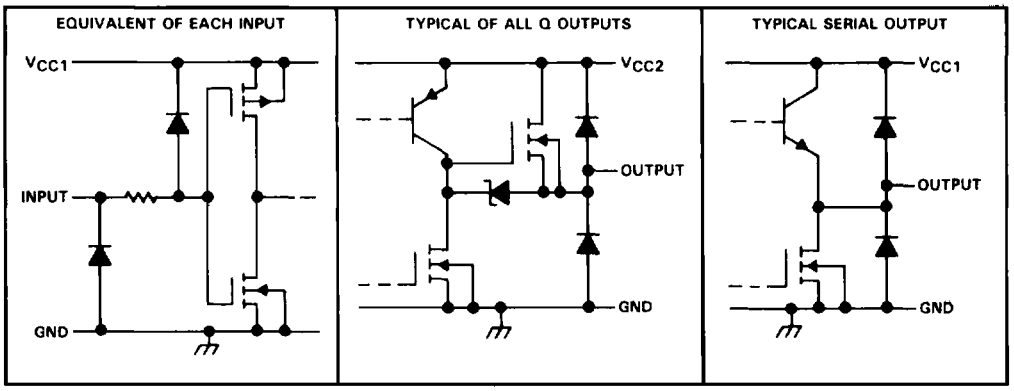
typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 100 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FD or FJ package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 125°C$ POWER RATING
FD or FJ	1825 mW	14.6 mW/°C	25°C	365 mW
J	1825 mW	22.0 mW/°C	67°C	550 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	V
High-level input voltage, V_{IH}		0.75 V_{CC1}			
Low-level input voltage, V_{IL}				0.25 V_{CC1}	
Peak high-level Q output current, I_{OH}				−20	mA
Peak low-level Q output current, I_{OL}				20	mA
High-level Q output clamp current, I_{OKH}				20	mA
Low-level Q output clamp current, I_{OKL}				−20	mA
Clock frequency, f_{clock}, at or below, 25°C junction temperature (see Note 2)		0		8	MHz
Duration of high or low clock pulse, t_w		62			ns
Setup time, t_{su}	Data inputs before CLOCK↑	20			ns
Hold time, t_h	Data hold time after CLOCK↑	50			ns
	STROBE high after CLOCK↑	150			
	STROBE high after SUSTAIN↑	250			
Operating free-air temperature, T_A		−55		125	°C
Operating case temperature, T_C				125	

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above T_J = 25°C.

electrical characteristics over recommended operating temperature range

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = 12 mA		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		V
				I_{OH} = −10 mA	92	94.5		
				I_{OH} = −15 mA	90	93.5		
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2	V
				I_{OL} = 10 mA		2	4	
				I_{OL} = 15 mA		2.75	5	
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1	
V_{OK}	Output clamp voltage	Q outputs	V_{CC2} = 0	I_{OK} = 20 mA		1	2.5	V
				I_{OK} = −20 mA		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IH} = V_{IH}min,			1	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IL} = V_{IL}max,			−1	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	V_{CC2} = 100 V‡		0.05	1	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 13.2 V, V_{CC2} = 100 V	Outputs low		0.1	1	mA
				Outputs high		1	5	

†Typical values are at V_{CC1} = 12 V, T_A = 25°C.
‡Measure with inputs at V_{CC1} and again with inputs at GND.

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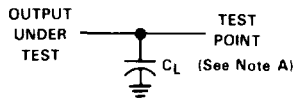
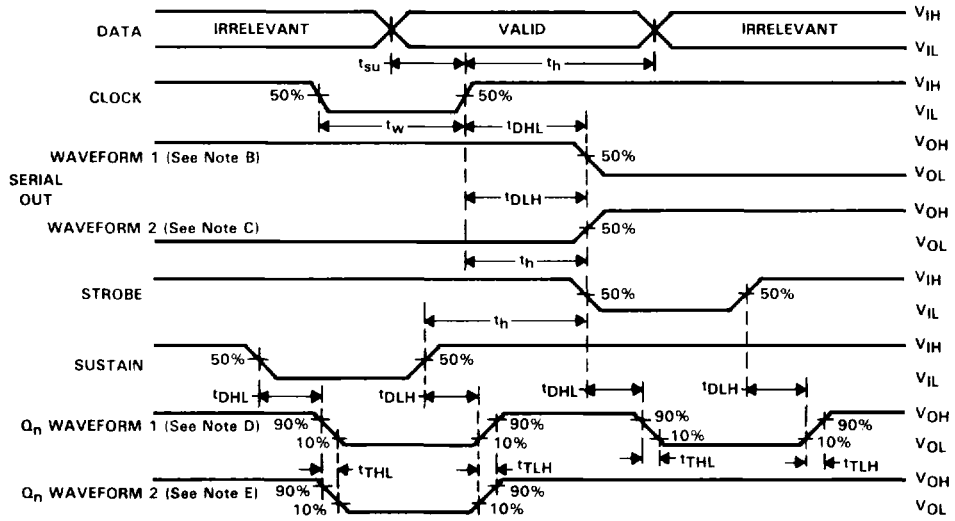
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level outputs	STROBE to Q outputs	C_L = 30 pF			250	ns
		SUSTAIN to Q outputs	C_L = 30 pF			250	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{DLH}	Delay time, low-to-high-level outputs	STROBE to Q outputs	C_L = 30 pF			450	ns
		SUSTAIN to Q outputs	C_L = 30 pF			450	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{THL}	Transition time, high-to-low-level Q output		C_L = 30 pF			200	ns
t_{TLH}	Transition time, low-to-high-level Q output		C_L = 30 pF			300	ns

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.
B. Serial out waveform for internal conditions such that a low is registered in R32.
C. Serial out waveform for internal conditions such that a high is registered in R32.
D. Q_n output with a low stored in associated register R_n.
E. Q_n output with a high stored in associated register R_n.

VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

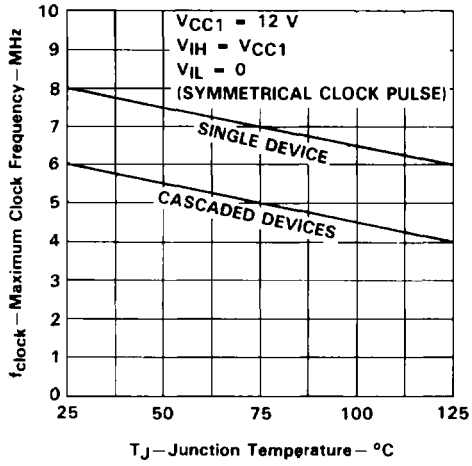


FIGURE 2

INPUT VOLTAGE LOGIC LEVEL LIMITS
vs
V_{CC1} SUPPLY VOLTAGE

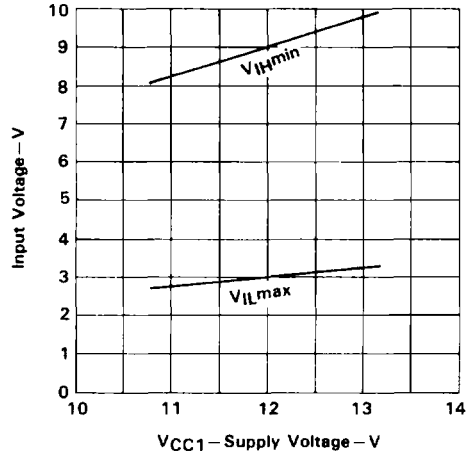


FIGURE 3

THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$
FD or FJ	68°C/W	20°C/W
J	45°C/W	12°C/W

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