Am9310/9316

BCD Decade Counter/Four-Bit Binary Counter

010038

Distinctive Characteristics:

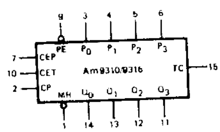
- Fully synchronous counting and parallel loading
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.

FUNCTIONAL DESCRIPTION

The Am9310 and Am9316 are four-bit synchronous up-counters. The 9310 is a modulo 10 counter and the 9316 is a hexadecimal counter. Each counter contains four master-slave flip-flops driven by a common clock input (CP). When CP is LOW, data is entered into the masters of the flip-flops. If the Parallel enable ($\overline{PE}$) is HIGH, then data is entered into each master from the slaves of the other flip-flops via J and K type inputs. If $\overline{PE}$ is LOW, then data is entered into the masters via the D-type parallel inputs (P_0, P_1, P_2, P_3). When the clock changes from LOW to HIGH, the data in the masters is transferred to the slaves and the outputs (Q_0, Q_1, Q_2, Q_3). The masters are inhibited from change as long as the clock is HIGH. In the count mode ($\overline{PE}$ HIGH), there are two count enables, count enable parallel (CEP) and count enable trickle (CET). Both must be HIGH for counting to occur. The terminal count state of each device (9 for the 9310 and 15 for the 9316) is decoded and ANDed with the CET input to produce a terminal count output (TC). Long synchronous counter systems are constructed by connecting the TC output of the first counter to the CEP inputs of all other counters and the TC output of each counter after the first to the CET input of the next counter. Both counters have an asynchronous master reset ($\overline{MR}$) which clears all four flip-flops independent of any other inputs.

For proper operation, the $\overline{PE}$ input must not change from LOW to HIGH during the clock LOW time unless the P_i inputs are identical to the Q_i outputs. If CEP and CET are both HIGH at any time during the clock LOW time, (and $\overline{PE}$ is HIGH), then the count will increment when the clock goes HIGH.

LOGIC SYMBOL

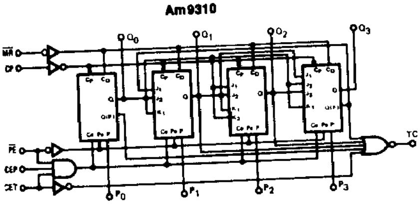


V_{CC} = PIN 16
GND = PIN 8

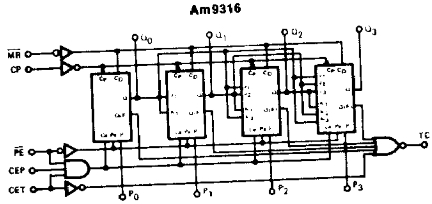
The basic cell for the Am9310/9316 is illustrated in Figure 8

LOGIC DIAGRAMS

Am9310



Am9316



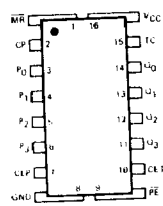
Am9310 ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am9310	Molded DIP	0°C to +75°C	U6M931059X
Am9310	Hermetic DIP	0°C to +75°C	U7B931059X
Am9310	Hermetic DIP	−55°C to +125°C	U7B931051X
Am9310	Hermetic Flat Pak	−55°C to +125°C	U4L931051X
Am9310	Dice	Note	UXX9310XXD
Am9316	Molded DIP	0°C to +75°C	U6M931659X
Am9316	Hermetic DIP	0°C to +75°C	U7B931659X
Am9316	Hermetic DIP	−55°C to +125°C	U7B931651X
Am9316	Hermetic Flat Pak	−55°C to +125°C	U4L931651X
Am9316	Dice	Note	UXX9316XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM

Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am931059X/ Am931659X $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 5\%$
Am931051X/ Am931651X $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.8$ mA $V_{IN} = V_{IH}$ or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 16.0$ mA $V_{IN} = V_{IH}$ or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4$ V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V		−20		−80	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am931051X Am931651X		65	100	mA
			Am931059X Am931659X		65	94	

Notes: 1) Typical Limits are at $V_{CC} = 5.0$ V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay—Q Outputs	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 1)	10	20	30	ns
t_{pd-}	Turn On Delay—Q Outputs		7	15	25	ns
t_{pd+}(TC)	Turn Off Delay TC		17	35	50	ns
t_{pd-}(TC)	Turn On Delay TC		10	20	30	ns
t_s(CE)	Set-up Time CEP or CET	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 2)	0	13	30	ns
t_s(P)	Set-up Time P-Inputs	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 3)	0	18	38	ns
$t_s(\overline{PE})$	Set-up Time $\overline{PE}$		7	29	45	ns
$t_{pd-}(\overline{MR})$	Turn-on Delay for $\overline{MR}$	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 1)	15	33	48	ns
t_{pd+}(CET to TC)	Turn Off Delay for CET to TC	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 4)	7	14	30	ns
t_{pd-}(CET to TC)	Turn On Delay for CET to TC		7	14	30	ns
f_c	Count Frequency	$V_{CC} = 5.0$ V, $C_L = 15$ pF	20	28		MHz

DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

FUNCTIONAL TERMS:

Asynchronous (ripple) Counter All outputs (flip flops) change state on command from a preceding stage.

C_D Input Asynchronous direct clear input.

CEP Input The count mode is inhibited by a LOW input. Outputs TC, Q_0, Q_1, Q_2 and Q_3 remain unchanged. Refer to Truth Table II.

CET Input The count mode is inhibited and Terminal Count (TC) output is forced LOW by a LOW input. Outputs Q_0, Q_1, Q_2 and Q_3 remain unchanged. Refer to Truth Table II.

Fan-Out The logic HIGH or LOW output drive capability in terms of input Unit Loads.

Input Unit Load One T²L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

JK Flip Flop Properties similar to an RS Flip Flop except that J = K = 1 is allowed. Refer to Truth Table I.

J, K Inputs The logic inputs for setting the JK flip flop of the register. Refer to Table I.

$\overline{MR}$ Input The master reset input.

$\overline{PE}$ Input The input for selection of parallel data entry to the register. Parallel Enable (PE) LOW allows parallel data entry.

P_0, P_1, P_2, P_3 Inputs The inputs for data entry into the four synchronous clocked JK Flip Flops. Refer to Table II.

Q_0, Q_1, Q_2, Q_3 Outputs The four outputs of the 9310/9316 register flip flops.

Q_i (t_n) The output after the n'th clock pulse.

Q_i (t_{n+1}) The output after the (n+1) clock pulse.

Synchronous Counter All outputs (flip flops) change state on command from the clock.

Terminal Count The highest number a counter can attain when operated in the count mode.

TC Output This output is HIGH when CET is HIGH and the counter is at terminal count. The output is LOW when CET is LOW or the counter not at terminal count.

OPERATIONAL TERMS:

I_{FH} Forward input load current for unit input load.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_{IL} Reverse input load current with V_{IL} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 6.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 6.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

CP Clock Pin, pulsed. The subscript, if any, refers to pulse waveshape.

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition. Refer to Figure 1.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition. Refer to Figure 1.

t_{pd-}($\overline{MR}$) The propagation delay from the master reset signal HIGH-LOW transition to the TRUE output signal HIGH-LOW transition. Refer to Figure 4.

t_{pd+}(CET to TC) The propagation delay from the CET input LOW-HIGH transition to the TC output LOW-HIGH transition. Refer to Figure 5.

t_{pd-}(CET to TC) The propagation delay from the CET input HIGH-LOW transition to the TC output HIGH-LOW transition. Refer to Figure 5.

t_{pd+}(TC) The propagation delay from the clock signal LOW-HIGH transition to the TC output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(TC) The propagation delay from the clock signal LOW-HIGH transition to the TC output HIGH-LOW transition. Refer to Figure 1.

t_s (CE) The set-up time of the count enable inputs (CET or CEP) relative to either edge of the clock. To inhibit counting, one of the count enables must be LOW by t_s (CE) max before the clock goes LOW and must remain LOW until after t_s (CE) min before the clock goes HIGH. To enable counting, both of the count enables must be HIGH before t_s (CE) max before the clock goes HIGH.

t_s (P) The set-up time for data on the P inputs, relative to the clock LOW to HIGH transition. In order to correctly load data into the counter, the P inputs must be steady between t_s (P) max and t_s (P) min before the clock goes HIGH.

t_s ($\overline{PE}$) The set-up time on the parallel enable input. To load data from the P inputs into the counter, the parallel enable must be LOW by t_s ($\overline{PE}$) max before the clock goes HIGH and must remain LOW until after t_s ($\overline{PE}$) min before the clock goes HIGH.

SWITCHING TIME WAVEFORMS

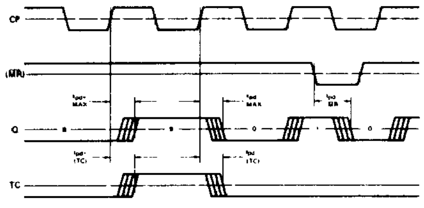


Figure 1

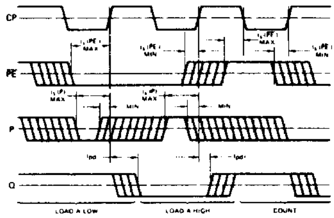


Figure 3

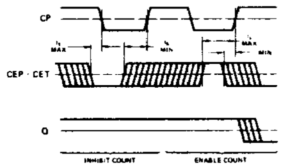


Figure 2

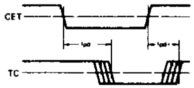


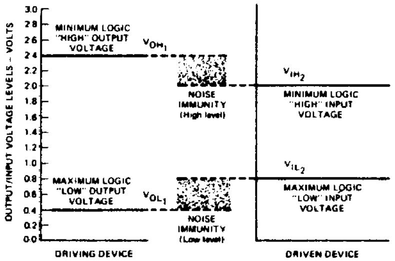
Figure 4

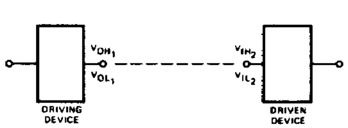
Switching tests are performed with CP input driven by a TTμL9002 gate and the outputs loaded by 15 pF capacitance to include jig capacitance. All unused inputs are tied to V_{CC}. The pulse generator driving the TTμL9002 is set up in the following condition:

Rise Time <15 ns
Fall Time <15 ns
Amplitude ~4 V
Frequency = 2 MHz ±5% at 50% duty cycle

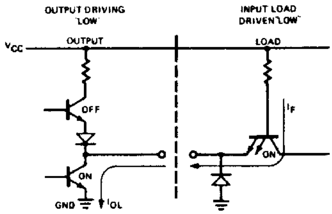
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

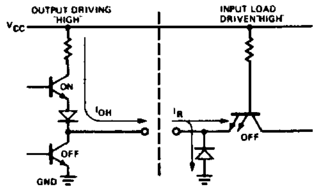




Current Interface Conditions — LOW

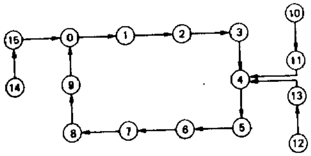


Current Interface Conditions — HIGH

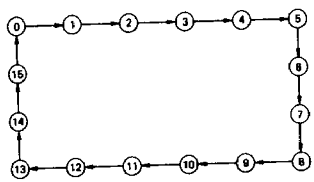


Am9310/16 STATE DIAGRAMS

Am9310



Am9316



The state diagrams show the count sequence after the counters are preset to any one of the sixteen possible states.

Figure 7

Am9310/16 LOADING RULES (in unit loads)

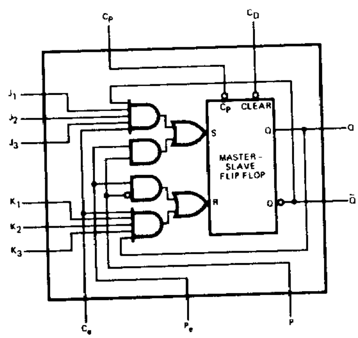
Input/Output	Pin No.'s	Input Unit Load	Output Drive (note) Output HIGH	Output LOW
$\overline{MR}$	1	1	—	—
CP	2	2	—	—
P_0	3	2/3	—	—
P_1	4	2/3	—	—
P_2	5	2/3	—	—
P_3	6	2/3	—	—
CEP	7	1	—	—
GND	8	—	—	—
$\overline{PE}$	9	2	—	—
CET	10	2	—	—
Q_3	11	—	20	10
Q_2	12	—	20	10
Q_1	13	—	20	10
Q_0	14	—	20	10
TC	15	—	20	10
V_{CC}	16	—	—	—

Note: 10 loads are allowed on any output, but the total number of loads on all outputs must not exceed 30. A unit load is defined as 40μA at 2.4V and 1.6mA at 0.4V

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am9310/16 BASIC CELL



This basic cell illustrates how data is entered and controlled internally. Count enable gating is also shown.

Figure 8

TRUTH TABLES

Mode Selection

CEP	CET	$\overline{PE}$	Mode
H	H	H	Count
L	X	H	Count Inhibited
X	L	H	Count Inhibited
X	X	L	Presetting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE II

JK Flip Flop

J	K	Q_0 (tn+1)
L	L	Q_0(tn) No change
L	H	L
H	L	H
H	H	$\bar{Q}_0$(tn) Toggle

$J = J_1 \bullet J_2 \bullet J_3$
$K = K_1 \bullet K_2 \bullet K_3$

TABLE I

MULTI-STAGE SYNCHRONOUS COUNTER

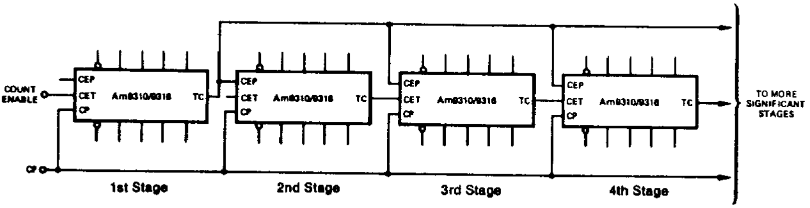


Figure 9

Am9310/9316 APPLICATION

Counter stages can be cascaded, as shown above, to provide multiple stage BCD or Binary synchronous counting by using the 9310 or the 9316 respectively. With a TC fan-out of six the above scheme allows seven stages to operate at the maximum frequency equivalent to a two stage counter.

Each stage is enabled for counting when both its CEP and CET inputs are HIGH. CEP of subsequent stages are HIGH when the first stage is at Terminal Count. CET of a stage is HIGH when all of its preceding stages (first stage not included) are at Terminal Count.

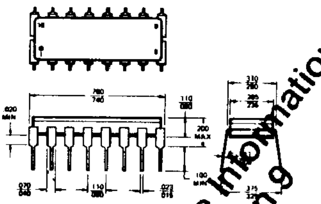
This indicates that CET_n is enabled by TC_{n-1}. TC_{n-1} in turn is HIGH when CET_{n-1} is enabled. CET_{n-1} is enabled by TC_{n-2}, until the second stage, where the CET_2 is always open (HIGH). This TC/CET look ahead ripple is initiated when the second stage reaches Terminal Count and must arrive at the CET input of the last stage before the first stage reaches Terminal Count again. This will happen ten clock pulses (sixteen for the 9316) after the look ahead ripple is initiated.

A multi stage counter as illustrated above can operate at a typical clock frequency of 20 MHz.

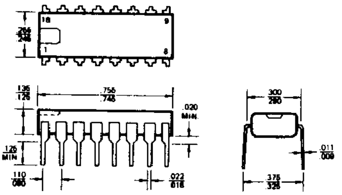
PHYSICAL DIMENSIONS

Dual-In-Line

Hermetic

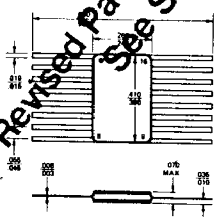


Molded



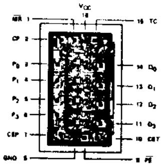
Revised Package Information
See Section 9

Flat Package



Metallization and Pad Layout

74 x 124 Mils



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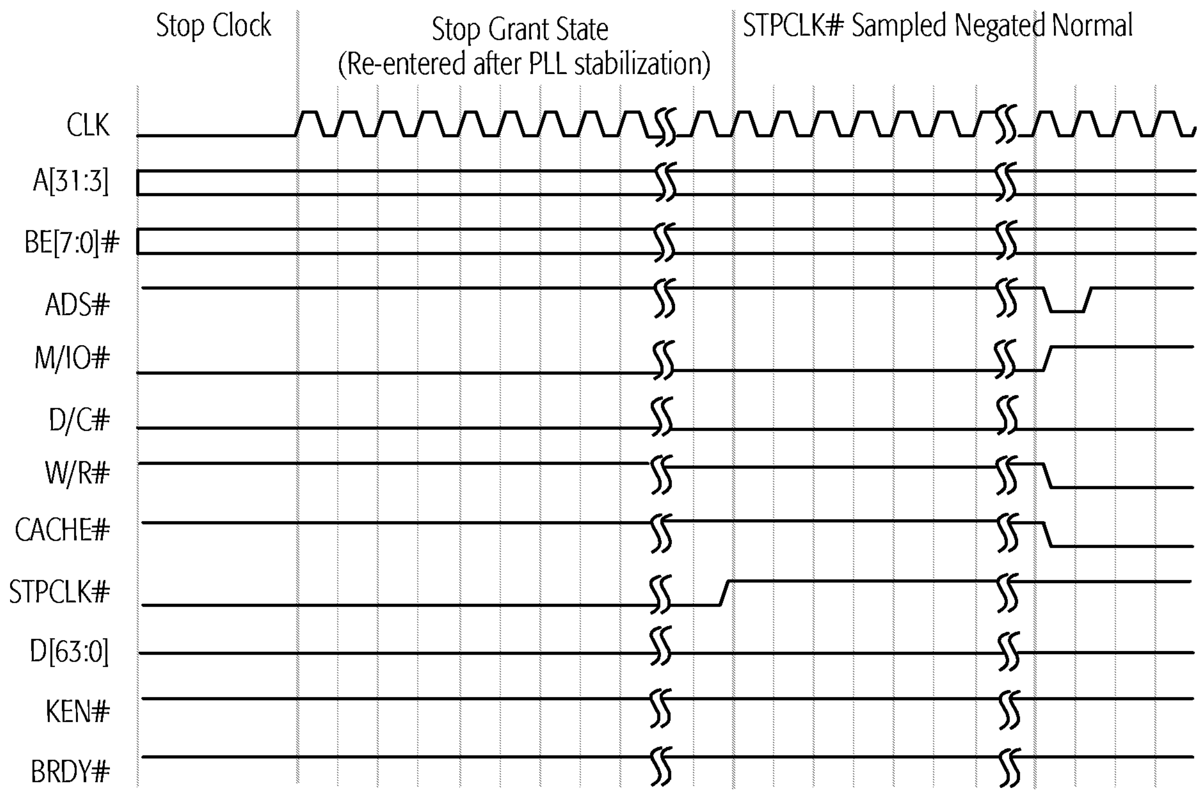

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

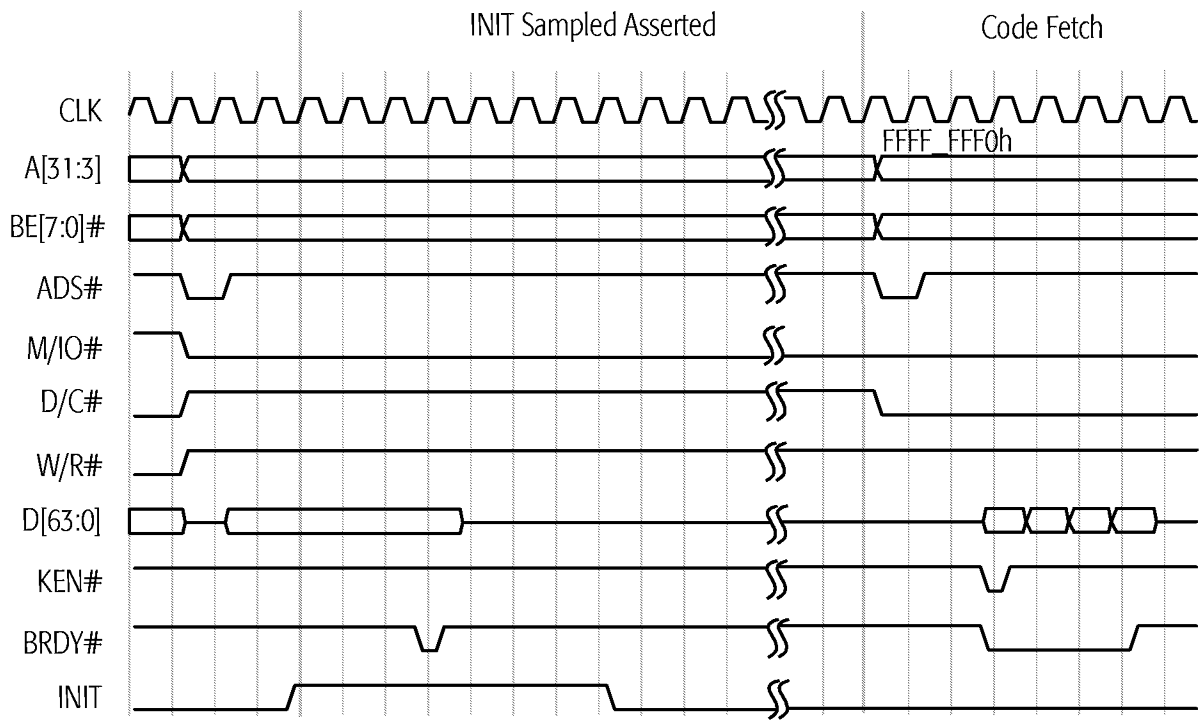

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.