

PM8621

NSE-8G

Narrowband Switch Element

Data Sheet

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Table of Contents

Legal Information	2
Copyright	2
Disclaimer	2
Trademarks	2
Patents	2
Contacting PMC-Sierra	3
Revision History	4
Table of Contents	5
List of Registers	7
List of Figures	9
List of Tables	11
1 Features	12
2 Applications	13
3 References	14
4 Application Examples	15
5 Block Diagram	18
6 Description	20
7 Ball Diagram	21
8 Pin Description	25
9 Functional Description	38
9.1 LVDS Overview	38
9.2 Receive 8B/10B Frame Aligner (R8TD)	40
9.3 Transmit 8B/10B Encoder (T8TE)	41
9.4 DS0 Cross Bar switch (DCB)	47
9.5 Clock Synthesis and Transmit Reference Digital Wrapper (CSTR)	48
9.6 Fabric Latency	48
9.7 JTAG Support	48
9.8 Microprocessor Interface	49
9.9 In-band Link Controller (ILC)	49
9.10 Microprocessor Interface	51
10 Normal Mode Register Description	55
11 Test Features Description	125
11.1 JTAG Test Port	125

12	Operation	131
12.1	Software Default settings	131
12.2	“C1” Synchronization.....	132
12.3	Synchronized Control Setting Changes	133
12.4	NSE CPU Interaction With the Switching Cycle When Using the ILC	139
12.5	Controlling Frame Alignment in the Receive Port	140
12.6	DS0 Cross-Bar Switch (DCB) Operation.....	141
12.7	Telecombus Mode Operation	143
12.8	SBI Column Mode Operation	144
12.9	SBI DS0 Mode Operation.....	144
12.10	SBI DS0 with CAS Mode Operation.....	144
12.11	Using the Inband Link Controller (ILC).....	145
12.12	Switch Setting Algorithm	148
12.13	JTAG Support.....	148
13	Functional Timing.....	153
13.1	Receive Interface Timing.....	153
13.2	Transmit Interface Timing.....	154
14	Absolute Maximum Ratings	156
15	Power Information.....	158
15.1	Power Requirements.....	158
15.2	Power Sequencing	158
15.3	Analog Power Filtering Recommendations.....	159
16	D.C. Characteristics	160
17	Microprocessor Interface Timing Characteristics.....	162
18	A.C. Timing Characteristics.....	165
18.1	Input Timing.....	165
18.2	Reset Timing	166
18.3	Serial SBI Bus Interface	167
18.4	JTAG Port Interface.....	167
19	NSE-8G Ordering and Thermal Information	168
19.1	Packaging Information	168
19.2	Thermal Information	168
20	Mechanical Information.....	170
20.1	480 Pin UBGA -35x35mm Body - (B Suffix).....	170
	Notes	171

List of Registers

Register 000H: NSE Master Reset.....	56
Register 001H: NSE Individual Channel Reset.....	57
Register 002H: NSE Master JTAG ID	58
Register 003H: NSE In-Band Link Transmit Page Bit 0	59
Register 004H: NSE In-Band Link Transmit Page Bit 1	60
Register 005H: NSE Master Interrupt Source	61
Register 006H: NSE Master ILC Interrupt Source	63
Register 007H: NSE Master R8TD Interrupt Source.....	64
Register 008H: NSE Master T8TE Interrupt Source	65
Register 009H: NSE Master Clock Monitor, Accumulation Trigger.....	66
Register 00AH: NSE DCB CMP select.....	67
Register 00BH: NSE Interrupt Enable Register	68
Register 00CH: NSE Subsystem Interrupt Enable Register	69
Register 00DH: NSE R8TD TIP Register	70
Register 00EH: NSE In-Band Link Transmit User Bit 0	71
Register 00FH: NSE In-Band Link Transmit User Bit 1.....	72
Register 010H: NSE In-Band Link Transmit User Bit 2.....	73
Register 011H: NSE FREE User Register	74
Register 012H: Correct R8TD_RX_C1 Pulse Monitor	75
Register 013H: Unexpected R8TD_RX_C1 Interrupt.....	76
Register 014H: Missing R8TD_RX_C1 Interrupt.....	77
Register 015H: Unexpected R8TD_RX_C1 Interrupt Enable	78
Register 016H: Missing R8TD_RX_C1 Interrupt Enable	79
Register 017H: R8TD C1 Disable	80
Register 020H, 024H: CSTR #1, #2 Control	81
Register 021H, 025H: CSTR #1, #2 Interrupt Enable and CSU Lock Status.....	82
Register 022H, 026H: CSTR #1, #2 Interrupt Indication.....	83
Register 044H: DCB Configuration Port 11-6 Register	84
Register 045H: DCB Configuration Port 5-0 Register	86
Register 046H: DCB Configuration Output Register	88
Register 047H: DCB Access Mode Register.....	89
Register 048H: DCB C1 delay (RC1DLY) Register	92
Register 04AH: DCB Frame size Register	93

Register 04CH: DCB Configuration Register	94
Register 04DH: DCB Interrupt Status Register	97
Register 100H + N*20H, R8TD Control and Status	98
Register 101H + N*20H, R8TD Interrupt Status.....	100
Register 102H + N*20H, R8TD Line Code Violation Count	102
Register 103H + N*20H, RXLV and DRU Control.....	103
Register 108H + N*20H, T8TE Control and Status	104
Register 109H + N*20H, T8TE Interrupt Status	106
Register 10AH + N*20H: T8TE Time-slot Configuration #1	107
Register 10BH + N*20H: T8TE Time-slot Configuration #2	109
Register 10CH + N*20H, T8TE Test Pattern.....	110
Register 10DH + N*20H, TXLV and PISO Control.....	111
Register 110H + N*20H, ILC Transmit FIFO Data	112
Register 111h + N*20H, ILC Transmit Control Register	113
Register 112h + N*20H, ILC Transmit Misc.Status and FIFO Synch Register	114
Register 113h + N*20H, ILC Receive FIFO Data Register	116
Register 114h + N*20H, ILC Receive Control Register	117
Register 115h + N*20H, ILC Receive Auxiliary, Status and FIFO Synch Register.....	118
Register 116h + N*20H, ILC Interrupt Enable and Control Register.....	122
Registers: 117h + N*20H, ILC Interrupt Reason Register	124

List of Figures

Figure 1	Voice/Media Gateway DS0 TDM Switch Fabric Solution	15
Figure 2	OC-48 T1/E1 ADM (Individually Drop/Add any T1/E1 in STS-48).....	16
Figure 3	DS0/T1/E1/VT/TU/STS-1-Capable OC-48/STM-12 Any-Service-Any- Port (ASAP) Architecture	17
Figure 4	NSE-8G Block Diagram	19
Figure 5	NSE UBGA-480 Ball Diagram (Bottom-View).....	21
Figure 6	Generic LVDS Link Block Diagram	38
Figure 7	Character Alignment State Machine	45
Figure 8	Frame Alignment State Machine.....	46
Figure 9	In-Band Signaling Channel Message Format	50
Figure 10	In-Band Signaling Channel Header Format	50
Figure 11	Input Observation Cell (IN_CELL)	129
Figure 12	Output Cell (OUT_CELL)	129
Figure 13	Bidirectional Cell (IO_CELL)	130
Figure 14	Layout of Output Enable and Bidirectional Cells.....	130
Figure 15	Shutting down a link	132
Figure 16	“C1” Synchronization Control	133
Figure 17	Temux84/SBS/NSE/SBS/AALIGATOR32 system DS0 Switching with CAS	135
Figure 18	CAS Multiframe Timing	135
Figure 19	Switch Timing DSOs with CAS	136
Figure 20	Temux84/SBS/NSE/SBS/FREEDM336 system DS0 Switch no CAS	137
Figure 21	Switch Timing - DSOs without CAS	137
Figure 22	Non DS0 Switch Timing	138
Figure 23	NSE CPU Operation with ILC	140
Figure 24	Boundary Scan Architecture	149
Figure 25	TAP Controller Finite State Machine.....	150
Figure 26	Receive Interface Timing	153
Figure 27	Transmit Interface Timing	154
Figure 28	CMP Timing.....	155
Figure 29	Analog Power Filter Circuit.....	159
Figure 30	Microprocessor Interface Read Timing	162
Figure 31	Microprocessor Interface Write Timing	163
Figure 32	NSE Input Timing	165

Figure 33 RSTB Timing.....	166
Figure 34 JTAG Port Interface Timing.....	167

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List of Tables

Table 1	Pin Descriptions	25
Table 2	SBI336S Character Encoding	41
Table 3	Serial Telecom Bus Character Encoding	43
Table 4	Switching Control RAM Layout.....	47
Table 5	In-band Message Header Fields	50
Table 6	NSE-8G Register Map.....	52
Table 7	TX FIFO Message Level	115
Table 8	RX FIFO Message Level	120
Table 9	RXFIFO Threshold Values	123
Table 10	RXFIFO Timeout Delay	123
Table 11	Instruction Register (Length - 3 bits)	125
Table 12	Identification Register	125
Table 13	Boundary Scan Register	125
Table 14	Absolute Maximum Ratings.....	156
Table 15	Power Requirements	158
Table 16	Analog Power Filters	159
Table 17	D.C Characteristics	160
Table 18	Microprocessor Interface Read Access	162
Table 19	Microprocessor Interface Write Access.....	163
Table 20	NSE Input Timing (Figure 32).....	165
Table 21	RSTB Timing (Figure 33)	166
Table 22	Serial SBI Bus Interface	167
Table 23	JTAG Port Interface (Figure 34).....	167
Table 24	Outside Plant Thermal Information	168
Table 25	Device Compact Model ³	168
Table 26	Heat Sink Requirements	168
Table 27	Outside Plant Thermal Information	169
Table 28	Thermal Resistance vs. Air Flow ³	169
Table 29	Device Compact Model ⁴	169

1 Features

- Implements a Scaleable Bandwidth Interconnect DS0 granularity Space switch.
- Implements a SONET/SDH VT1.5/VT2/TU11/TU12 granularity Space switch for the serial 777.6MHz LVDS telecom bus.
- With the allied SBS device, implements a DS0 granularity Memory-Space-Memory switch.
- Supports 12 STS-12/STM-4 equivalent serial ports via 777.6MHz, 8b/10b encoded LVDS links (each port can be either Serial TeleCombus or Serial SBI336)
- When configured for SBI mode switches DS0 or N*DS0 for all T1 and E1 tributaries and aggregate columns for switching T1, E1, Transparent VT1.5 (TVT1.5), Transparent VT2 (TVT2), DS3 and E3 tributaries.
- When configured for the serial 777.6MHz telecom bus interface switches any SONET/SDH virtual tributary or tributary unit up to STS-1.
- Switching of arbitrary non-standard octet aggregates is supported.
- Unicast, multicast, and broadcast are supported for all switching modes.
- The NSE provides: 7.5Gbps (96,768 DS0s, 4,032 T1s/VT1.5s, 3,024 E1s/VT2s, 144 DS3s/E3s) full-duplex switching.
- The allied SBS and SBSLITE devices support up to four 19.44MHz SBI or one 77.76MHz SBI336 bus which communicate with PMC's SBI device family. Alternatively the SBS and SBSLITE devices support up to four 19.44MHz STS-3 telecom buses or one 77.76MHz STS-12 telecom bus for connection with PMC's SPECTRA family of devices.
- Can be combined in applications with PMC Chess Set devices (TSE and TBS).
- Supports a 32-bit microprocessor interface that is used to configure/control the NSE, to make DS0-granularity switch settings.
- Supports clean error checked 8Mb/s full-duplex, in-band communications channels from the NSE's attached microprocessor to the attached microprocessors of each of the 12 attached SBS336S devices. This channel is used to initialize and control the SBSs, or other such devices, and to implement call-establishment set-up changes.
- Supports JTAG for all non-LVDS signals.
- Requires dual power supplies at 1.8V and 3.3V.
- Packaged as a 480 ball UBGA.
- In conjunction with the SBS or SBSLITE, supports "1+1" and "1:n" fabric redundancy.

2 Applications

- T1/E1 SONET/SDH Cross-connects
- T1/E1 SONET/SDH Add-Drop Multiplexors
- OC-48 Multiservice Access Multiplexors
- Channelized OC-12/OC-48 Any Service Any Port Switches
- Serial backplane board interconnect
- Shelf to Shelf cabled serial interconnect
- Voice Gateways

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10. U.S. Patent No. 4,486,739, P.A. Franaszek and A.X. Widmer, "Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code," December 4, 1984.
11. IEEE Std 1596.3-1996, "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)", Approved March 21, 1996
12. L.R. Ford, D.R. Fulkerson, "Flows in Networks", Maximum Cardinality Matchings in Bipartite Graphs.

4 Application Examples

The voice/media gateways, softswitches and wireless voice gateways (MSC/BSC/BTS) may require a DS0 cross-connect to groom the TDM traffic among the line cards and the voice/data processing cards. Figure 1 illustrates a typical voice/media gateway implementation. An FPGA is required to interconnect the SBI and H-MVIP interfaces on the voice/data processing cards. The code for the FPGA (SHB) is available from PMC-Sierra under the license agreement.

Figure 1 Voice/Media Gateway DS0 TDM Switch Fabric Solution

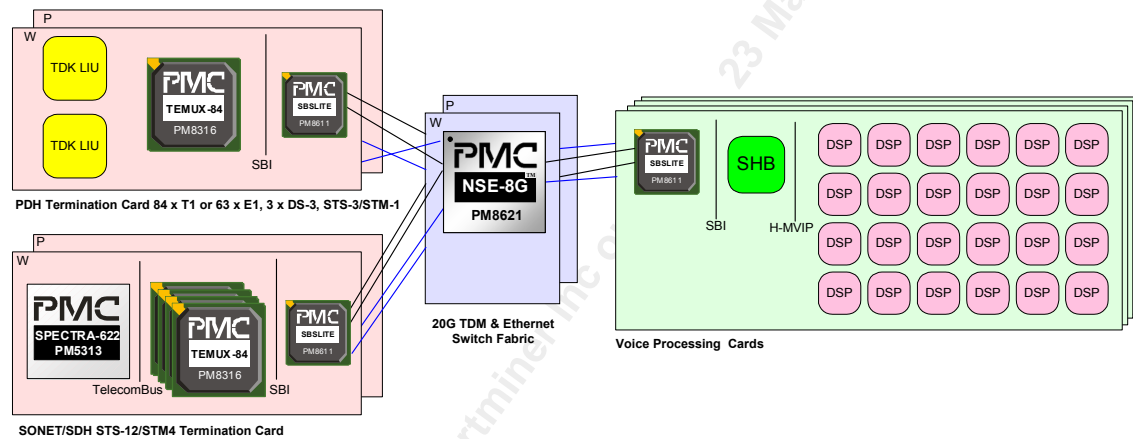


Figure 2 illustrates the possible T1/E1 add/drop multiplexer (ADM) architectures. In this example, the SBSLITE and the NSE-8G operate in the TelecomBus mode. The SBSLITE requires all path pointer justifications to be translated into tributary pointer movements so that J1 is fixed to the location following C1 or H3. The TUPP+622 performs the J1. Switching within the SBSLITE and NSE is utilizing the Transparent Virtual Tributary (TVT), mapping across the SBI336S LVDS links.

Figure 2 OC-48 T1/E1 ADM (Individually Drop/Add any T1/E1 in STS-48)

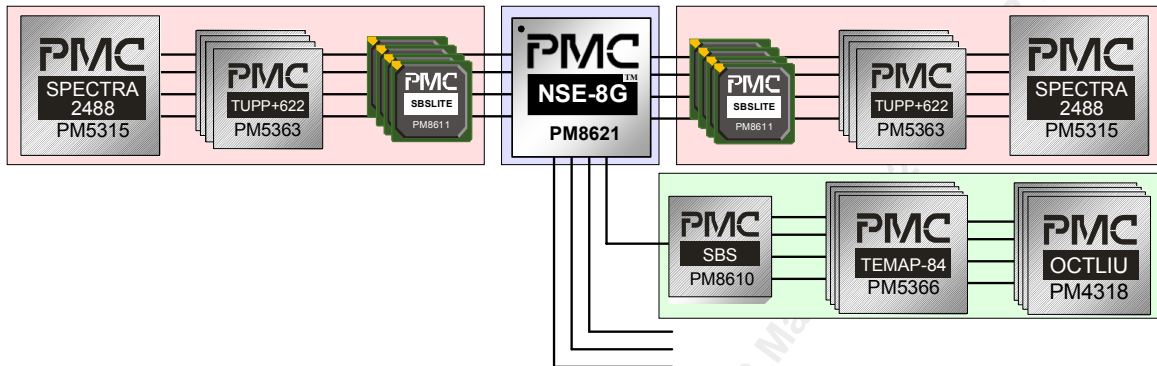
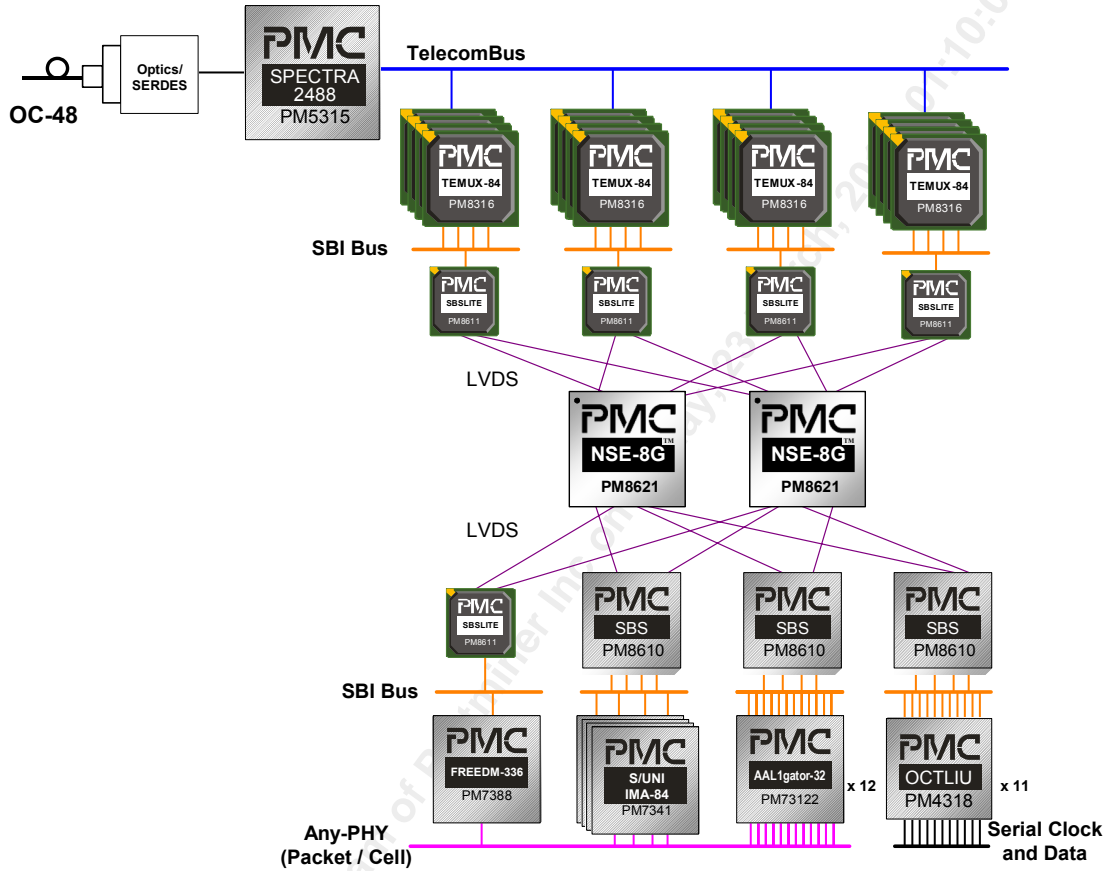


Figure 3 illustrates a DS0/T1/E1/VT/TU/STS-1-capable OC-48/STM-12 Any-Service-Any-Port (ASAP) architecture. The high-capacity optical signals are channellized down to the DS0 level and groomed to a variety of service cards. T1s, E1s, Transparent VTs, E3, DS3 and sub-rate rate links can be switched between the physical layer and layer 2 devices using the SBS, SBSLITE and NSE-8G devices.

Figure 3 DS0/T1/E1/VT/TU/STS-1-Capable OC-48/STM-12 Any-Service-Any-Port (ASAP) Architecture

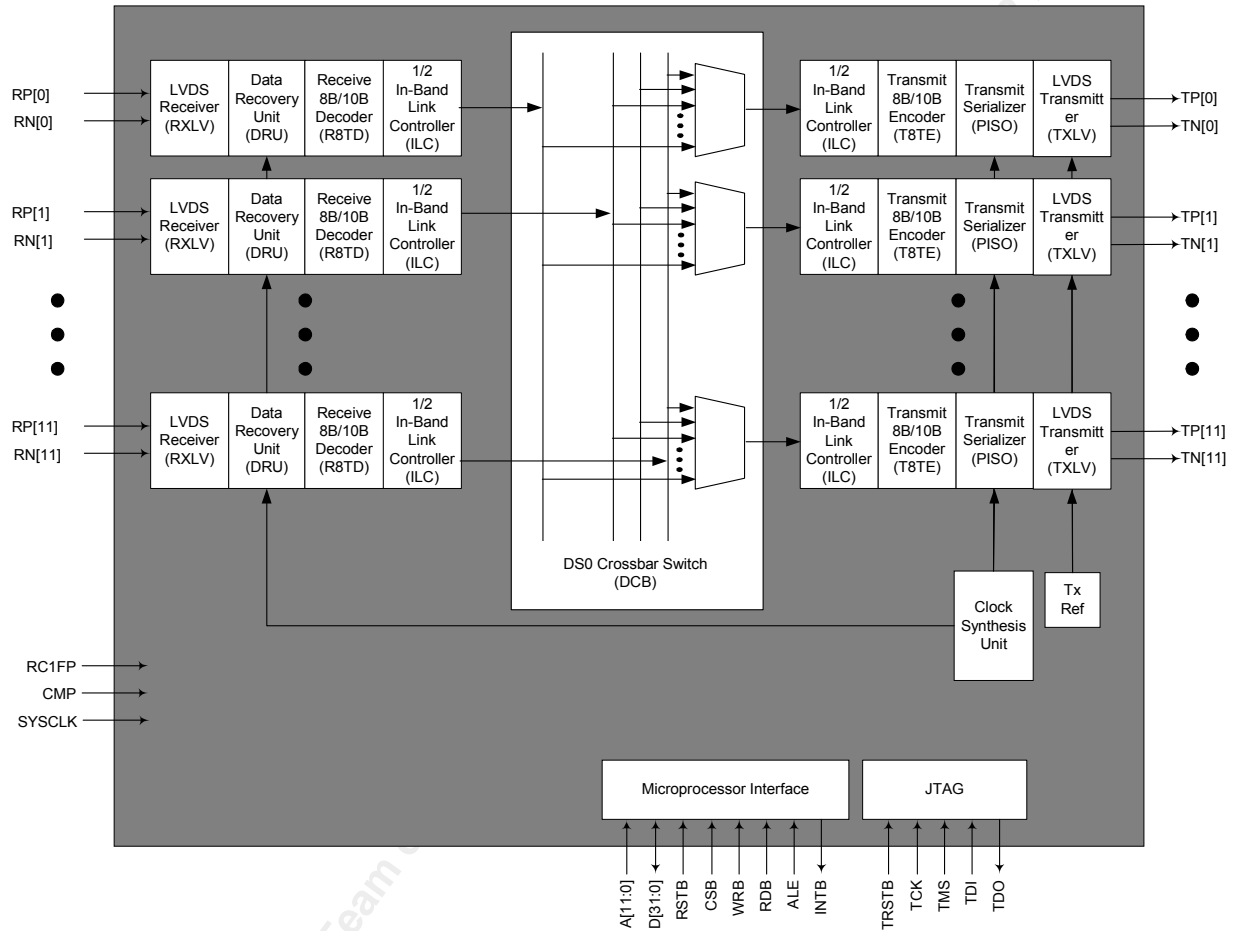


5 Block Diagram

The NSE is organized as a DS0 granularity space switch. Alternatively the NSE is organized as a self-aligning (with respect to STS-12 boundaries in telecom bus mode) VT1.5/VT2 granularity space switch.

1. The R8TD, in combination with the RXLV and DRU receive, decode and align incoming SBI336/STS-12-equivalent LVDS links; outputs are provided to the primary switching flow, and to the in-band signaling channel. These provide all analog and digital functions to terminate a full-duplex 777.6MHz serial SBI336 or 777.6MHz serial telecom bus on LVDS.
2. A 12 X 12 DS0 Crossbar Switch (DCB) stage switches data and control signals between the 12 ports. The switching instructions are stored in two pages of ram configured as offline and online allowing the user to modify the offline page.
3. The T8TE, in combination with the PISO and TXLV perform 8b/10b coding and emits the LVDS bit streams. These provide all analog and digital functions to launch a full-duplex 777.6MHz serial SBI336 bus or 777.6MHz serial telecom bus on LVDS.
4. The microprocessor bus interface and in-band link controllers, (ILCs) provide a clean (error checked) channel between the NSE and SBS or SBSLITEs. This can be used to send messages between the NSE microprocessor-and the SBS microprocessors in a user-defined format. .

Figure 4 NSE-8G Block Diagram



6 Description

The PM8621 NSE-8G is a monolithic CMOS integrated circuits packaged as a 480 ball UBGAs that performs DS0 and above granularity space switching on 12 full duplex SBI336 streams carried as SBI336Sin 8b/10b coding over LVDS at 777.6Mb/s. The NSEs also perform VT1.5/VT2 and above granularity switching on 12 full-duplex STS-12/STM-4 SONET/SDH streams, carried as Serial Telecom bus signals in 8b/10b coding over LVDS at 777.6Mb/s. The NSE-8G is typically used with up to 12 PM8610 SBS or PM8611 SBSLITE devices to provide Memory-Space-Memory switching systems. As each SBS supports either four SBI buses at 19.44MHz or one SBI336 bus at 77.76MHz, the overall system supports any mixture of SBI and SBI336 byte serial buses, ranging from 48 19.44MHz SBI buses to 12 SBI336 77.76MHz buses which does not exceed an aggregate bandwidth of about 7.5Gb/s. In telecom bus mode the SBS devices support the same range of flexibility for 48 19.44MHz and 12 77.76MHz telecom buses at VT1.5/VT2 granularity

Central to the NSE is a cross bar switch, 12 x 12 for the NSE-8G. Every clock cycle the cross bar switches a byte of data with control signals from each input port to an output port. The byte of data may be a DS0 channel from a T1/E1 or may be one byte of a column comprising a T1, E1, DS3, E3, VT1.5, VT2 or STS-1.

In order for switching to take place all input and output streams must be synchronized. This is done via the RC1FP input signal. When switching T1s, E1s, VTs and other higher order units only SBI336 multiframe alignment is required. The same applies for telecom bus mode where only frame alignment is required.

An in-band control link over the serial LVDS interface allows the NSE to communicate with the microprocessors attached to the SBS, SBSLITE or other serial SBI336 devices. The effective bandwidth of each inband link to each device is 8Mb/s. The inband link provides error detection on 32 byte user messages and some near realtime control signals between devices. Using the near realtime control signals the NSE is able to synchronize page switching, indicate switchover between working or protected links and exchange three user defined signals (software) and 8 Auxilliary signals (software). The User and Auxilliary signals can be used to indicate events such as interrupt or handshaking between the end point microprocessors. The message format is left to the user of the devices. The only constraint is that each message has a maximum length of 32 bytes.

7 Ball Diagram

The NSE-8G is packaged in 35mm x 35mm 480 ball UBGA's.

Figure 5 NSE UBGA-480 Ball Diagram (Bottom-View)

Upper Left Corner

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
A	VSS	VSS	VSS	VSS	VDDO	VSS	NC	VSS	NC	VSS	RESERVED	VSS	RESERVED	VSS	RESERVED	VSS	VDDI
B	VSS	AVDH	VDDO	VDDO	VDDO	VDDI	NC	NC	NC	VDDI	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RSTB
C	VSS	AVDH	AVDH	VDDO	VDDI	RESERVED	NC	NC	VDDI	NC	RESERVED	VDDI	RESERVED	RESERVED	RESERVED	RESERVED	VDDI
D	VSS	AVDH	AVDH	AVDH	VDDO	VSS	VDDI	VDDO	NC	NC	RESERVED	VDDO	RESERVED	RESERVED	RESERVED	VDDO	VDDI
E	RESK1	RES1	NC	NC													
F	VSS	NC	NC	AVDL													
G	NC	NC	NC	NC													
H	VSS	NC	NC	AVDH													
J	NC	NC	NC	NC													
K	VSS	NC	NC	VDDI													
L	NC	NC	NC	NC													
M	VSS	NC	NC	AVDH													
N	VDDI	AVDL	NC	NC													
P	VSS	NC	NC	VDDI													
R	NC	NC	NC	NC													
T	NC	NC	CSU_A VDL	CSU_A VDL													
U	NC	NC	CSU_A VDL	CSU_A VDH													

Upper Right Corner

17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

NC	SYSCLK	NC	VSS	NC	VSS	NC	VSS	RESERVED	VSS	RESERVED	VSS	NC	VSS	VSS	VSS	A	
NC	NC	NC	TCK	TMS	NC	VDDI	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NC	VDDO	VDDO	VDDO	VSS	B
TC1FP	NC	VDDI	NC	VDDI	TDI	TDO	NC	RESERVED	RESERVED	RESERVED	RESERVED	VDDI	VDDO	VDDO	AVDH	VSS	C
NC	RC1FP	VDDI	TRSTB	VDDI	VDDO	VDDI	CMP	RESERVED	VDDO	RESERVED	RESERVED	NC	VDDO	AVDH	AVDH	VSS	D
													AVDH	ATB0[1]	AVDH	AVDH	E
													ATB1[1]	TN[0]	TP[0]	VSS	F
													TN[2]	TP[2]	TN[1]	TP[1]	G
													AVDH	VDDI	NC	VSS	H
													RP[0]	RN[0]	TN[3]	TP[3]	J
													VDDI	RP[1]	RN[1]	VSS	K
													VDDI	AVDL	RP[2]	RN[2]	L
													AVDH	RP[3]	RN[3]	VSS	M
													TN[5]	TP[5]	TN[4]	TP[4]	N
													VDDI	TN[6]	TP[6]	VSS	P
													RP[4]	RN[4]	TN[7]	TP[7]	R
													AVDH	VDDI	AVDL	VSS	T
													RP[6]	RN[6]	RP[5]	RN[5]	U

Lower Left Corner

V	NC	NC	NC	NC													
W	VSS	AVDL	VDDI	AVDH													
Y	NC	NC	NC	NC													
AA	VSS	NC	NC	VDDI													
AB	NC	NC	NC	NC													
AC	VSS	NC	NC	AVDH													
AD	NC	NC	AVDL	VDDI													
AE	VSS	NC	NC	VDDI													
AF	NC	NC	NC	NC													
AG	VSS	NC	VDDI	AVDH													
AH	NC	NC	NC	NC													
AJ	VSS	NC	NC	ATB1[2]													
AK	AVDH	AVDH	ATB0[2]	AVDH													
AL	VSS	AVDH	AVDH	VDDO	ALE	NC	VDDI	VDDO	A[6]	A[2]	VDDI	VDDO	D[27]	VDDI	NC	NC	VDDI
AM	VSS	AVDH	VDDO	VDDO	CSB	RDB	VDDI	A[9]	A[5]	A[3]	D[31]	D[29]	VDDI	D[25]	VDDI	D[21]	D[20]
AN	VSS	VDDO	VDDO	VDDO	INTB	WRB	NC	A[10]	A[7]	A[4]	A[0]	D[30]	D[28]	D[26]	NC	D[22]	D[19]
AP	VSS	VSS	VSS	VSS	NC	VSS	A[11]	VSS	A[8]	VSS	A[1]	VSS	NC	VSS	D[24]	D[23]	D[18]
	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18

Lower Right Corner

													CSU_A VDH	CSU_A VDL	RP[7]	RN[7]	V
													CSU_A VDL	CSU_A VDL	TN[8]	TP[8]	W
													TN[9]	TP[9]	TN[10]	TP[10]	Y
													VDDI	TN[11]	TP[11]	VSS	AA
													RP[8]	RN[8]	AVDL	VDDI	AB
													AVDH	RP[9]	RN[9]	VSS	AC
													RP[10]	RN[10]	RP[11]	RN[11]	AD
													VDDI	NC	NC	VSS	AE
													NC	NC	NC	NC	AF
													AVDH	NC	NC	VSS	AG
													NC	NC	NC	NC	AH
													AVDL	NC	NC	VSS	AJ
													NC	NC	RES2	RESK2	AK
D[17]	VDDO	D[13]	D[11]	D[8]	VDDO	D[5]	D[3]	D[0]	VDDO	NC	NC	VDDO	AVDH	AVDH	AVDH	VSS	AL
VDDI	D[15]	VDDI	D[10]	D[9]	D[7]	NC	D[2]	D[1]	NC	NC	NC	NC	VDDO	AVDH	AVDH	VSS	AM
D[16]	D[14]	D[12]	NC	VDDI	D[6]	D[4]	VDDI	NC	NC	NC	NC	VDDO	VDDO	VDDO	AVDH	VSS	AN
NC	VSS	VDDI	VSS	VDDI	VSS	NC	VSS	NC	VSS	NC	VSS	VDDO	VSS	VSS	VSS	VSS	AP
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8 Pin Description

Table 1 Pin Descriptions

Pin Name	Type	Pin No.	Function
LVDS Ports (48 Balls)			
RP[0] RN[0] RP[1] RN[1] RP[2] RN[2] RP[3] RN[3] RP[4] RN[4] RP[5] RN[5] RP[6] RN[6] RP[7] RN[7] RP[8] RN[8] RP[9] RN[9] RP[10] RN[10] RP[11] RN[11]	Analog LVDS Input	J4 J3 K3 K2 L2 L1 M3 M2 R4 R3 U2 U1 U4 U3 V2 V1 AB4 AB3 AC3 AC2 AD4 AD3 AD2 AD1	<p>Receive Serial Data. The differential receive serial data links (RP[11:0]/RN[11:0]) carry the receive SBI336S or SONET/SDH STS-12 frame data from upstream sources in bit serial format. Each differential pair RP[X]/RN[X] carries a constituent SBI336 or STS-12 stream. Data on RP[X]/RN[X] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. All RP[X]/RN[X] differential pairs must be frequency locked and phase aligned (within a certain tolerance) to each other. RP[11:0]/RN[11:0] are nominally 777.6 Mbps data streams.</p> <p>Unused RP[X]/RN[X] pad pairs can be left floating, or can be grounded. In either case the analog blocks (RXLV and the DRU) can be disabled to reduce power consumption. Tying one pin high and the corresponding pin of an input pair low will apply voltage across the internal termination resistor, which will increase system power consumption.</p>
TP[0] TN[0] TP[1] TN[1] TP[2] TN[2] TP[3] TN[3] TP[4] TN[4] TP[5] TN[5] TP[6] TN[6] TP[7] TN[7] TP[8] TN[8] TP[9] TN[9] TP[10] TN[10] TP[11] TN[11]	Analog LVDS Output	F2 F3 G1 G2 G3 G4 J1 J2 N1 N2 N3 N4 P2 P3 R1 R2 W1 W2 Y3 Y4 Y1 Y2 AA2 AA3	<p>Transmit Serial Data. The differential transmit working serial data links (TP[11:0]/TN[11:0]) carry the transmit SBI336S or SONET/SDH STS-12 frame data to a downstream sinks in bit serial format. Each differential pair carries a constituent STS-12 stream. Data on TP[X]/TN[X] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. All TP[X]/TN[X] differential pairs are frequency locked and phase aligned (within a certain tolerance) to each other. TP[11:0]/TN[11:0] are nominally 777.6 Mbps data streams.</p> <p>Unused TP[X]/TN[X] pad pairs should be left floating</p>

Pin Name	Type	Pin No.	Function
NSE-8G Control and Clocking (5 Balls)			
SYCLK	Input	A16	<p>System Clock. The system clock signal (SYCLK) is the master clock for the NSE-8G device. SYCLK must be a 77.76 MHz clock, with a nominal 50% duty cycle.</p> <p>CMP and RC1FP are sampled on the rising edge of SYCLK.</p>
RC1FP	Input	D16	<p>Receive Serial Interface Frame Pulse. The receive serial interface frame pulse signal (RC1FP) provides system timing for the receive serial interface. RC1FP is supplied in common to all devices in a system containing one or more NSE-8G devices. In telecom bus mode RC1FP is set high once every 4 frames, in SBI mode without any DS0 switching, or when switching DS0s (WITHOUT CAS) RC1FP is also set high once every 4 frames, or multiple thereof. When in SBI mode switching DS0s WITH CAS RC1FP indicates signaling multiframe alignment by pulsing once every 48 frames or multiples thereof.</p> <p>A software configurable delay from RC1FP is used to indicate that the C1 multiframe boundary 8B/10B characters have been delivered on all the receive serial data links (RP[11:0]/RN[11:0]) and are ready for processing by the time-space-time switching elements.</p> <p>RC1FP is sampled on the rising edge of SYCLK.</p>
Reserved	Output	C17	Factory test pin, must be left floating
CMP	Input	D10	<p>Connection Memory Page. The connection memory page select signal (CMP) controls the selection of the connection memory page in the NSE. When CMP is set high, connection memory page 1 is selected. When CMP is set low, connection memory page 0 is selected. Changes to the connection memory page selection are synchronized to the boundary of the next C1FP frame or multiframe depending on the mode:</p> <p><u>4-Frame SBI/SBI336 mode:</u></p> <p>CMP is sampled at the C1 byte position of the incoming bus on the first frame of the four-frame multiframe. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next four-frame multiframe.</p> <p><u>48-Frame SBI/SBI336 mode:</u></p> <p>CMP is sampled at the C1 byte position of the</p>

Pin Name	Type	Pin No.	Function
			<p>incoming bus on the first frame of the 48-frame multiframe. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next 48-frame multiframe.</p> <p><u>Telecom Bus mode:</u></p> <p>CMP is sampled at the C1 byte position of every frame on the incoming bus. Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame.</p> <p>CMP is sampled on the rising edge of SYSCLK at the RC1FP frame position.</p>
RSTB	Input	B18	<p>Reset Enable Bar. The active low reset signal (RSTB) provides an asynchronous reset for the NSE. RSTB is a Schmitt triggered input with an integral pull-up resistor.</p>
Microprocessor Interface (49 Balls)			
CSB	Input	AM30	<p>Chip Select Bar. The active low chip select signal (CSB) controls microprocessor access to registers in the NSE-8G device. CSB is set low during NSE-8G Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses.</p> <p>If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.</p>
RDB	Input	AM29	<p>Read Enable Bar. The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the NSE-8G device. RDB is set low and CSB is also set low during NSE-8G Microprocessor Interface Port register read accesses. The NSE-8G drives the D[31:0] bus with the contents of the addressed register while RDB and CSB are low.</p>
WRB	Input	AN29	<p>Write Enable Bar. The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the NSE-8G device. WRB is set low and CSB is also set low during NSE-8G Microprocessor Interface Port register write accesses. The contents of D[31:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.</p>
D[31] D[30] D[29] D[28] D[27] D[26]	I/O	AM24 AN23 AM23 AN22 AL22 AN21	<p>Microprocessor Data Bus. The bi-directional data bus, D[31:0] is used during NSE-8G Microprocessor Interface Port register reads and write accesses. D[31] is the most significant bit of the data words and D[0] is the least significant bit.</p>

Pin Name	Type	Pin No.	Function
D[25] D[24] D[23] D[22] D[21] D[20] D[19] D[18] D[17] D[16] D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]		AM21 AP20 AP19 AN19 AM19 AM18 AN18 AP18 AL17 AN17 AM16 AN16 AL15 AN15 AL14 AM14 AM13 AL13 AM12 AN12 AL11 AN11 AL10 AM10 AM9 AL9	
A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	AP28 AN27 AM27 AP26 AN26 AL26 AM26 AN25 AM25 AL25 AP24 AN24	Microprocessor Address Bus. The microprocessor address bus (A[11:0]) selects specific Microprocessor Interface Port registers during NSE-8G register accesses.
ALE	Input	AL30	Address Latch Enable. The address latch enable signal (ALE) is active high and latches the address bus (A[11:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the NSE-8G to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	Open Drain Output	AN30	Interrupt Request Bar. The active low interrupt enable signal (INTB) output goes low when an NSE-8G interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
JTAG Port (5 Balls)			
TCK	Input	B14	Test Clock. The JTAG test clock signal (TCK) provides timing for test operations that

Pin Name	Type	Pin No.	Function
			are carried out using the IEEE P1149.1 test access port.
TMS	Input	B13	Test Mode Select. The JTAG test mode select signal (TMS) controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	C12	Test Data Input. The JTAG test data input signal (TDI) carries test data into the NSE-8G via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tri-state	C11	Test Data Output. The JTAG test data output signal (TDO) carries test data out of the NSE-8G via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	D14	Test Reset Bar. The active low JTAG test reset signal (TRSTB) provides an asynchronous NSE-8G test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when TRSTB is not being used, it must be connected to the RSTB input.
Reserved (34 Balls)			
RESERVED	Input	C29 B6 C6 D6 A7 B7 D7 C7 B8 C8 A9 B9 D9 C9 B10 C19 B19 C20 D20 B20 A20 D21 C21 B21 C22	These pins are RESERVED . Must be left floating.

Pin Name	Type	Pin No.	Function
		D22 B22 A22 B23 C24 D24 B24 A24	
RESERVED	Input	D29	This pin is RESERVED and must be tied low for normal operation.
External Resistors (4 Balls)			
RES[2] RES[1]	Analog Input	AK2 E33	Reference Resistor Connection. An off-chip 3.16kΩ ±1% resistor is connected between these the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force the 0.8V VREF voltage onto RES, therefore forcing 252μA of current to flow through the resistor.
RESK[2] RESK[1]	Analog Input	AK1 E34	Reference Resistor Connection. An off-chip 3.16kΩ ±1% resistor is connected between these the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force the 0.8V VREF voltage onto RES, therefore forcing 252μA of current to flow through the resistor.
Analog Test Bus (4 Balls)			
ATB0[2] ATB0[1]	Analog	AK32 E3	Analog test bus for PMC validation and testing. Should be tied to VSS for normal operation.
ATB1[2] ATB1[1]	Analog	AJ31 F4	Analog test bus for PMC validation and testing. Should be tied to VSS for normal operation.
Digital Core Power (45 Balls)			
VDDI[44:0]	Power	AA4 AB1 AE4 AN10 AN13 AP13 AP15 AM15 AM17 AL18 AM20 AL21 AM22 AL24 AM28 AL28 AG32	The digital core power pins (VDDI[44:0]) should be connected to a well-decoupled +1.8 V DC supply.

Pin Name	Type	Pin No.	Function
		AE31 AD31 AA31 W32 P31 N34 K31 T3 P4 L4 K4 H3 C5 B11 D11 D13 C13 C15 D15 C18 D18 A18 C23 B25 C26 D28 B29 C30	
Digital I/O Power (34 Balls)			
VDDO[33:0]	Power	AL5 AM4 AN3 AN4 AN5 AP5 AL8 AL12 AL16 AL23 AL27 AL31 AM31 AM32 AN31 AN32 AN33 A30 B30 B31 B32 C31 D30 D27 D23 D19 D12	The digital I/O power pins (VDDO[33:0]) should be connected to a well-decoupled +3.3 V DC supply.

Pin Name	Type	Pin No.	Function
		D8 B2 B3 B4 C3 C4 D4	
Digital Ground (73 Balls)			
VSS [72:0]	Ground	A1 A2 A3 A4 A6 A8 A10 A12 A14 A19 A21 A23 A25 A27 A29 A31 A32 A33 A34 AP1 AP2 AP3 AP4 AP6 AP8 AP10 AP12 AP14 AP16 AP21 AP23 AP25 AP27 AP29 AP31 AP32 AP33 AP34 B1 C1 D1 F1 H1 K1 M1 P1 T1 AA1	The digital ground pins (VSS [72:0]) should be connected to GND.

Pin Name	Type	Pin No.	Function
		AC1 AE1 AG1 AJ1 AL1 AM1 AN1 B34 C34 D34 F34 H34 K34 M34 P34 W34 AA34 AC34 AE34 AG34 AJ34 AL34 AM34 AN34	
Analog Power (8 Balls)			
AVDL[7:0]	Power	F31 N33 W33 AD32 AJ4 AB2 T2 L3	These balls should be connected to a well-decoupled +1.8 V DC supply. These balls supply the RXLVs.
Clock Synthesis 1.8V Power (6 Balls)			
CSU_AVDL[5:0]	Power	T31 T32 U32 W4 W3 V3	These balls should be connected to a well-decoupled +1.8 V DC supply. These balls supply the CSUs.
Clock Synthesis 3.3V Power (2 Balls)			
CSU_AVDH[1:0]	Power	U31 V4	These two balls should be connected to a well-decoupled +3.3 V DC supply.
Analog I/O Power (34 Balls)			
AVDH[33:0]	Power	H4 M4 T4 AC4 AG4 AL2 AL3 AL4 AM2	The analog I/O power pins (AVDH[33:0]) should be connected to a well-decoupled +3.3 V DC supply.

Pin Name	Type	Pin No.	Function
		AM3 AN2 C2 D2 D3 E1 E2 E4 B33 C32 C33 D31 D32 D33 AG31 AC31 W31 M31 H31 AK31 AK33 AK34 AL32 AL33 AM33	
No Connect (130 Balls)			
NC[129:0]		AG33 AP30 AL29 AN28 AP22 AN20 AL20 AL19 AP17 AN14 AM11 AP11 AN9 AP9 AM8 AN8 AM7 AL7 AN7 AP7 AL6 AM6 AN6 AM5 H2 A5 B5 D5 C10 A11	The No Connect pins (NC[129:0]) should be left floating.

Pin Name	Type	Pin No.	Function
		B12	
		A13	
		C14	
		A15	
		B15	
		B16	
		C16	
		D17	
		B17	
		A17	
		D25	
		C25	
		D26	
		B26	
		A26	
		C27	
		B27	
		C28	
		B28	
		A28	
		AH4	
		AH3	
		AH2	
		AH1	
		AJ3	
		AJ2	
		AK4	
		AK3	
		AF31	
		AF32	
		AE32	
		AE33	
		AD33	
		AD34	
		AC32	
		AC33	
		Y31	
		Y32	
		V33	
		V34	
		V31	
		V32	
		U33	
		U34	
		N31	
		N32	
		M32	
		M33	
		L31	
		L32	
		L33	
		L34	
		G31	
		G32	
		G33	
		G34	
		F32	

Pin Name	Type	Pin No.	Function
		F33 E31 E32 AE2 AE3 AF4 AF3 AF1 AF2 AG2 AG3 AJ33 AJ32 AH34 AH33 AH32 AH31 AF34 AF33 AB34 AB33 AB32 AB31 AA33 AA32 Y34 Y33 T34 T33 R32 R31 R34 R33 P33 P32 K33 K32 J32 J31 J34 J33 H33 H32	
Total		480	

Notes on Pin Description:

1. All NSE-8G inputs and bi-directional balls except the LVDS links present minimum capacitive loading and operate at TTL logic levels.
2. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
3. All outputs have a minimum 8mA drive capability – this includes TDO, INTB and D[31:0]).
4. The VDDI and AVDL power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the device.
5. The AVDH, CSU_AVDH and VDDO power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the device.

-
6. The VDDI, VDDO, AVDH, CSU_AVDH and AVDL power pins all share the common ground VSS.
 7. For details on power-up and power-down of the VDDI, VDDO, AVDH, CSU_AVDH and AVDL power pins, see section 15.2.
 8. For details on analog power filtering, please see section 15.3.

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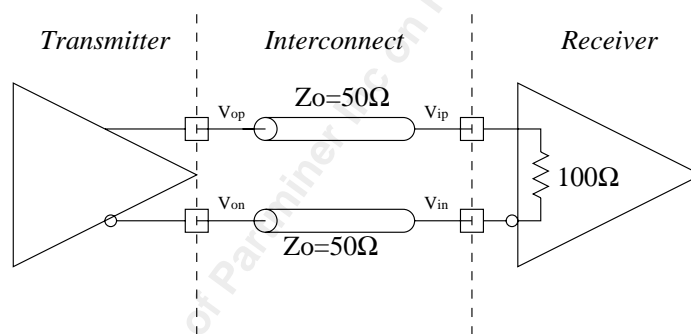
9 Functional Description

9.1 LVDS Overview

The LVDS family of cells allow the implementation of 777.6 Mb/s LVDS links. A reference clock of 77.76MHz is required.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated in Figure 6 below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 6 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Ten-bit parallel data is sampled by the line rate divided-by-10 clock (77.76MHz SYSCLK) and then serialized at the line rate on the LVDS output pins by a 777.6MHz clock synthesized from SYSCLK. Serial line rate LVDS data is sampled and de-serialized to 10-bit parallel data. Parallel output transfers are synchronized to a gated line rate divided-by-10 clock. The 10-bit data is passed to an 8B/10B decoding block. The gating duty cycle is adjusted such that the throughput of the parallel interface equals the receive input data rate (Line Rate +/- 100ppm). It is expected that the clock source of the transmitter is the same as the clock source of the receiver to ensure the data throughput at both ends of the link are identical.

Data is guaranteed to contain sufficient transition density to allow reliable operation of the data recovery units by 8B/10B block coding and decoding provided by the T8TE and R8TD blocks.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Namely, a worst-case eye opening of $0.7UI$ and $100mV$ differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of backplane connectors, up to $1m$ of backplane interconnect. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. Due to power constraints, the output differential amplitude is approximately $350mV$

The LVDS system is comprised of the LVDS Receiver (RXLV), LVDS Transmitter (TXLV), Transmitter reference (TXREF), data recovery unit (DRU), parallel to serial converter (PISO) and Clock Synthesis Unit (CSU).

9.1.1 LVDS Receiver (RXLV)

The RXLV block is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Receiver according to the IEEE 1596.3-1996 LVDS Specification.

The RXLV block is the receiver in Figure 6, accepting 777.6 Mb/s LVDS signals from the transmitter, over RP[X]/RN[X] pins, amplifying them and converting them to digital signals, then passing them to a data recovery unit (DRU). Holding to the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than $100mV$, and includes at least $25mV$ of hysteresis.

There are 12 instances of the RXLV block in the NSE-8G.

9.1.2 LVDS Transmitter (TXLV)

The TXLV block is a 777.6 Mb/s Low Voltage Differential Signaling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS Specification.

The TXLV accepts 777.6 Mb/s differential data from a “parallel-in, serial-out” (PISO) circuit and then transmits the data off-chip as a low voltage differential signal on TP[X]/TN[X] pins.

The TXLV uses a reference current and voltage from the TXREF block to control the output differential voltage amplitude and the output common-mode voltage.

There are 12 instances of the TXLV block in the NSE-8G.

9.1.3 LVDS Transmit Reference (TXREF)

The TXREF provides an on-chip bandgap voltage reference ($1.20V \pm 5\%$) and a precision current to the TXLV (777.6 Mb/s LVDS Transmitter) block's. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude.

The precision currents are generated by forcing the reference voltage across an external, off-chip $3.16K\Omega (\pm 1\%)$ resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

There are 2 instances of the TXREF in the NSE-8G.

9.1.4 Data Recovery Unit (DRU)

The DRU is a fully integrated data recovery and serial to parallel converter that can be used for 777.6 Mb/s NRZ data. 8B/10B block code is used to guarantee transition density for optimal performance.

The DRU recovers data and outputs a ten-bit word synchronized with a line rate divided by ten, gated clock to allow frequency deviations between the data source and the local oscillator. The output clock is not a recovered clock. The DRU accumulates 10 data bits and outputs them on the next clock edge. If 10-bits are not available for transfer at a given clock cycle, the output clock is gated.

The DRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ± 100 ppm.

There are 12 instances of the DRU on the NSE-8G.

9.1.5 Parallel to Serial Converter (PISO)

The PISO is a parallel-to-serial converter designed for high-speed transmit operation, supporting up to 777.6 Mb/s.

There are 12 instances of the PISO on the NSE-8G.

9.1.6 Clock Synthesis Unit (CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for the use by the transmitter. The CSU must be reset for 1ms for proper operation.

There are 2 instances of the CSU on the NSE-8G.

9.2 Receive 8B/10B Frame Aligner (R8TD)

The Receive 8B/10B SBI336S Bus frame aligner, R8TD, frames to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. The R8TD blocks perform framing and elastic store functions on data retrieved from the receive LVDS links, RP[x]/RN[x].

9.2.1 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domains of the associated receive LVDS link and that of the system clock, SYSCLK. Data with arbitrary alignment to the 8B/10B characters, are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every SYSCLK cycle.

9.3 Transmit 8B/10B Encoder (T8TE)

The Transmit 8B/10B Encoder blocks, T8TE, construct an 8B/10B character stream from an incoming translated SBI336 or telecom bus carrying an STS-12/STM-4 equivalent channelized stream. The T8TE block corrects the running disparity of an 8B/10B character stream and buffers data in a FIFO before transmission to the transmit serializer block. A total of 12 T8TE blocks are instantiated in the NSE-8G device.

In SBI mode, these blocks encode the SBI336S stream as shown in Table 2. When configured for Synchronous mode for DS0 switching, the 8B/10B encoder transmits CAS signaling multiframe alignment across the SBI336S interface by generating a C1FP character every 48 frame times. When not configured for DS0 switching the C1FP character is sent every 4 frames.

9.3.1 SBI336S 8B/10B Character Encoding

Table 2 shows the mapping of SBI336S bus control bytes and signals into 8B/10B control characters. The linkrate octet in location V4, V1 and V2, the in-band programming channel, the V3 octet when it contains data are all carried as data. Justification requests for master timing are carried in the V5 character so there are three V5 characters used, nominal, negative timing adjustment request, positive timing adjustment request.

Table 2 SBI336S Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Common to All Link Types			
K28.5	001111 1010	110000 0101	IC1FP='b1 C1FP frame and multiframe alignment
K23.7-	111010 1000	-	Overhead Bytes (columns 1-60 or 1-72 except for C1 and in-band programming channel), V3 or H3 byte except during negative justification, byte after V3 or H3 byte during positive justification, unused bytes in fraction rate links
Asynchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request
K29.7-	101110 1000	-	V5 byte, positive justification request
Synchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte
Asynchronous DS3/E3 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request*
K29.7-	101110 1000	-	V5 byte, positive justification request*
Fractional Rate Links			
K28.7-	001111 1000	-	V5 byte, send one extra byte request**

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
K29.7-	101110 1000	-	V5 byte, send one less byte request**
Floating Transparent Virtual Tributaries			
K27.7-	110110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0
K27.7+	-	001001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1
K28.7-	001111 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b0
K28.7+	-	110000 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b1
K29.7-	101110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b0
K29.7+	-	010001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b1
K30.7-	011110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b0
K30.7+	-	100001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b1

* Note there can be multiple V5s per SBI frame when in DS3 or E3 mode but only one justification can occur per SBI frame. Positive and negative justification request through V5 required by the SBI336S interface should be limited to one per frame.

** Note fractional rate links are symmetric in the transmit and receive direction over SBI336S. When using clock slave mode with a fractional rate link the clock master makes single byte adjustments to the slaves rate once per frame.

9.3.2 Serial Telecom Bus 8B/10B Character Encoding

Table 3 shows the mapping of Telecom bus control bytes and signals into 8B/10B control characters. When the Telecom bus control signals conflict each other, the 8B/10B control characters are generated according to the sequence of the table, with the characters at the top of the table taking precedence over those lower in the table.

Table 3 Serial Telecom Bus Character Encoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Level			
K28.5	001111 1010	110000 0101	IC1FP = 'b1 IPL = 'b0 C1FP frame and multiframe alignment
High Order Path Termination (HPT) Mode			
K28.5	001111 1010	110000 0101	IC1FP='b1 IPL='b0 C1FP frame and multiframe alignment
K28.0-	001111 0100	-	IPL='b0 High-order path H3 byte position, no negative justification event.
K28.0+	-	110000 1011	IPL='b0 High-order path PSO byte position, positive justification event.
K28.6	001111 0110	110000 1001	IC1FP='b1, IPL='b1 High-order path frame alignment (J1).
Low Order Path Termination (LPT) Mode			
K28.4+	-	110000 1101	IT AIS='b1 Low-order path AIS.
K27.7-	110110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K27.7+	-	001001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7-	001111 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7+	-	110000 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7-	101110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
			and REI are encoded in the V5 byte.
K29.7+	-	010001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7-	011110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b0 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7+	-	100001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b1 Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K23.7-	111010 1000	000101 0111	ITPL='b0 Non low-order path payload bytes.

9.3.3 Serial SBI336 and Telecom Bus Alignment

The alignment functionality performed by each receiver can be broken down into two parts, character alignment and frame alignment. Character alignment finds the 8B/10B character boundary in the arbitrarily aligned incoming data. Frame alignment finds SBI336S or Telecom bus frame and multiframe boundaries within the Serial link.

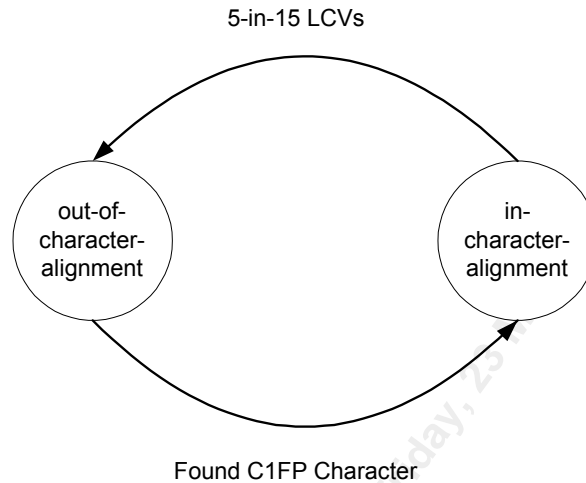
The character and frame alignment are expected to be robust enough for operation over a cabled interconnect.

9.3.4 Character Alignment Block

Character alignment locates character boundaries in the incoming 8B/10B data stream. The character alignment algorithm may be in one of two states, in-character-alignment state and out-of-character-alignment state. The two states of the character alignment algorithm is shown in Figure 7.

When the character alignment state machine is in the out-of-character-alignment state, it maintains the current alignment, while searching for a C1FP character. If it finds the C1FP character it will re-align to the C1FP character and move to the in-character-alignment state. The C1FP character is found by searching for the 8B/10B C1FP character, K28.5+ or K28.5-, simultaneously in ten possible bit locations. While in the in-character-alignment state, the state machine monitors LCVs. If 5 or more LCVs are detected within a 15 character window the character alignment state machine transitions to out-of-character-alignment state. The special characters listed in Table 2 and Table 3 are ignored for LCV purposes. Upon return to in-character-alignment state the LCV count is cleared.

Figure 7 Character Alignment State Machine



9.3.5 Frame Alignment

Frame alignment locates SBI or Telecom bus frame and multiframe boundaries in the incoming 8B/10B data stream. The frame alignment state machine may be in one of two states, in-frame-alignment state and out-of-frame-alignment state. Each SBI336S frame is 125uS in duration.

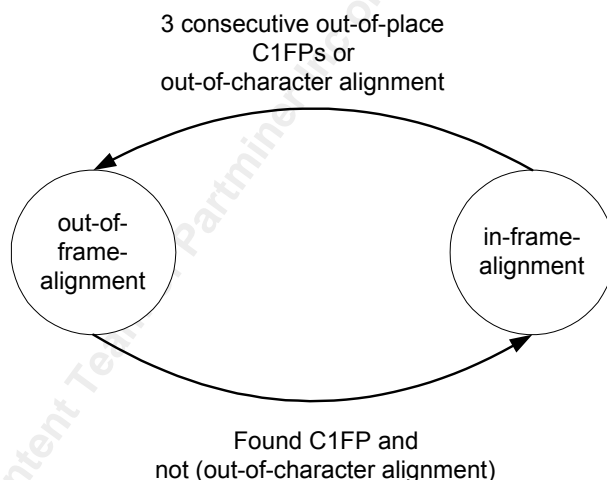
In SBI mode: Encoded over the SBI336S frame alignment is SBI336S multiframe alignment which is every four SBI336S frames or 500uS. When carrying DS0 traffic in synchronous mode, signaling multiframe alignment is also necessary and is also encoded over SBI336S alignment. Signaling multiframe alignment is every 24 frames for T1 links and every 16 frames for E1 links, therefore signaling multiframe alignment covering both T1 and E1 multiframe alignment is every 48 SBI336S frames or 6ms. Therefore C1FP characters are sent every four or every 48 frames.

In Telecom Bus mode: Encoded over the serial link is the tributary multiframe alignment which is every 4 frames or 500uS. Multiframe alignment is required so that a downstream device can extract the T1 or E1 data from the tributary. The multiframe information is preserved by only sending out C1FP characters every four frames.

The frame alignment state machine establishes frame alignment over the link and is based on the frame and not the multiframe alignments. When the frame alignment state machine is in the out-of-frame-alignment state, it maintains the current alignment, while searching for a C1FP character. When it finds the C1FP character the state machine transitions to the in-frame-alignment state. While in the in-frame-alignment state the state machine monitors out-of-place C1FP characters. Out-of-place C1FP characters are identified by maintaining a frame counter based on the C1FP character. The counter is initialized by the C1FP character when in the out-of-character-alignment state, and is unaffected in the in-character-alignment state. If 3 consecutive C1FPs have been found that do not agree with the expected location as defined by the frame counter, the state will change to out-of-frame-alignment state.

The frame alignment state machine is also sensitive to character alignment. When the character alignment state machine is in the out-of-character-alignment state, the frame alignment state machine is forced out-of-alignment, and is held in that state until the character alignment state machine transitions to the in-character alignment state.

Figure 8 Frame Alignment State Machine



9.3.6 SBI336S Multiframe Alignment

SBI336S multiframe alignment is communicated across the link by controlling the frequency of the C1FP character. The most frequent transmission of the C1FP character is every four SBI336S frame times. This is the SBI336S multiframe and is used when there are no synchronous tributaries requiring signalling multiframe alignment on the SBI336S bus. When there are synchronous tributaries on the SBI336S bus the C1FP character is transmitted every 48 frame times. This is the CAS signalling multiframe and is the lowest common multiple of the 24 frame T1 multiframe and the 16 frame E1 multiframe.

The SBI336S multiframe and signaling multiframe alignment is based a free running multiframe counter that is reset with each C1FP character received. Under normal operating conditions each received C1FP character will coincide with the free running multiframe counter. SBI336S multiframe alignment is always required, SBI336S signaling multiframe alignment is optional and only required when synchronous tributaries are supported with DS0 level switching.

9.4 DS0 Cross Bar switch (DCB)

Each of 12 R8TD blocks provides an eight-bit data signal on each 77.76MHz clock edge. These signals are the STS-12 frame aligned ingress octets. Likewise, each of 12 egress T8TE blocks expects to receive a STS-12 frame aligned signal on each clock edge. The DS0 Cross Bar switch (DCB) connects these inputs to these outputs.

The DCB constitutes a Space switch that connects each output to some input during each clock period in the STS-12 frame structure. The STS-12 frame structure consists of $12 \times 9 \times 90 = 9720$ octets (of overheads and payload). Being a DS0 granularity space switch, the DCB must provide separate switch settings for each of these 9720 octet times.

These 9720 switch settings are stored in an on-chip SRAM. Each of twelve egress ports must be told which of each of twelve ingress ports it should read during each of the 9720 clock periods. Five bits are required to specify which ingress port should be read by each output. Thus, we require 9720 words of five bits each for twelve egress ports. Thus each clock period requires $12 \times 5 = 60$ bits. To support controlled switchover from one set of switch settings to another, we require two banks of 9720 words each. The aggregate memory requirement is $2 \times 9720 \times 60b = 1,166,400b$ of SRAM. The table below illustrates the mapping of this memory. Each control page in the table is a vector of 60 bits containing five bits (specifying the source port) for each of 12 egress ports. One page will be on-line translating ports in the core switch while the other is offline for CPU update. When the new configuration is ready, and the appropriate system synchronized frame boundary arrives, the pages will be swapped.

Table 4 Switching Control RAM Layout

RAM Address	Control Page 0			Control Page 1		
	STS	Row	Col	STS	Row	Col
0	1	1	1	1	1	1
1	2	1	1	2	1	1
2	3	1	1	3	1	1
3	4	1	1	4	1	1
4	5	1	1	5	1	1
5	6	1	1	6	1	1
6	7	1	1	7	1	1
7	8	1	1	8	1	1
8	9	1	1	9	1	1
9	10	1	1	10	1	1
10	11	1	1	11	1	1

	Control Page 0			Control Page 1		
11	12	1	1	12	1	1
12	1	1	2	1	1	2
13	2	1	2	2	1	2
...	...					
1078	11	1	90	11	1	90
1079	12	1	90	12	1	90
1080	1	2	1	1	2	1
1081	2	2	1	2	2	1
...	...					
9718	11	9	90	11	9	90
9719	12	9	90	12	9	90

The multiplexers that select the inputs for each egress port are straight forward 12 to-1 multiplexers. They require five bits of control during each 77.76 MHz clock cycle. Their outputs go to the T8TEs. This design permits unicast, multicast, and broadcast.

9.5 Clock Synthesis and Transmit Reference Digital Wrapper (CSTR)

The CSTR contains the configuration registers for the CSU and TXREF LVDS analog locks.

9.6 Fabric Latency

The flow of octets from ingress LVDS to egress LVDS has variable latency, depending on the timing of the arriving LVDS stream, and the clock variation on the egress LVDS drivers. A reasonable estimate of the NSE's latency can be arrived at by making assumptions about the depths of the receive and transmit FIFOs: we assume the "C1" timing is set to maintain about 4 samples in the ingress FIFO; the egress FIFO is designed to be centered at 4 samples – so typically delay due to FIFOs will be 8 clock cycles. The latency through the space switch stage is three clock cycles. Data latency through the analog blocks is around 90 ns. The typical latency of the NSE-8G is 24 clock cycles or 308ns. With worst case conditions in both FIFOs, latency rises to 36 clock cycles or 463ns.

9.7 JTAG Support

The NSE-8G provides JTAG support for testing device interconnection on a PC board.

9.8 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the NSE-8G to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the NSE. The register set is accessed as shown in the Register Memory Map table below. Addresses that are not shown are not used and must be treated as Reserved.

9.9 In-band Link Controller (ILC)

In order to permit centralized control of distributed NSE/SBS/SBSLITE fabrics from the NSE microprocessor interface (for applications in which NSEs are located on fabric cards, and SBSs are located on multiple line cards), an in-band signaling channel is provided between the NSE and the SBS over the SBI336S interface. Each NSE can control up to 12 SBSs that are attached by the LVDS links. The NSE-SBS in-band channel is full duplex, but the NSE-8G has active control of the link.

The in-band channel is carried in the first 36 columns of four rows of the SBI structure, rows 3, 6, 7 and 8. The overall in-band channel capacity is thus $36 \times 4 \times 64\text{kb/s} = 9.216\text{Mb/s}$. Each 36 bytes per row allocated to the in-band signaling channel is its own in-band message between the end points. Four bytes of each 36-byte, inband message are reserved for end-to-end control information and error protection, leaving 8.192Mb/s available for data transfer between the end points.

The data transferred between the end points has no fixed format, effectively providing a clear channel for packet transfer between the attached microprocessors at each of the LVDS link terminating devices. The user is able to send and receive any packet upto 32 bytes in length. The last two reserved bytes of the 36 byte in-band message is a CRC-16 which detects errors in the message. This block provides a microprocessor interface to the in-band signaling channel.

This in-band channel is expected to be used almost entirely to carry out switching control changes in the SBSs. To configure a DS0 in an SBS device most often requires a local microprocessor to write to one memory location consisting of a 16-bit address and a 16-bit data. Using this as a baseline and assuming an efficient use of the in-band channel bandwidth we can set a maximum of $(32\text{bytes/row} \times 4\text{ rows/frame} \times 8000\text{ frames/sec} / 4\text{ bytes/write})$ 256,000 DS0 configurations per second.

Considering that configuring a T1 when switching DS0s requires 27 DS0 writes indicates that the in-band signaling channel bandwidth sets maximum limit of over 9000 T1 configurations per second. In real life these limits will not be achieved but this shows that the in-band link should not be the bottleneck. In telecom bus mode this same configuration will require only 3 writes per T1 link. Another more efficient communication scheme could be used to increase this performance.

In N+1 protected architectures it is likely that full configuration of a port card will be necessary during the switchover. This would require the entire connection memory be reconfigured. Assuming connections for overhead bytes are also reconfigured, the fastest that a complete reconfiguration can take place is 9720 register writes for each of the two configuration pages in the SBS. This equates to $(2 * 9720 \text{ writes} * 4 \text{ bytes/write} / (32 \text{ bytes/row} * 4 \text{ rows/frame} * 8000 \text{ frames/second}))$ 76 milliseconds. It is also possible that the spare card could hold all the connection configurations for all the port cards it is protecting locally, for even faster switch over.

9.9.1 In-Band Signaling Channel Fixed Overhead

The In-Band Link Controller block generates and terminates two bytes of fixed header and a CRC-16 per every 32 byte in-band message (total 36 bytes). The two byte header provides control and status between devices at the ends of the LVDS link. The CRC-16 is calculated over the 32 byte (and header - 34 bytes) in-band message and provides the terminating end the ability to detect errors in the in-band message. The format of the in-band message and header bytes is shown in Figure 9 and Figure 10.

Figure 9 In-Band Signaling Channel Message Format

1 byte	1 byte	32 bytes	2 bytes
Header1	Header2	Free Format Information	CRC-16

Figure 10 In-Band Signaling Channel Header Format

Header1							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
VALID	LINK[1:0]		PAGE[1:0]		USER[2:0]		

Header2							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
AUX[7:0]							

Table 5 In-band Message Header Fields

Field Name	NSE to SBS/SBSLITE	SBS/SBSLITE to NSE
Valid	Message slot contains a message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)	Message slot contains a message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)
Link[1:0]#	These bits are optional for SBI336S devices, intended for devices which have multiple redundant links. Each bit either indicates which Link to use, Working(0) or Protect(1) when sourced from the master device, or which link is being used, when sourced from the slave device. Other algorithms are possible to indicate	These bits are optional for SBI336S devices, intended for devices which have multiple redundant links. Each bit either indicates which Link to use, Working(0) or Protect(1) when sourced from the master device, or which link is being used, when sourced from the slave device. Other algorithms are possible to indicate

Field Name	NSE to SBS/SBSLITE	SBS/SBSLITE to NSE
	Working or Protect over these 2 bits but all SBI336S devices must be able to revert back to this meaning. Transmitted immediately.	Working or Protect over these 2 bits but all SBI336S devices must be able to revert back to this meaning. Transmitted immediately.
Page[1:0]#	Each bit indicates which control page to use, page 1 or 0, two bits, bit 1 for the ingress MSU and bit 0 for the egress MSU. Only transmitted from the beginning of the first message of the frame	Each bit shows current control page in use, page 1 or 0, two bits, bit 1 for the ingress MSU and bit 0 for the egress MSU. Only transmitted from the beginning of the first message of the frame.
User[2:0]#	User defined register indication to SBS reflected in the SBS as external hardware signal outputs. Transmitted immediately.	User defined register indication to NSE from external hardware inputs to the SBS. Transmitted immediately.
Aux[7:0]#	User defined auxiliary register indication to SBS. Transmitted immediately.	User defined auxiliary register indication to NSE. Transmitted immediately.

Change in these bits (received side) will not be processed if the received message CRC-16 indicates an error.

Interrupts can be generated when CRC errors are detected or the USER or LINK bits change state. There is no inherent flow control provided by the In-Band Link Controller. The attached microprocessor is able to provide flow control via interrupts when the in-band message fifo overflows and via the USER and Auxiliary bits in the header.

As each message arrives, the CRC-16 and valid bit is checked; if the valid bit is not set the message is discarded, if it fails the CRC check it is flagged as being in error and an interrupt is generated if enabled. If the CRC-16 is OK, regardless of the valid bit, the Page Link, User and Aux bits are passed on immediately. If the fifo erroneously overflows, an interrupt is generated.

9.10 Microprocessor Interface

The following register map shows the registers used to provide control of the NSE. The first 100h addresses provide access to the top level NSE configuration and control registers, the Clock synthesis units through the CSTR blocks and the DSO Crossbar (DCB). The DCB is the space switch at the core of the NSE. From 100h are 12 identical, 20h spaces used to control the ports of the NSE on an individual basis. Each port has an In-Band Link Controller (ILC), an 8B/10B encoder (T8TE) and an 8B/10B decoder (R8TD). These blocks provide functions specific to the ports such as Line Code Violation counts (for data integrity monitoring) and receive and transmit in-band link message buffers. Table 6 shows the registers. Only port 0 is fully described as the other ports are identical, being incrementally distributed from address 100h in 20h steps.

Table 6 NSE-8G Register Map

Address	Register
000	NSE Master Reset
001	NSE Individual Channel Reset
002	NSE Master JTAG ID
003	NSE In-Band Link Transmit Page Bit 0
004	NSE In-Band Link Transmit Page Bit 1
005	NSE Master Interrupt Source
006	NSE Master ILC Interrupt Source
007	NSE Master R8TD Interrupt Source
008	NSE Master T8TE Interrupt Source
009	NSE Master Clock Monitor, Accumulation Trigger
00A	NSE DCB CMP select
00B	NSE Master Interrupt Enable
00C	NSE Subsystem Interrupt Enable
00D	NSE R8TD TIP
00E	NSE In-Band Link Transmit User Bit 0
00F	NSE In-Band Link Transmit User Bit 1
010	NSE In-Band Link Transmit User Bit 2
011	NSE FREE User Register
012	Correct R8TD_RX_C1 Pulse Monitor Register
013	Unexpected R8TD_RX_C1 Interrupt Register
014	Missing R8TD_RX_C1 Interrupt Register
015	Unexpected R8TD_RX_C1 Interrupt Enable Register
016	Missing R8TD_RX_C1 Interrupt Enable Register
017	R8TD C1 Disable
01C-01F	Reserved
020	CSTR #1 Control
021	CSTR #1 Interrupt Enable and CSU Lock Status
022	CSTR #1 Interrupt Indication
023	Reserved
024	CSTR #2 Control
025	CSTR #2 Configuration and Status
026	CSTR #2 Interrupt Status
027-03F	Reserved
040	Reserved
041	Reserved
042	Reserved
043	Reserved
044	DCB CONFIGURATION PORT 11-6 REGISTER

Address	Register
045	DCB CONFIGURATION PORT 5-0 REGISTER
046	DCB CONFIGURATION OUTPUT REGISTER
047	DCB ACCESS MODE REGISTER
048	DCB C1 DELAY (RC1FP) REGISTER
04A	DCB FRAME SIZE REGISTER
04C	DCB CONFIGURATION REGISTER
04D	DCB INTERRUPT REGISTER
04E – 0FF	Reserved
100-1FF	Port Register Set 0 – Port 0 (Channel 0)
100	Port Register Set 0: R8TD Control and Status
101	Port Register Set 0: R8TD Interrupt Status
102	Port Register Set 0: R8TD LCV Count
103	Port Register Set 0: RXLV and DRU Control
104 – 107	Port Register Set 0: Reserved
108	Port Register Set 0: T8TE Control and Status
109	Port Register Set 0: T8TE Interrupt Status
10A	Port Register Set 0: T8TE Time-slot Configuration #1
10B	Port Register Set 0: T8TE Time-slot Configuration #2
10C	Port Register Set 0: T8TE Test Pattern
10D	Port Register Set 0: TXLV and PISO Control
10E – 10F	Port Register Set 0: Reserved
110	Port Register Set 0: ILC Transmit Message FIFO Data
111	Port Register Set 0: ILC Transmit Control
112	Port Register Set 0: ILC Transmit Status and FIFO Synch
113	Port Register Set 0: ILC Receive Message FIFO DATA
114	Port Register Set 0: ILC Receive Control
115	Port Register Set 0: ILC Receive Status and FIFO Synch
116	Port Register Set 0: ILC Interrupt enable and Control
117	Port Register Set 0: ILC Interrupt reason Register
118-11F	Reserved
120-13F	Port Register Set 1 – Port 1 (Channel 1)
140-15F	Port Register Set 2 – Port 2 (Channel 2)
160-17F	Port Register Set 3 – Port 3 (Channel 3)
180-19F	Port Register Set 4 – Port 4 (Channel 4)
1A0-1BF	Port Register Set 5 – Port 5 (Channel 5)
1C0-1DF	Port Register Set 6 – Port 6 (Channel 6)
1E0-1FF	Port Register Set 7 – Port 7 (Channel 7)
200-21F	Port Register Set 8 – Port 8 (Channel 8)
220-23F	Port Register Set 9 – Port 9 (Channel 9)

Address	Register
240-25F	Port Register Set 10 – Port 10 (Channel 10)
260-27F	Port Register Set 11 – Port 11 (Channel 11)
280-29F, 2A0-7FF	Reserved
800-FFF	Reserved for Test

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.

10 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the NSE. Normal mode registers (as opposed to test mode registers) are selected when A[11] is set low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TSB to determine the programming state of the block.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect NSE operation unless otherwise noted.
5. For registers above 100H, only a one port set of the 12 ports are shown. The Register addresses are shown for example as: 0100H + N*20H, N here is the port number between 0 and 11. This is done to prevent unnecessary duplication of otherwise identical register sets.

Register 000H: NSE Master Reset

Bit	Type	Function	Default
Bit 31	R/W	DRESET	0
Bit 30	R/W	ARESET	0
Bit 29:0	R	Unused	X

This register allows separate software reset of digital and analog circuitry on the NSE.

ARESET

The ARESET bit allows the analog circuitry in the NSE to be reset under software control. If the ARESET bit is a logic one, all the NSE analog circuitry is held in reset. ARESET must be held at logic 1 for at least 1ms to ensure correct reset of the CSU. This bit is not self-clearing. Therefore, a logic zero must be written to bring the NSE out of reset. Holding the NSE in a reset state places it into a low power, analog stand-by mode. A hardware reset clears the ARESET bit, thus negating the analog software reset.

DRESET

The DRESET bit allows the digital circuitry in the NSE to be reset under software control. If the DRESET bit is a logic one, all the NSE digital circuitry is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the NSE out of reset. Holding the NSE in a reset state places it into a low power, digital stand-by mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register 001H: NSE Individual Channel Reset

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	1
Bit 11:0	R/W	RESET[11:0]	1

This register allows power saving by holding individual channels in reset.

RESET[n]

The RESET[n] bit allows the channel circuitry in the NSE to be reset under software control. If the RESET[n] bit is a logic one, the NSE channel circuitry for a particular channel is held in reset. RESET[n] does not affect the reset of the CSU. This bit is not self-clearing. Therefore, a logic zero must be written to bring the channel out of reset. Holding the channel in a reset state places it into a low power, analog stand-by mode. A hardware reset or software DRESET bit 000h sets the RESET[n] bit.

Reserved

The Reserved bits must be set to logic 1 for proper operation of the NSE-8G.

Register 002H: NSE Master JTAG ID

Bit	Type	Function	Default
Bit 31:28	R	VERSION[3:0]	0001
Bit 27:12	R	PART_NUMBER[15:0] NSE-8G	1000011000100000
Bit 11:1	R	MANUFACTURER_ID[10:0]	00001100110
Bit 0	R	JID	1

The NSE Master JTAG ID registers hold the jtag identification code for the device. The device version number and device part number are available through these registers.

VERSION[3:0]

The VERSION[3:0] bits report the binary revision number of the NSE silicon.
VERSION[3:0] = 'b0001 for revision B of the NSE.

PART_NUMBER[15:0]

The PART_NUMBER[15:0] bits represent the part number of the NSE device.
PART_NUMBER[15:0] = 8620H for NSE-8G.

MANUFACTURER_ID[10:0]

The MANUFACTURER_ID[10:0] bits represent the 11 bit manufacturer's code assigned to PMC-Sierra, Inc. for inclusion in the JTAG Boundary Scan Identification Code. For more information on JTAG Boundary Scan, refer to Section 11.2.

JID

The JID bit is bit 0 in the JTAG identification code.

Register 003H: NSE In-Band Link Transmit Page Bit 0

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	TX_ILC_PAGE_0[11:0]	0

TX_ILC_PAGE_0[n]

This bit will be the Page bit 0 send out over the In-Band channel – where n is the transmit LVDS links numbered from 0 to 11.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 004H: NSE In-Band Link Transmit Page Bit 1

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	TX_ILC_PAGE_1[11:0]	0

TX_ILC_PAGE_1[n]

This bit will be the Page bit 1 send out over the In-Band channel – where n is the transmit LVDS links numbered from 0 to 11.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 005H: NSE Master Interrupt Source

Bit	Type	Function	Default
Bit 31:8	R	Unused	X
Bit 7	R	R8C1EXTRAIINT	0
Bit 6	R	R8C1MISSINT	0
Bit 5	R	CSU2INT	0
Bit 4	R	CSU1INT	0
Bit 3	R	R8TDINT	0
Bit 2	R	T8TEINT	0
Bit 1	R	ILCINT	0
Bit 0	R	DCBINT	0

R8C1EXTRAIINT

If the R8C1EXTRAIINT bit is a logic 1, an interrupt of unexpected C1 character in one or more of the receive LVDS link has occurred. The source of the R8C1EXTRAIINT bit comes from Register 013h. The Unexpected R8TD_RX_C1 Interrupt register (Reg013h) must be read to clear this interrupt.

R8C1MISSINT

If the R8C1MISSINT bit is a logic 1, an interrupt of missing C1 characters in one or more of the receive LVDS link has occurred. The source of the R8C1MISSINT bit comes from Register 014h. The Missing R8TD_RX_C1 Interrupt register (Reg014h) must be read to clear this interrupt.

CSU2INT

If the CSU2INT bit is a logic 1, an interrupt has been generated by CSU #2. The CSTR #2 Interrupt Indication register (Reg026h) must be read to clear this interrupt.

CSU1INT

If the CSU1INT bit is a logic 1, an interrupt has been generated by CSU #1. The CSTR #1 Interrupt Indication register (Reg022h) must be read to clear this interrupt.

R8TDINT

If the R8TDINT bit is a logic 1, an interrupt has been generated by one of the R8TD blocks. The internal R8TD Interrupt register must be read to clear this interrupt. Which R8TD caused the interrupt can be ascertained by reading the NSE Master R8TD Interrupt Source register (Reg007h).

T8TEINT

If the T8TEINT bit is a logic 1, an interrupt has been generated by one of the T8TE blocks. The internal T8TE Interrupt register must be read to clear this interrupt. Which T8TE caused the interrupt can be ascertained by reading the NSE Master T8TE Interrupt Source register (Reg008h).

ILCINT

If the ILCINT bit is a logic 1, an interrupt has been generated by one of the ILC blocks. The relevant ILC Interrupt register must be read to clear this interrupt. Which ILC caused the interrupt can be ascertained by reading the NSE Master ILC Interrupt Source register (Reg006h).

DCBINT

If the DCBINT bit is a logic 1, an interrupt has been generated by the DCB block. The DCB Interrupt Status Register (Reg04Dh) must be read to clear this interrupt.

Register 006H: NSE Master ILC Interrupt Source

Bit	Type	Function	Default
Bit 31:12	R	Reserved	X
Bit 11:0	R	ILCINT[11:0]	0

ILCINT[n]

If the ILCINT[n] bit is a logic 1, an interrupt has been generated by that ILC block. The relevant ILC Interrupt register must be read to clear this interrupt.

Reserved

The Reserved bits should be masked when reading this register.

Register 007H: NSE Master R8TD Interrupt Source

Bit	Type	Function	Default
Bit 31:12	R	Reserved	X
Bit 11:0	R	R8TDINT[11:0]	0

R8TDINT[n]

If the R8TDINT[n] bit is a logic 1, an interrupt has been generated by that R8TD block. The relevant R8TD Interrupt register must be read to clear this interrupt.

Reserved

The Reserved bits should be masked when reading this register.

Register 008H: NSE Master T8TE Interrupt Source

Bit	Type	Function	Default
Bit 31:12	R	Reserved	X
Bit 11:0	R	T8TEINT[11:0]	0

T8TEINT[n]

If the T8TEINT[n] bit is a logic 1, an interrupt has been generated by that T8TE block. The relevant T8TE Interrupt register must be read to clear this interrupt.

Reserved

The Reserved bits should be masked when reading this register.

Register 009H: NSE Master Clock Monitor, Accumulation Trigger

Bit	Type	Function	Default
Bit 31:2	R	Unused	X
Bit 1	R	RC1FPA	X
Bit 0	R	SYSCCLKA	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register reading low. This register should be read at periodic intervals to detect clock failures.

Writing to this register delimits the accumulation intervals in the 12 R8TD LCV Count registers. Counts accumulated in those registers are transferred to holding registers where they can be read (Register 102H + N*20). The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 1.0 second or shorter. The bits in this register are not affected by write accesses.

SYSCCLKA

The SYSCCLK active bit (SYSCCLKA) detects low to high transitions on the SYSCCLK input. SYSCCLKA is set high on a rising edge of SYSCCLK, and is set low when this register is read.

RC1FPA

The RC1FP active bit (RC1FPA) detects low to high transitions on the RC1FP input. RC1FPA is set high on a rising edge of RC1FP, and is set low when this register is read.

Register 00AH: NSE DCB CMP select

Bit	Type	Function	Default
Bit 31:2	R	Unused	X
Bit 1	R/W	CMP_SRC	0
Bit 0	R/W	CMP_VAL	0

The connection memory page select signal (CMP) controls the selection of the connection memory page in the NSE. When CMP is set high, connection memory page 1 is selected. When CMP is set low, connection memory page 0 is selected. Changes to the connection memory page selection are synchronized to the boundary of the next C1FP multiframe.

This Register controls a software override to the CMP pin.

CMP_SRC

This bit dictates whether CMP is to be source from the CMP_VAL bit when set to '1' or from the external CMP pin when set to '0'.

CMP_VAL

CMP_VAL is used to provide the CMP signal when CMP_SRC is set to '1' other wise this bit is ignored.

Register 00BH: NSE Interrupt Enable Register

Bit	Type	Function	Default
Bit 31:1	R	Unused	X
Bit 0	R/W	INTE	0

This register allows the CPU to disable or enable NSE interrupts with a single write.

INTE

This bit, when '1', enables the INTB pin on the NSE. When set to '0' INTB is held high impedance.

Register 00CH: NSE Subsystem Interrupt Enable Register

Bit	Type	Function	Default
Bit 31:6	R	Unused	X
Bit 5	R/W	TOPINTE	0
Bit 4	R/W	CSUINTE	0
Bit 3	R/W	R8TDINTE	0
Bit 2	R/W	T8TEINTE	0
Bit 1	R/W	ILCINTE	0
Bit 0	R/W	DCBINTE	0

This register allows the CPU to disable or enable NSE Subsystem interrupts with a single write.

TOPINTE

This bit, when '1', enables the generation of interrupts from the Top_level i.e. R8C1EXTRAIINT and R8C1MISSINT interrupts. When set to '0' R8C1EXTRAIINT and R8C1MISSINT interrupts are disabled .

CSUINTE

This bit, when '1', enables the generation of interrupts from CSU1 and CSU2 control. When set to '0' CSU1 and CSU2 control interrupts are disabled .

R8TDINTE

This bit, when '1', enables the generation of interrupts from R8TD blocks. When set to '0' all R8TD interrupts are disabled .

T8TEINTE

This bit, when '1', enables the generation of interrupts from T8TE blocks. When set to '0' all T8TE interrupts are disabled .

ILCINTE

This bit, when '1', enables the generation of interrupts from ILC blocks. When set to '0' all ILC interrupts are disabled .

DCBINTE

This bit, when '1', enables the generation of interrupts from the DCB block. When set to '0' DCB interrupts are disabled .

Register 00DH: NSE R8TD TIP Register

Bit	Type	Function	Default
Bit 31:1	R	Unused	X
Bit 0	R	TIP	0

This register monitors the reporting of the R8TD's LCV counter registers.

TIP

The Transfer In Progress bit reflects the state of the LCV counter transfer in R8TD. When TIP is high, an LCV counter transfer has been initiated, but the counters are not transferred in the holding registers yet (i.e. Reg. 102H + N*20H R8TD Line Code Violation Count register). When TIP is low, the value of the LCV counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

Register 00EH: NSE In-Band Link Transmit User Bit 0

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	TX_ILC_USER_0[11:0]	0

TX_ILC_USER_0[n]

This bit will be the USER 0 bit sent out over the In-Band channel – where n is any transmit LVDS links numbered from 0 to 11.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 00FH: NSE In-Band Link Transmit User Bit 1

Bit	Type	Function	Default
31:12	R/W	Reserved	0
Bit 11:0	R/W	TX_ILC_USER_1[11:0]	0

TX_ILC_USER_1[n]

This bit will be the USER 1 bit sent out over the In-Band channel – where n is any transmit LVDS links numbered from 0 to 11.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 010H: NSE In-Band Link Transmit User Bit 2

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	TX_ILC_USER_2[11:0]	0

TX_ILC_USER_2[n]

This bit will be the USER 2 bit sent out over the In-Band channel – where n is any transmit LVDS links numbered from 0 to 11.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 011H: NSE FREE User Register

Bit	Type	Function	Default
Bit 31:8	R	Unused	X
Bit 7:0	R/W	FREE[7:0]	0

FREE[7:0]

The software ID register (FREE) holds whatever value is written into it. Reset clears the contents of this register. This register has no impact on the operation of the NSE.

Register 012H: Correct R8TD_RX_C1 Pulse Monitor

Bit	Type	Function	Default
Bit 31:12	R	Reserved	X
Bit 11:0	R	R8C1_OK_MON[11:0]	0

R8C1_OK_MON[11:0]

The R8C1_OK_MON bit is set to logic 1 when a C1 character is received on the receive LVDS link in its expected position with respect to the RC1FP input. This bit is set to logic 0 when this register is read.

Section 12.5: Controlling Frame Alignment in the Receive Port Describes the proper use of this register.

Reserved

The Reserved bits should be masked when reading this register.

Register 013H: Unexpected R8TD_RX_C1 Interrupt

Bit	Type	Function	Default
Bit 31:12	R	Reserved	X
Bit 11:0	R	R8C1_EXTRA_INT[11:0]	0

R8C1_EXTRA_INT[11:0]

The R8C1_EXTRA_INT bit is set to a logic 1 when a C1 character is received on the receive LVDS link in an unexpected position with respect to the RC1FP input. These interrupts are enabled with the R8C1_EXTRA_INTE bits in the Unexpected R8TD_RX_C1 Interrupt Enable register (Reg015h). These interrupt bits will be cleared when read.

Section 12.5: Controlling Frame Alignment in the Receive Port Describes the proper use of this register.

Reserved

The Reserved bits should be masked when reading this register.

Register 014H: Missing R8TD_RX_C1 Interrupt

Bit	Type	Function	Default
Bit 31:12	R	Reserved	X
Bit 11:0	R	R8C1_MISS_INT[11:0]	0

R8C1_MISS_INT[11:0]

The R8C1_MISS_INT bit is set to a logic 1 when a C1 character is not received on the receive LVDS link in its expected position with respect to the RC1FP input. These interrupts are enabled with the R8C1_MISS_INTE bits in the Missing R8TD_RX_C1 Interrupt Enable register (Reg016h). These interrupt bits will be cleared when read.

Section 12.5: Controlling Frame Alignment in the Receive Port Describes the proper use of this register.

Reserved

The Reserved bits should be masked when reading this register.

Register 015H: Unexpected R8TD_RX_C1 Interrupt Enable

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	R8C1_EXTRA_INTE[11:0]*	0

R8C1_EXTRA_INTE[11:0]

The R8C1_EXTRA_INTE interrupt enable bit is an active high interrupt enable. When R8C1_EXTRA_INTE is set to a logic 1, an interrupt will be asserted on the INTB output when the R8C1_EXTRA_INT interrupt bits in register 013H are set high, and the TOPINTE bit in register 00CH and INTE bit in register 00BH are set high. When R8C1_EXTRA_INTE is set to a logic 0, The R8C1_EXTRA_INT interrupt bits will not cause an interrupt. This is on per channel* basis.

*Any unused ports must be set to '0'.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 016H: Missing R8TD_RX_C1 Interrupt Enable

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	R8C1_MISS_INTE[11:0]*	0

R8C1_MISS_INTE[11:0]

The R8C1_MISS_INTE interrupt enable bit is an active high interrupt enable. When R8C1_MISS_INTE is set to a logic 1, an interrupt will be asserted on the INTB output when the R8C1_MISS_INT interrupt bits in register 013H are set high, and the TOPINTE bit in register 00CH and INTE bit in register 00BH are set high. When R8C1_MISS_INTE is set to a logic 0, The R8C1_MISS_INT interrupt bits will not cause an interrupt. This is on per channel* basis.

*Any unused ports must be set to '0'.

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 017H: R8TD C1 Disable

Bit	Type	Function	Default
Bit 31:12	R/W	Reserved	0
Bit 11:0	R/W	R8TD_C1_DISABLE [11:0]	0

R8TD_C1_DISABLE[n]

The R8TD_C1_DISABLE bits control the way the C1 pulse is passed from the R8TD to the DCB. If R8TD_C1_DISABLE[n] is a logic 0, the C1 pulse passed to the DCB is the AND of the decoded C1 (from the serial link) and the reference C1 (from RC1FP).

If R8TD_C1_DISABLE is a logic 1, the C1 pulse passed to the DCB is the same as the reference C1 (from RC1FP).

Reserved

The Reserved bits must be set to logic 0 for proper operation of the NSE-8G.

Register 020H, 024H: CSTR #1, #2 Control

Bit	Type	Function	Default
Bit 31-16		Unused	X
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

This register provides reset control and enable control for CSTR blocks #1 through #2.

Reserved

The Reserved bits must be set to the indicated default value for correct operation of the NSE.

CSU_RSTB

The CSU_RSTB signal is a software reset signal that forces the CSU1250 into a reset. In order to properly reset the CSU, CSU_RSTB should be held low for at least 1 ms.

The CSU is also reset by the NSE master analog reset signal.

CSU_ENB

The active low CSU enable control signal (CSU_ENB) bit can be used to force the CSU1250 into low power configuration if it is set to logic 1. For normal operation, it is set to logic 0.

Register 021H, 025H: CSTR #1, #2 Interrupt Enable and CSU Lock Status

Bit	Type	Function	Default
Bit 31-2	R	Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

This register configures the operation of CSTR blocks #1 through #2.

LOCKE

The CSU lock interrupt enable bit (LOCKE) controls the contribution of CSU lock state interrupts by the CSTR to the device interrupt INTB. When LOCKE is high, INTB is asserted low when the CSU lock state changes. Interrupts due to CSU lock state are masked when LOCKE is set low.

LOCKV

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit has successfully locked with the system clock. LOCKV is set low when the CSU has not successfully locked with the reference clock. LOCKV is set high if when the CSU has locked with the reference clock.

Register 022H, 026H: CSTR #1, #2 Interrupt Indication

Bit	Type	Function	Default
Bit 31-1	R	Unused	X
Bit 0	R	LOCKI	X

LOCKI

The CSU lock interrupt status bit (LOCKI) reports and acknowledges changes in the CSU lock state. LOCKI is set high when the CSU achieves lock with the reference clock or loses its lock to the reference clock. LOCKI is cleared on a read to this register. INTB is asserted low when both LOCKE and LOCKI are high. If LOCKE is asserted, LOCKI must be cleared before INTB will be reasserted.

Register 044H: DCB Configuration Port 11-6 Register

Bit	Type	Function	Default
Bit 31-30	R	Unused	X
Bit 29	R/W	Reserved	0
Bit 28-25	R/W	Port11[3:0]	0
Bit 24	R/W	Reserved	0
Bit 23-20	R/W	Port10[3:0]	0
Bit 19	R/W	Reserved	0
Bit 18-15	R/W	Port9[3:0]	0
Bit 14	R/W	Reserved	0
Bit 13-10	R/W	Port8[3:0]	0
Bit 9	R/W	Reserved	0
Bit 8-5	R/W	Port7[3:0]	0
Bit 4	R/W	Reserved	0
Bit 3-0	R/W	Port6[3:0]	0

PORT11[3:0]

This register selects the input port number to map to output port 11 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT10[3:0]

This register selects the input port number to map to output port 10 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT9[3:0]

This register selects the input port number to map to output port 9 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT8[3:0]

This register selects the input port number to map to output port 8 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT7[3:0]

This register selects the input port number to map to output port 7 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT6[3:0]

This register selects the input port number to map to output port 6 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

Reserved

The Reserved bits must be set to the indicated default value for correct operation of the NSE.

Register 045H: DCB Configuration Port 5-0 Register

Bit	Type	Function	Default
Bit 31-30	R	Unused	X
Bit 29	R/W	Reserved	0
Bit 28-25	R/W	Port5[3:0]	0
Bit 24	R/W	Reserved	0
Bit 23-20	R/W	Port4[3:0]	0
Bit 19	R/W	Reserved	0
Bit 18-15	R/W	Port3[3:0]	0
Bit 14	R/W	Reserved	0
Bit 13-10	R/W	Port2[3:0]	0
Bit 9	R/W	Reserved	0
Bit 8-5	R/W	Port1[3:0]	0
Bit 4	R/W	Reserved	0
Bit 3-0	R/W	Port0[3:0]	0

PORT5[3:0]

This register selects the input port number to map to output port 5 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT4[3:0]

This register selects the input port number to map to output port 4 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT3[3:0]

This register selects the input port number to map to output port 3 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT2[3:0]

This register selects the input port number to map to output port 2 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT1[3:0]

This register selects the input port number to map to output port 1 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

PORT0[3:0]

This register selects the input port number to map to output port 0 of the DCB for an arbitrary position in the SBI336/telecombus frame. Valid values are 0-11 when performing writes.

Reserved

The Reserved bits must be set to the indicated default value for correct operation of the NSE.

Register 046H: DCB Configuration Output Register

Bit	Type	Function	Default
Bit 31-30	R	Unused	X
Bit 29-0	R	CFG_O[29:0]	0

CFG_O[29:0]

This field contains configuration data read from the offline connection memory page. Configuration data in this field is read from the location specified by the WORDADDR and PORTADDR fields in the Access Mode register. There is a 6 SYSCLK cycle latency from when an indirect read is requested until when correct data appears in this register.

Register 047H: DCB Access Mode Register

Bit	Type	Function	Default
Bit 31	R/W	WRB	1
Bit 30	R/W	ACCMDE	0
Bit 29	R	Unused	X
Bit 28	R/W	Reserved	0
Bit 27-24	R/W	PORTCFG[3:0]	0
Bit 23-21	R	Unused	X
Bit 20	R/W	Reserved	0
Bit 19-16	R/W	PORTADDR[3:0]	0
Bit 15-14	R	Unused	X
Bit 13-0	R/W	WORDADDR [13:0]	0

Writing to this register with the WRB register bit set high initiates an indirect read from the offline connection memory page. WORDADDR selects the offline connection memory page to read from. There is a latency of 6 SYSCLK cycles from when this register is written to with the WRB bit set high until when valid data appears on the Configuration Output register. Indirect reads should be spaced at least 6 SYSCLK cycles apart to permit valid data to appear in the Configuration Output register.

Writing to this register with the WRB register bit set low initiates an indirect write to the offline connection memory page. WORDADDR selects the offline connection memory page to write to. Indirect writes should be spaced at least 4 SYSCLK cycles apart to ensure the writes complete successfully.

While page copy is in progress (UPDATEV register bit = '1'), writing to this register will NOT cause data to be updated to/from the offline connection memory page.

While a page swap is pending (SWAPV register bit = '1'), writing to this register MAY cause unpredictable results as data may be transferred while a page swap is occurring, causing data to be updated to a different connection memory page from the intended.

WRB

The indirect access control bit selects between a write (0) or read (1) access to the offline connection memory page.

ACCMDE

These bits indicate the access mode of the offline connection memory page.

0 : PORT transfer mode.

1 : WORD transfer mode.

In port transfer mode, one port is updated per word of the offline connection memory page.

PORTCFG : new port mapping to be updated to the connection memory page.

WORDADDR : specifies the address of the offline connection memory page.

PORTADDR : port address of the offline connection memory page.

In word transfer mode, an entire word of the offline connection memory page is updated.

PORTCFG : is ignored.

WORDADDR : specifies the address to the offline connection memory page.

PORTADDR : is ignored.

In either mode, the contents read from the offline connection memory page can be read by the microprocessor through the Configuration Output register.

PORTCFG[3:0]

This field contains the input port mapping to a particular output port specified in PORTADDR. Used only in PORT transfer mode. At all other modes, this field is ignored. Valid values are 0-11 when performing writes.

PORTADDR[3:0]

When performing writes to the offline connection memory page, this field indicates the output port to be updated with new mapping in PORTCFG. A PORTADDR of 0 relates to output port 0 of the DCB.

This field is valid in PORT transfer mode and during reading from the Configuration Output register and is ignored in WORD transfer mode. Valid values are 0-11 when performing writes.

When performing reads through the Configuration Output register, PORTADDR indicates the ports being read as follows:

00xx : Ports 5-0

01xx : Ports 11-6

WORDADDR[13:0]

This field indicates the address of the update connection memory page to be accessed. This field relates to the time location within the SBI/TeleCombus frame. i.e. Location 0 would be the first A1 byte of the frame and location 24 is the C1 character.

This field is ignored in page copy mode. Valid values are 0-9719.

Reserved

The Reserved bits must be set to the indicated default value for correct operation of the NSE.

Register 048H: DCB C1 delay (RC1DLY) Register

Bit	Type	Function	Default
Bit 31-6	R	Unused	X
Bit 13-0	R/W	RC1DLY[13:0]	0

RC1DLY[13:0]

This value, equaling the delay (in 77.76 MHz clock periods), between RC1FP and the arrival of the C1 characters in the R8TD. This delay will synchronize the C1 input to the R8TD blocks assuming all the C1 characters have arrived. As the delay on those links is dependent on the system design, backplane propagation delays, cable lengths etc. This value will have to be arrived at empirically. And will have an upper and lower limit for which the middle value should be selected. Refer to the Operations section for more detail and some recommended starting values. For proper operation of the NSE, RC1DLY must not be set to all zeros.

Register 04AH: DCB Frame size Register

Bit	Type	Function	Default
Bit 31-14	R	Unused	X
Bit 13-0	R/W	FRMSZ[13:0]	25F7h

This register specifies the frame size of the SBI or telecom bus frame.

FRMSZ[13:0]

This register specifies the size of the connection memory page in the various switching modes. Legal values:

Value	Switching Mode
1079 (0437h)	Telecombus switching
1079 (0437h)	SBI column switching
9719 (25F7h)	SBI DS0 switching
9719 (25F7h)	SBI DS0 switching with CAS

Register 04CH: DCB Configuration Register

Bit	Type	Function	Default
Bit 31- 8	R	Unused	X
Bit 7-6	R/W	MF_SWAP[1:0]	0
Bit 5	R/W	AUTO	0
Bit 4	R/W	SWAP_PE	0
Bit 3	R/W	UPDATEE	0
Bit 2	R/W	FRAMEE	0
Bit 1	R	SWAPV	0
Bit 0	R	UPDATEV	0

MF_SWAP [1:0]

This bit selects when RC1FP is expected and synchronizes when page swaps can occur. Table below relates MFSWAP to all vital variables from the DCB:

MFSWAP	Config. Page Size	Frame Switching @ (9720 byte frame)	Frame Interrupt	RC1FP expected every	Switching Mode
00	1080	1 frame	1 frame	4 frame	Telecom bus
01	1080	4 frame	4 frame	4 frame	SBI column mode
10	9720	4 frame	4 frame	4 frame	SBI DS0 mode
11	9720	48 frame	48 frame	48 frame	SBI DS0 with CAS

AUTO

This bit enables an automatic copy of the online connection memory page to the offline connection memory page after the connection memory page is switched. Toggling the AUTO bit to '0' while a page copy is in progress will terminate the page copy process.

- 0: automatic update disabled.
- 1: automatic update enabled.

If automatic page copying is used, the page copy will take place automatically whenever the connection memory page swaps. This means that the UPDATEV register bit will be asserted immediately following a change from 1 to 0 in the SWAPV register bit. When the AUTO bit is set, access to the offline connection memory page is restricted from when a page swap is pending until when the page copy is complete.

SWAP_PE

This bit enables the propagation of interrupt to the INT output due to a change in state of SWAPV. This bit does not have an impact on SWAPI bit.

- 0: disables interrupt propagation to the INT output.
- 1: enables interrupt propagation to the INT output.

UPDATEE

This bit enables the propagation of interrupt to the INT output when UPDATEEV changes state from 1 to 0. This bit does not have impact on UPDATEEI bit

- 0: disables interrupt propagation to the INT output.
- 1: enables interrupt propagation to the INT output.

FRAMEE

This bit enables the propagation of interrupt to the INT output when CMP is sampled at the expected RC1FP position. This bit does not have an impact on FRAMEEI bit.

- 0: disables interrupt propagation to the INT output.
- 1: enables interrupt propagation to the INT output.

SWAPV

The SWAPV bit contains the current state of the page swap. This bit is logic 1 when a switch to the connection memory page (CMP) input has been recognized but the page swap has not yet happened. This bit is a logic 0 when page swap is not pending.

When a page swap is pending, writing to the offline page, initiating a page copy or changing the connection memory page through the CMP input pin or the CMP_VAL register bit in the NSE DCB CMP select register (Reg00Ah) may cause corruption of the memory pages.

UPDATEV

This bit is updated when the active connection memory page is copied to the offline connection memory page.

- 0: copying completed.
- 1: copying in progress.

The duration of a page copy is highly dependent on MF_SWAP.

MF_SWAP	SYSCLK Clock cycles required
"00"	1083
"01"	1083
"10"	9723
"11"	9723

When a page copy is in progress, attempting to write to the offline connection memory page will be ignored and attempting to read from the offline connection memory page will return unpredictable results.

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Register 04DH: DCB Interrupt Status Register

Bit	Type	Function	Default
Bit 31-3	X	Unused	0
Bit 2	I	SWAPI	X
Bit 1	I	UPDATEI	X
Bit 0	I	FRAMEI	X

Writing to this register initiates copying of the active connection memory page to the offline connection memory page. When a page swap is pending (SWAPV = '1') writing to this register may cause a corruption of the connection memory pages.

SWAPI

This bit reports and acknowledges a change of state in the SWAPV bit of the Configuration register. This bit is cleared when this register is read. When enabled by SWAPE, the INT output reflects the state of this bit.

UPDATEI

The offline page copy interrupt status bit, UPDATEI reports and acknowledges a change of state from 1 to 0 in the UPDATEV bit of the Configuration register. This signifies that a page copy is complete. This bit is cleared when read. When enabled by the UPDATEE bit, the INT output reflects the state of this bit.

FRAMEI

The frame interrupt status bit reports the sampling of the CMP bit at the expected RC1FP position. When enabled by FRAMEE, frequency of occurrence of FRAMEI is dependent on MF_SWAP. When enabled by the FRAMEE bit, the INT output reflects the state of this bit.

MF_SWAP	FRAMEI occurs every
"00"	1 frame
"01"	4 frames
"10"	4 frames
"11"	48 frames

This bit is cleared when read.

A change in the CMP input should be sequenced to occur as soon as possible after the occurrence of FRAMEI. Changing CMP prior to the occurrence of FRAMEI may cause unpredictable behavior as it may cause CMP to be sampled later than expected.

Register 100H + N*20H, R8TD Control and Status

Bit	Type	Function	Default
Bit 31:16	R	Unused	X
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13:10	R	Unused	X
Bit 9	R/W	RXINV	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the R8TD blocks.

FOCA

The force out-of-character-alignment bit (FOCA) control the operation of the character alignment block in the R8TD block. A 0-1 transition on this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). Before another force operation can be performed, FOCA must first be set to logic 0.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block in the R8TD block. A 0-1 transition on this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). Before another force operation can be performed, FOFA must first be set to logic 0.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block in the R8TD block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block in the R8TD block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out of character alignment interrupt enable bit (OCAE) masks the contribution of the change of character alignment event indication bit (OCAI) in the R8TD block to INTB. When OCAE is high, INTB is asserted low when OCAI is high. INTB is not affected by the value of OCAI when OCAE is low.

OFAE

The out of frame alignment interrupt enable bit (OFAE) masks the contribution of the change of frame alignment event indication bit (OFAI) in the R8TD block to INTB. When OFAE is high, INTB is asserted low when OFAI is high. INTB is not affected by the value of OFAI when OFAE is low.

LCVE

The line code violation interrupt enable bit (LCVE) masks the contribution of the line code violation event indication bit (LCVI) in the R8TD block to INTB. When LCVE is high, INTB is asserted low when LCVI is high. INTB is not affected by the value of LCVI when LCVE is low.

FUOE

The FIFO underrun/overflow status interrupt enable bit (FUOE) masks the contribution of the FIFO underrun/overflow event indication bit (FUOI) in the R8TD block to INTB. When FUOE is high, INTB is asserted low when FUOI is high. INTB is not affected by the value of FUOI when FUOE is low.

RXINV

The receive data invert bit (RXINV) controls the active polarity of the incoming data stream. When RXINV is set high, the data is complemented before any processing by the R8TD. When RXINV is set low, data is not complemented before R8TD processing.

Reserved

The Reserved bits must be set to the indicated default value for correct operation of the NSE.

Register 101H + N*20H, R8TD Interrupt Status

Bit	Type	Function	Default
Bit 31:8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3:0		Unused	X

These registers reports interrupt status due to change of character alignment events and detection of line code violations for the R8TD block.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state events for the R8TD block. OCAI is set high when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state since the last clear for the register. OCAI is cleared on a read to this register when WCIMODE is logic 0. OCAI is cleared on a write (of any value) to this register when WCIMODE is logic 1. INTB is asserted low when both OCAE and OCAI are high. If OCAE is asserted, OCAI must be cleared before INTB will be reasserted.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state events for the R8TD block. OFAI is set high when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is cleared on a read to this register when WCIMODE is logic 0. OFAI is cleared on a write (of any value) to this register when WCIMODE is logic 1. INTB is asserted low when both OFAE and OFAI are high. IF OFAE is asserted, OFAI must be cleared before INTB will be reasserted.

LCVI:

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation events for the R8TD block. LCVI is set high when the character alignment block detects a line code violation in the incoming data stream. LCVI is cleared on a read to this register when WCIMODE is logic 0. LCVI is cleared on a write (of any value) to this register when WCIMODE is logic 1. INTB is asserted low when both LCVE and LCVI are high. IF LCVE is asserted, LCVI must be cleared before INTB will be reasserted.

FUOI

The FIFO underrun/overflow event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overflow events for the R8TD block. FUOI is set high when R8TD detects a that the FIFO read and write pointers are within one slot of each other. FUOI is cleared on a read to this register. INTB is asserted low when both FUIOE and FUOI are high. IF FUIOE is asserted, FUOI must be cleared before INTB will be reasserted.

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Register 102H + N*20H, R8TD Line Code Violation Count

Bit	Type	Function	Default
Bit 31:16		Unused	X
Bit 15:0	R	LCV[15:0]	X

This register reports the number of line code violations in the previous accumulation period for the R8TD blocks.

LCV[15:0]

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing to this register or by writing to the NSE Master Clock Monitor, Accumulation Trigger register (Reg009h). The write access transfers the internally accumulated error count to the LCV register within 6 SYSCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation. The NSE R8TD TIP register (Reg00Dh) can be used to determine when it is safe to read the LCV count register (instead of waiting for 6 SYSCLK cycles).

Register 103H + N*20H, RXLV and DRU Control

Bit	Type	Function	Default
Bit 31:16	R	Unused	X
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the DRU and RXLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

NOTE: THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE R8TD BLOCKS. TO DISABLE THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H

DRU_ENB

Setting this bit high will disable the DRU.

RX_ENB

Setting this bit high will disable the RXLV.

A_RSTB

Setting this bit low will reset the DRU and RXLV blocks.

Reserved

The Reserved bits should be set as described above.

Register 108H + N*20H, T8TE Control and Status

Bit	Type	Function	Default
Bit 31:6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

These registers provide, control and report the status of the T8TE blocks.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the outgoing data stream. While DLCV is logic 1 and TCBMODE is logic 0, the transmitted 8B/10B codes are inverted. This will result in at least one disparity error at a receive 8B/10B decoder. When the NSE is configured with TCBMODE logic 1, and DLCV logic 1, 8B/10B data characters are inverted while the TeleCombus control characters are not inverted. When DLCV is logic 0, no code inversion is performed.

CENTER:

The FIFO centering control bit (CENTER) controls the separation of the T8TE FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set after CSU lock has been achieved to properly center the FIFO.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, TP[9:0] in the T8TE Test Pattern register is selected for output.

FIFOERRE

The FIFO underrun/overflow error interrupt enable bit (FIFOERRE) masks the contribution of the FIFO underrun/overflow event indication bit (FIFOERRI) in the T8TE block to INTB. When FIFOERRE is high, INTB is asserted low when FIFOERRI is high. INTB is not affected by the value of FIFOERRI when FIFOERRE is low.

Reserved

The Reserved bit must be set to the indicated default value for correct operation of the NSE.

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Register 109H + N*20H, T8TE Interrupt Status

Bit	Type	Function	Default
Bit 31:5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3:0		Unused	X

These registers report the interrupt status for T8TE blocks #0 through #11.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFOERRI is set high when when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is cleared on a read to this register when WCIMODE is logic 0. FIFOERRI is cleared on a write (of any value) to this register when WCIMODE is logic 1. INTB is asserted low when both FIFOERRE and FIFOERRI are high. IF FIFOERRE is asserted, FIFOERRI must be cleared before INTB will be reasserted.

Register 10AH + N*20H: T8TE Time-slot Configuration #1

Bit	Type	Function	Default
Bit 31:16	R	Unused	X
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

Register 02H configures the path termination mode of time-slots 1 to 8 of the T8TE.

TMODE1[1:0]-TMODE8[1:0]

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the T8TE. Time-slots are numbered in order of transmission in the Incoming TeleCombus stream (ID[7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-12) determines which set of TeleCombus control signals are to be encoded in 8B/10B characters.

In TeleCombus mode, the T8TE encodes TeleCombus control signals such as transport frame and payload boundaries, pointer justification events and alarm conditions into three levels of an extended set of 8B/10B characters as well as performing the IEEE mode conversion on data. The three hierarchical levels are Multiplex Section Termination (MST) High-order Path Termination (HPT) and Low-order Path Termination (LPT). For correct operation see table below:

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in Telecom Bus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in Telecom bus mode where valid

TMODEx[1]	TMODEx[0]	Functional Description
		V1/V2 pointers must be preserved.
1	0	LPT level. This mode must be used for SBI336 mode and in Telecom bus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

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Register 10BH + N*20H: T8TE Time-slot Configuration #2

Bit	Type	Function	Default
Bit 31:8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

Register 03H configures the path termination mode of time-slots 9 to 12 of the T8TE.

TMODE9[1:0]-TMODE12[1:0]

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the T8TE. Time-slots are numbered in order of transmission in the Incoming TeleCombus stream (ID[7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-12) determines which set of TeleCombus control signals are to be encoded in 8B/10B characters.

In TeleCombus mode, the T8TE encodes TeleCombus control signals such as transport frame and payload boundaries, pointer justification events and alarm conditions into three levels of an extended set of 8B/10B characters as well as performing the IEEE mode conversion on data. The three hierarchical levels are Multiplex Section Termination (MST), High-order Path Termination (HPT) and Low-order Path Termination (LPT). For correct operation see table below

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST level. This mode must be used when in Telecom Bus mode with valid H1/H2 pointers where it is not important to mark the location of the J1 byte.
0	1	HPT level. This mode must be used when in Telecom bus mode where valid V1/V2 pointers must be preserved.
1	0	LPT level. This mode must be used for SBI336 mode and in Telecom bus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

Register 10CH + N*20H, T8TE Test Pattern

Bit	Type	Function	Default
Bit 31:10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

These registers store the test pattern for test pattern insertion for the T8TE blocks.

TP[9:0]

The Test Pattern register (TP[9:0]) for T8TE block #X contains the test pattern conditionally inserted into output data stream #X. TP[9:0] is inserted into the output data stream when the TPINS bit is set high.

Register 10DH + N*20H, TXLV and PISO Control

Bit	Type	Function	Default
Bit 31:12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

These registers control the operation of LVDS Transmit and PISO blocks.

ARSTB

Setting this bit low will reset the PISO and TXLV blocks.

PISO_ENB

Setting this bit high will disable the PISO circuitry.

TXLV_ENB

Setting this bit high will disable the TXLV circuitry.

Reserved

The Reserved bits must be set to the indicated default value for correct operation of the NSE.

Register 110H + N*20H, ILC Transmit FIFO Data

Bit	Type	Function	Default
Bit 31:0	R/W	TDAT[31:0]	0

TDAT[31:0]

TDAT[31: 0] Transmit FIFO form the 32 bit wide data word to be written to the register file FIFO. A single 32 bit write to this register will update TDAT[31:0]. A write to this address initiates a FIFO write sequence.

Register 111h + N*20H, ILC Transmit Control Register

Bit	Type	Function	Default
Bit 31:16		Unused	X
Bit 15:8	R/W	TX_AUX[7:0]	00000000
Bit 7:6	R	Reserved	00
Bit 5:4	R/W	TX_LINK[1:0]	00
Bit 3:2	R	Reserved	00
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

TX_BYPASS

When this bit is set to '1', the blocks message transmit functions are bypassed. No messages are inserted into the Transmit Bus data. The respective signals are passed through the block's pipeline unmodified. Transmit message FIFO RAM is disabled and thus message data writes are ignored.

TX_CRC_SWIZ_EN

When this bit is set to '1', the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

TX_LINK[1:0]

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.

TX_AUX[7:0]

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the inband link. A new value of TX_AUX will be transmitted at the next available message.

Data read from this register will be the data previously written.

Register 112h + N*20H, ILC Transmit Misc.Status and FIFO Synch Register

Bit	Type	Function	Default
Bit 31:16		Unused	X
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14:13	R	TX_LINK[1:0]	00
Bit 12:11	R	IPAGE[1:0]	00
Bit 10:8	R	IUSER[2:0]	000
Bit 7:6	R	Reserved	00
Bit 5:2	R	TX_MSG_LVL[3:0]	0000
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

This register serves a dual purpose dependant on whether it is being read or written.

When it is read it returns the status for the Message Transmit Channel.

When it is written (with 0001h) to it is used it synchronize the Transmit FIFO to the start of a message boundary.

TX_XFER_SYNC

Writing '1' to this bit initializes the next write sequence to be to the beginning of the next message. After a '1' had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX_XFER_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a '1' will have no affect.

On reads this bit is always returned as a '0'.

TX_FI_BUSY

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

User and Page bits are a copy of the User bits received, and being transmitted in 0Ch. These allow one read in the 32 bit device to gain a snapshot of the entire ILC.

TX_MSG_LVL[3:0]

This indicates the current number of messages in the TXFIFO.

Table 7 TX FIFO Message Level

TX_MSG_LVL[3:0]	Number of messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by (8 – TX_MSG_LVL).

IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the transmit serial link. IUSER[2:0] is source from the TX_ILC_USER_2[31:0], TX_ILC_USER_1[31:0], TX_ILC_USER_0[31:0] bits of registers 010H, 00FH, 00EH relatively at a bit position equal to the link number.

IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the transmit serial link. IPAGE[1:0] is source from the TX_ILC_PAGE_1[31:0], TX_ILC_PAGE_0[31:0] bits of registers 004H, 003H relatively at a bit position equal to the link number.

TX_LINK[1:0]

These bits reflect the last written value of the TX_LINK field of the TX Control register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

TX_MSG_LVL_VALID

This bit indicates that the value of TX_MSG_LVL is valid. When read with a '0' this register should be re-read until TX_MSG_LVL_VALID is a '1'. This bit will be clear for only approximately 0.12% of time.

Register 113h + N*20H, ILC Receive FIFO Data Register

Bit	Type	Function	Default
Bit 31:0	R	RDAT[31:0]	00000000h

RDAT[31:0]

RDAT[31: 0] is the 32 bit wide data word read from the FIFO.

A single read from this register will update RDAT[31:0]. A read from this address initiates a FIFO read sequence.

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Register 114h + N*20H, ILC Receive Control Register

Bit	Type	Function	Default
Bit 31:3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

RX_BYPASS

When this bit is set to '1', the blocks message receive functions are bypassed. No messages are extracted from the Receive Telecom bus. The RXTPL , RXPL and RXDATA signals are passed through the blocks pipeline unmodified. Receive message FIFO RAM is disabled and thus message data reads return undefined data.

RX_CRC_SWIZ_EN

When this bit is set to '1', the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

Reserved

Default Value is '0', but should be set to '1' for correct operation.

Register 115h + N*20H, ILC Receive Auxiliary, Status and FIFO Synch Register

Bit	Type	Function	Default
Bit 31:24		Unused	X
Bit 23:16	R	RX_AUX[7:0]	00h
Bit 15	R	RX_STTS_VALID	X
Bit 14:13	R	RX_LINK[1:0]	00
Bit 12:11	R	RX_PAGE[1:0]	00
Bit 10:8	R	RX_USER[2:0]	000
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5:2	R	RX_MSG_LVL[3:0]	0000
Bit 1	R	RX_FI_BUSY	0
Bit 0	W	RX_XFER_SYNC	X
Bit 0	R	RX_SYNC_DONE	0

When this register is read, it returns the status for the Receive Message Channel. When a logic 1 is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.

RX_XFER_SYNC

Writing a logic 1 to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the ILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the ILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic 1 at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX_MSG_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1st message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic 1 software should not start reading the FIFO until the RX_FI_BUSY bit has cleared. In the worst case this will take 4 SYSCLK cycles.

At this point the 1st DWORD of the message is available for reading and the CRC_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic 1 again.

Whenever the R8TD block is not in frame or character alignment, the ILC will be receiving random data and the ILC receive message FIFO will be filled with this random data. Once the R8TD is in character alignment and in frame alignment (OCAV and OFAV in register Reg100H + N*20H are low), this bit should be written to 8 times before attempting to use the ILC. This will flush out the receive message FIFO.

On reads this bit is always returns the RX_SYNC_DONE status.

RX_SYNC_DONE

This bit indicates the status of an RX_XFER_SYNC operation. When this bit is a logic 1, it indicates that an RX_XFER_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

RX_FI_BUSY

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX_XFER_SYNC bit set or following a read from the ILC Receive FIFO Data Low register.

Following an RX_XFER_SYNC write this bit need not be read by software if

the time interval to the successive Receive FIFO DATA register read is greater than approximately 4 SYSCLK cycles.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 3 SYSCLK cycles.

RX_MSG_LVL[3:0]

This indicates the current number of messages in the Receive FIFO.

Table 8 RX FIFO Message Level

RX_MSG_LVL[3:0]	Number of messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

HDR_CRC_ERR

If this bit is set to a logic 1, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

CRC_ERR

If this bit it set to '1', the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX_XFER_SYNC operation has completed. This bit is valid when RX_FI_BUSY is a logic 0 following a Receive FIFO Synchronization.

The software must only check the status of this bit before reading the first Dword of a message from the receive FIFO.

RX_USER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) of the in-band link on the receive serial link.

RX_PAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) of the in-band link on the receive serial link.

RX_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link.

RX_STTS_VALID

This bit indicates that the values of RX_MSG_LVL , RX_LINK, RX_PAGE, RX_USER, RX_AUX are valid. When read with a logic 0 this register should be re-read until RX_STTS_VALID is a logic 1. This bit will be cleared for only approximately 0.15% of time.

RX_AUX[7:0]

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

Register 116h + N*20H, ILC Interrupt Enable and Control Register

Bit	Type	Function	Default
Bit 31:16		Unused	X
Bit 15:13	R	Reserved	000
Bit 12:11	R/W	RX_TIMEOUT_VAL[1:0]	00
Bit 10:8	R/W	RX_THRESHOLD_VAL[2:0]	101
Bit 7	R	Reserved	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2:1	R/W	RX_PAGE_CHGE[1:0]	0
Bit 0	R/W	RX_USER0_CHGE	0

Bits 0 through 6 are updated on the reception of a message, regardless of payload, as long as the CRC check indicated no error.

The indicated default values in this register is only valid after clearing the associated NSE individual Channel Reset bit in register 001h.

RX_USER0_CHGE:

Writing a '1' to the RX_USER0_CHGE bit enables the generation of an interrupt on a change of state from a '0' to a '1' of received message header bit RX_USER[0].

RX_PAGE_CHGE[1:0]:

Writing a '1' to the RX_PAGE_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The RX_PAGE bits that changed value are indicated by a '1' in the corresponding RX_PAGE_CHGI[n].

RX_LINK_CHGE:

Writing a '1' to the RX_LINK_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX_LINK_CHGI bit will be set to a '1'.

If the RXFIFO level had reached the threshold value an interrupt will be generated if this bit is '1'. To disable set to '0'.

RX_OVFLWE

Writing a '1' to the RX_OVFLWE bit enables the generation of an interrupt when RX_OVFLWI is a '1'.

RX_THRSHLDE

Writing a '1' to the RX_THRSHLDE bit enables the generation of an interrupt when RX_THRSHLDI is a '1'

RX_TIMEOUTE

Writing a '1' to the RX_TIMEOUTE bit enables the generation of an interrupt when RX_TIMEOUTI is a '1'

RX_THRSHLD_VAL[2:0]

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

Table 9 RXFIFO Threshold Values

RX_THRSHLD_VAL [2:0]	Messages
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

RX_TIMEOUT_VAL:

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

Table 10 RXFIFO Timeout Delay

RX_TIMEOUT_VAL [1:0]	Nominal Delay In Frames	Minimum Delay from message reception	Maximum Delay from message reception	Minimum Delay from FIFO read	Maximum Delay from FIFO read
00	1	152us	222 us	125us	250 us
01	2	277us	347 us	250us	375us
10	3	402us	472 us	375us	500us
11	4	527us	597 us	500us	625 us

Registers: 117h + N*20H, ILC Interrupt Reason Register

Bit	Type	Function	Default
Bit 31:16		Unused	X
Bit 15:7	R	Reserved	00000000
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2:1	R	RX_PAGE_CHGI[1:0]	0
Bit 0	R	RX_OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts.

All bits in this register are cleared on read

RX_OUSER0_CHGI

A '1' in this bit indicates that the last received value of the RX_USER[0] header bit has changed from a '0' to a '1' from the previously received values. This bit is cleared on a read.

RX_PAGE_CHGI [1:0]

A '1' in these bits indicates that the last received value of the corresponding RX_PAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

RX_LINK_CHGI

A '1' in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.

RX_OVFLWI

This bit, when '1', indicates a Receive FIFO Overflow. This bit is cleared on a read.

RX_THRSHLDI

This bit, when '1', indicates a Receive FIFO Threshold reached. This bit is cleared on a read.

RX_TIMEOUTI

This bit, when '1', indicates a Receive FIFO Timeout. This bit is cleared on read.

11 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the NSE. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[11]) is high.

In addition, the NSE also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

11.1 JTAG Test Port

The NSE JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 11 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 12 Identification Register

Length	32 bits
Version Number	1H
Part Number – NSE-8G	8620H
Manufacturer's Identification Code	0CDH
Device Identification – NSE-8G Rev. B	186200CDH

Table 13 Boundary Scan Register

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OEB_INTB	121	OUT_CELL	L

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
INTB	120	OUT_CELL	L
ALE	119	IN_CELL	L
CSB	118	IN_CELL	H
WRB	117	IN_CELL	H
RDB	116	IN_CELL	L
A[11]	115	IN_CELL	L
A[10]	114	IN_CELL	L
A[9]	113	IN_CELL	L
A[8]	112	IN_CELL	H
A[7]	111	IN_CELL	H
A[6]	110	IN_CELL	L
A[5]	109	IN_CELL	L
A[4]	108	IN_CELL	L
A[3]	107	IN_CELL	H
A[2]	106	IN_CELL	L
A[1]	105	IN_CELL	L
A[0]	104	IN_CELL	L
OEB_D[31]	103	OUT_CELL	L
D[31]	102	IO_CELL	L
OEB_D[30]	101	OUT_CELL	L
D[30]	100	IO_CELL	L
OEB_D[29]	99	OUT_CELL	L
D[29]	98	IO_CELL	L
OEB_D[28]	97	OUT_CELL	H
D[28]	96	IO_CELL	H
OEB_D[27]	95	OUT_CELL	L
D[27]	94	IO_CELL	L
OEB_D[26]	93	OUT_CELL	H
D[26]	92	IO_CELL	H
OEB_D[25]	91	OUT_CELL	L
D[25]	90	IO_CELL	H
OEB_D[24]	89	OUT_CELL	-
D[24]	88	IO_CELL	-
OEB_D[23]	87	OUT_CELL	-
D[23]	86	IO_CELL	-
OEB_D[22]	85	OUT_CELL	-
D[22]	84	IO_CELL	-
OEB_D[21]	83	OUT_CELL	-
D[21]	82	IO_CELL	-
OEB_D[20]	81	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
D[20]	80	IO_CELL	-
OEB_D[19]	79	OUT_CELL	-
D[19]	78	IO_CELL	-
OEB_D[18]	77	OUT_CELL	-
D[18]	76	IO_CELL	-
OEB_D[17]	75	OUT_CELL	-
D[17]	74	IO_CELL	-
OEB_D[16]	73	OUT_CELL	-
D[16]	72	IO_CELL	-
OEB_D[15]	71	OUT_CELL	-
D[15]	70	IO_CELL	-
OEB_D[14]	69	OUT_CELL	-
D[14]	68	IO_CELL	-
OEB_D[13]	67	OUT_CELL	-
D[13]	66	IO_CELL	-
OEB_D[12]	65	OUT_CELL	-
D[12]	64	IO_CELL	-
OEB_D[11]	63	OUT_CELL	-
D[11]	62	IO_CELL	-
OEB_D[10]	61	OUT_CELL	-
D[10]	60	IO_CELL	-
OEB_D[9]	59	OUT_CELL	-
D[9]	58	IO_CELL	-
OEB_D[8]	57	OUT_CELL	-
D[8]	56	IO_CELL	-
OEB_D[7]	55	OUT_CELL	-
D[7]	54	IO_CELL	-
OEB_D[6]	53	OUT_CELL	-
D[6]	52	IO_CELL	-
OEB_D[5]	51	OUT_CELL	-
D[5]	50	IO_CELL	-
OEB_D[4]	49	OUT_CELL	-
D[4]	48	IO_CELL	-
OEB_D[3]	47	OUT_CELL	-
D[3]	46	IO_CELL	-
OEB_D[2]	45	OUT_CELL	-
D[2]	44	IO_CELL	-
OEB_D[1]	43	OUT_CELL	-
D[1]	42	IO_CELL	-
OEB_D[0]	41	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
D[0]	40	IO_CELL	-
Logic 1	39	IN_CELL	-
Logic 1	38	IN_CELL	-
Logic 1	37	IN_CELL	-
Logic 1	36	IN_CELL	-
Logic 1	35	IN_CELL	-
Logic 1	34	IN_CELL	-
Logic 1	33	IN_CELL	-
Logic 1	32	IN_CELL	-
Logic 1	31	IN_CELL	-
Logic 1	30	IN_CELL	-
Logic 1	29	IN_CELL	-
Logic 1	28	IN_CELL	-
Logic 1	27	IN_CELL	-
Logic 1	26	IN_CELL	-
CMP	25	IN_CELL	-
SYSCLK	24	IN_CELL	-
RC1FP	23	IN_CELL	-
OEB_TC1FP	22	OUT_CELL	-
TC1FP	21	OUT_CELL	-
RSTB	20	IN_CELL	-
Logic 1	19	IN_CELL	-
Logic 1	18	IN_CELL	-
Logic 1	17	IN_CELL	-
Logic 1	16	IN_CELL	-
Logic 1	15	IN_CELL	-
Logic 1	14	IN_CELL	-
Logic 1	13	IN_CELL	-
Logic 1	12	IN_CELL	-
Logic 1	11	IN_CELL	-
Logic 1	10	IN_CELL	-
Logic 1	9	IN_CELL	-
Logic 1	8	IN_CELL	-
Logic 1	7	IN_CELL	-
Logic 1	6	IN_CELL	-
Logic 1	5	IN_CELL	-
Logic 1	4	IN_CELL	-
Logic 1	3	IN_CELL	-
Logic 1	2	IN_CELL	-
Logic 0	1	IN_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
Logic 1	0	IN_CELL	-

Notes:

1. When set high, INTB will be set to high impedance.
2. Enable cell OEB_ *pinname*, tristates pin *pinname* when set high.
3. OEB_INTB is the first bit of the boundary scan chain.
4. Cells 'Logic 1' are Input Observation cells whose input pad is pull-up to VDD internally.
5. Cells "Logic 0" are Input Observation cells whose input pad is tied to VSS.

11.1.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 11 Input Observation Cell (IN_CELL)

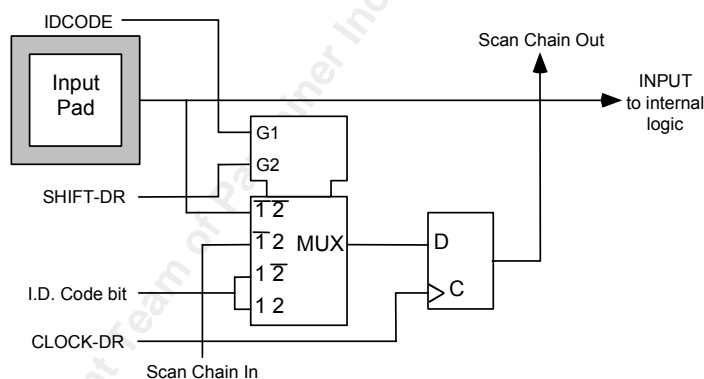
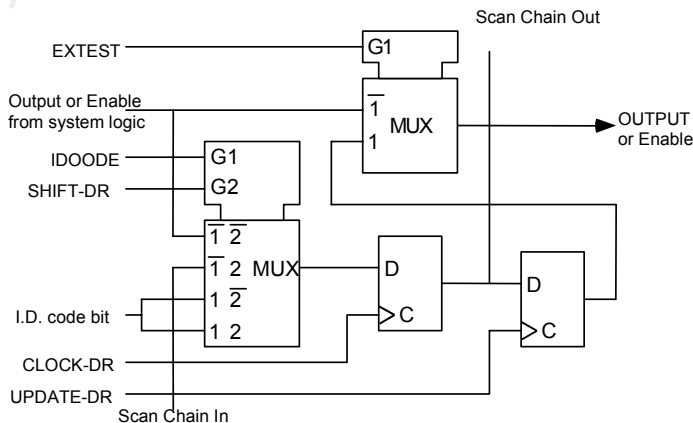


Figure 12 Output Cell (OUT_CELL)



12 Operation

There are several important aspects regarding the operation of NSE-based switch fabrics; these are dealt with in turn in the following sections.

12.1 Software Default settings

12.1.1 T8TE Time-slot Configuration #1 register:

To be set to 0000AAAAh to set T8TE to LPT mode to ensure Low Order Path signals are encoded in outgoing 8b/10b characters. Or, set to 00005555h to set T8TE to HPT mode to ensure V1/V2 bytes are preserved. Or, set to 00000000h to set T8TE to MST mode to ensure J1 bytes are preserved.

12.1.2 T8TE Time-slot Configuration #2 register:

To be set to 000000AAh to set T8TE to LPT mode to ensure Low Order Path signals are encoded in outgoing 8b/10b characters. Or, set to 00000055h to set T8TE to HPT mode to ensure V1/V2 bytes are preserved. Or, set to 00000000h to set T8TE to MST mode to ensure J1 bytes are preserved.

12.1.3 Configuring the NSE to use fewer links:

The NSE powers up with the software digital reset disabled, software analog reset disabled and individual link reset enabled. This means that only the digital blocks are enabled post hardware reset (since setting channel reset also disable the associated analog blocks). The CSU by default will be start upon NSE powers up; it can only be reset by the firmware writing '1' to the ARESET bit in NSE Master Reset register (000H). By writing '0' to appropriate channels in NSE Individual Channel Reset register (001H) will bring the associated link out of reset and operational for normal mode operation.

When fewer than 12 links are used in the NSE 8G, the unused links should be disabled individually by writing '1' to the appropriate NSE Individual Channel Reset register (001H) bit. Writing '1' to bit N of NSE Individual Channel Reset register will disable the R8TD, ILC, and T8TE of channel N. This reset controls both the digital as well as the analog reset inputs of the R8TD and T8TE. The analog reset input of R8TD and T8TE gates the analog reset and enable output that is used to disable the associated DRU/RXLV, PISO/TXLV analog blocks. This will cause the entire link from input N to output N to be disabled.

Reset states of various operation modes:

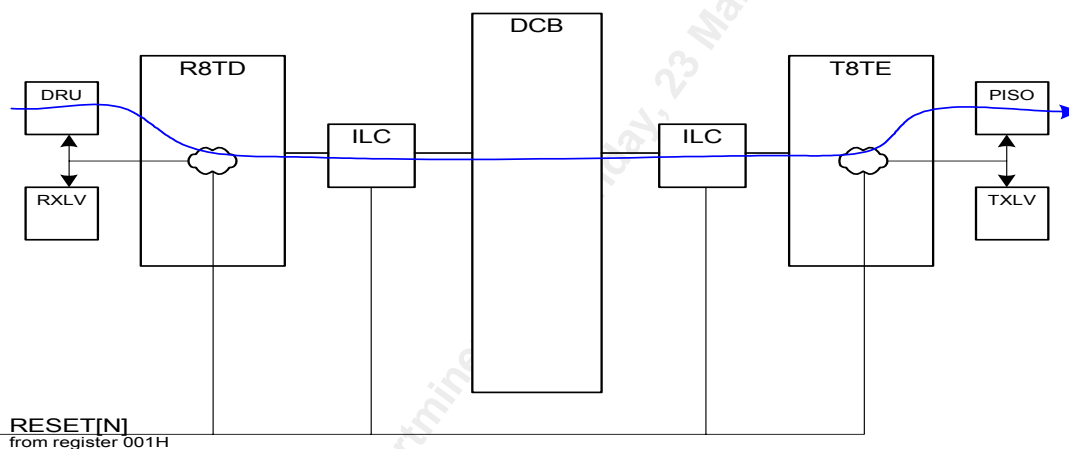
Post Hardware Reset:

Register 000H : DRESET	'0'
Register 000H : ARESET	'0'
Register 001H : RESET	'0xFFFFFFFF'

Normal mode:

Register 000H : DRESET	'0'
Register 000H : ARESET	'0'
Register 001H : RESET	link dependent

Figure 15 Shutting down a link



12.1.4 PCB Design Notes

To maintain flexibility, all unused LVDS outputs should be left floating, all unused LVDS inputs can either be left floating or grounded. This will prevent accidental damage caused by firmware enabling outputs, or releasing resets of inactive ports.

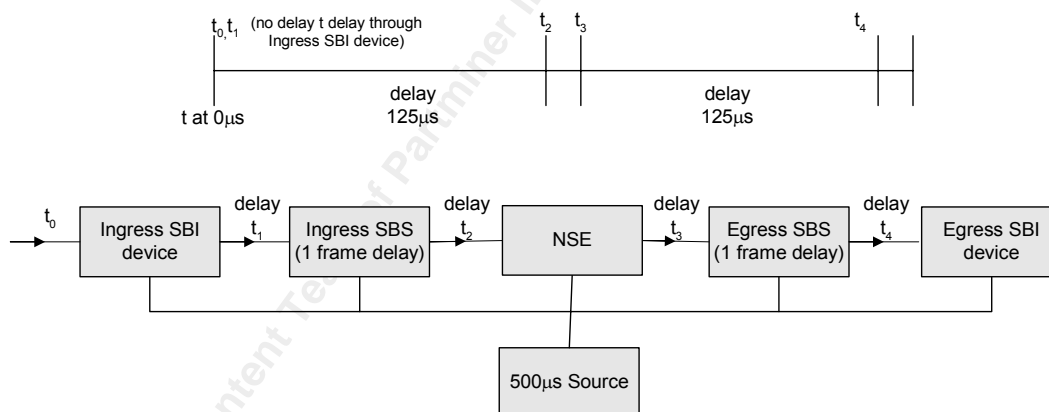
12.2 “C1” Synchronization.

Any NSE/SBS/SBSLITE fabric can be viewed as a collection of five “columns” of devices: column 0 consists of the ingress flow from the load devices (e.g., some SBI device); column 1 consists of the ingress flow through the SBS devices; column 2 consists of the NSE-8G device; column 3 consists of the egress flow through the SBS devices; and column 4 consists of the egress flow through the load devices (e.g. some SBI device). Note that the devices in columns 0 and 4 are SBI bus devices while columns 1 and 3 are SBS or SBSLITE devices. The dual column references refer to their two separate simplex flows. Path-aligned STS-12 frames are pipelined through this structure in a regular fashion, under control of a single clock source and frame pulse. There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.

A timing pulse for SBI frames (2kHz, 500 μ s) is generated and fed to each device in the fabric. Each chip has a *FrameDelay* register (RC1DLY) which contains the count of 77.76 MHz clock ticks that device should delay from the reference timing pulse before expecting the C1 characters of the ingress STS-12 frames to have arrived. The base timing pulse is called t . The delays from t based on the settings of the RC1DLY registers in the successive columns of the devices are called t_0, \dots, t_4 . The first signal, t_1 (equal to t_0), determines the start of an STS-12 frame; this signal is used to instruct the ingress load devices (column 0) to start emitting an STS-12 frame (with its special “C1” control character) at that time. t_1 is determined by the customer, based on device and wiring delays to be approximately the earliest time that all “C1” characters will have arrived in the ingress FIFOs of the t_1 column of devices. t_1 is selected to provide assurance that all “C1” characters have arrived at the i^{th} column. The i^{th} column of devices use the t_1 signal to synchronize emission of the STS-12 frames. The ingress FIFOs permit a variable latency in C1 arrival of up to 16 clock cycles.

Note: the SBS device, being a memory switch adds a latency of one complete frame or row plus a few clock ticks to the data, as described in the SBS Engineering Document.

Figure 16 “C1” Synchronization Control



12.3 Synchronized Control Setting Changes

The NSE-8G and SBS/SBSLITE support dual switch control settings. These dual settings permit one bank of settings to be operational while the other bank is updated as a result of some new connection requests. The CMP input selects the current operational switch control settings. CMP is sampled by the NSE-8G on the RC1FP. The internal blocks sample the registered CMP value as they receive the next C1 character –after a delay of RC1DLY. The new CMP value is applied on the first A1 character of the following STS-12 multiframe. This switchover is hitless; the control change does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted (see the discussion of the connection routing algorithm in this document).

The DS0-granularity switch settings RAM is organized into two control setting banks, these are switched by the above mechanisms on C1 boundaries. The NSE also has to coordinate the switching of the connected SBS devices (if using the In-Band link facility), so a broader understanding of the issues is required.

To illustrate the system, the following describes actual examples:

12.3.1 SBS/NSE Systems with DS0 and CAS Switching

When building a DS0 and Channel Associated Signaling switching system with the SBS, SBSLITE and NSE devices the overall timing is based on the CAS signaling multiframe on the SBI bus. In this configuration the delay through the SBS devices is a single 125uS SBI frame plus a few 77.76MHz clocks and the delay through the NSE is a few 77.76MHz clocks. A single C1FP frame synchronization signal is distributed around the system. Internal to the SBS and NSE devices are programmable offsets used to account for propagation delays through the system. The key constraint is that all SBI frames are aligned going into the NSE device.

Compatible devices are TEMUX84, FREEDM336, FREEDM336-84, IMA84, and other future SBI336 devices.

The SBS and NSE devices have two configuration pages controlling the switching of each DS0 with CAS. The SBS has independent configuration pages for each direction of data flow through the device. The NSE has one set of configuration pages. System configuration changes are made by writing to the offline configuration page in all affected devices and then swapping from the old configuration page to the new configuration page. The ICMP and OCOMP signals control the current configuration page of the SBS and the CMP signal controls the current configuration page of the NSE. Swapping of configuration pages must be aligned to frame switching through the system to avoid any possible data corruption. The ICMP, OCOMP and CMP signals are sampled with the SBS IC1FP and RC1FP signals and the NSE RC1FP signals respectively. The CMP signals can be connected together at the expense of having to ensure all device configuration pages are current.

The following diagram shows how the devices are connected together. The following timing diagrams show the external signals and the internal device frame alignment signal generated from the programmed delays. Although the CMP signals are sampled externally with the C1FP signals they are also delayed internally to coincide with the internally delayed frame signals. These are also shown in the timing diagram. All internal signals are identified by the .INT suffix.

Figure 17 Temux84/SBS/NSE/SBS/AALIGATOR32 system DS0 Switching with CAS

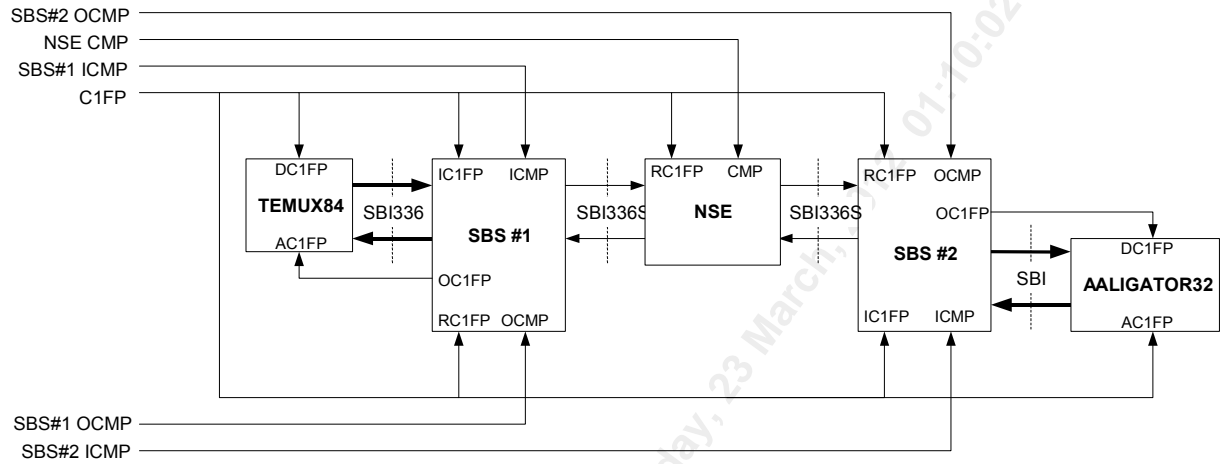


Figure 18 CAS Multiframe Timing

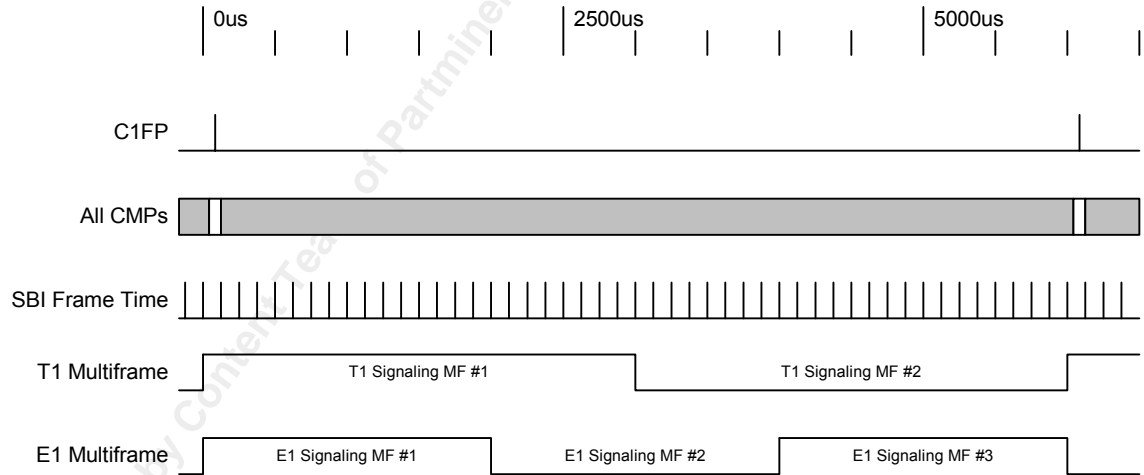
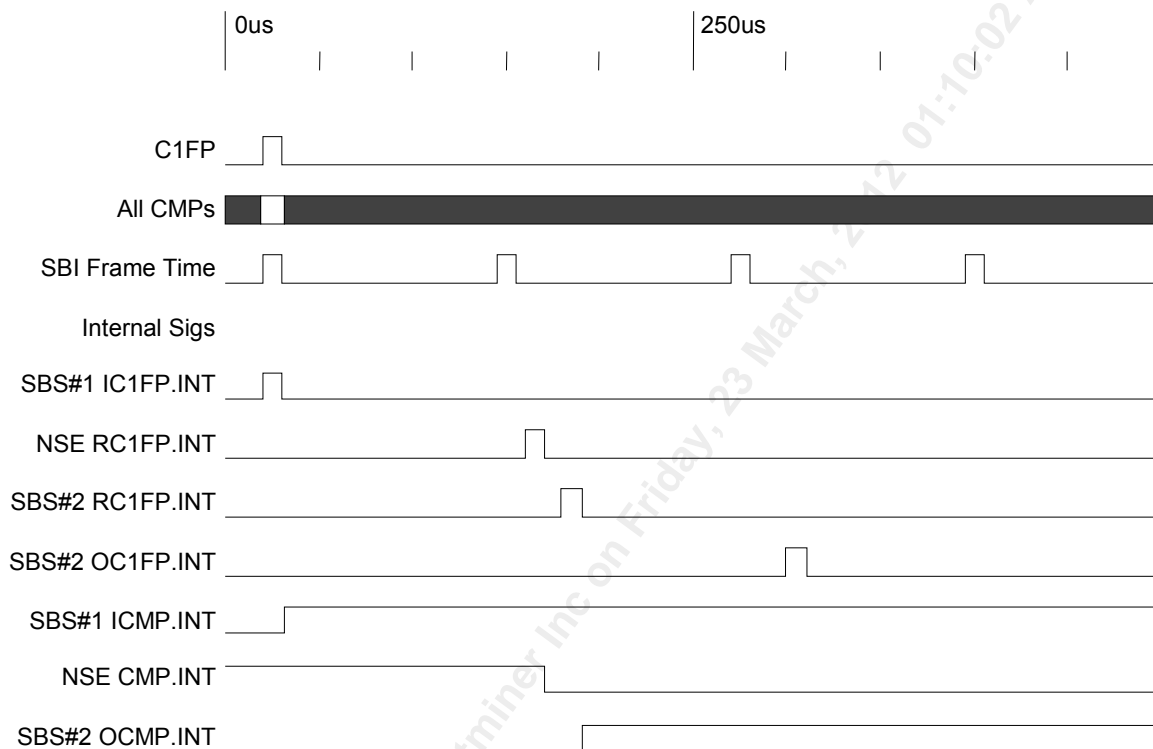


Figure 19 Switch Timing DSOs with CAS

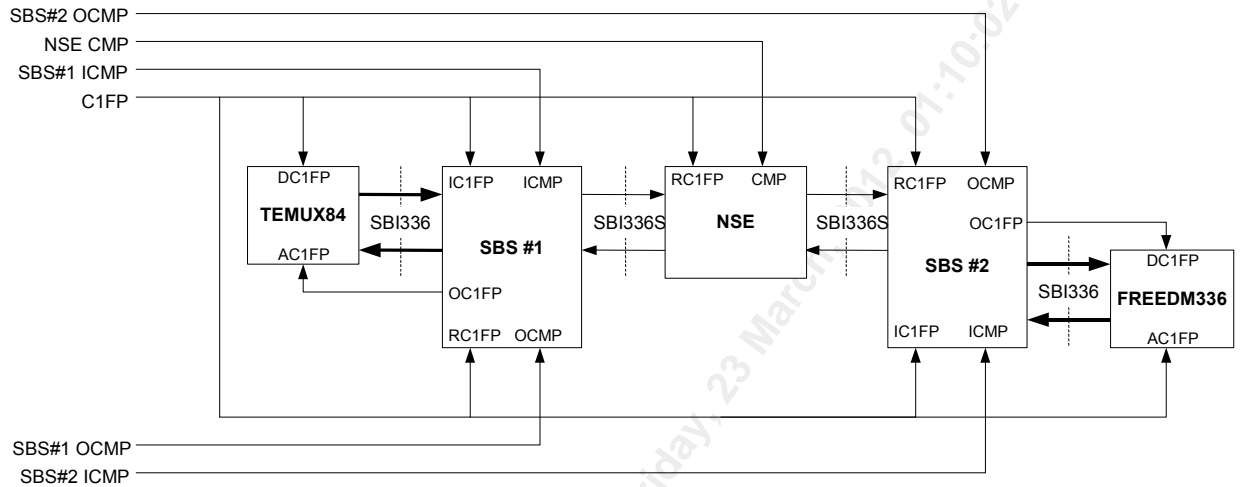


12.3.2 SBS/NSE Systems Switching DS0s without CAS

This is very similar to the DS0 switching system configuration with CAS described in the previous section. The only difference is that in this system the global C1FP can be reduced to every SBI multiframe rather than the longer 48-frame SBI bus signaling multiframe. The advantage is that there is less latency when making switch configuration changes via the CMP signals.

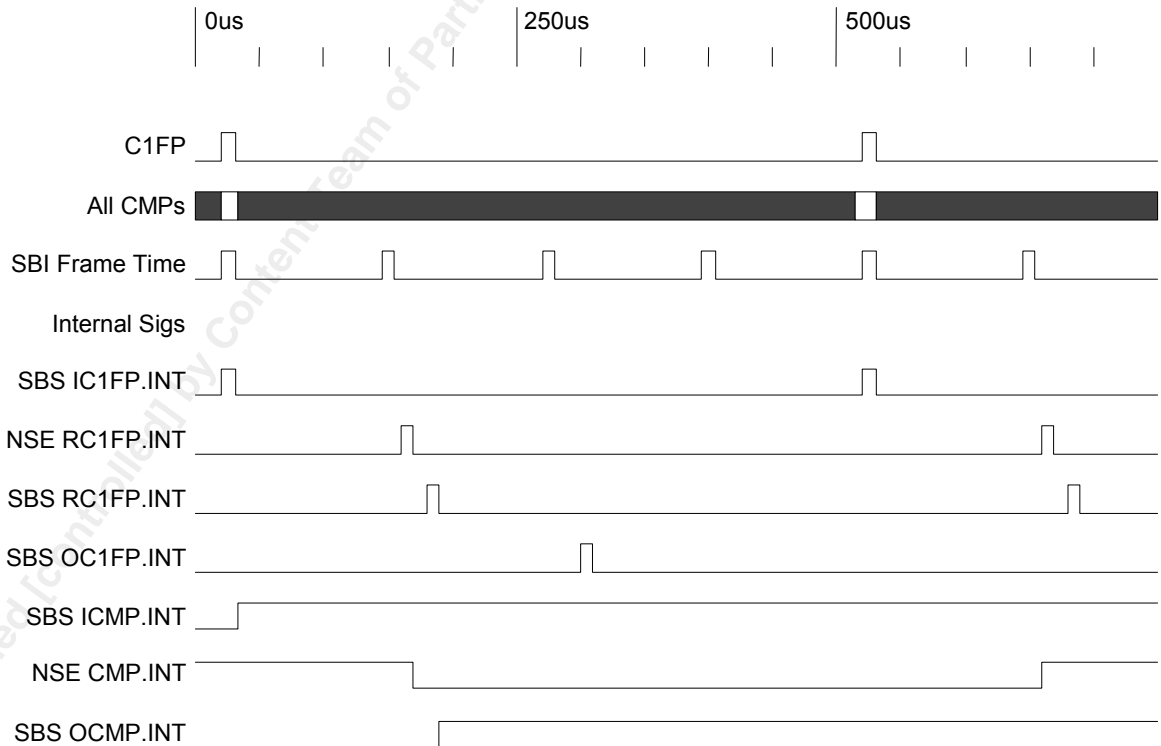
The following diagram shows the system with the FREEDM336, which does not require Channel Associated Signaling. Notice that the data latency through the system is the same as the case when switching DS0s with CAS.

Figure 20 Temux84/SBS/NSE/SBS/FREEDM336 system DS0 Switch no CAS



The following timing diagram shows the system timing when in this configuration.

Figure 21 Switch Timing - DSOs without CAS



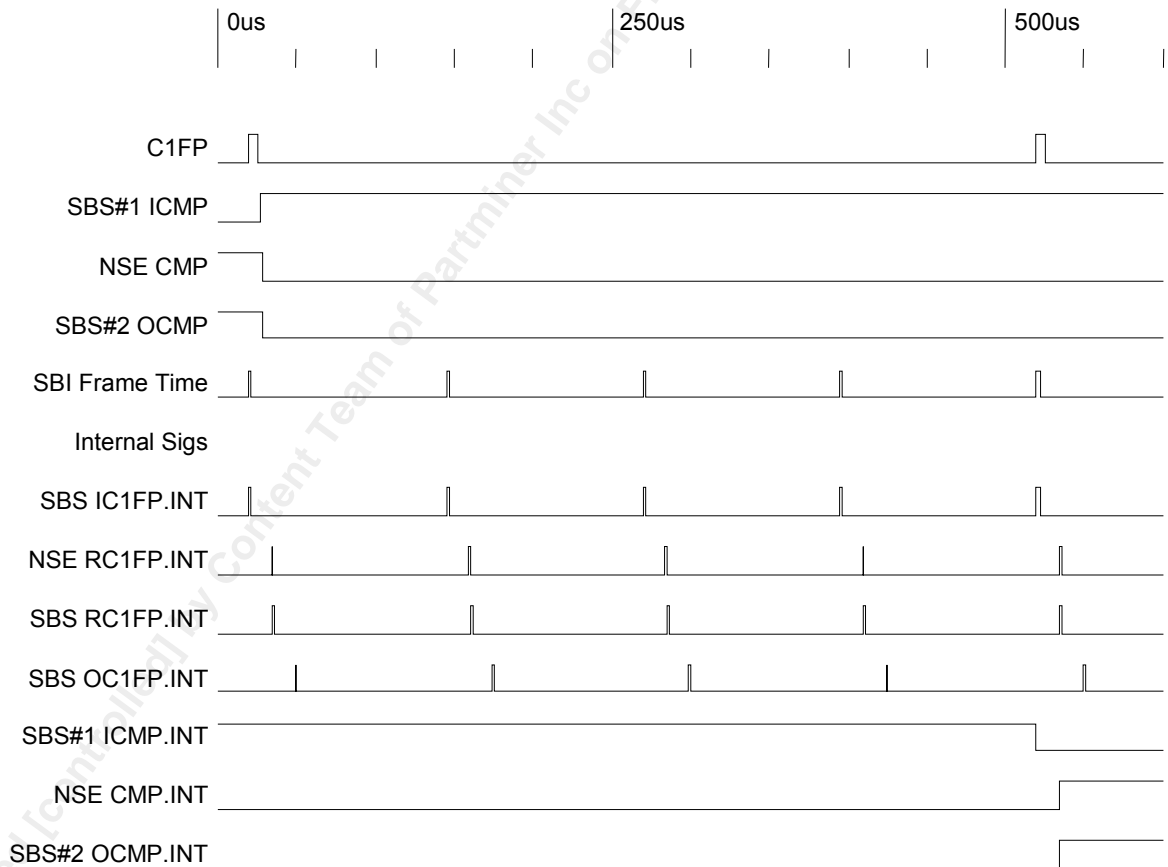
12.3.3 SBS/NSE non-DS0 Level Switching with SBI336 Devices

The SBS/SBSLITE and NSE supports another mode of operation that has lower latency and lower power when not switching at the DS0 level. In this mode both of these devices become a column switch rather than a DS0 switch. This also saves SW configuration since only one row of the switch configuration rams has to be configured rather than all nine rows.

When switching DS0 through the system the SBS must store an entire frame of DS0s before routing them to the destination to allow for the last DS0 of a frame to be switched to the first DS0 of the output. When doing column switching only one row of the SBI structure needs to be stored before switching can take place.

The same diagram from the previous section can be used here. The following timing diagram shows the system timing for this mode of operation.

Figure 22 Non DS0 Switch Timing



12.4 NSE CPU Interaction With the Switching Cycle When Using the ILC

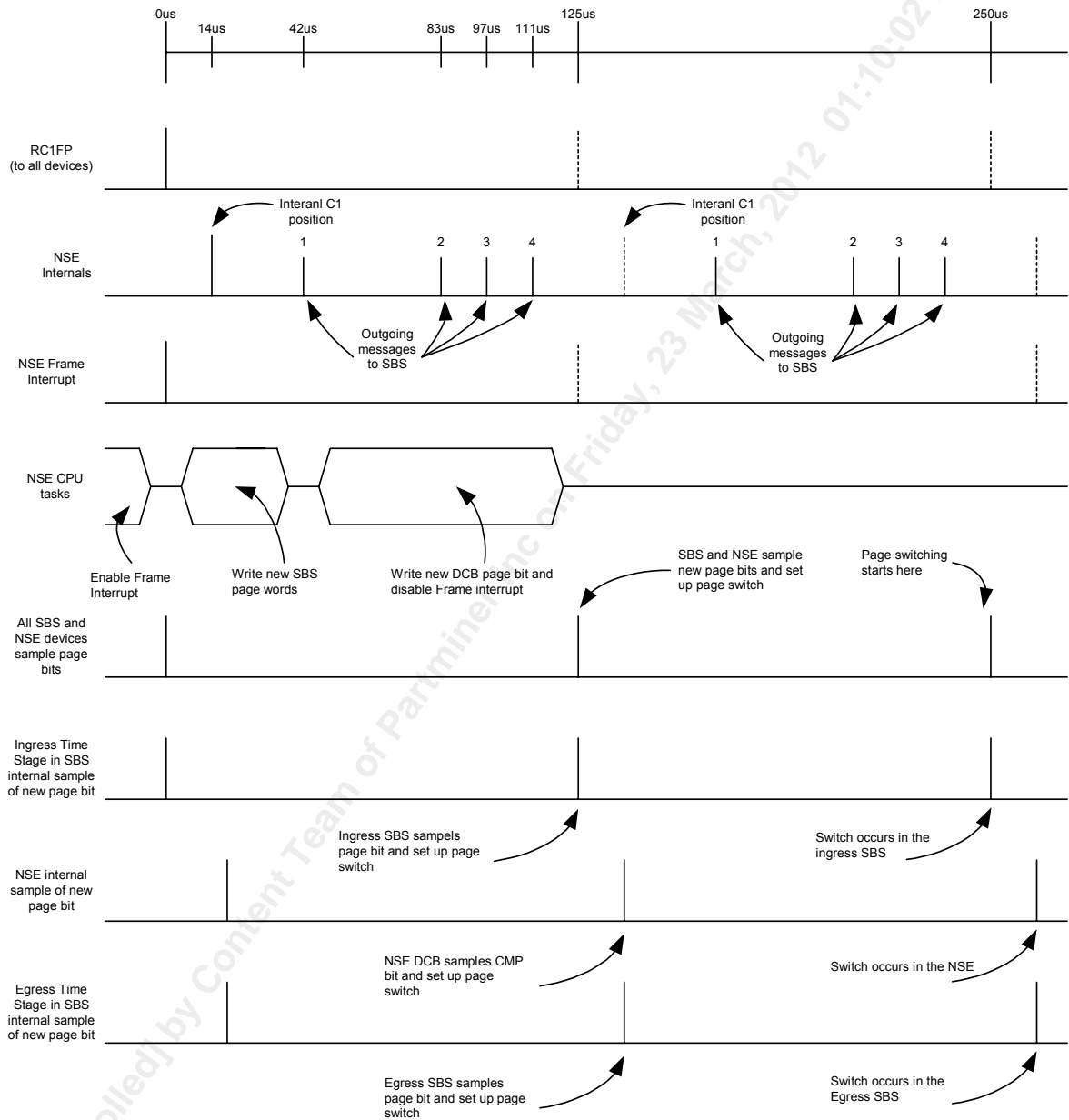
An interrupt is made available to the NSE CPU called the Frame Interrupt this occurs at the start of the internal frame and marks a time in the NSE where updates to the system page bits can occur. This interrupt is maskable and would normally be masked.

The CPU will need to enable this interrupt before a page switch is required, then respond to this interrupt immediately and complete writing the new page bit settings (a two double word operation) within 27us..

This is required as the ILC will sample the SBS page bits (in the ILCs) once during the frame before the first message is assembled and sent (starting at the beginning of row 3). If the page bits are updated late, the SBS pages will switch a frame late, which means the NSE DCB may switch early giving disastrous results.

The NSE CPU will have the rest of the frame to signal a page switch to the DCB as this is sampled on the next frame

Figure 23 NSE CPU Operation with ILC



12.5 Controlling Frame Alignment in the Receive Port

After external data corruption on any port it may be necessary to force OCA to reset the alignment of the R8TD block. In order to detect this out of alignment condition, three hardware functions are implemented for each port. The registers are:

- “Correct R8TD_RX_C1 Pulse Monitor”, 012h,

- “Unexpected R8TD_RX_C1 Interrupt”, 013h, and the
- “Missing R8TD_RX_C1 Interrupt”, 014h,

These are qualified against a delayed version of the RC1FP input, which should occur every 4 or 48 frames and in agreement with mf_swap mode (DCB Configuration Register, 04Ch). If all active ports are using carrying the same frequency of C1 frame pulses (1 in 4 or 1 in 48) then the unexpected interrupt (013h) should be used to signal that a C1 code word was detected at the wrong time, software can then poll the monitor register (012h) to see if the error condition is permanent.

If some links are switching DS0 traffic (“1 in 48” frame mode) and some are not (“1 in 4” frame mode), the input RC1FP and the qualifying signal from the DCB (from mf_swap), will be running at “1 in 48” frame mode. The links in “1 in 48” frame mode should use the unexpected interrupt while the others should use the missing interrupt.

If a link no longer has any C1 activity, the firmware should assume the link has lost alignment, and should force R8TD OCA for the port.

These instructions assume the PMC NSE Device driver is not being used. If the supplied driver is being used, this will all be handled within that driver.

12.6 DS0 Cross-Bar Switch (DCB) Operation

The DCB C1 Delay Register (0x48) must be programmed with a value (in 77.76MHz clock cycles) that approximates the delay between RC1FP (RC1DLY) and the expected arrival of the C1 character at the LVDS inputs to the device. This value is expected to be in the order of 51 + 9720 for SBI mode or 51 + 1080 for Telecombus mode respectively. The value of 51 is approximate and very dependant on the system architecture and transmission line lengths between the SBS or SBSLITE and NSE components. This must be obtained empirically by the system designer during product commissioning.

12.6.1 Configuring the DCB using Port Transfer Mode:

In port transfer mode, the microprocessor updates only one configuration entry within a word of offline connection memory page. The steps to perform a port transfer are shown in the following example:

Example: Suppose one wishes to change the cross bar to map input port 10 to output port 6 for just the 4097th byte of the frame and wishes to keep all other mappings of the 4097th byte the same.

Steps:

1. CPU writes 0x8a061000 to the DCB Access Mode register (0x47) (i.e., WRB=1, ACCMDE=0, PORTCFG[4:0]=0x0A, PORTADDR[4:0]=0x06, WORDADDR[13:0]=0x1000).
 - Triggers a read from offline memory connection page at location 0x1000

2. Wait 4 SYSCLK cycles.
3. CPU writes 0x0a061000 to the DCB Access Mode register (0x47) (i.e., WRB=0, ACCMDE=0, PORTCFG[4:0]=0x0A, PORTADDR[4:0]=0x06, WORDADDR[13:0]=0x1000).
 - Triggers a write to offline connection memory page at location 0x1000.
4. Wait 4 SYSCLK cycles before returning to step 1 to perform another mapping change.

12.6.2 Configuring the DCB Using Word Transfer Mode:

In word transfer mode, the microprocessor updates the entire word of offline connection memory page. The steps to perform a word transfer is shown in the following example:

Example: Suppose one wishes to change the entire cross bar mapping for the 4097th byte of the frame.

Steps:

1. CPU writes new mapping to the Configuration 11-6 Port register (0x44).
2. CPU writes new mapping to the Configuration 5-0 Port register (0x45).
3. CPU write 0x40001000 to the DCB Access Mode register (0x47).
 - triggers a write to offline connection memory page at 0x1000.

Go to step 1 to begin the mapping change for a new byte in the frame.

12.6.3 Reading Configuration:

It is possible to read configurations from the offline connection memory page. The following example shows this reading operation.

Example: Suppose one wishes to read which input ports mapped to output ports 11-6 for the 4097th byte of the frame within the offline connection memory page.

Steps:

1. CPU writes 0x80081000 to the DCB Access Mode register (0x47) (a binary value of 001XX on PORTADDR[4:0] will retrieve the mapping for output ports 11-6).
2. Wait for 6 SYSCLK cycles.
3. CPU reads the mapping from the DCB Configuration Output register (0x46).

Notes:

1. The Access Mode register should NOT be accessed more frequently than once ever 4 SYSCLK cycles when initiating write transfers.

2. When initiating a read from the offline connection memory page to the Configuration Output register, there is a latency of 6 SYSCLK cycles from when a read is initiated till when valid data appears on CFG_O.
3. User should perform this operation only when there is no page swap pending (SWAPV = '0') and page copy is inactive (UPDATEV = '0')

12.6.4 DCB Online to Offline Memory Page Copy:

There are 2 ways in which a connection memory page copy can occur: forced and automatic.

- In forced mode, the CPU initiates a page copy by writing to the DCB Interrupt Status register (0x4D). The page copy begins immediately after being initiated.
- In automatic mode, the AUTO field must be set to 1. When a connection memory page swap occurs, the online connection memory page is copied to the offline connection memory page.

Interrupt generation to signal the page copying status can be enabled to simplify software scheduling by setting the UPDATEE field in the DCB Configuration register to 1. In this mode, the UPDATEI field in the DCB Interrupt Status register (0x4D) can be used as the interrupt signal to control the microprocessor.

Alternatively, the microprocessor can poll the UPDATEV field within the DCB Configuration register (0x4C) to detect the status of the connection memory page update logic. 1 indicates copying in progress. And 0 indicates copying complete.

Warning: Attempting a page copy while a page swap is pending can lead to corruption of both online and offline memory pages if the page swap occurred while the page copy is in progress.

12.7 Telecombust Mode Operation

In Telecombust mode operation, only 1080 words of the configuration RAM are utilized. This same configuration is repeated 9 times for switching the entire 9720 byte OC-12 frame. In this mode, RC1FP is flywheeled internally every frame so that page swaps can also occur at this frequency.

To configure for this mode of operation, the following programming steps needs to be taken (precedence of steps is irrelevant)

1. DCB Frame Size register (0x4A) should be programmed to 1079.
 - This programs the DCB to use just 1080 location of the RAMs.
2. DCB MF_SWAP bits in Configuration register (0x4C) should be programmed to 00.
 - This will program the DCB to effect page changes at every 9720 byte frame when a page swap request is received.
 - CMP inputs will be sampled every frame at the internally flywheeled RC1FP location.
 - If enabled, FRAMEI will occur every frame at the internally flywheeled RC1FP location.

12.8 SBI Column Mode Operation

In SBI column mode operation, only 1080 rows of the configuration RAM is utilized, this same configuration is repeated 9 times for switching the entire 9720 byte OC12 frame and 36 times to form the 4 frame multiframe. In this mode, RC1FP is flywheeled internally every 4 frame so that page swap can also occur at this frequency.

To configure for this mode of operation, the following programming steps needs to be taken (precedence of steps is irrelevant)

1. DCB Frame Size register (0x04A) should be programmed to 1079.
 - This programs the DCB to use just 1080 location of the RAMs.
2. MF_SWAP bits in DCB Configuration register (0x04C) should be programmed to 01.
 - This will program the DCB to effect page changes at every 4 x 9720 frame when a page swap request is received.
 - CMP inputs will be sampled every 4 frame at the internally flywheeled RC1FP location.
 - If enabled, FRAMEI will occur every 4 frame at the internally flywheeled RC1FP location.

12.9 SBI DS0 Mode Operation

In SBI DS0 mode operation, all 9720 words of the configuration RAM are utilized. This same configuration is repeated 4 times to switch the 4 frame multiframe. In this mode, RC1FP is flywheeled internally every 4 frames so that page swaps can also occur at this frequency

To configure for this mode of operation, the following programming steps needs to be taken (precedence of steps is irrelevant)

1. DCB Frame Size register (0x4A) should be programmed to 9719.
 - This programs the DCB to use all 9720 location of the RAMs.
2. MF_SWAP bits in DCB Configuration register (0x4C) should be programmed to 10.
 - This will program the DCB to effect page changes at every 4 x 9720 frame when a page swap request is received.
 - CMP inputs will be sampled every 4th frame at the internally flywheeled RC1FP location.
 - If enabled, FRAMEI will occur every 4th frame at the internally flywheeled RC1FP location.

12.10 SBI DS0 with CAS Mode Operation

In SBI DS0 with CAS mode operation, all 9720 words of the configuration RAM are utilized. This same configuration is repeated 48 times to switch the 48 frame multiframe. In this mode, RC1FP is flywheeled internally every 48th frame so that page swaps can also occur at this frequency.

To configure for this mode of operation, the following programming steps needs to be taken (precedence of steps is irrelevant)

1. DCB Frame Size register (0x4A) should be programmed to 9719.
 - This programs the DCB to use all 9720 location of the RAMs.
2. MF_SWAP bits in DCB Configuration register (0x4C) should be programmed to 11.
 - This will program the DCB to effect page changes at every 48 x 9720 frame when a page swap request is received.
 - CMP inputs will be sampled every 48th frame at the internally flywheeled RC1FP location.
 - If enabled, FRAMEI will occur every 48 frame at the internally flywheeled RC1FP location.

Note: It is vital to ensure that proper switching of the DS0 bytes containing CAS bits be performed correctly through software configuration. I.e. these bytes should all be preserved and switched to the same output link to preserve the CAS for downstream devices.

12.11 Using the Inband Link Controller (ILC)

The In-Band Link Controllers provides a mechanism for communication between devices over the serial interface. The ILC inserts and retrieves messages from the transport overhead of the SBI336 or Telecom Bus frame. The messages are 36 bytes each and 4 messages are transmitter each frame. These messages are inserted into the Data Communication Channel (DCC) bytes, in rows 3,6,7 and 8. Each message contains 2 header bytes, 32 bytes containing the free format information, and 2 bytes for a CRC-16. There is an independent in-band link controller for each of the 12 links. Operating each of the 12 ILC blocks requires the same procedure.

If no information bytes are available to transmit, the ILC will continue to send messages but will insert all zeros into the information bytes and will set the VALID bit in the header to zero. The header and CRC bytes will be transmitted normally. When the receive link recognizes that the VALID bit is a zero, it will not write the all zero message into the receive FIFO.

12.11.1 Transmitting Messages

When writing to the transmit FIFO in the ILC, the following procedure should be followed:

1. Write a logic 1 to the TX_XFER_SYNC bit of the ILC Transmit Misc.Status and FIFO Synch Register (Reg112h + N*20h). This will ensure the subsequent writes to the FIFO start at the beginning of a message.
2. Write to the ILC Transmit FIFO Data Register (Reg110h + N*20h). Writing to this register will initiate a transfer of the Transmit FIFO Data Register into the transmit FIFO.
3. Read the TX_FI_BUSY bit in the ILC Transmit Misc.Status and FIFO Synch Register (Reg112h + N*20h) or wait a minimum of 3 SYSCLK cycles. If TX_FI_BUSY is a logic 0, continue to step 4. If it is a logic 1, continue polling the TX_FI_BUSY bit.

4. Loop back to Step 2 until the entire message has been written in to the FIFO.

When transmitting multiple 32 byte messages, the TX_XFER_SYNC bit does not have to be written to between each message.

When transmitting a message shorter than 32 bytes, the TX_XFER_SYNC bit should be set after writing the last byte of the message into the FIFO. This will allow the short message to be transmitted and move the FIFO to the next 32 byte partition.

12.11.2 Retrieving Messages

When reading messages from the receive FIFO in the ILC, the following procedure should be followed:

1. Write a logic 1 to the RX_XFER_SYNC bit of the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h). This will initiate a read from the receive FIFO.
2. Read the RX_FI_BUSY bit in the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h) or wait a minimum of 4 SYSCLK cycles. If RX_FI_BUSY is a logic 0, continue to step 3. If it is a logic 1, continue polling the RX_FI_BUSY bit.
3. Read the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h) and check the state of the CRC_ERR. If this bit is a logic 1, the current message in the FIFO had a CRC error and the data is not reliable and the user may want to skip to the next message.
4. Read the ILC Receive FIFO Data Register (Reg113h + N*20h).
5. Read the RX_FI_BUSY bit in the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h) or wait a minimum of 4 SYSCLK cycles. If RX_FI_BUSY is a logic 0, continue to step 6. If it is a logic 1, continue polling the RX_FI_BUSY bit.
6. Loop back to Step 4 until the entire message has been read out of the FIFO.

When reading more than one message from the receive FIFO, the RX_XFER_SYNC does not have to be set between each message.

Before reading any messages, the software may want to check how many messages are contained in the receive FIFO. This can be done by reading the RX_MSG_LVL[3:0] bits in the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h). When reading these bits, the RX_STTS_VALID bit must also be checked. If RX_STTS_VALID is a logic 1, the RX_MSG_LVL[3:0] bits are valid. If RX_STTS_VALID is a logic 0, the RX_MSG_LVL[3:0] bits are not valid and this register should be read again until RX_STTS_VALID is a logic 1.

12.11.3 Transmit Message Header Bytes

- **LINK[1:0]:** These bits reflect the state of the TX_LINK[1:0] bits in the ILC Transmit Control Register (Reg111h + N*20h).

- **PAGE[1:0]:** These bits transmitted by the ILC reflect the state of the TX_ILC_PAGE_1[11:0], TX_ILC_PAGE_0[11:0] bits in registers 004h, 003h relatively at a bit position equal to the link number.
- **USER[2:0]:** These bits transmitted by the ILC reflect the state of the TX_ILC_USER_2[11:0], TX_ILC_USER_1[11:0], TX_ILC_USER_0[11:0] bits in registers 010h, 00Fh, 00Eh relatively at a bit position equal to the link number.
- **AUX[7:0]:** These bits reflect the state of the TX_AUX[7:0] bits in the ILC Transmit Control Register (Reg111h + N*20h).

12.11.4 Receive Message Header Bytes

- **LINK[1:0]:** The LINK[1:0] bits from the latest received message are reflected in the RX_LINK[1:0] bits of the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state of either of these bits can be configured to cause an interrupt by setting the RX_LINK_CHGE bit in the ILC Interrupt Enable and Control Register (Reg116h + N*20h).
- **PAGE[1:0]:** The PAGE[1:0] bits from the latest received message are reflected in the RX_PAGE[1:0] bits of the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state in either of these bits can be configured to cause an interrupt by setting the RX_PAGE_CHGE[1:0] bits in the ILC Interrupt Enable and Control Register (Reg116h + N*20h).
- **USER[2:0]:** The USER[2:0] bits from the latest received message are reflected in the RX_USER[2:0] bits of the ILC Receive Status and FIFO Synch Register (Reg115h + N*20h). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value. A change in state of the RX_USER[0] bit can be configured to cause an interrupt by setting the RX_USER0_CHGE bits in the ILC Interrupt Enable and Control Register (Reg116h + N*20h).
- **AUX[7:0]:** The AUX[7:0] bits from the latest received message are reflected in the RX_AUX[7:0] bits of the ILC Receive Auxiliary, Status and FIFO Synch Register (Reg115h + N*20h). These bits are only update if the receive message contains a correct CRC value. If the CRC is in error, these bits will keep their previous value.

12.11.5 Disabling the ILC

The functions of the 12 ILC blocks may be disabled individually. When disabled, no messages are inserted or retrieved. All data passes through the ILC unmodified.

The TX_BYPASS bit in the ILC Transmit Control Register (Reg111h + N*20h) will disable the transmit half of the ILC. The RX_BYPASS bit in the ILC Receive Control Register (Reg114h + N*20h) will disable the receive half of the ILC.

12.12 Switch Setting Algorithm

Please see the Open Path Algorithm (OPA), Chip Set Driver (CSD) and the related CHES-Narrowband application notes for more information on the switch setting algorithms and software support.

CHES-Narrowband Open Path Algorithm API Design Specification (PMC-2010601)

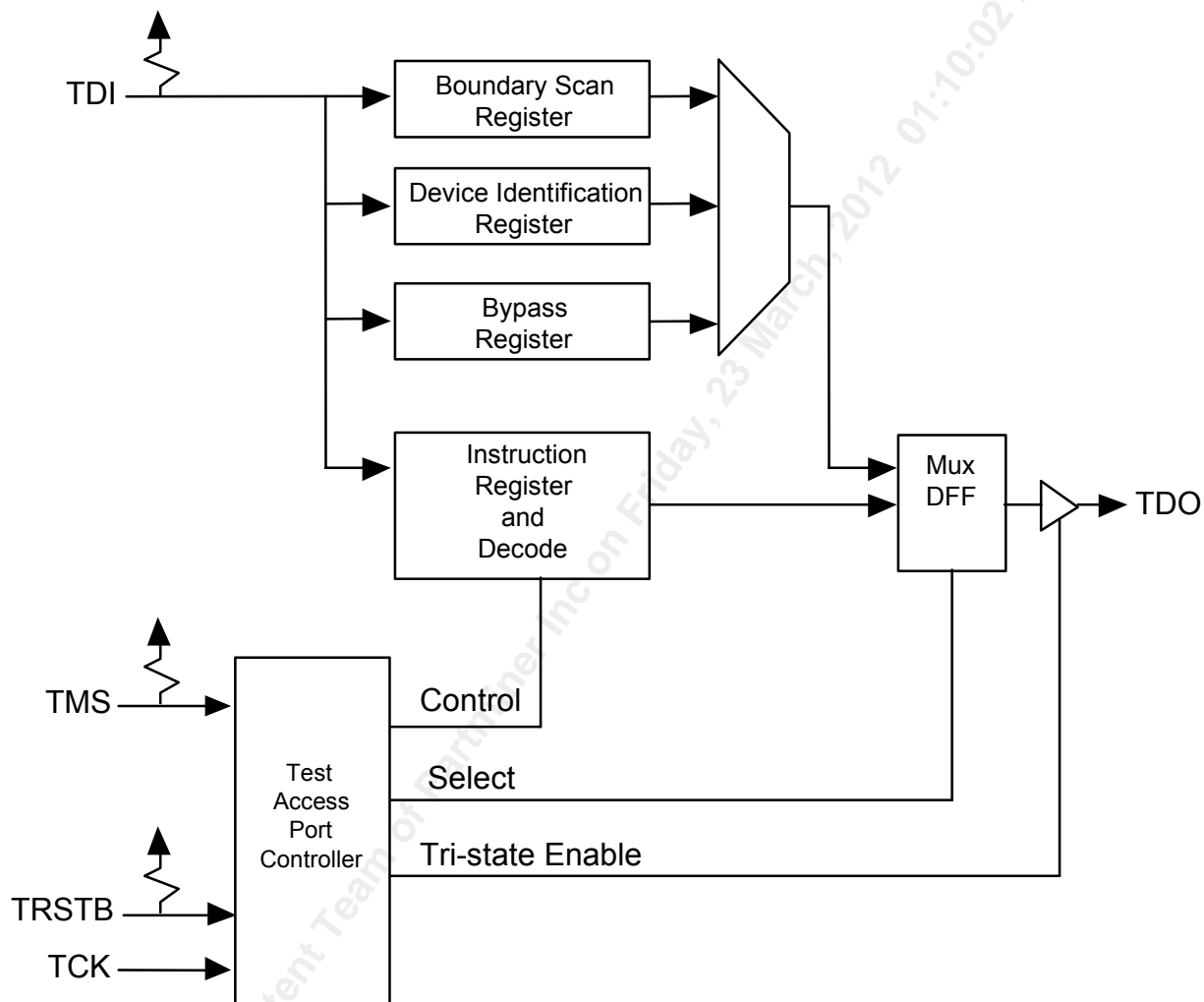
Open Path Algorithm Application Note (PMC-2012161)

NSE/SBS Narrowband Chipset Driver Design Specification (PMC-2002294)

12.13 JTAG Support

The NSE supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 24 Boundary Scan Architecture



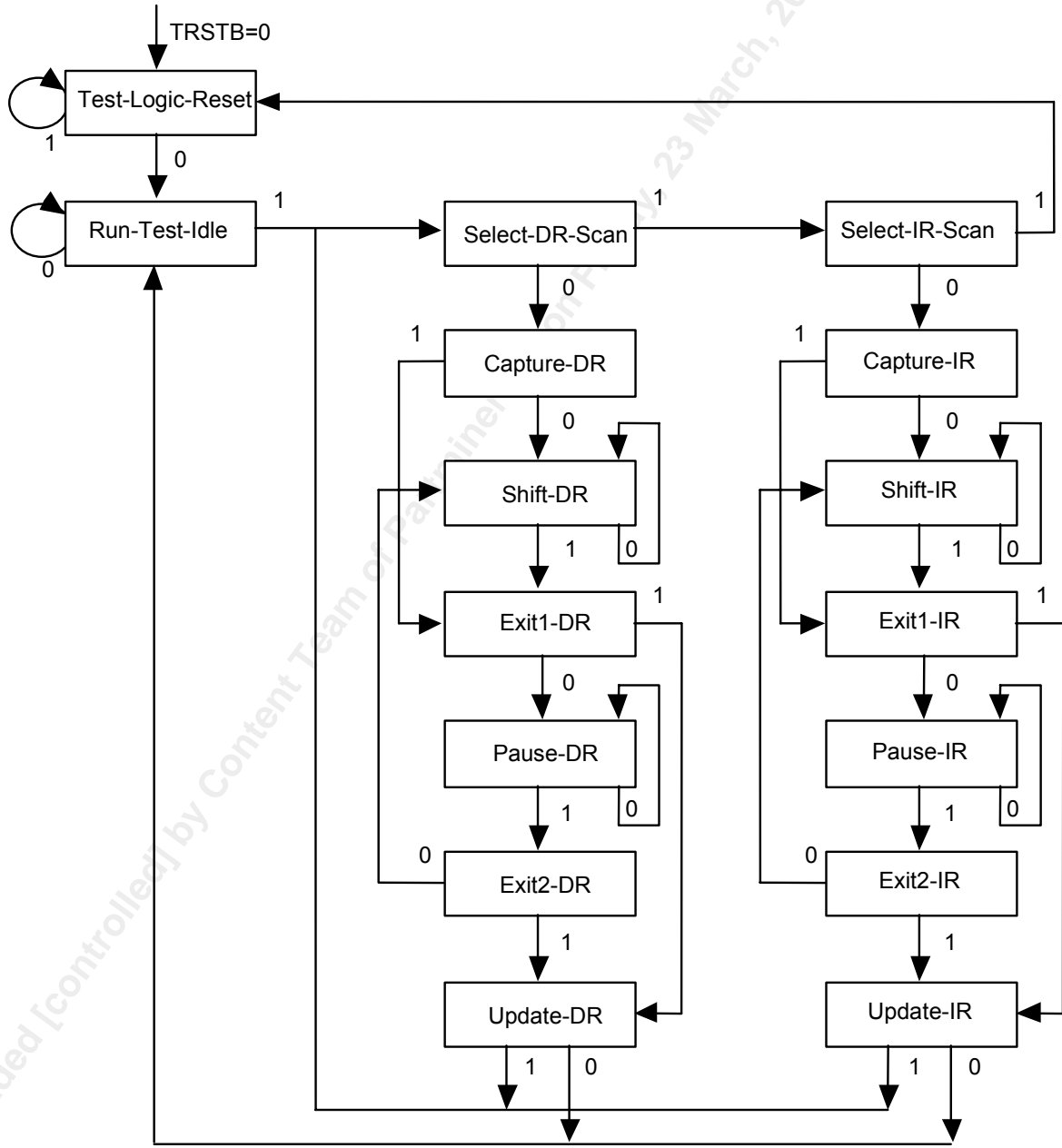
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

12.13.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 25 TAP Controller Finite State Machine



All transitions dependent on input TMS

12.13.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

12.13.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

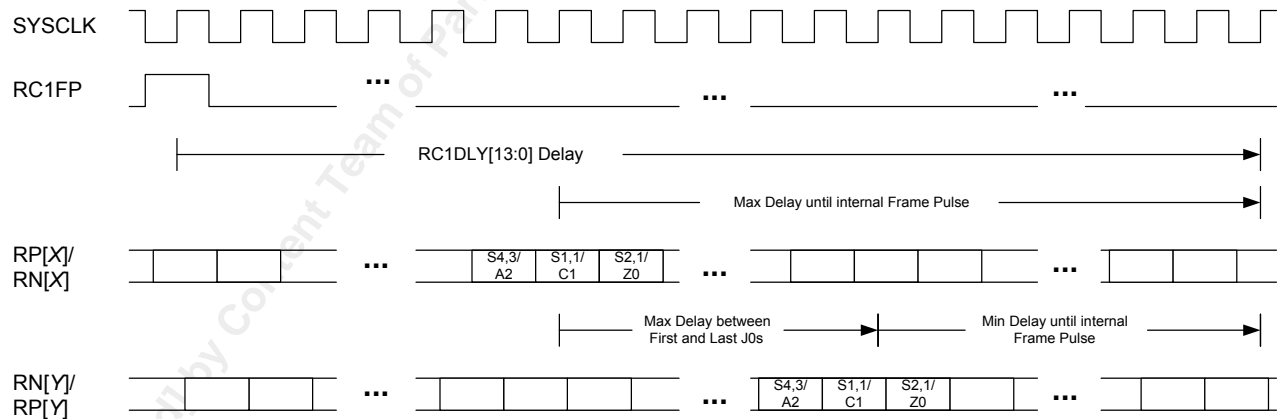
The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13 Functional Timing

13.1 Receive Interface Timing

Figure 26 below, shows the relative timing of the receive interface. The LVDS links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RC1FP). Due to phase noise of clock multiplication circuits and backplane routing or cable length discrepancies, the links will not phase aligned to each other but are frequency locked. The delay from RC1FP being sampled high to the first and last C1 character is shown in Figure 26. In this example, the first C1 is delivered on link RN[X]/RP[X]. The delay to the last C1 represents the time when the all the links have delivered their C1 character. In the example below, link RN[Y]/RP[Y] is shown to be the slowest. The minimum value for the internal programmable delay (RC1DLY[13:0]) is the delay through the SBS/SBSLITE¹ plus 15. The maximum value is the delay through the SBS plus 31. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes. The relative phases of the links in Figure 26 are shown for illustrative purposes only. Links may have different delays relative to other links than what is shown.

Figure 26 Receive Interface Timing



¹ This delay will be either one frame (9720 clock cycles) or one row (1080 clock cycles) depending on the mode employed.

13.2 Transmit Interface Timing

Figure 27 below shows the delay from assertion of RC1FP to the transmit serial data links. Due to the presence of FIFOs in the data path, the delay to the various links can differ by up to 7 cycles. The minimum delay ($RC1DLY + 14$ SYSCLK cycles) is shown to be incurred by one of the transmit protect serial data links (TP[X]/TN[X]). The maximum delay ($RC1DLY + 21$ cycles) is shown to be incurred by one of the transmit auxiliary serial data links (TP[Y]/TN[Y]). The maximum delay from RC1FP to the transmission of a C1 pulse is $RC1DLY + 21$ cycles. Figure 27 shows the delay from RC1FP being sampled high to the first and last C1 character being send out to the transmit serial data links. The relative phases of the links in Figure 27 are shown for illustrative purposes only. Links may have different delays than what is shown.

Figure 27 Transmit Interface Timing

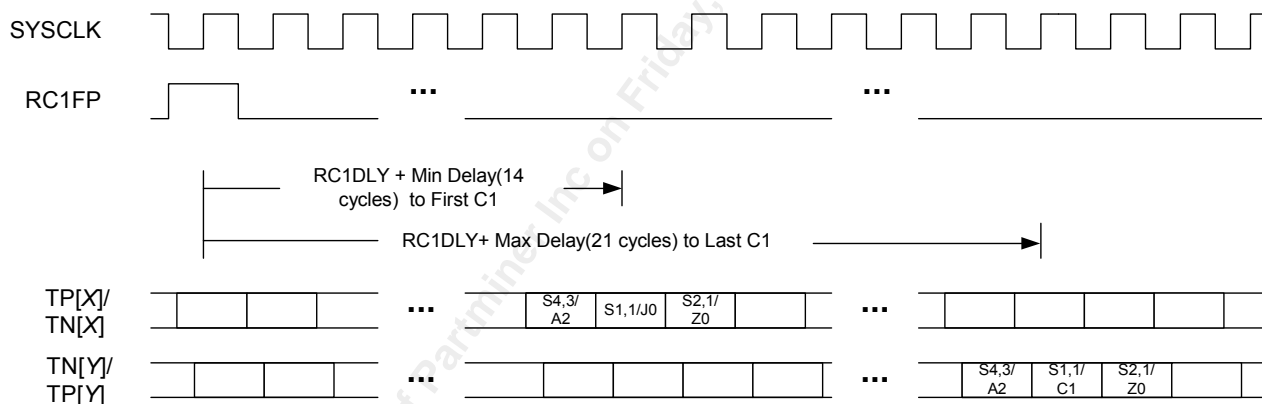
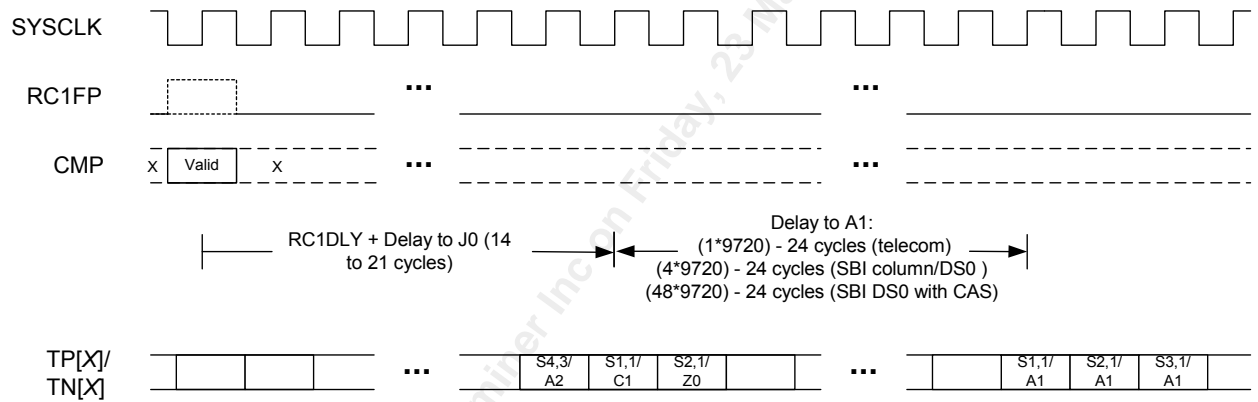


Figure 28 below shows the delay from CMP to the transmit serial data links. CMP is valid only at the RC1FP pulse time, whether RC1FP is pulsed or not. It is ignored at other locations in the transport frame. A change in value to the connection memory page signal (CMP) results in changing the active switch settings. Given that CMP is sampled on the RC1FP pulse time, the first data that is switched according to the newly selected connection memory page are the first A1 byte of the frame transmitted by the NSE-8G. The delay from RC1FP being sampled high (hence sample the CMP) to the first and last A1 bytes (switched by the newly selected connection memory page) being send out to the transmit serial data links on different switching modes are summarized as follows:

Switching Mode	Frame Switching @ (9720 byte frame)	RC1FP expected every	Delay from RC1FP to A1 byte transmitted at serial data links.
Telecom bus	1 frame	4 frame	$RC1DLY + 14 + (1*9720) - 24$ cycles (min) $RC1DLY + 21 + (1*9720) - 24$ cycles (max)
SBI column	4 frame	4 frame	$RC1DLY + 14 + (4*9720) - 24$ cycles (min)

Switching Mode	Frame Switching @ (9720 byte frame)	RC1FP expected every	Delay from RC1FP to A1 byte transmitted at serial data links.
mode			RC1DLY + 21 + (4*9720) - 24 cycles (max)
SBI DS0 mode	4 frame	4 frame	RC1DLY + 14 + (4*9720) - 24 cycles (min) RC1DLY + 21 + (4*9720) - 24 cycles (max)
SBI DS0 with CAS	48 frame	48 frame	RC1DLY + 14 + (48*9720) - 24 cycles (min) RC1DLY + 21 + (48*9720) - 24 cycles (max)

Figure 28 CMP Timing



14 Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 14 Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
1.8V Supply Voltage (VDDI, AVDL)	-0.5V to +2.2V
3.3V Supply Voltage (VDDO, AVDH, CSU_AVDH)	-0.5V to +4.6V
input pad tolerance	-2V < VDDO < +2V for 10ns, 100mA max
output pad overshoot limits	-2V < VDDO < +2V for 10ns, 20mA max
Voltage on Any Digital Pin	-0.5V to VDDO+0.5V
Voltage on LVDS Pin	-0.5V to AVDH+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current on RN[I], RP[I], TN[I], TP[I] pins	±90 mA
Latch-Up Current on RESK pin	±50 mA
Latch-Up Current	±100 mA except RN[I], RP[I], TN[I], TP[I], and RESK
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C

Notes on Power Supplies:

- When powering up the NSE, the following power supply sequence should be observed:
VDDO, AVDH, CSU_AVDH

VDDI, AVDL
- Powering down should be the reverse.

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15 Power Information

15.1 Power Requirements

Table 15 Power Requirements

Conditions	Parameter	Typ ^{1,3}	High ⁴	Max ²	Units
PM8621 (NSE-8G) normal mode	IDDOP (VDDI)	0.517	—	0.588	A
	IDDOP (VDDO)	0.019	—	0.042	A
	IDDOP (AVDL)	0.191	—	0.235	A
	IDDOP (AVDH)	0.187	—	0.216	A
	Total Power	1.96	2.11	—	W

Notes:

- Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
- Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
- Typical power values are calculated using the formula:

$$\text{Power} = \sum_i (\text{VDDNomi} \times \text{IDDTypi})$$

Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system

- High power values are a “normal high power” estimate and are calculated using the formula:

$$\text{Power} = \sum_i (\text{VDDMaxi} \times \text{IDDHighi})$$

Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

15.2 Power Sequencing

To prevent damage to the NSE and to ensure proper operation, power must applied according to the following rules:

The 1.8 V supplies can come up at the same time or after the 3.3 V supplies as long as the 1.8V supplies never exceed the 3.3V supplies by more than 0.3V.

Analog supplies must not exceed digital supplies of the same nominal voltage by more than 0.3V.

Data applied to I/O pins must not exceed VDDO by more than 0.3V unless the data is current-limited to 20 mA *.

There are no power-up ramp rate restrictions.

The NSE must be powered down according to the same restrictions above.

* These rules are intended to allow for hot-swap of LVDS signals, as the differential links are appropriately current-limited.

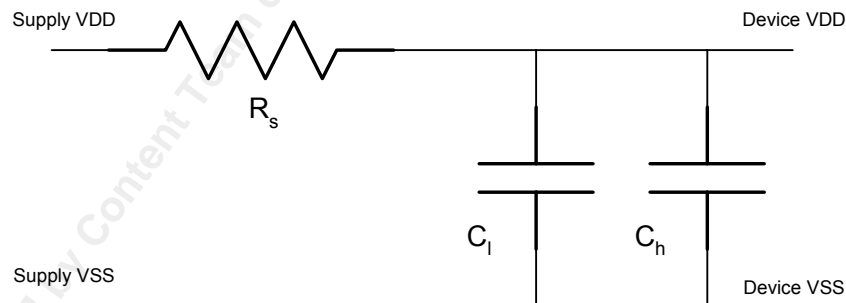
15.3 Analog Power Filtering Recommendations

To achieve best performance of the LVDS links, an analog filter network should be installed between the power balls and the supply.

Table 16 Analog Power Filters

	Rs	Cl	Ch	Notes
CSU AVDH (2 balls)	3.3-ohm	100nF	10nF	One Filter network per VDD ball.
CSU AVDL (6 balls)	0.47-ohm	4.7uF	10nF	One Filter network per VDD ball.
AVDH (34 balls)	3.3-ohm	1.0uF	10nF	Two VDD balls per filter network

Figure 29 Analog Power Filter Circuit



16 D.C. Characteristics

$T_A = -40^{\circ}\text{C}$ to $T_J = 125^{\circ}\text{C}$, $V_{DDO} = 3.3\text{V} \pm 5\%$, $V_{DDI} = 1.8\text{V} \pm 5\%$

(Typical Conditions: $T_C = 25^{\circ}\text{C}$, $V_{DDO} = 3.3\text{V}$, $V_{DDI} = 1.8\text{V}$)

Table 17 D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDDI	Power Supply at 1.8V	1.71	1.8	1.89	Volts	
VDDO	Power Supply at 3.3V	3.14	3.3	3.47	Volts	
V _{AVDH}	Power Supply	3.14	3.3	3.47	Volts	
V _{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V _{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V _{OL}	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at $V_{DD} = 3.14\text{V}$ and I_{OL} = maximum rated for pad.
V _{OH}	Output or Bi-directional High Voltage	2.4	2.7		Volts	Guaranteed output High voltage at $V_{DD} = 3.14\text{V}$ and I_{OH} = maximum rated current for pad.
V _{T+}	Reset Input High Voltage	2.2			Volts	Applies to RSTB and TRSTB only.
V _{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V _{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
I _{ILPU}	Input Low Current	-200	-50	-4	μA	$V_{IL} = \text{GND}$. Notes 1 and 3.
I _{IHPU}	Input High Current	-10	0	+10	μA	$V_{IH} = V_{DD}$. Notes 1 and 3.
I _{IL}	Input Low Current	-10	0	+10	μA	$V_{IL} = \text{GND}$. Notes 2 and 3.
I _{IH}	Input High Current	-10	0	+10	μA	$V_{IH} = V_{DD}$. Notes 2 and 3.
C _{IN}	Input Capacitance		5		PF	$t_A = 25^{\circ}\text{C}$, $f = 1\text{MHz}$
C _{OUT}	Output Capacitance		5		PF	$t_A = 25^{\circ}\text{C}$, $f = 1\text{MHz}$
C _{IO}	Bi-directional Capacitance		5		PF	$t_A = 25^{\circ}\text{C}$, $f = 1\text{MHz}$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{ICM}	LVDS Input Common-Mode Range	0		2.4	V	
V _{IDM}	LVDS Input Differential Sensitivity			100	mV	
R _{IN}	LVDS Differential Input Impedance	85	100	115	Ω	
V _{LOH}	LVDS Output voltage high		1375	1475	mV	R _{LOAD} =100Ω ±1%
V _{LOL}	LVDS Output voltage low	925	1025		mV	R _{LOAD} =100Ω ±1%
V _{ODM}	LVDS Output Differential Voltage	300	350	400	mV	R _{LOAD} =100Ω ±1%
V _{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R _{LOAD} =100Ω ±1%
R _O	LVDS Output Impedance, Differential	85	110	115	Ω	
ΔV _{ODM}	Change in V _{ODM} between "0" and "1"			25	mV	R _{LOAD} =100Ω ±1%
ΔV _{OCM}	Change in V _{OCM} between "0" and "1"			25	mV	R _{LOAD} =100Ω ±1%
I _{SP} , I _{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I _{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

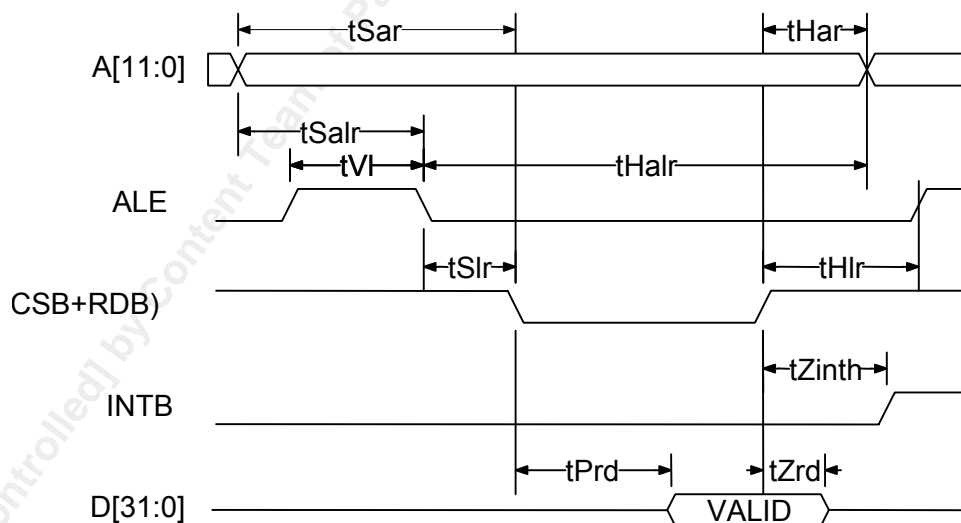
17 Microprocessor Interface Timing Characteristics

($T_A = -40^{\circ}\text{C}$ to $T_J = 125^{\circ}\text{C}$, $V_{DDO} = 3.3\text{V} \pm 5\%$)

Table 18 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
t _{SAR}	Address to Valid Read Set-up Time	5		ns
t _{HAR}	Address to Valid Read Hold Time	3		ns
t _{SALR}	Address to Latch Set-up Time	5		ns
t _{HALR}	Address to Latch Hold Time	3		ns
t _{VL}	Valid Latch Pulse Width	5		ns
t _{SLR}	Latch to Read Set-up	0		ns
t _{HLR}	Latch to Read Hold	0		ns
t _{PRD}	Valid Read to Valid Data Propagation Delay		30	ns
t _{ZRD}	Valid Read Negated to Output Tri-state		10	ns
t _{ZINTH}	Valid Read Negated to INTB High		25	ns

Figure 30 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

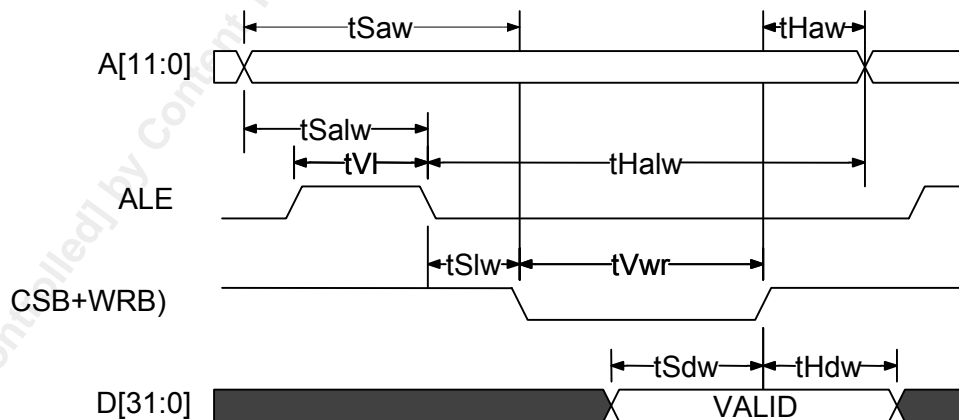
- Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
- Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[31:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters t_{SALR} , t_{HALR} , t_{VL} , t_{SLR} , and t_{HLR} are not applicable.
5. Parameter t_{HAR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 19 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
t_{SAW}	Address to Valid Write Set-up Time	5		ns
t_{SDW}	Data to Valid Write Set-up Time	10		ns
t_{SALW}	Address to Latch Set-up Time	5		ns
t_{HALW}	Address to Latch Hold Time	3		ns
t_{VL}	Valid Latch Pulse Width	5		ns
t_{SLW}	Latch to Write Set-up	0		ns
t_{HLW}	Latch to Write Hold	5		ns
t_{HDW}	Data to Valid Write Hold Time	10		ns
t_{HAW}	Address to Valid Write Hold Time	5		ns
t_{VWR}	Valid Write Pulse Width	10		ns

Figure 31 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters t_{SALW} , t_{HALW} , t_{VL} , t_{SLW} , and t_{HLW} are not applicable.
3. Parameter t_{HAW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

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18 A.C. Timing Characteristics

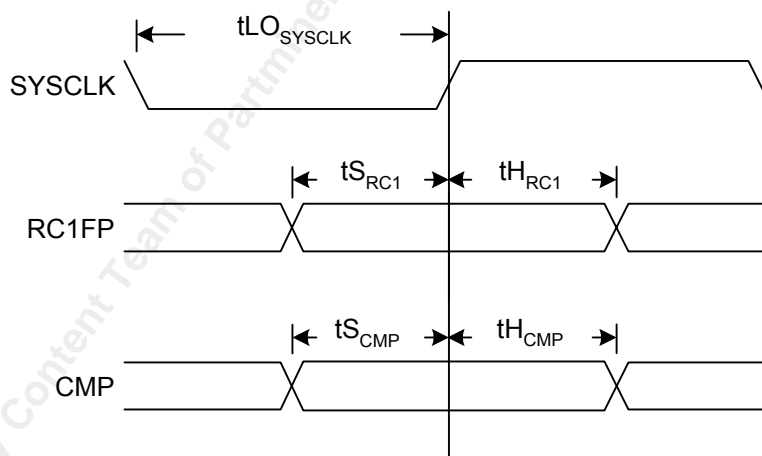
(TA = -40°C to TJ = 125°C, VDDO= 3.3 V ±5%, VDDI= 1.8 V ±5%)

18.1 Input Timing

Table 20 NSE Input Timing (Figure 32)

Symbol	Description	Min	Max	Units
FSYSCLK	SYSCLK Frequency (nominally 77.76 MHz)	-50	+50	ppm
THISYSCLK	SYSCLK High Pulse Width	5		ns
TLOSYSCLK	SYSCLK Low Pulse Width	5		ns
TSCMP	CMP Set-Up Time	3		ns
THCMP	CMP Hold Time	0		ns
TSRC1	RC1FP Set-Up Time	3		ns
THRC1	RC1FP Hold Time	0		ns

Figure 32 NSE Input Timing



Notes on Input Timing:

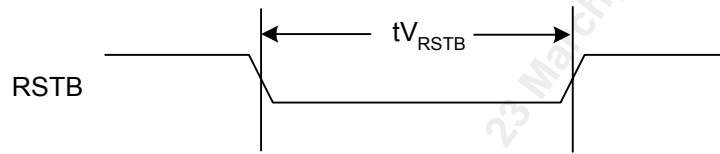
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

18.2 Reset Timing

Table 21 RSTB Timing (Figure 33)

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 33 RSTB Timing



18.3 Serial SBI Bus Interface

Table 22 Serial SBI Bus Interface

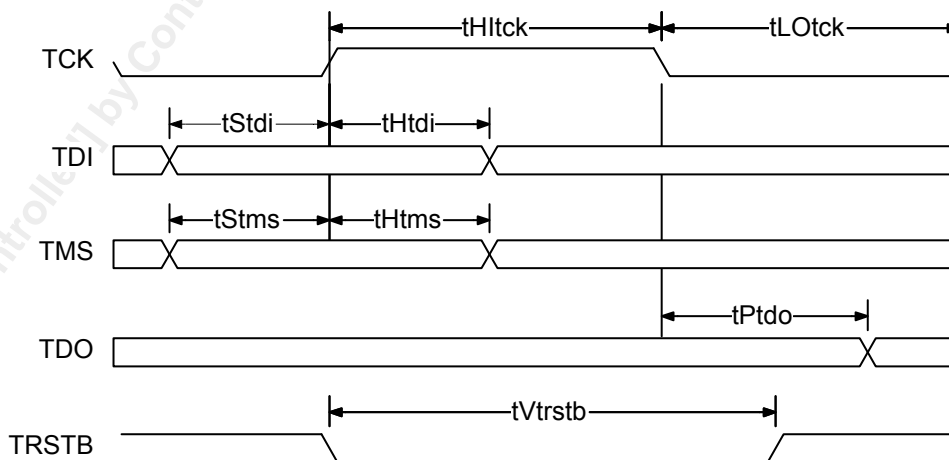
Symbol	Description	Min	Typical	Max	Units
fRLVDS	RP[11:0], RN[11:0] Bit Rate	10f _{SYSCLK}	10f _{SYSCLK}	10f _{SYSCLK}	Mbps
tFALL	VODM fall time, 80%-20%, (RLOAD=100Ω ±1%)	200	300	400	ps
tRISE	VODM rise time, 20%-80%, (RLOAD=100Ω ±1%)	200	300	400	ps
tSKEW	Differential Skew			50	ps

18.4 JTAG Port Interface

Table 23 JTAG Port Interface (Figure 34)

Symbol	Description	Min	Max	Units
fTCK	TCK Frequency		4	MHz
tHITCK	TCK HI Pulse Width	100		ns
tLOTCK	TCK LO Pulse Width	100		ns
tSTMS	TMS Set-up time to TCK	25		ns
tHTMS	TMS Hold time to TCK	25		ns
tSTDI	TDI Set-up time to TCK	25		ns
tHTDI	TDI Hold time to TCK	25		ns
tPTDO	TCK Low to TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 34 JTAG Port Interface Timing



19 NSE-8G Ordering and Thermal Information

19.1 Packaging Information

Part No.	Description
PM8621-BIAP	480 Uni Ball Grid Array (UBGA) Package

19.2 Thermal Information

In a dense board application, this product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment¹.

Table 24 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life	105°C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance ² . This condition will typically be reached when local ambient reaches 85 °C.	125°C
Minimum ambient temperature (T_A)	-40 °C

Table 25 Device Compact Model³

Junction-to-Case Thermal Resistance, θ_{JC}	0.31 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	5.5 °C/W

Table 26 Heat Sink Requirements

$\theta_{SA} + \theta_{CS}$ ⁴	<p>The sum of $\theta_{SA} + \theta_{CS}$ must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}$ °C/W</p> <p>where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package</p>
	θ_{SA} and θ_{CS} are required for long-term operation

Power depends upon the operating mode. To obtain power information, refer 'High' power values in section 15.1 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core; for more information about this standard, see 5.
3. θ_{JC} , the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB} , the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see 4.

- θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

In a non-dense board application, this product is designed to operate over a wide temperature range and is suited for outside plant equipment¹.

Table 27 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life	105°C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance ² . This condition will typically be reached when local ambient reaches 85 °C.	125°C
Minimum ambient temperature (T_A)	-40 °C

Table 28 Thermal Resistance vs. Air Flow³

Airflow	Natural Convection	1 m/s	2 m/s
θ_{JA} (°C/W)	11.22	8.4	7.2

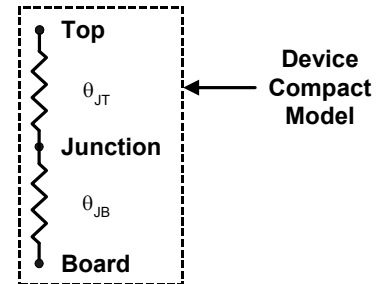


Table 29 Device Compact Model⁴

Junction-to-Top Thermal Resistance, θ_{JT}	0.31 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	5.5 °C/W

Power depends upon the operating mode. To obtain power information, refer 'High' power values in section 15.1 Power Requirements.

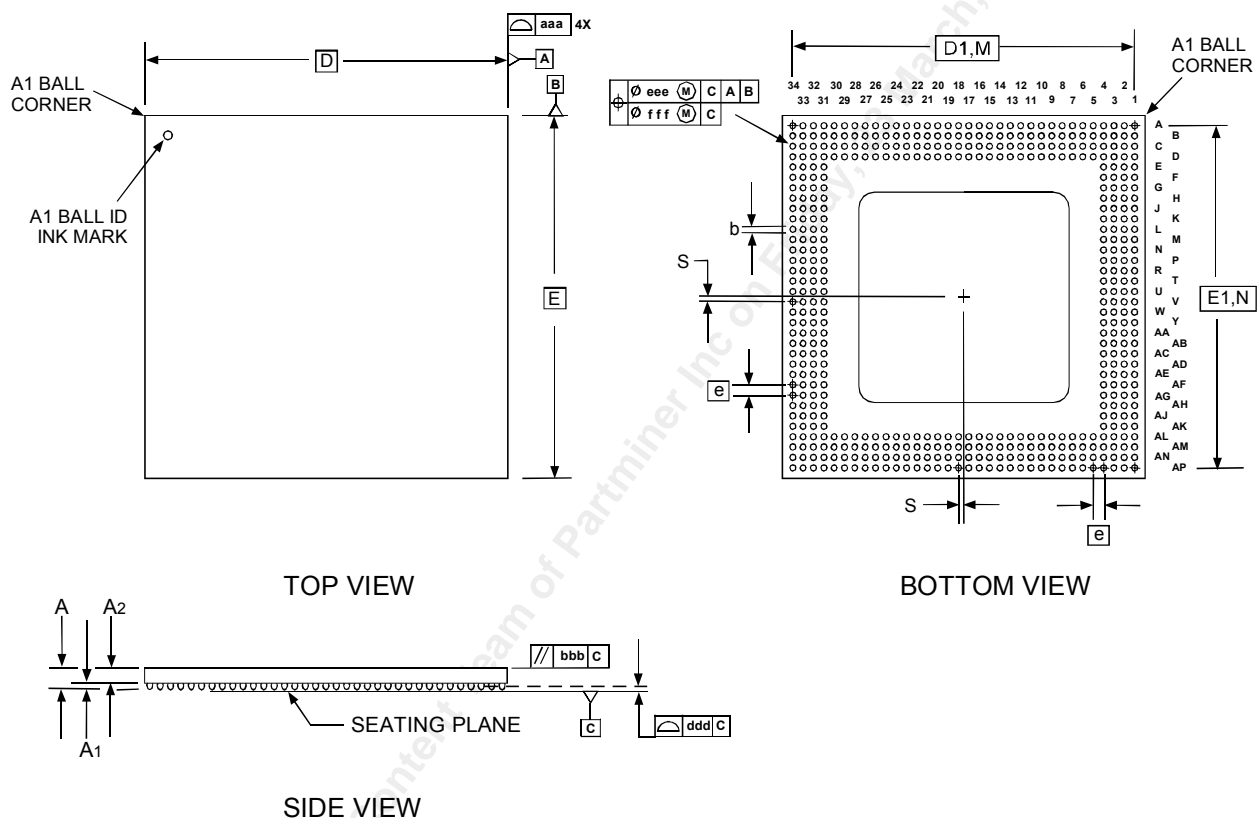
Notes

- The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
- Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core; for more information about this standard, see 5.
- θ_{JA} , the total junction to ambient thermal resistance, is measured according to JEDEC Standard JESD51 (2S2P); for more information about this standard, see 4.
- θ_{JB} , the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8 (for more information about this standard, see 4) and θ_{JT} , the junction-to-top thermal resistance, is obtained by simulating conditions described in SEMI Standard G30-88 (for more information about this standard, see 6).

20 Mechanical Information

The NSE-8G is packaged in the 480 UBGA package.

20.1 480 Pin UBGA -35x35mm Body - (B Suffix)



- NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
 2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
 3) DIMENSION bbb DENOTES PARALLEL.
 4) DIMENSION ccc DENOTES FLATNESS.
 5) DIMENSION ddd DENOTES COPLANARITY.
 6) DIAMETER OF SOLDER MASK OPENING IS 0.45 +/- 0.025 MM (SMD).

PACKAGE TYPE : 480 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 35 x 35 x 1.47 MM																
Dim.	A	A1	A2	D	D1	E	E1	M,N	b	e	aaa	bbb	ddd	eee	fff	S
Min.	1.32	0.40	0.92	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.47	0.50	0.97	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.63	1.00 BSC	-	-	-	-	-	-
Max.	1.62	0.60	1.02	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.30	0.10	0.05

Notes

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