CD29FCT520T

December 1996

Fast CMOS Multilevel Pipeline Register

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pinout and Function Compatible with IDT29FCT520, QS29FCT520 and AMD's Am29520**
- **Four 8-bit High-Speed Registers**
- **Hold, Transfer, and Load Instructions**
- **Dual Two-Level or Single Four-Level Pipeline Operation**
- **TTL Input and Output Levels, Reducing Problematic Ground Bounce**
- **High Output Drive ..... I_{OL} = 48mA**
- **Extremely Low Static Power ..... 1mW (Typ)**

Description

These devices are multilevel pipeline registers containing four 8-bit positive triggered registers which can be configured as a dual 2-level or a single 4-level pipeline. These products are designed for use as temporary storage or for storage delays in pipelined systems. When data is entered into the first level (I = 2 or I = 1) of the CD29FCT520T, the existing data in the first level is moved to the second level. The I = 3 shift instruction puts the registers on hold.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD29FCT520ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT520ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD29FCT520BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT520BTQM	-40 to 85	24 Ld QSOP	M24.15-P

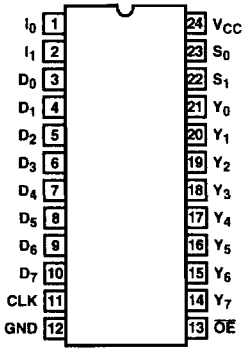
NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

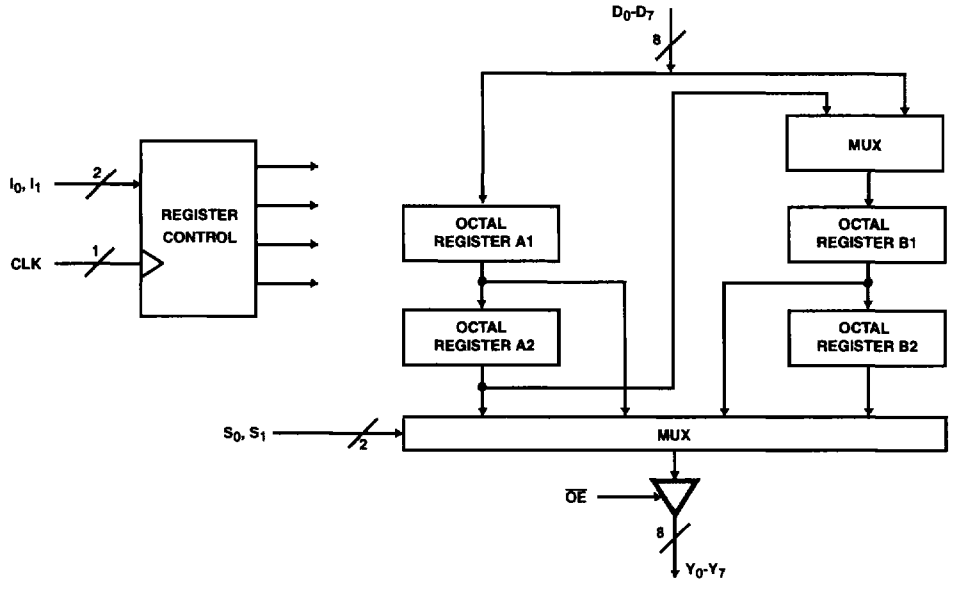
CD29FCT520T
(QSOP, SOIC)

TOP VIEW



File Number **4164.1**

Functional Block Diagram



Register Selection

S1	S0	REGISTER
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW) for Three-State Output Port
CLK	Clock Input. Enter Data into Registers on LOW-to-HIGH Transistions
I_0, I_1	Instruction Inputs
S_0, S_1	Multiplexer Select. Inputs Either Register A_1, A_2, B_1, or B_2 Data to be Avaialbe at the Output Ports
D_X	Register Inputs
Y_X	Register Outputs
GND	Ground
V_{CC}	Power

CD29FCT520T Data Loading (Note 1)

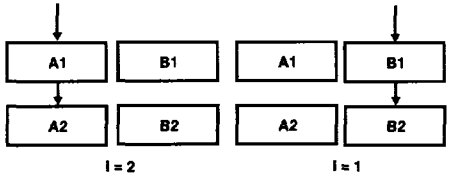


FIGURE 1. DUAL 2-LEVEL

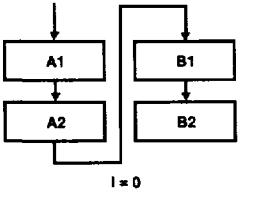


FIGURE 2. SINGLE 4-LEVEL

NOTE: I = 3 for hold.

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µ A
High Impedance Output Current	I_{OZH}	VCC = Max	V_{OUT} = 2.7V	-	-	1	µ A
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µ A
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µ A
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µ A
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 9)	mA

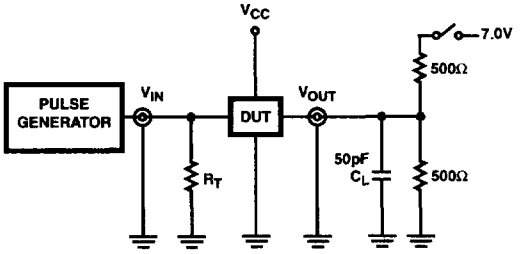
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	UNITS
Propagation Delay CLK to Y_X	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	2.0	14.0	2.0	7.5	ns
Propagation Delay S_0 or S_1 to Y_X	t_{PLH}, t_{PHL}		2.0	13.0	2.0	7.5	ns
Setup Time HIGH or LOW D_X to CLK	t_{SU}		5.0	-	2.5	-	ns
Hold Time HIGH or LOW D_X to CLK	t_H		2.0	-	2.0	-	ns
Setup Time HIGH or LOW I_0 or I_1 to CLK	t_{SU}		5.0	-	4.0	-	ns
Hold Time HIGH or LOW I_0 or I_1 to CLK	t_H		2.0	-	2.0	-	ns
Output Enable Time $\overline{OE}$ to Y_X	t_{PZH}, t_{PZL}		1.5	12.0	1.5	7.0	ns
Output Disable Time $\overline{OE}$ to Y_X (Note 13)	t_{PHZ}, t_{PLZ}		1.5	15.0	1.5	7.5	ns
Clock Pulse Width HIGH or LOW (Note 13)	t_W		7.0	-	5.5	-	ns

NOTES:

2. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
3. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. This parameter is determined by device characterization but is not production tested.
6. Per TTL driven input (V_{IN} = 3.4V, control inputs only); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
10. See test circuit and wave forms.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:
C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

13. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 3. TEST CIRCUIT

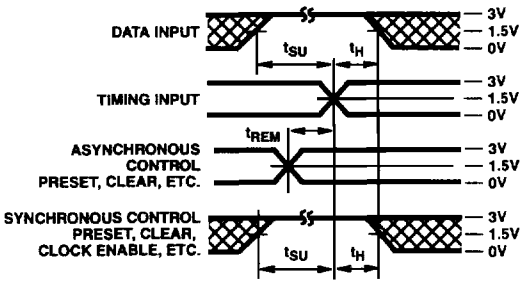


FIGURE 4. SETUP, HOLD, AND RELEASE TIMING

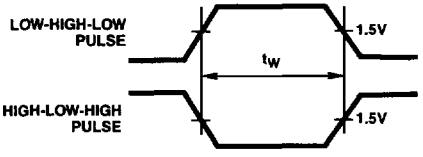


FIGURE 5. PULSE WIDTH

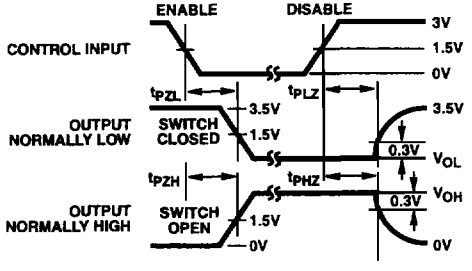


FIGURE 6. ENABLE AND DISABLE TIMING

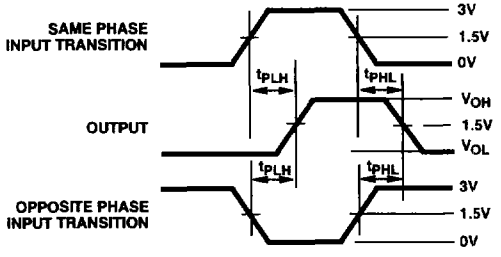


FIGURE 7. PROPAGATION DELAY