V826632M24SA
32M x 64 HIGH PERFORMANCE UNBUFFERED DDR SDRAM MICRODIMM MODULE

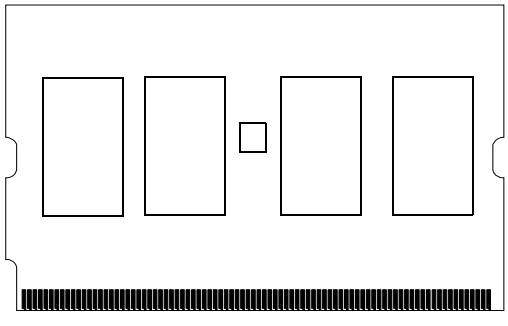
Features

- 172 Pin Unbuffered 33,554,432 x 64 bit Organization DDR MICRODIMM Modules
- Utilizes High Performance 32M x 8 DDR SDRAM in SOC Packages
- Single +2.5V (± 0.2V) Power Supply
- Single +2.6V (± 0.1V) Power Supply for DDR400
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are SSTL-2 Compatible
- 8192 Refresh Cycles every 64 ms
- Serial Presence Detect (SPD)

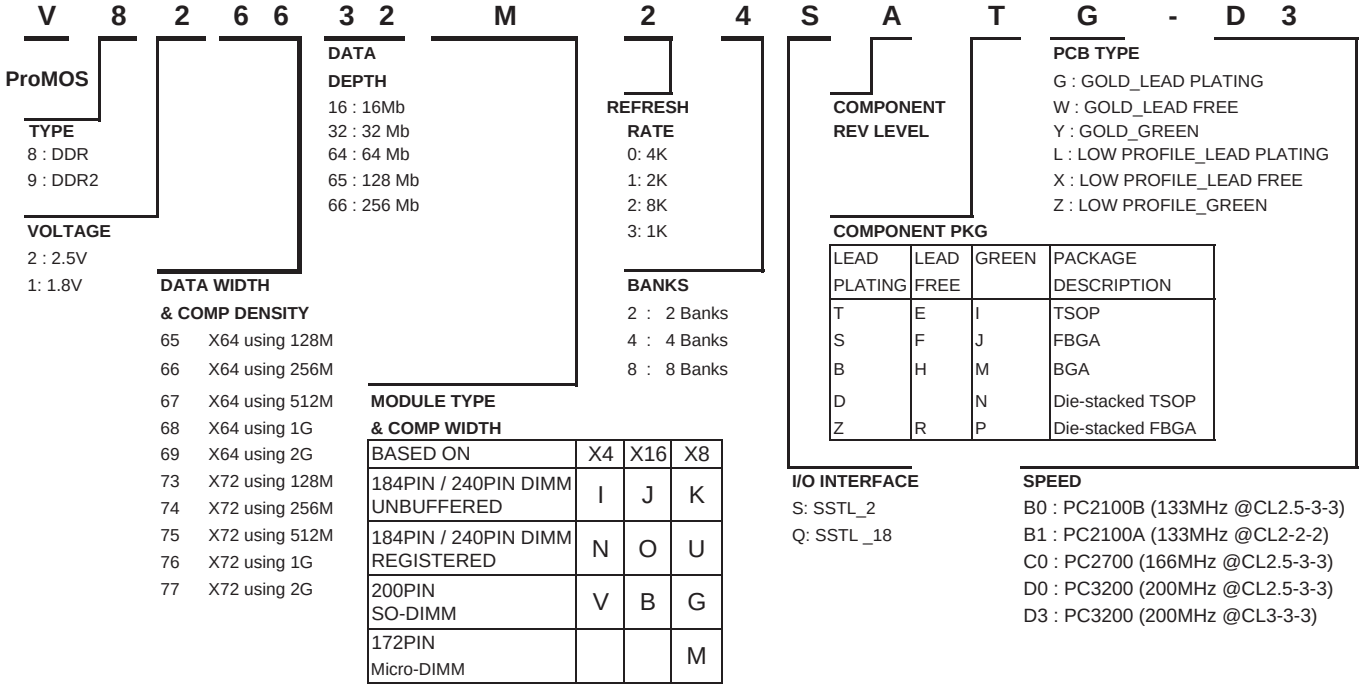
Description

The V826632M24SA memory module is organized 33,554,432 x 64 bits in a 172 pin memory module. The 32M x 64 memory module uses 8 ProMOS 32M x 8 DDR SDRAM. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

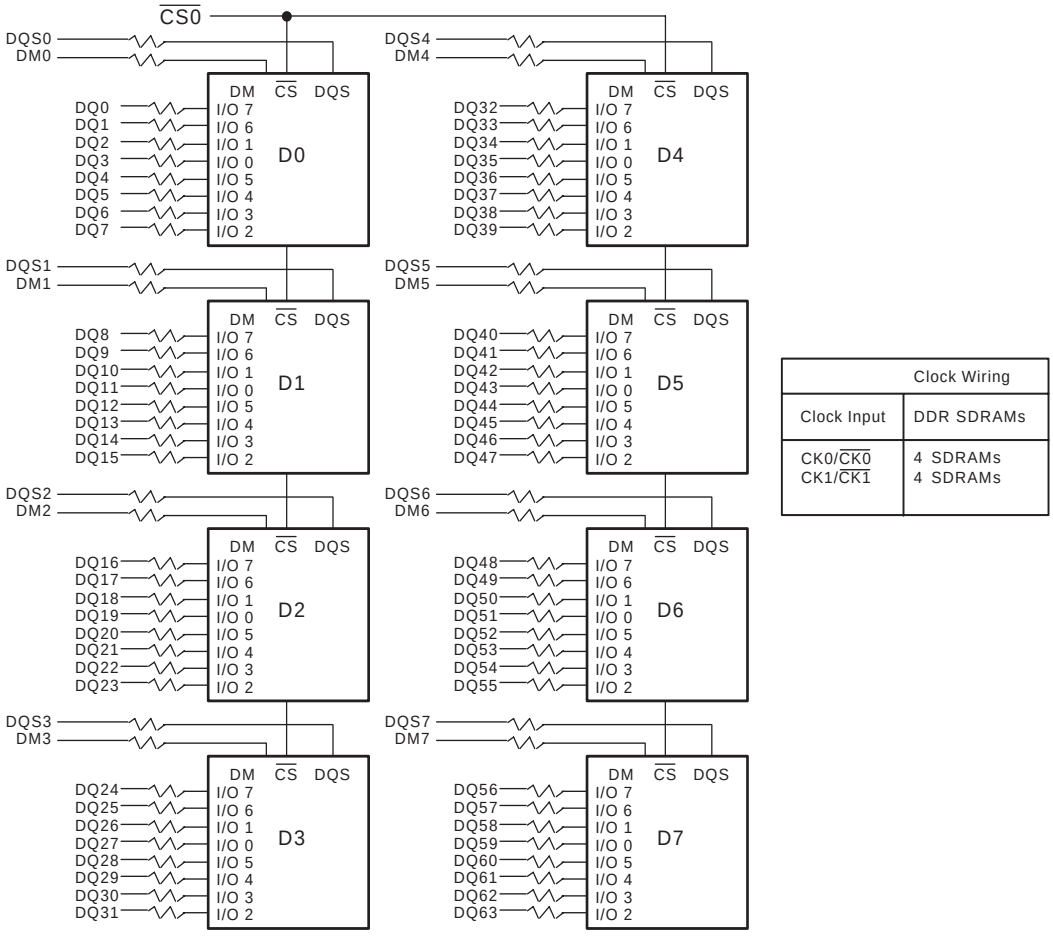
	Module Speed	D0	D3	C0	B1	B0	Units
	Clock Frequency (max.)	200 (PC400A)	200 (PC400B)	166 (PC333)	143 (PC266A)	133 (PC266B)	MHz
t_{CK}	Clock Cycle Time $\overline{\text{CAS}}$ Latency = 2	7.5	7.5	7.5	7.5	10	ns
	Clock Cycle Time $\overline{\text{CAS}}$ Latency = 2.5	5	6	6	7	7.5	ns
	Clock Cycle Time $\overline{\text{CAS}}$ Latency = 3	5	5	-	-	-	ns
t_{RCD}	tRP parameter	3	3	3	2	3	CLK
t_{RP}	tRCD parameter	3	3	3	2	3	CLK



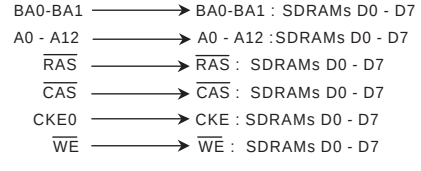
Part Number Information

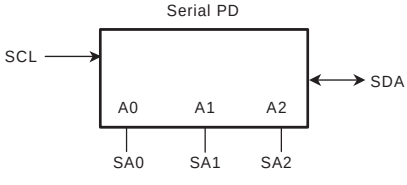


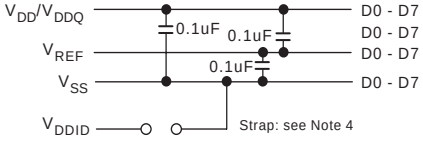
Block Diagram



Clock Wiring	
Clock Input	DDR SDRAMs
CK0/$\overline{CK0}$	4 SDRAMs
CK1/$\overline{CK1}$	4 SDRAMs







Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ,DQS, DM/DQS resistors : 22 Ohms.
4. VDDID strap connections
   (for memory device VDD, VDDQ) :
   STRAP OUT (OPEN): VDD=VDDQ
   STRAP IN (V_{SS}): VDD VDDQ

Pin Configurations (Front Side/Back Side)

Front Side

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	45	V_{DD}	87	A10/AP	131	V_{DD}
3	V_{SS}	47	DQS2	89	V_{DD}	133	V_{SS}
5	DQ0	49	DQ18	91	BA0	135	V_{SS}
7	DQ1	51	V_{SS}	93	WE#	137	DQ48
9	V_{DD}	53	DQ19	95	S0#	139	DQ49
11	DQS0	55	DQ24	97	NC	141	V_{DD}
13	DQ2	57	V_{DD}	99	V_{SS}	143	DQS6
15	V_{SS}	59	DQ25	101	DQ32	145	DQ50
17	DQ3	61	DQS3	103	DQ33	147	V_{SS}
19	DQ8	63	V_{SS}	105	V_{DD}	149	DQ51
21	V_{DD}	65	DQ26	107	DQS4	151	DQ56
23	DQ9	67	DQ27	109	DQ34	153	V_{DD}
25	DQS1	69	V_{DD}	111	V_{SS}	155	DQ57
27	V_{SS}	71	DNU	113	DQ35	157	DQS7
29	DQ10	73	A12	115	DQ40	159	V_{SS}
31	DQ11	75	A9	117	V_{DD}	161	DQ58
33	V_{DD}	77	A7	119	DQ41	163	DQ59
35	CK0	79	V_{SS}	121	DQS5	165	V_{DD}
37	CK0#	81	A5	123	V_{SS}	167	SDA
39	V_{SS}	83	A3	125	DQ42	169	SCL
41	DQ16	85	A1	127	DQ43	171	V_{DDSPD}
43	DQ17			129	V_{DD}		

Back Side

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
2	V_{REF}	46	V_{DD}	88	BA1	132	CK1#
4	V_{SS}	48	DM2	90	V_{DD}	134	CK1
6	DQ4	50	DQ22	92	RAS#	136	V_{SS}
8	DQ5	52	V_{SS}	94	CAS#	138	DQ52
10	V_{DD}	54	DQ23	96	DNU	140	DQ53
12	DM0	56	DQ28	98	NC	142	V_{DD}
14	DQ6	58	V_{DD}	100	V_{SS}	144	DM6
16	V_{SS}	60	DQ29	102	DQ36	146	DQ54
18	DQ7	62	DM3	104	DQ37	148	V_{SS}
20	DQ12	64	V_{SS}	106	V_{DD}	150	DQ55
22	V_{DD}	66	DQ30	108	DM4	152	DQ60
24	DQ13	68	DQ31	110	DQ38	154	V_{DD}
26	DM1	70	V_{DD}	112	V_{SS}	156	DQ61
28	V_{SS}	72	CKE0	114	DQ39	158	DM7
30	DQ14	74	A11	116	DQ44	160	V_{SS}
32	DQ15	76	A8	118	V_{DD}	162	DQ62
34	V_{DD}	78	A6	120	DQ45	164	DQ63
36	V_{DD}	80	V_{SS}	122	DM5	166	V_{DD}
38	V_{SS}	82	A4	124	V_{SS}	168	SA0
40	V_{SS}	84	A2	126	DQ46	170	SA1
42	DQ20	86	A0	128	DQ47	172	SA2
44	DQ21			130	V_{DD}		

Pin Names

Pin	Pin Description
CK0, $\overline{CK0}$ CK1, $\overline{CK1}$	Differential Clock Inputs
$\overline{CS0}$	Chip Select Input
CKE0	Clock Enable Input
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Commend Sets Inputs
A0 ~ A12	Address
BA0, BA1	Bank Address
DQ0~DQ63	Data Inputs/Outputs
DQS0~DQS7	Data Strobe Inputs/Outputs
DM0~DM7	Data-in Mask
VDD	Power Supply

Pin	Pin Description
VDDQ	DQs Power Supply
VSS	Ground
VREF	Reference Power Supply
VDDSPD	Power Supply for SPD
SA0~SA2	E^2 PROM Address Inputs
SCL	E^2 PROM Clock
SDA	E^2 PROM Data I/O
VDDID	VDD Identification Flag
DU	Do not Use
NC	No Connection

Serial Presence Detect Information

Bin Sort:
D0 (PC3200 @ CL 2.5-3-3)
D3 (PC3200 @ CL 3-3-3)
C0 (PC2700 @ CL 2.5-3-3)
B1 (PC2100A @ CL 2-2-2)
B0 (PC2100B @ CL 2.5-3-3)

Byte #	Function described	Function Supported					Hex value				
		D0	D3	C0	B1	B0	D0	D3	C0	B1	B0
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes					80h				
1	Total # of Bytes of SPD memory device	256bytes					08h				
2	Fundamental memory type	SDRAM DDR					07h				
3	# of row address on this assembly	13					0Dh				
4	# of column address on this assembly	10					0Ah				
5	# of module Rows on this assembly	1 Bank					01h				
6	Data width of this assembly	64 bits					40h				
7	.....Data width of this assembly	-					00h				
8	VDDQ and interface standard of this assembly	SSTL 2.5V					04h				
9	DDR SDRAM cycle time at highest CAS Latency	5ns	5ns	6ns	7ns	7.5ns	50h	50h	60h	70h	75h
10	DDR SDRAM Access time from clock at highest CL	±0.65ns	±0.65ns	±0.70ns	±0.75ns	±0.75ns	65h	65h	70h	75h	75h
11	DIMM configuration type(Non-parity, Parity, ECC)	Non-parity, ECC					00h				
12	Refresh rate & type	7.8us & Self refresh					82h				
13	Primary DDR SDRAM width	x8					08h				
14	Error checking DDR SDRAM data width	N/A					00h				
15	Minimum clock delay for back-to-back random column address	t_{CCD}=1CLK					01h				
16	DDR SDRAM device attributes : Burst lengths supported	2,4,8					0Eh				
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	4 banks					04h				
18	DDR SDRAM device attributes : CAS Latency supported	2,2.5,3					1Ch	1Ch	0Ch	0Ch	0Ch
19	DDR SDRAM device attributes : CS Latency	0CLK					01h				
20	DDR SDRAM device attributes : WE Latency	1CLK					02h				
21	DDR SDRAM module attributes	Differential clock / non Registered					20h				
22	DDR SDRAM device attributes : General	+/-0.2V voltage tolerance					00h				
23	DDR SDRAM cycle time at second highest CL	5.0ns	6.0ns	7.5ns	7.5ns	10ns	50h	60h	75h	75h	A0h
24	DDR SDRAM Access time from clock at second highest CL	±0.65ns	±0.70ns	±0.70ns	±0.75ns	±0.75ns	65h	70h	70h	75h	75h
25	DDR SDRAM cycle time at third highest CL	7.5ns	7.5ns	-	-	-	75h	75h	00h	00h	00h

Serial Presence Detect Information (cont.)

Byte #	Function described	Function Supported					Hex value				
		D0	D3	C0	B1	B0	D0	D3	C0	B1	B0
26	DDR SDRAM Access time from clock at third highest CL	±0.75ns	±0.75ns	-	-	-	75h	75h	00h	00h	00h
27	Minimum row precharge time (=t_{RP})	15ns	15ns	18ns	15ns	20ns	3Ch	3Ch	48h	3Ch	50h
28	Minimum row activate to row active delay (=t_{RRD})	10ns	10ns	12ns	15ns	15ns	28h	28h	30h	3Ch	3Ch
29	Minimum RAS to CAS delay (=t_{RCD})	15ns	15ns	18ns	15ns	20ns	3Ch	3Ch	48h	3Ch	50h
30	Minimum active to precharge time (=t_{RAS})	40ns	40ns	42ns	45ns	45ns	28h	28h	2Ah	2Dh	2Dh
31	Module ROW density	256MB					40h				
32	Command and address signal input setup time	0.6ns	0.6ns	0.75ns	0.9ns	0.9ns	60h	60h	75h	90h	90h
33	Command and address signal input hold time	0.6ns	0.6ns	0.75ns	0.9ns	0.9ns	60h	60h	75h	90h	90h
34	Data signal input setup time	0.4ns	0.4ns	0.45ns	0.5ns	0.5ns	40h	40h	45h	50h	50h
35	Data signal input hold time	0.4ns	0.4ns	0.45ns	0.5ns	0.5ns	40h	40h	45h	50h	50h
36-40	Superset information (may be used in future)						00h				
41	SDRAM device minimum active to active/auto-refresh time (=t_{RC})	60ns	60ns	60ns	65ns	65ns	3Ch	3Ch	3Ch	41h	41h
42	SDRAM device minimum active to autorefresh to active/auto-refresh time (=t_{RFC})	70ns	70ns	72ns	75ns	75ns	46h	46h	48h	4Bh	4Bh
43	SDRAM device maximum device cycle time (=$t_{CK\ MAX}$)	12ns	12ns	12ns	12ns	12ns	30h	30h	30h	30h	30h
44	SDRAM device maximum skew between DQS and DQ signals (=t_{DQSQ})	0.4ns	0.4ns	0.45ns	0.5ns	0.5ns	28h	28h	2Dh	32h	32h
45	SDRAM device maximum read datahold skew factor (=t_{QHS})	0.55ns	0.55ns	0.60ns	0.75ns	0.75ns	55h	55h	60h	75h	75h
46-61	Superset information (may be used in future)	-					00h				
62	SPD data revision code	Initial release					11h	11h	00h	00h	00h
63	Checksum for Bytes 0 ~ 62	-					A3h	BEh	4Bh	CAh	22h
64	Manufacturer JEDEC ID code	ProMOS					40h				
65 -71	..... Manufacturer JEDEC ID code						00h				
72	Manufacturing location	02=Taiwan 05=China 0A=S-CH									
73-90	Module part number (ASCII)	V826632M24SA									
91	Manufacturer revison code (For PCB)	0					00				
92	Manufacturer revison code (For component)	0					00				
93	Manufacturing date (Year)	-					-				
94	Manufacturing date (Week)	-					-				
95~98	Assembly serial #	-					-				

Byte #	Function described	Function Supported					Hex value				
		D0	D3	C0	B1	B0	D0	D3	C0	B1	B0
99~127	Manufacturer specific data (may be used in future)	Undefined					00h				
128~255	Open for customer use	Undefined					00h				

DC Operating Conditions

(T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Power Supply Voltage for DDR400	V_{DD}	2.5	2.6	2.7	V	
Power Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Power Supply Voltage for DDR400	V_{DDQ}	2.5	2.6	2.7	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	V_{REF} - 0.15	V	2
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	
Reference Voltage	V_{REF}	$V_{DDQ/2}$ - 0.05	-	$V_{DDQ/2}$ + 0.05	V	
Input Leakage Current	I_I	-2	-	2	µA	
Output Leakage Current	IO_z	-5	-	5	µA	
Output High Current (V_{OUT} = 1.95V)	IO_H	-16.8	-	-	mA	
Output Low Current (V_{OUT} = 0.35V)	IO_L	16.8	-	-	mA	

Notes: 1. V_{DDQ} must not exceed the level of V_{DD}.
2. V_{IL} (min) is acceptable -1.5V AC pulse width with <= 5ns of duration.

AC Operating Conditions

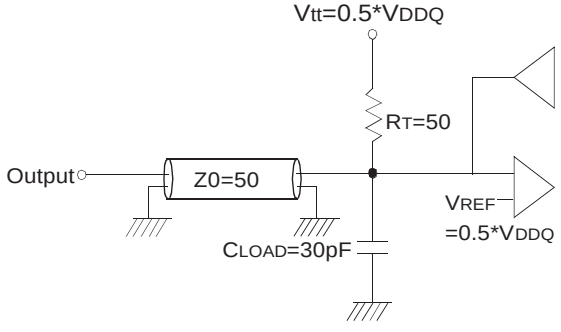
(T_A = 0 to 70 °C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	$V_{IL(AC)}$		V_{REF} - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX(AC)}$	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V	2

Notes: 1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of VIX is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

AC Operating Test Conditions (T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Value	Unit
Reference Voltage	V_{DDQ} x 0.5	V
Termination Voltage	V_{DDQ} x 0.5	V
AC Input High Level Voltage (V_{IH}, min)	V_{REF} + 0.31	V
AC Input Low Level Voltage (V_{IL}, max)	V_{REF} - 0.31	V
Input Timing Measurement Reference Level Voltage	V_{REF}	V
Output Timing Measurement Reference Level Voltage	V_{TT}	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (R_T)	50	ohm
Series Resistor (R_S)	25	ohm
Output Load Capacitance for Access Time Measurement (C_L)	30	pF



Output Load Circuit (SSTL_2)

Input/Output Capacitance

(V_{DD} = 2.5V, V_{DD} = 2.6V, V_{DDQ} = 2.5V, V_{DDQ} = 2.6V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	CIN_1	29	34	pF
Input capacitance (CKE_0)	CIN_2	29	34	pF
Input capacitance ($\overline{CS_0}$)	CIN_3	26	30	pF
Input capacitance (CLK_1, CLK_2)	CIN_4	30	32	pF
Data & DQS input/output capacitance (DQ_0~DQ_{63})	C_{OUT}	8	9	pF
Input capacitance (DM0~DM8)	CIN_5	8	9	pF

DDR SDRAM Module I_{DD} Spec Table

Symbol		D0 / D3 PC3200@CL=3	C0 PC2700A@CL=2.5	B1 PC2100A@CL=2	B0 PC2100B@CL=2.5	Unit
IDD0		960	880	800	800	mA
IDD1		1280	1120	960	960	mA
IDD2P		60	60	60	60	mA
IDD2F		330	280	250	250	mA
IDD2Q		220	190	170	170	mA
IDD3P		340	300	260	260	mA
IDD3N		580	480	380	380	mA
IDD4R		2160	1840	1520	1520	mA
IDD4W		2000	1680	1360	1360	mA
IDD5		1680	1600	1520	1520	mA
IDD6	Normal	48	48	48	48	mA
	Low power	29	29	29	29	mA
IDD7		3200	2800	2400	2400	mA

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

Detailed test conditions for DDR SDRAM IDD1 & IDD

IDD1 : Operating current: One bank operation
1. Typical Case : Vdd = 2.5V, T=25' C

2. Worst Case : Vdd = 2.7V, T= 10' C

3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA

4. Timing patterns
- DDR333 (166MHz, CL=2.5) : tCK=6ns, CL=2.5, BL=4, tRCD=3*tCK, tRC=10*tCK, tRAS=7*tCK
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

- DDR400B (200MHz, CL=3) : tCK=5ns, CL=3, BL=4, tRCD=3*tCK, tRC=12*tCK, tRAS=8*tCK
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

- DDR400A (200MHz, CL=2.5) : tCK=5ns, CL=2.5, BL=4, tRCD=3*tCK, tRC=12*tCK, tRAS=8*tCK
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Sym-bol	(PC400A) D0		(PC400B) D3		(PC333) C0		(PC266A) B1		(PC266B) B0		Units	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row Cycle Time		t_{RC}	60	-	60	-	60	-	65	-	65	-	ns	
Auto Refresh Row Cycle Time		t_{RFC}	70	-	70	-	72	-	75	-	75	-	ns	
Row Active Time		t_{RAS}	40	120K	40	120K	42	120K	45	120K	45	120K	ns	
Row Address to Column Address Delay		t_{RCD}	15	-	15	-	18	-	15	-	20	-	ns	
Row Active to Row Active Delay		t_{RRD}	10	-	10	-	12	-	15	-	15	-	ns	
Column Address to Column Address Delay		t_{CCD}	1	-	1	-	1	-	1	-	1	-	tCK	
Row Precharge Time		t_{RP}	15	-	15	-	18	-	15	-	20	-	ns	
Write Recovery Time		t_{WR}	15	-	15	-	15	-	15	-	15	-	ns	
Last Data-In to Read Command		t_{DRL}	1	-	1	-	1	-	1	-	1	-	tCK	
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	35	-	35	-	35	-	35	-	35	-	ns	
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK}	5	12	5	12	-	12	-	12	-	12	ns	
	$\overline{CAS}$ Latency = 2.5		5	12	6	12	6	12	7	12	7.5	12	ns	
	$\overline{CAS}$ Latency = 2		7.5	12	7.5	12	7.5	12	7.5	12	10	12	ns	
Clock High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Data-Out edge to Clock edge Skew		t_{AC}	-0.65	0.65	-0.65	0.65	-0.75	0.75	-0.75	0.75	-0.75	0.75	tCK	
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.60	0.60	-0.60	0.60	-0.75	0.75	-0.75	0.75	-0.75	0.75	tCK	
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.40	-	0.40	-	0.45	-	0.5	-	0.5	tCK	
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	t_{HPmin} -0.75ns	-	tCK	1
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	tCK	1
Input Setup Time (fast slew rate)		t_{IS}	0.6	-	0.6	-	0.75	-	0.9	-	0.9	-	tCK	2,3,5,6
Input Hold Time (fast slew rate)		t_{IH}	0.6	-	0.6	-	0.75	-	0.9	-	0.9	-	tCK	2,3,5,6
Input Setup Time (slow slew rate)		t_{IS}	0.75	-	0.75	-	0.8	-	1.0	-	1.0	-	tCK	2,4,5,6
Input Hold Time (slow slew rate)		t_{IH}	0.75	-	0.75	-	0.8	-	1.0	-	1.0	-	tCK	2,4,5,6
Input Pulse Width		t_{IPW}	0.4	0.6	0.4	0.6	0.4	0.6	2.2	-	2.2	-	tCK	6
Write DQS High Level Width		t_{DQSH}	0.35		0.35		0.35		0.35		0.35		tCK	
Write DQS Low Level Width		t_{DQSL}	0.35		0.35		0.35		0.35		0.35		tCK	
CLK to First Rising edge of DQS-In		t_{DQSS}	0.72	1.25	0.72	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	

AC Characteristics (cont.)

Parameter	Sym-bol	(PC400A) D0		(PC400B) D3		(PC333) C0		(PC266A) B1		(PC266B) B0		Units	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data-In Setup Time to DQS-In (DQ & DM)	t_{DS}	0.40	-	0.40	-	0.45	-	0.5	-	0.5	-	tCK	7
Data-in Hold Time to DQS-In (DQ & DM)	t_{DH}	0.40	-	0.40	-	0.45	-	0.5	-	0.5	-	tCK	7
DQ & DM Input Pulse Width	t_{DIPW}	1.75	-	1.75	-	1.75	-	1.75	-	1.75	-	tCK	
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read DQS Postamble Time	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write DQS Preamble Setup Time	t_{WPRES}	0	-	0	-	0	-	0	-	0	-	tCK	
Write DQS Preamble Hold Time	t_{WPREH}	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK	
Write DQS Postamble Time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Mode Register Set Delay	t_{MRD}	2	-	2	-	2	-	2	-	2	-	tCK	
Power Down Exit Time to any command	t_{XPDN}	1	-	1	-	1	-	1	-	1	-	tCK	
Exit Self Refresh to Non-Read Command	t_{XSNR}	200	-	200	-	200	-	200	-	200	-	tCK	8
Average Periodic Refresh Interval	t_{REFI}	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us	

Notes: 1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
5. CK, $\overline{CK}$ slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(DQS) : DQ, DM
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

Absolute Maximum Ratings

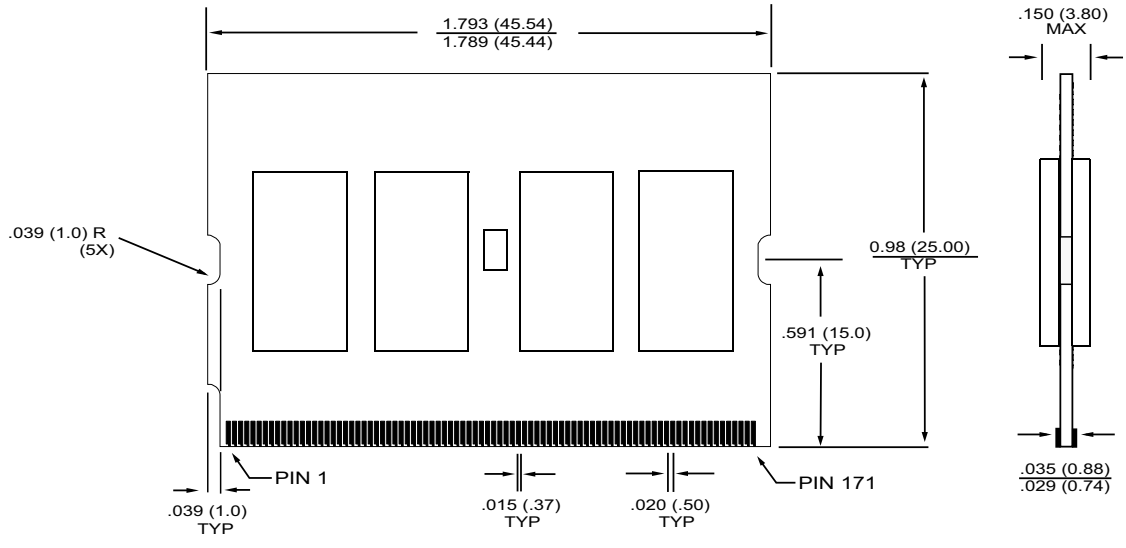
Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 3.6	V
Output Short Circuit Current	I_{OS}	50	mA
Power Dissipation	P_D	6	W
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • Sec

Note: Operation at above absolute maximum rating can adversely affect device reliability

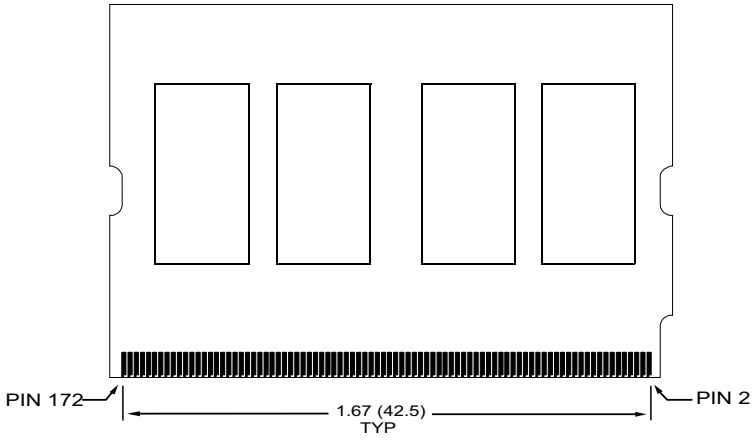
Package Dimensions

172-PIN MicroDIMM
All Modules

Front View

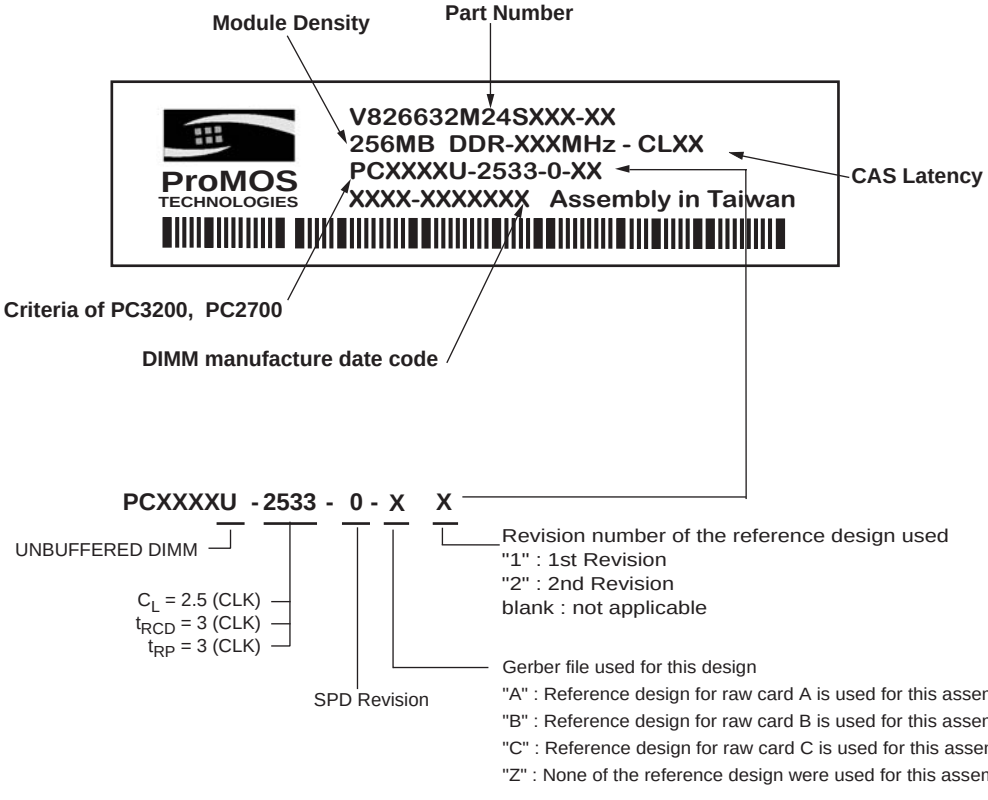


Back View



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Label Information



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