REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y. Change memory skew timing , t9, in Table I. - PHN	10-01-06	Thomas M. Hess
B	Change the maximum values of Core supply voltage and I/O supply voltage in section 1.3. Change and add the tests for t_{22}, t_{23a}, t_{23b}, t_{24} in Table IA. Change Figure 13 and add Figure 14 for timing waveforms and test circuits. Update boilerplate to current MIL-PRF-38535 requirements. - PHN	13-02-19	Thomas M. Hess

REV	B	B	B	B	B	B	B	B	B	B	B	B								
SHEET	35	36	37	38	39	40	41	42	43	44	45	46								
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS OF SHEETS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles F. Saffle

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
09-05-28

REVISION LEVEL
B

MICROCIRCUIT, DIGITAL, CMOS, RADIATION HARDENED, 32-BIT FAULT-TOLERANT V8/LEON 3FT PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-08228**

SHEET 1 OF 46

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	F	08228	01	V	X	C
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	UT699	32-bit fault-tolerant V8/LEON 3FT processor
02 1/	UT699	32-bit fault-tolerant V8/LEON 3FT processor With additional screening 2/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	352	Ceramic quad flat-pack
Y	See figure 1	484	Ceramic land grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

.

1/ This device has restricted temperature range of -40°C to +105°C.
2/ Device type 02 provides a QML class Q product with the additional testing as specified in paragraph 4.4.2.d herein.

1.3 Absolute maximum ratings. 1/ 2/

Core supply voltage range (V_{DDC})	-0.3 V dc to 3.6 V dc
I/O supply voltage range (V_{DD})	-0.3 V dc to 4.3 V dc
Input voltage range on any pin (V_{IN})	V_{SS} - 0.3 V dc to V_{DD} + 0.3 V dc
Power dissipation (P_D) (T_C = 105°C)	9 W 3/
Storage temperature range (T_{STG})	-65°C to 150°C
Maximum junction temperature (T_J)	150°C 4/
Thermal resistance, junction to case (θ_{JC})	5°C/W
Case operating temperature range (T_C)	-40°C to +105°C
Minimum ESD protection (human body model) (ESD_{HBM})	2000 V

1.4 Recommended operating conditions.

Core supply voltage range (V_{DDC})	2.3 V dc to 2.7 V dc
I/O supply voltage range (V_{DD})	3.0 V dc to 3.6 V dc
Input voltage range on any pin (V_{IN})	0 V dc to V_{DD}
Case operating temperature range (T_C)	-40°C to +105°C
Maximum rise time, all CMOS and PCI inputs (t_r)	20 ns
Maximum fall time, all CMOS and PCI inputs (t_f)	20 ns

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	≥ 300 krad (Si)	
Single event phenomenon (SEP):		
Linear energy transfer (LET) with no latchup (SEL)	≥ 108 MeV-cm^2/mg	5/ 6/
Linear energy transfer (LET) with no upset (SEU)	≥ 54 MeV-cm^2/mg	5/ 7/
Neutron fluence	≥ 1 x 10^{14} neutrons/cm^2	5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values are with respect to V_{SS} (Ground).

3/ Per MIL-STD-883, method 1012, section 3.4.1, $P_D = (T_J(\max) - T_C(\max))/\theta_{JC}$.

4/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life testing.

5/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

6/ Worst case temperature and voltage of T_A = +125°C, V_{DD} = 3.6 V, V_{DDC} = 2.7 V.

7/ Onset LET is for flip-flop memory. Single event upsets for embedded RAM memory are driven by charged particle flux, rather than 'LET', due to the fault tolerant design architecture. Contact manufacturer for details.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices

(Copies of this document are available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959).

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as specified on figures 4 through 17.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance. These devices shall be compliant to IEEE 1149.1.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-40°C \le T_C \le +105°C$, $+3.0\ V \le V_{DD} \le +3.6\ V$, $+2.3\ V \le V_{DDC} \le +2.7\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power Supply Operating Characteristics							
Active core power supply current	I_{DDC} 2/ 3/	V_{DDC} = 2.7 V, V_{DD} = 3.6 V For 25 MHz ≤ f_{SYSCLK} ≤ 66 MHz All clock inputs are running at f_{SYSCLK}.	1, 2, 3	All		27	mA/ MHz
Active I/O power supply current	I_{DD} 2/ 4/	V_{DDC} = 2.7 V, V_{DD} = 3.6 V For 25 MHz ≤ f_{SYSCLK} ≤ 66 MHz All clock inputs are running at f_{SYSCLK}.				0.75	mA/ MHz
Standby core power supply current	I_{DDCS}	T_C = -40°C and 25°C V_{DDC} = 2.7 V, V_{DD} = 3.6 V f_{SYSCLK} = 0 MHz, f_{ETH_CLK} = 0 MHz, f_{PCI_CLK} = 0 MHz, f_{SWP_CLK} = 0 MHz	1, 3			2	mA
		F				20	
		T_C = 105°C V_{DDC} = 2.7 V, V_{DD} = 3.6 V f_{SYSCLK} = 0 MHz, f_{ETH_CLK} = 0 MHz, f_{PCI_CLK} = 0 MHz, f_{SWP_CLK} = 0 MHz	2			20	
Standby I/O power supply quiescent current	I_{DDS}	V_{DDC} = 2.7 V, V_{DD} = 3.6 V f_{SYSCLK} = 0 MHz, f_{ETH_CLK} = 0 MHz, f_{PCI_CLK} = 0 MHz, f_{SWP_CLK} = 0 MHz	1, 2, 3			0.75	mA
Core power supply current power-down mode	I_{PDC} 5/	V_{DDC} = 2.7 V, V_{DD} = 3.6 V f_{SYSCLK} = 66 MHz, f_{ETH_CLK} = 0 MHz,				2.75	mA/ MHz
		f_{PCI_CLK} = 0 MHz, f_{SWP_CLK} = 0 MHz F				5	
I/O power supply current power-down mode	I_{PD} 5/	V_{DDC} = 2.7 V, V_{DD} = 3.6 V f_{SYSCLK} = 66 MHz, f_{ETH_CLK} = 0 MHz, f_{PCI_CLK} = 0 MHz, f_{SWP_CLK} = 0 MHz				0.75	mA/ MHz

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-40°C \le T_C \le +105°C$, $+3.0\ V \le V_{DD} \le +3.6\ V$, $+2.3\ V \le V_{DDC} \le +2.7\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC Characteristics for LVCMOS3 Inputs							
High-level input voltage	V_{IH}		1, 2, 3	All	$0.7V_{DD}$		V
Low-level input voltage	V_{IL}					$0.3V_{DD}$	V
Positive going threshold voltage for Schmitt inputs	V_{T+}					$0.7V_{DD}$	V
Negative going threshold voltage for Schmitt inputs	V_{T-}				$0.3V_{DD}$		V
Hysteresis voltage for Schmitt inputs	V_H				0.4		V
Input leakage current	I_{IN}	$V_{IN} = V_{DD}$				1	µA
		$V_{IN} = V_{SS}$			-1		
Input pin capacitance	C_{IN} 6/	f = 1 MHz; $V_{DD} = 0$ V, $V_{DDC} = 0$ V Case outline X	4			19	pF
		Case outline Y				16	
DC Characteristics for LVCMOS3 Outputs							
High-level output voltage	V_{OH} 7/	$I_{OH} = -100$ µA	1, 2, 3	All	V_{DD} – 0.25		V
		$I_{OH} = -12$ mA			2.4		
Low-level output voltage	V_{OL}	$I_{OL} = 100$ µA				0.25	V
		$I_{OL} = 12$ mA				0.4	
Three-state output current	I_{OZ}	$V_O = V_{DD}$			-10	10	µA
		$V_o = V_{SS}$			-10	10	
Short-circuit output current	I_{OS} 8/	$V_o = V_{DD}$, $V_{DD} = 3.6$ V				130	mA
		$V_o = V_{SS}$, $V_{DD} = 3.6$ V			-65		
Output pin capacitance	C_{OUT} 6/	f = 1 MHz; $V_{DD} = 0$ V, $V_{DDC} = 0$ V	4			16	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -40°C ≤ T_C ≤ +105°C, +3.0 V ≤ V_{DD} ≤ +3.6 V, +2.3 V ≤ V_{DDC} ≤ +2.7 V, unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
AC Electrical Characteristics for LVCMOS3 Inputs and Outputs								
System clock frequency	f_{CLK}			9, 10, 11	All		66	MHz
System clock high time	t_{HIGH}	See figure 4.				6.67		ns
System clock low time	t_{LOW}	See figure 4.				6.67		ns
System clock to SDRAM clock propagation delay	t_{DSD} 9/	See figure 4.				2	5	ns
SDRAM clock rise time	t_{RSD} 8/	f_{CLK} = 66 MHz V_O transitioning between V_{OH}(min) and V_{OL}(max)					2	ns
SDRAM clock fall time	t_{FSD} 8/	f_{CLK} = 66 MHz V_O transitioning between V_{OH}(min) and V_{OL}(max)					2	ns
SDRAM clock cycle-to-cycle jitter	t_{JCCSD} 8/	f_{CLK} = 66 MHz					500	ps
DC Electrical Characteristics for PCI Inputs								
High-level input voltage	V_{IH}			1, 2, 3	All	$0.5V_{DD}$		V
Low-level input voltage	V_{IL}						$0.3V_{DD}$	V
Input leakage current	I_{IN}	V_{IN} = V_{DD}					10	µA
		V_{IN} = V_{SS}				-10		
Input pin capacitance	C_{IN} 6/	f = 1 MHz; V_{DD} = 0 V, V_{DDC} = 0 V	Case outline X	4			19	pF
			Case outline Y				22	
DC Electrical Characteristics for PCI Outputs								
High-level output voltage	V_{OH}	I_{OH} = -500 µA		1, 2, 3	All	$0.9V_{DD}$		V
Low-level output voltage	V_{OL}	I_{OL} = 1500 µA					$0.1V_{DD}$	V
Three-state output current	I_{OZ}	V_O = V_{DD}				-10	10	µA
		V_O = V_{SS}				-10	10	
Short-circuit output current	I_{OS} 8/	V_O = V_{DD}, V_{DD} = 3.6 V					270	mA
		V_O = V_{SS}, V_{DD} = 3.6 V				-130		
Output pin capacitance	C_{OUT} 6/	f = 1 MHz; V_{DD} = 0 V, V_{DDC} = 0 V	Case outline X	4			19	pF
			Case outline Y				22	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-40°C \le T_C \le +105°C$, $+3.0\ V \le V_{DD} \le +3.6\ V$, $+2.3\ V \le V_{DDC} \le +2.7\ V$, unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
AC Electrical Characteristics for PCI Inputs							
PCI clock frequency	f_{PCI_CLK}		9, 10, 11	All		33	MHz
PCI clock high time	t_{HIGH}	See figure 5.			11		ns
PCI clock low time	t_{LOW}	See figure 5.			11		ns
Power Sequencing and Reset							
V_{DD} valid to V_{DDC} delay	t_{VCD} 10/	See figure 6. $V_{DD} \ge 3.0$ V, $V_{DDC} \ge 2.30$ V	9, 10, 11	All	0		ns
V_{DD} valid to control signals high-z ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROMS}}$[1:0], $\overline{\text{RWE}}$[3:0], $\overline{\text{RAMOE}}$[4:0], READ, $\overline{\text{SDWE}}$, and $\overline{\text{SDCS}}$[1:0] V_{DD} valid to outputs high-z (DATA[31:0], CB[7:0], and GPIO[15:0])	t_{VHBZ} 10/	See figure 6. $V_{DD} \ge 1.5$ V, $V_{DDC} = 0$ V				4	t_{CLK}
V_{DDC} valid to control signals valid-inactive ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROMS}}$[1:0], $\overline{\text{RWE}}$[3:0], $\overline{\text{RAMOE}}$[4:0], READ, $\overline{\text{SDWE}}$, $\overline{\text{SDCS}}$[1:0])	t_{CHBV} 10/	See figure 6. $V_{DD} \ge 3.0$ V, $V_{DDC} \ge 2.30$ V				4	t_{CLK}
V_{DDC} valid to $\overline{\text{RESET}}$ deassert	t_{RESET1} 10/	See figure 6. $V_{DDC} \ge 2.30$ V			4		t_{CLK}
$\overline{\text{RESET}}$ deasserted to outputs valid-active ($\overline{\text{ROMS}}$[0] and $\overline{\text{OE}}$)	t_{RESET2}	See figure 6.				12	t_{CLK}
$\overline{\text{RESET}}$ asserted to control signals valid-inactive ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROMS}}$[1:0], $\overline{\text{RWE}}$[3:0], $\overline{\text{RAMOE}}$[4:0], READ, $\overline{\text{SDWE}}$, $\overline{\text{SDCS}}$[1:0], $\overline{\text{RESET}}$ asserted to outputs high-z (DATA[31:0], CB[7:0], and GPIO[15:0])	t_{RESET3} 11/	See figure 6.				4	t_{CLK}

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-40°C \le T_C \le +105°C$, $+3.0\ V \le V_{DD} \le +3.6\ V$, $+2.3\ V \le V_{DDC} \le +2.7\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional testing							
Funtional tests		V_{DD} = 3.0 V, V_{DDC} = 2.25 V f = 1 MHz to 66 MHz	7, 8	All			
Output Timing Characteristics for Memory Interface, $\overline{\text{ERROR}}$, and $\overline{\text{WDOG}}$							
SDCLK↑ to output valid (ADDR[27:0], $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROMS[1:0]}}$, $\overline{\text{RWE[3:0]}}$, $\overline{\text{RAMOE[4:0]}}$, $\overline{\text{RAMS[4:0]}}$, READ, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{SDCS[1:0]}}$, and SDDQM[3:0])	t_1 12/	See figure 7.	9, 10, 11	All	2	8	ns
SDCLK↑ to output valid (DATA[31:0] and CB[7:0])	t_2 12/				2	8	ns
SDCLK↑ to output high-Z (DATA[31:0] and CB[7:0])	t_3 12/ 13/				2	8	ns
SDCLK↑ to signal low ($\overline{\text{ERROR}}$ and $\overline{\text{WDOG}}$)	t_4 12/				2	9	ns
$\overline{\text{WRITE}}$↑ or $\overline{\text{RWE[3:0]}}$↑ to output high-z (DATA [31:0] and CB[7:0])	t_8 12/ 13/				2.5		ns
Skew from first output signal transition to last memory output signal transition	t_9 12/				2		ns
Input Timing Characteristics for Memory Interface							
Setup time to SDCLK↑ (DATA[31:0], CB[6:0], $\overline{\text{BEXC}}$, and synchronous BRDY) 15/	t_5	See figure 8.	9, 10, 11	All	0		ns
Hold time from SDCLK↑ (DATA[31:0], CB[6:0], $\overline{\text{BEXC}}$, and synchronous BRDY) 15/	t_6				1		ns
Asynchronous $\overline{\text{BRDY}}$ pulse width	t_7 10/				1.5		t_{CLK}
Timing characteristics for General Purpose Input/Output (GPIO)							
SDCLK↑ to GPIO output valid (GPIO[15:0])	t_{10} 12/	See figure 9.	9, 10, 11	All	2	8	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -40°C ≤ T_C ≤ +105°C, +3.0 V ≤ V_{DD} ≤ +3.6 V, +2.3 V ≤ V_{DDC} ≤ +2.7 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing Characteristics for SpaceWire Interface							
SPW_CLK period	t_{11} 15/	See figure 10.	9, 10, 11	All	5		ns
SPW_CLK↑ to data delay (SPW_TXD[3:0])	t_{12} 12/				3	7	ns
SPW_CLK↑ to strobe delay (SPW_TXS[3:0])	t_{13} 12/				3	7	ns
Transmit data and strobe bit width variation (SPW_TXD[3:0] and SPW_TXS[3:0])	t_{14} 16/				UI–600 17/	UI+600 17/	ps
Receive data and strobe bit width (SPW_RXD[3:0] and SPW_RXS[3:0])	t_{15} 16/	See figure 11.			2.5		ns
Receive data and strobe edge separation (SPW_RXD[3:0] and SPW_RXS[3:0])	t_{16}				2.5		ns
Timing Characteristics for PCI Interface							
PCI_CLK↑ to output valid (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, PCI_DEVSEL, PCI_REQ, and PCI_ARB_GNT[7:0])	t_{17} 12/	See figure 12.	9, 10, 11	All	2	13	ns
PCI_CLK↑ to output valid from high-z (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, and PCI_DEVSEL)	t_{18} 12/ 13/				2	13	ns
PCI_CLK↑ to output high-Z (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, and PCI_DEVSEL)	t_{19} 12/ 13/					14	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-40°C \leq T_C \leq +105°C$, $+3.0\ V \leq V_{DD} \leq +3.6\ V$, $+2.3\ V \leq V_{DDC} \leq +2.7\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing Characteristics for PCI Interface - Continued.							
Setup time to PCI_CLK↑ (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, PCI_DEVSEL, PCI_IDSEL, PCI_GNT, and PCI_ARB_REQ[7:0])	t_{20}	See figure 12.	9, 10, 11	All	3		ns
Hold time from PCI_CLK↑ (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, PCI_DEVSEL, and PCI_IDSEL)	t_{21}				1		ns
PCI_CLK to RESET deassertion	t_{22} 10/	See figure 13, 14			10		PCI clocks
PCI_CLK to PCI_RST deassertion	t_{23a} 10/				10		
PCI_RST assertion to PCI_CLK invalid	t_{23b} 10/				10		
PCI_RST assertion to output high-Z, (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, AND PCI_DEVSEL	t_{24} 10/					40	ns
Timing Characteristics for Ethernet Interface							
ETX_CLK↑ to output valid (ETXD[3:0], and ETX_EN)	t_{25} 12/	See figure 15.	9, 10, 11	All	2	8	ns
Setup time to ERX_CLK↑ (ERX_DV, ERX_ER, and ERXD[3:0])	t_{26} 18/	PCI_FRAME, PCI_IRDY, PCI_TDRY			1		ns
Hold time from ERX_CLK↑ (ERX_DV, ERX_ER, and ERXD[3:0])	t_{27} 18/				1		ns
EMDC↑ to output valid (EMDIO)	t_{28} 18/	See figure 16. f_{SYSCLK} = 25 MHz, f_{EMDC} = 123 kHz 19/			2	11	ns
Setup time to EMDC↑ (EMDIO)	t_{29} 10/	See figure 16.			10		ns
Hold time from EMDC↑ (EMDIO)	t_{30} 10/				5		ns

See footnotes on next sheet.

TABLE IA. Electrical performance characteristics - Continued.

1/ RHA devices supplied to this drawing have been characterized through all levels of M, D, P, L, R, and F of irradiation. However, this device is only tested at the ‘F’ level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ During this measurement the processor is executing the Dhrystone benchmark.

3/ This measurement includes the contribution due to I_{DDCS}.

4/ This measurement includes the contribution due to I_{DDS}.

5/ Power-down mode is entered by performing a WRASR instruction wr %g0, %asr19.

6/ Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

7/ Except open-drain output.

8/ Supplied as a design limit. Neither guaranteed nor tested. Not more than one output may be shorted at a time, for a maximum duration of one second.

9/ Tested as shown in figure 16.

10/ Guaranteed by design.

11/ Guaranteed by design for control signals.

12/ All outputs are measured using the load conditions shown in figure 16.

13/ High-Z defined as +/-.300 mV change from steady state.

14/ CB[7] is not used for EDAC and is not tested.

15/ The SPW_CLK frequency must be less than 4x the SYS_CLK frequency. For example, if SPW_CLK is running at 200 MHz, the SYS_CLK frequency must be greater than 50 MHz.

16/ Applies to both high pulse and low pulse.

17/ A unit interval (UI) is defined as the nominal, or ideal, bit width.

18/ ERX_COL and ERX_CRS are asynchronous inputs and are not tested.

19/ $f_{EMDC} = f_{SYSCLK} / 202$.

Table IB. SEP test limits. 1/ 2/

Device type	V_{DD} = 3.0 V V_{DDC} = 2.3 V 3/		Bias for latch-up test V_{DD} = 3.6 V V_{DDC} = 2.7 V no latch-up LET = 4/ [MeV/(mg/cm2)]
	Effective LET no upsets [MeV/(mg/cm^2)]	Maximum bit cross section (cm^2/bit)	
All	≥ 54 5/	5/	≥ 108

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Tested at worst case temperature, T_A = +25°C ±10°C.

4/ Tested at worst case temperature, T_A = +125°C ± 10°C.

5/ Onset LET and maximum bit cross section are for flip-flop memory. Single event upsets for embedded RAM memory are driven by charged particle flux, rather than 'LET', due to the fault tolerant design architecture. Contact manufacturer for details.

Case outline X

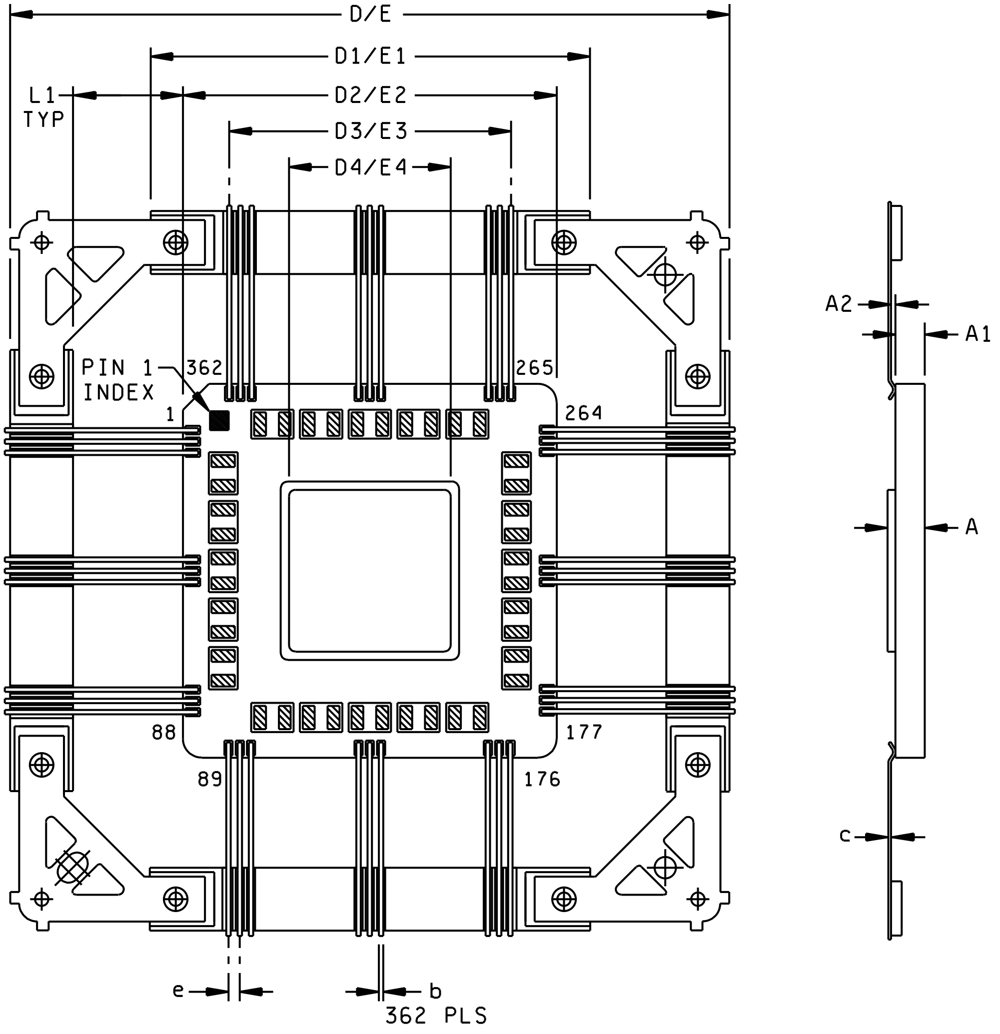


FIGURE 1. Case Outline.

Case outline X

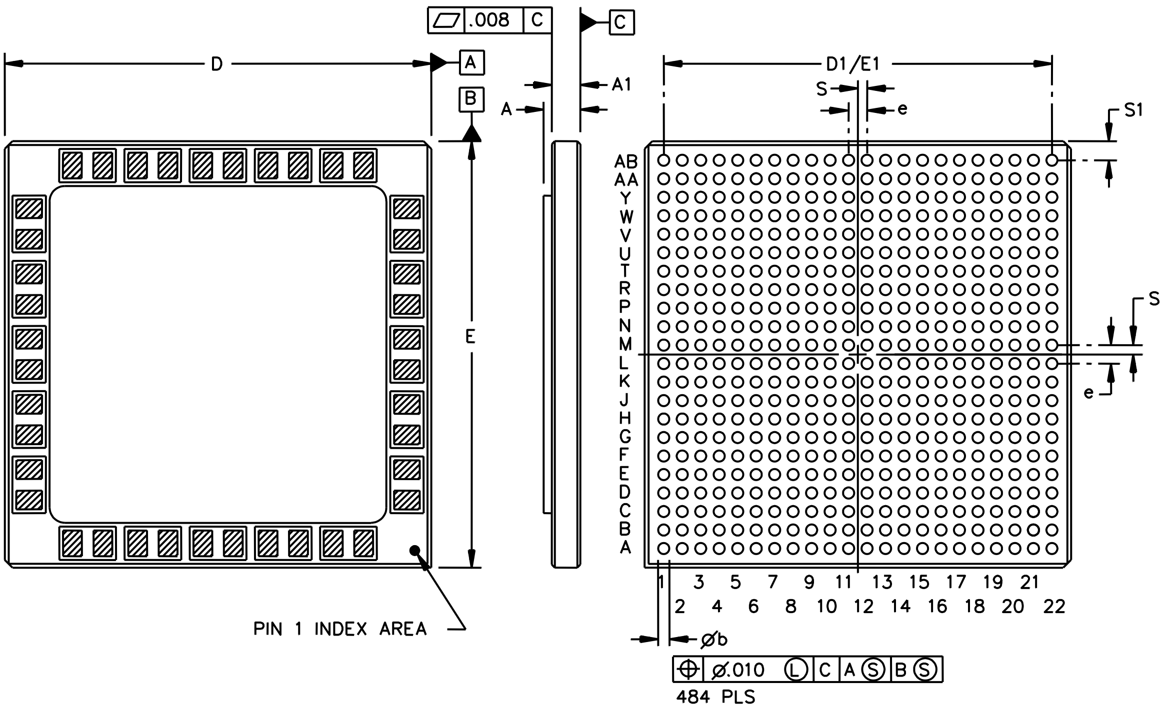
	Inches		Millimeters	
	Min	Max	Min	max
A	---	0.136	---	3.54
A1	---	0.117	---	2.97
A2	0.006	0.012	0.15	0.30
b	0.006	0.010	0.15	0.25
c	0.004	0.008	0.10	0.20
D/E	2.938	2.968	74.63	75.39
D1/E1	2.217 REF		56.31 REF	
D2/E2	1.880	1.900	47.75	48.26
D3/E3	1.7126 BSC		43.50 BSC	
D4/E4	0.870 TYP		22.10 TYP	
e	0.019685 BSC		0.50 BSC	
L1	0.301 TYP		7.65 TYP	

Notes:

1. All exposed metal areas are gold plated over nickelundercoating per MIL-PRF-38535.
2. Lead finishes are in accordance with MIL-PRF-38535.
3. The seal ring is electrically connected to V_{SS}.
4. Application note: Capacitor pads are dimensioned for a MIL-PRF-55681 CDR33BX capacitor or equivalent.
5. Dimensions are shown in inches. Metric equivalents are shown for reference use only.

FIGURE 1. <u>Case Outline</u> - Continued.

Case outline Y



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.126		3.20	e	.050 TYP		1.27 TYP	
A1	.090	.110	2.29	2.79	S	.025 TYP		0.64 TYP	
D/E	1.129	1.151	28.68	29.24	S1	.045 TYP		1.14 TYP	
D1/E1	1.050 TYP		26.67 TYP						

Notes:

1. All exposed metal areas are gold plated over nickel undercoating per MIL-PRF-38535.
2. The seal ring and die attach is electrically connected to V_{SS}.
3. Application note: Capacitor pads are dimensioned for a MIL-PRF-55681 CDR33BX capacitor or equivalent.
4. Dimensions are shown in inches. Metric equivalents are shown for reference use only.

FIGURE 1. Case Outline - Continued.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	ADDR[0]	41	SDCLK	81	DATA[27]
2	ADDR[1]	42	V_{SS}	82	V_{SS}
3	V_{DD}	43	DATA[0]	83	DATA[28]
4	ADDR[2]	44	V_{DD}	84	DATA[29]
5	ADDR[3]	45	DATA[1]	85	DATA[30]
6	ADDR[4]	46	DATA[2]	86	DATA[31]
7	ADDR[5]	47	DATA[3]	87	V_{DD}
8	V_{SS}	48	DATA[4]	88	SYSCLK
9	ADDR[6]	49	V_{SS}	89	CB[0]
10	ADDR[7]	50	DATA[5]	90	CB[1]
11	ADDR[8]	51	DATA[6]	91	CB[2]
12	ADDR[9]	52	DATA[7]	92	CB[3]
13	V_{SSC}	53	DATA[8]	93	CB[4]
14	V_{DDC}	54	V_{DD}	94	CB[5]
15	V_{DD}	55	V_{SSC}	95	V_{DD}
16	ADDR[10]	56	V_{DDC}	96	CB[6]
17	ADDR[11]	57	DATA[9]	97	CB[7]
18	ADDR[12]	58	DATA[10]	98	$\overline{\text{WRITE}}$
19	ADDR[13]	59	DATA[11]	99	$\overline{\text{OE}}$
20	V_{SS}	60	DATA[12]	100	V_{SSC}
21	ADDR[14]	61	V_{SS}	101	V_{DDC}
22	ADDR[15]	62	DATA[13]	102	$\overline{\text{IOS}}$
23	ADDR[16]	63	DATA[14]	103	$\overline{\text{ROMS[0]}}$
24	ADDR[17]	64	DATA[15]	104	$\overline{\text{ROMS[1]}}$
25	V_{DD}	65	V_{DD}	105	$\overline{\text{RWE[0]}}$
26	ADDR[18]	66	DATA[16]	106	V_{DD}
27	ADDR[19]	67	DATA[17]	107	V_{SS}
28	ADDR[20]	68	DATA[18]	108	$\overline{\text{RWE[1]}}$
29	ADDR[21]	69	DATA[19]	109	$\overline{\text{RWE[2]}}$
30	V_{SS}	70	V_{SS}	110	$\overline{\text{RWE[3]}}$
31	ADDR[22]	71	DATA[20]	111	$\overline{\text{RAMOE[0]}}$
32	ADDR[23]	72	DATA[21]	112	$\overline{\text{RAMOE[1]}}$
33	ADDR[24]	73	DATA[22]	113	$\overline{\text{RAMOE[2]}}$
34	ADDR[25]	74	DATA[23]	114	$\overline{\text{RAMOE[3]}}$
35	V_{DD}	75	V_{DD}	115	$\overline{\text{RAMOE[4]}}$
36	V_{SSC}	76	V_{SSC}	116	V_{DD}
37	V_{DDC}	77	V_{DDC}	117	$\overline{\text{RAMS[0]}}$
38	ADDR[26]	78	DATA[24]	118	$\overline{\text{RAMS[1]}}$
39	ADDR[27]	79	DATA[25]	119	$\overline{\text{RAMS[2]}}$
40	V_{DD}	80	DATA[26]	120	$\overline{\text{RAMS[3]}}$

FIGURE 2. Terminal connections.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
121	V_{SSC}	161	TDI	201	V_{DDC}
122	V_{DDC}	162	TDO	202	V_{SSC}
123	$\overline{\text{RAMS[4]}}$	163	EMDC	203	V_{DD}
124	$\overline{\text{SDRAS}}$	164	V_{SSC}	204	V_{SS}
125	$\overline{\text{SDCAS}}$	165	V_{DDC}	205	SPW_RXS[0]
126	$\overline{\text{SDWE}}$	166	ERX_CLK	206	SPW_RXD[0]
127	V_{DD}	167	EMDIO	207	SPW_TXS[0]
128	$\overline{\text{SDCS[0]}}$	168	ERX_COL	208	SPW_TXD[0]
129	$\overline{\text{SDCS[1]}}$	169	ERX_CRS	209	V_{DDC}
130	V_{SS}	170	V_{DD}	210	V_{SSC}
131	SDDQM[0]	171	ERX_DV	211	V_{DD}
132	SDDQM[1]	172	ERX_ER	212	SPW_RXS[1]
133	SDDQM[2]	173	ERXD[0]	213	SPW_RXD[1]
134	SDDQM[3]	174	ERXD[1]	214	SPW_TXS[1]
135	V_{DD}	175	ERXD[2]	215	SPW_TXD[1]
136	$\overline{\text{RESET}}$	176	ERXD[3]	216	V_{SS}
137	V_{DD}	177	ETXD[0]	217	V_{DD}
138	V_{SS}	178	ETXD[1]	218	V_{SSC}
139	READ	179	ETXD[2]	219	V_{SS}
140	$\overline{\text{BEXC}}$	180	ETXD[3]	220	V_{DDC}
141	$\overline{\text{BRDY}}$	181	V_{DD}	221	SPW_CLK
142	$\overline{\text{ERROR}}$ 1/	182	ETX_CLK	222	V_{DD}
143	V_{SSC}	183	V_{SS}	223	RXD
144	V_{DDC}	184	ETX_EN	224	TXD
145	$\overline{\text{WDOG}}$ 1/	185	ETX_ER	225	V_{SS}
146	CAN_RXD[0]	186	V_{DDC}	226	V_{DD}
147	CAN_TXD[0]	187	V_{SS}	227	V_{DDC}
148	CAN_RXD[1]	188	V_{DDC}	228	V_{SSC}
149	V_{DD}	189	V_{SSC}	229	V_{DD}
150	CAN_TXD[1]	190	V_{DD}	230	V_{SS}
151	DSUACT	191	GPIO[0]	231	V_{SSC}
152	DSUBRE	192	GPIO[1]	232	V_{DDC}
153	DSUEN	193	GPIO[2]	233	V_{DD}
154	DSURX	194	GPIO[3]	234	SPW_RXS[2]
155	DSUTX	195	V_{SS}	235	SPW_RXD[2]
156	$\overline{\text{TRST}}$	196	GPIO[4]	236	SPW_TXS[2]
157	$\overline{\text{TMS}}$	197	GPIO[5]	237	SPW_TXD[2]
158	V_{DD}	198	GPIO[6]	238	V_{SS}
159	V_{SS}	199	GPIO[7]	239	V_{DDC}
160	TCK	200	V_{DD}	240	V_{SSC}

FIGURE 2. Terminal connections - Continued.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
241	V_{DD}	279	PCI_AD[8]	317	PCI_AD[24]
242	SPW_RXS[3]	280	PCI_AD[9]	318	PCI_AD[25]
243	SPW_RXD[3]	281	PCI_AD[10]	319	V_{DDC}
244	SPW_TXS[3]	282	V_{SS}	320	V_{SSC}
245	SPW_TXD[3]	283	V_{DD}	321	PCI_AD[26]
246	V_{SS}	284	PCI_AD[11]	322	PCI_AD[27]
247	V_{DD}	285	PCI_AD[12]	323	PCI_AD[28]
248	N/C 2/	286	PCI_AD[13]	324	PCI_AD[29]
249	V_{DDC}	287	PCI_AD[14]	325	V_{DD}
250	V_{SS}	288	PCI_AD[15]	326	PCI_AD[30]
251	V_{DD}	289	PCI_C/$\overline{\text{BE}}$[1]	327	PCI_AD[31]
252	V_{DDC}	290	PCI_PAR	328	$\overline{\text{PCI\_GNT}}$
253	V_{SSC}	291	Unused 4/	329	$\overline{\text{PCI\_REQ}}$
254	GPIO[8]	292	V_{DD}	330	$\overline{\text{PCI\_HOST}}$
255	GPIO[9]	293	PCI_CLK	331	$\overline{\text{PCI\_ARB\_REQ[0]}}$
256	GPIO[10]	294	V_{DD}	332	$\overline{\text{PCI\_ARB\_REQ[1]}}$
257	GPIO[11]	295	$\overline{\text{PCI\_STOP}}$ 3/	333	$\overline{\text{PCI\_ARB\_GNT[0]}}$
258	V_{SS}	296	$\overline{\text{PCI\_DEVSEL}}$ 3/	334	V_{SS}
259	GPIO[12]	297	V_{DDC}	335	V_{DD}
260	GPIO[13]	298	V_{SSC}	336	$\overline{\text{PCI\_ARB\_GNT[1]}}$
261	GPIO[14]	299	$\overline{\text{PCI\_TDRY}}$ 3/	337	$\overline{\text{PCI\_ARB\_REQ[2]}}$
262	GPIO[15]	300	$\overline{\text{PCI\_IRDY}}$ 3/	338	$\overline{\text{PCI\_ARB\_GNT[2]}}$
263	V_{DD}	301	$\overline{\text{PCI\_FRAME}}$ 3/	339	$\overline{\text{PCI\_ARB\_REQ[3]}}$
264	V_{SS}	302	PCI_C/$\overline{\text{BE}}$[2]	340	V_{DDC}
265	$\overline{\text{PCI\_RST}}$	303	V_{SS}	341	V_{SSC}
266	PCI_AD[0]	304	V_{DD}	342	$\overline{\text{PCI\_ARB\_GNT[3]}}$
267	PCI_AD[1]	305	PCI_AD[16]	343	$\overline{\text{PCI\_ARB\_REQ[4]}}$
268	PCI_AD[2]	306	PCI_AD[17]	344	$\overline{\text{PCI\_ARB\_REQ[5]}}$
269	PCI_AD[3]	307	PCI_AD[18]	345	$\overline{\text{PCI\_ARB\_GNT[4]}}$
270	PCI_AD[4]	308	PCI_AD[19]	346	V_{DD}
271	V_{DD}	309	PCI_AD[20]	347	$\overline{\text{PCI\_ARB\_GNT[5]}}$
272	PCI_AD[5]	310	PCI_AD[21]	348	$\overline{\text{PCI\_ARB\_REQ[6]}}$
273	PCI_AD[6]	311	V_{SS}	349	$\overline{\text{PCI\_ARB\_GNT[6]}}$
274	PCI_AD[7]	312	PCI_AD[22]	350	$\overline{\text{PCI\_ARB\_REQ[7]}}$
275	PCI_C/$\overline{\text{BE}}$[0]	313	PCI_AD[23]	351	$\overline{\text{PCI\_ARB\_GNT[7]}}$
276	V_{DDC}	314	V_{DD}	352	V_{SS}
277	V_{SSC}	315	PCI_IDSEL		
278	V_{SS}	316	PCI_C/$\overline{\text{BE}}$[3]		

NOTES:

1/ This pin is actively driven low and must be tied to V_{DD} through a pull-up resistor.
2/ N/C refers to unconnected pin (248). This pin must be left floating.
3/ This pin must be tied to V_{DD} through a pull-up resistor.
4/ This pin must be tied to V_{DD} through a 10 kΩ pull-up resistor.

FIGURE 2. Terminal connections - Continued.

Case outline Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
W5	ADDR[0]	AA11	ADDR[27]	D13	V_{DDC}
Y5	ADDR[1]	E7	V_{DD}	Y17	DATA[24]
B1	V_{DD}	AB12	SDCLK	AA17	DATA[25]
W6	ADDR[2]	B11	V_{SS}	W18	DATA[26]
AA5	ADDR[3]	W12	DATA[0]	AB19	DATA[27]
Y6	ADDR[4]	E9	V_{DD}	D4	V_{SS}
AB5	ADDR[5]	W13	DATA[1]	Y19	DATA[28]
A1	V_{SS}	Y12	DATA[2]	AB20	DATA[29]
W7	ADDR[6]	AA13	DATA[3]	Y18	DATA[30]
AA6	ADDR[7]	AA12	DATA[4]	AA20	DATA[31]
Y7	ADDR[8]	C8	V_{SS}	F10	V_{DD}
AA7	ADDR[9]	AB13	DATA[5]	Y20	SYSCLK
A10	V_{SSC}	W14	DATA[6]	V19	CB[0]
A2	V_{DDC}	AA14	DATA[7]	AA21	CB[1]
B10	V_{DD}	Y13	DATA[8]	Y21	CB[2]
AB6	ADDR[10]	E14	V_{DD}	W19	CB[3]
W8	ADDR[11]	C14	V_{SSC}	Y22	CB[4]
AB7	ADDR[12]	D10	V_{DDC}	W20	CB[5]
Y8	ADDR[13]	W15	DATA[9]	F13	V_{DD}
A12	V_{SS}	AB15	DATA[10]	W22	CB[6]
AA8	ADDR[14]	Y14	DATA[11]	W21	CB[7]
W9	ADDR[15]	AB14	DATA[12]	V21	$\overline{\text{WRITE}}$
AB8	ADDR[16]	C10	V_{SS}	U19	$\overline{\text{OE}}$
Y9	ADDR[17]	W16	DATA[13]	D12	V_{SSC}
B12	V_{DD}	AA18	DATA[14]	E5	V_{DDC}
W10	ADDR[18]	Y15	DATA[15]	T20	$\overline{\text{IOS}}$
AB9	ADDR[19]	E16	V_{DD}	V22	$\overline{\text{ROMS[0]}}$
Y10	ADDR[20]	AB16	DATA[16]	U20	$\overline{\text{ROMS[1]}}$
AA9	ADDR[21]	AA15	DATA[17]	U22	$\overline{\text{RWE[0]}}$
A22	V_{SS}	AB17	DATA[18]	F17	V_{DD}
W11	ADDR[22]	AA16	DATA[19]	D9	V_{SS}
AA10	ADDR[23]	C13	V_{SS}	T19	$\overline{\text{RWE[1]}}$
Y11	ADDR[24]	AA19	DATA[20]	T22	$\overline{\text{RWE[2]}}$
AB10	ADDR[25]	W17	DATA[21]	T21	$\overline{\text{RWE[3]}}$
B22	V_{DD}	AB18	DATA[22]	V20	$\overline{\text{RAMOE[0]}}$
C9	V_{SSC}	Y16	DATA[23]	R21	$\overline{\text{RAMOE[1]}}$
A21	V_{DDC}	F6	V_{DD}	R20	$\overline{\text{RAMOE[2]}}$
AB11	ADDR[26]	D11	V_{SSC}	R22	$\overline{\text{RAMOE[3]}}$

FIGURE 2. Terminal connections - Continued.

Case outline Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
R19	$\overline{\text{RAMOE[4]}}$	G19	DSUEN	B17	GPIO[0]
G5	V_{DD}	G20	DSURX	C17	GPIO[1]
P22	$\overline{\text{RAMS[0]}}$	G21	DSUTX	A17	GPIO[2]
P20	$\overline{\text{RAMS[1]}}$	F20	$\overline{\text{TRST}}$	D17	GPIO[3]
P21	$\overline{\text{RAMS[2]}}$	F21	$\overline{\text{TMS}}$	E10	V_{SS}
P19	$\overline{\text{RAMS[3]}}$	H8	V_{DD}	C16	GPIO[4]
E8	V_{SSC}	D19	V_{SS}	D16	GPIO[5]
E11	V_{DDC}	G22	TCK	C15	GPIO[6]
N19	$\overline{\text{RAMS[4]}}$	F22	TDI	D15	GPIO[7]
N22	$\overline{\text{SDRAS}}$	F19	TDO	J7	V_{DD}
N20	$\overline{\text{SDCAS}}$	E22	EMDC	G7	V_{DDC}
N21	$\overline{\text{SDWE}}$	F5	V_{SSC}	F9	V_{SSC}
		E18	V_{DDC}	J16	V_{DD}
M21	$\overline{\text{SDCS[0]}}$	D22	ERX_CLK	E13	V_{SS}
M22	$\overline{\text{SDCS[1]}}$	D20	EMDIO	A16	SPW_RXS[0]
D14	V_{SS}	E21	ERX_COL	A15	SPW_RXD[0]
L21	SDDQM[0]	E20	ERX_CRS	B16	SPW_TXS[0]
M20	SDDQM[1]	H10	V_{DD}	B15	SPW_TXD[0]
L20	SDDQM[2]	D21	ERX_DV	G10	V_{DDC}
L22	SDDQM[3]	C21	ERX_ER		
G9	V_{DD}	C22	ERXD[0]	J18	V_{DD}
L19	$\overline{\text{RESET}}$	B21	ERXD[1]	A14	SPW_RXS[1]
G14	V_{DD}	C20	ERXD[2]	A13	SPW_RXD[1]
D18	V_{SS}	B20	ERXD[3]	B14	SPW_TXS[1]
K20	READ	C19	ETXD[0]	B13	SPW_TXD[1]
K22	$\overline{\text{BEXC}}$	C18	ETXD[1]	E17	V_{SS}
K21	$\overline{\text{BRDY}}$	B18	ETXD[2]	K5	V_{DD}
K19	$\overline{\text{ERROR}}$ 1/	B19	ETXD[3]	F11	V_{SSC}
E15	V_{SSC}	H13	V_{DD}	E19	V_{SS}
E12	V_{DDC}	A19	ETX_CLK	G13	V_{DDC}
J19	$\overline{\text{WDOG}}$ 1/	E4	V_{SS}	A11	SPW_CLK
J20	CAN_RXD[0]	A18	ETX_EN	K8	V_{DD}
J22	CAN_TXD[0]	A20	ETX_ER	C12	RXD
J21	CAN_RXD[1]	F8	V_{DDC}	C11	TXD
H6	V_{DD}	E6	V_{SS}	F4	V_{SS}
H22	CAN_TXD[1]	F15	V_{DDC}	K15	V_{DD}
H19	DSUACT	F7	V_{SSC}	G16	V_{DDC}
H20	DSUBRE	H15	V_{DD}	F12	V_{SSC}

FIGURE 2. Terminal connections - Continued.

Case outline Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
K17	V_{DD}	AA3	PCI_AD[1]	J1	PCI_AD[16]
G4	V_{SS}	Y1	PCI_AD[2]	K2	PCI_AD[17]
F14	V_{SSC}	Y2	PCI_AD[3]	K1	PCI_AD[18]
G18	V_{DDC}	Y3	PCI_AD[4]	G1	PCI_AD[19]
L6	V_{DD}	N17	V_{DD}	H3	PCI_AD[20]
A9	SPW_RXS[2]	W1	PCI_AD[5]	H2	PCI_AD[21]
A8	SPW_RXD[2]	W2	PCI_AD[6]	H18	V_{SS}
B9	SPW_TXS[2]	W3	PCI_AD[7]	F1	PCI_AD[22]
B8	SPW_TXD[2]	V1	PCI_C/$\overline{\text{BE}}$[0]	F2	PCI_AD[23]
G8	V_{SS}	H12	V_{DDC}	R8	V_{DD}
H5	V_{DDC}	G6	V_{SSC}	G3	PCI_IDSEL
F16	V_{SSC}	H4	V_{SS}	G2	PCI_C/$\overline{\text{BE}}$[3]
M6	V_{DD}	V2	PCI_AD[8]	E1	PCI_AD[24]
A7	SPW_RXS[3]	V3	PCI_AD[9]	E2	PCI_AD[25]
A6	SPW_RXD[3]	U1	PCI_AD[10]	H17	V_{DDC}
B7	SPW_TXS[3]	H7	V_{SS}	J5	V_{SSC}
B6	SPW_TXD[3]	P7	V_{DD}	F3	PCI_AD[26]
G11	V_{SS}	U2	PCI_AD[11]	D1	PCI_AD[27]
N5	V_{DD}	U3	PCI_AD[12]	D2	PCI_AD[28]
D8	N/C 2/	T1	PCI_AD[13]	E3	PCI_AD[29]
H9	V_{DDC}	R2	PCI_AD[14]	R10	V_{DD}
G12	V_{SS}	R1	PCI_AD[15]	D3	PCI_AD[30]
N8	V_{DD}	P2	PCI_C/$\overline{\text{BE}}$[1]	C1	PCI_AD[31]
H11	V_{DDC}	P1	PCI_PAR	B2	$\overline{\text{PCI\_GNT}}$
F18	V_{SSC}	N2	Unused 4/	A4	$\overline{\text{PCI\_REQ}}$
C7	GPIO[8]	P16	V_{DD}	AB3	$\overline{\text{PCI\_HOST}}$
B5	GPIO[9]	C2	PCI_CLK	B4	$\overline{\text{PCI\_ARB\_REQ[0]}}$
D7	GPIO[10]	P18	V_{DD}	AB4	$\overline{\text{PCI\_ARB\_REQ[1]}}$
A5	GPIO[11]	N1	$\overline{\text{PCI\_STOP}}$ 3/	B3	$\overline{\text{PCI\_ARB\_GNT[0]}}$
G15	V_{SS}	M2	$\overline{\text{PCI\_DEVSEL}}$ 3/	J2	V_{SS}
D6	GPIO[12]	H14	V_{DDC}	R13	V_{DD}
C5	GPIO[13]	H21	V_{SSC}	AA4	$\overline{\text{PCI\_ARB\_GNT[1]}}$
C6	GPIO[14]	M1	$\overline{\text{PCI\_TDRY}}$ 3/	Y4	$\overline{\text{PCI\_ARB\_REQ[2]}}$
D5	GPIO[15]	L2	$\overline{\text{PCI\_IRDY}}$ 3/	W4	$\overline{\text{PCI\_ARB\_GNT[2]}}$
N15	V_{DD}	L1	$\overline{\text{PCI\_FRAME}}$ 3/	T3	$\overline{\text{PCI\_ARB\_REQ[3]}}$
G17	V_{SS}	H1	PCI_C/$\overline{\text{BE}}$[2]	J6	V_{DDC}
C3	$\overline{\text{PCI\_RST}}$	H16	V_{SS}	J10	V_{SSC}
AA2	PCI_AD[0]	R6	V_{DD}	R3	$\overline{\text{PCI\_ARB\_GNT[3]}}$

FIGURE 2. Terminal connections - Continued.

Case outline Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P3	$\overline{\text{PCI\_ARB\_REQ[4]}}$	L3	$\overline{\text{PCI\_ARB\_GNT[5]}}$	A3	$\overline{\text{PCI\_ARB\_GNT[7]}}$
M3	$\overline{\text{PCI\_ARB\_REQ[5]}}$	K3	$\overline{\text{PCI\_ARB\_REQ[6]}}$	J4	V_{SS}
N3	$\overline{\text{PCI\_ARB\_GNT[4]}}$	J3	$\overline{\text{PCI\_ARB\_GNT[6]}}$		
R15	V_{DD}	C4	$\overline{\text{PCI\_ARB\_REQ[7]}}$		
Additional Power/Ground Assignments					
T5	V_{DD}	P9	V_{SS}	L18	V_{DDC}
T9	V_{DD}	P14	V_{SS}	M4	V_{DDC}
T14	V_{DD}	R4	V_{SS}	M8	V_{DDC}
U6	V_{DD}	R7	V_{SS}	M15	V_{DDC}
U9	V_{DD}	R16	V_{SS}	M18	V_{DDC}
U11	V_{DD}	R18	V_{SS}	N7	V_{DDC}
U12	V_{DD}	T2	V_{SS}	N16	V_{DDC}
U14	V_{DD}	T4	V_{SS}	P6	V_{DDC}
U17	V_{DD}	T8	V_{SS}	P8	V_{DDC}
V10	V_{DD}	T15	V_{SS}	P15	V_{DDC}
V13	V_{DD}	T17	V_{SS}	R5	V_{DDC}
AA1	V_{DD}	U4	V_{SS}	R9	V_{DDC}
AA22	V_{DD}	U10	V_{SS}	R11	V_{DDC}
J9	V_{SS}	U13	V_{SS}	R12	V_{DDC}
J14	V_{SS}	V4	V_{SS}	R14	V_{DDC}
K4	V_{SS}	V5	V_{SS}	R17	V_{DDC}
K10	V_{SS}	V8	V_{SS}	T7	V_{DDC}
K13	V_{SS}	V11	V_{SS}	T10	V_{DDC}
L7	V_{SS}	V12	V_{SS}	T13	V_{DDC}
L11	V_{SS}	V15	V_{SS}	T16	V_{DDC}
L12	V_{SS}	V18	V_{SS}	T18	V_{DDC}
L17	V_{SS}	AB1	V_{SS}	U8	V_{DDC}
M7	V_{SS}	AB22	V_{SS}	U15	V_{DDC}
M11	V_{SS}	J8	V_{DDC}	V6	V_{DDC}
M12	V_{SS}	J15	V_{DDC}	V17	V_{DDC}
M17	V_{SS}	K7	V_{DDC}	AB2	V_{DDC}
N4	V_{SS}	K16	V_{DDC}	AB21	V_{DDC}
N10	V_{SS}	L4	V_{DDC}	J11	V_{SSC}
N13	V_{SS}	L8	V_{DDC}	J12	V_{SSC}
P4	V_{SS}	L15	V_{DDC}	J13	V_{SSC}

FIGURE 2. Terminal connections - Continued.

Case outline Y

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
J17	V_{SSC}	M10	V_{SSC}	P13	V_{SSC}
K6	V_{SSC}	M13	V_{SSC}	P17	V_{SSC}
K9	V_{SSC}	M14	V_{SSC}	T6	V_{SSC}
K11	V_{SSC}	M16	V_{SSC}	T11	V_{SSC}
K12	V_{SSC}	M19	V_{SSC}	T12	V_{SSC}
K14	V_{SSC}	N6	V_{SSC}	U5	V_{SSC}
K18	V_{SSC}	N9	V_{SSC}	U7	V_{SSC}
L5	V_{SSC}	N11	V_{SSC}	U16	V_{SSC}
L9	V_{SSC}	N12	V_{SSC}	U18	V_{SSC}
L10	V_{SSC}	N14	V_{SSC}	U21	V_{SSC}
L13	V_{SSC}	N18	V_{SSC}	V7	V_{SSC}
L14	V_{SSC}	P5	V_{SSC}	V9	V_{SSC}
L16	V_{SSC}	P10	V_{SSC}	V14	V_{SSC}
M5	V_{SSC}	P11	V_{SSC}	V16	V_{SSC}
M9	V_{SSC}	P12	V_{SSC}		

NOTES:

1/ This pin is actively driven low and must be tied to V_{DD} through a pull-up resistor.
2/ N/C refers to unconnected pin (248). This pin must be left floating.
3/ This pin must be tied to V_{DD} through a pull-up resistor.
4/ This pin must be tied to V_{DD} through a 10 kΩ pull-up resistor.

FIGURE 2. Terminal connections - Continued.

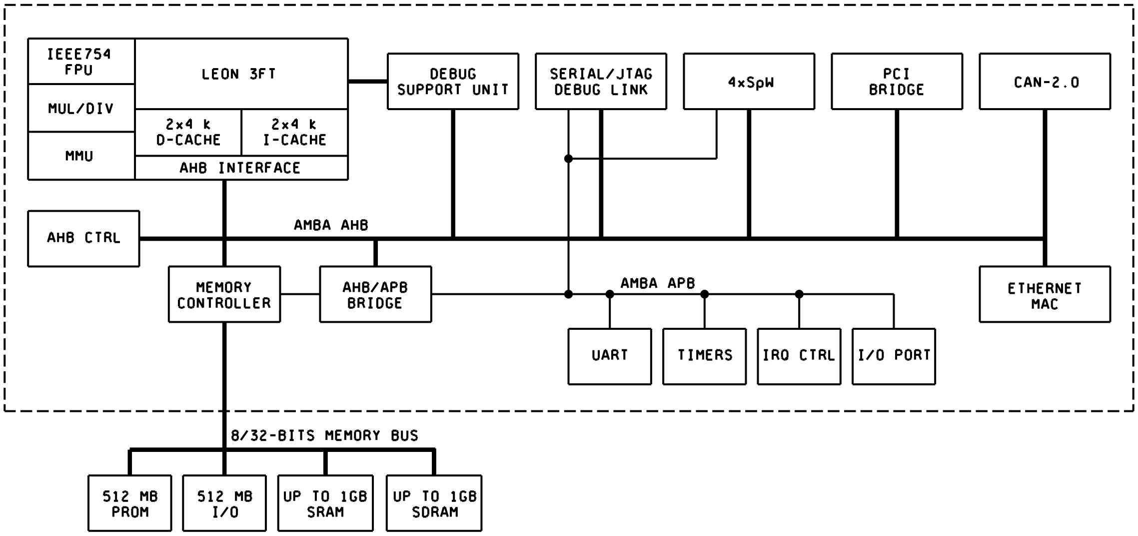
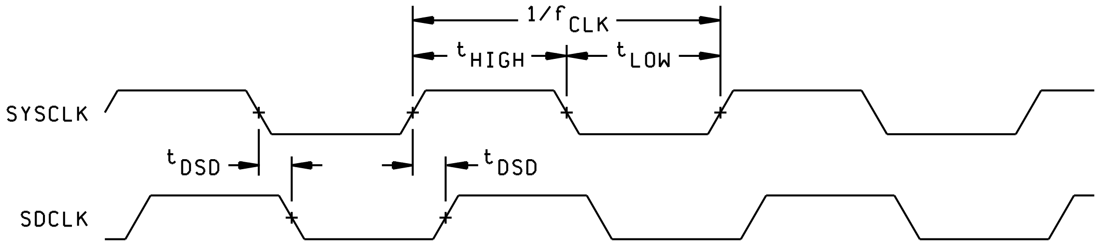
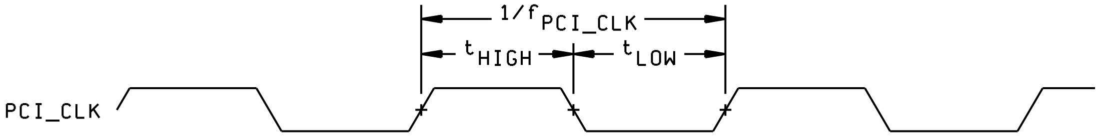


FIGURE 3. Functional block diagram.



SYSTEM CLOCK AND SDCLOCK TIMING DIAGRAM

FIGURE 4. Timing waveforms and test circuits.



PCI CLOCK TIMING DIAGRAM

FIGURE 5. Timing waveforms and test circuits.

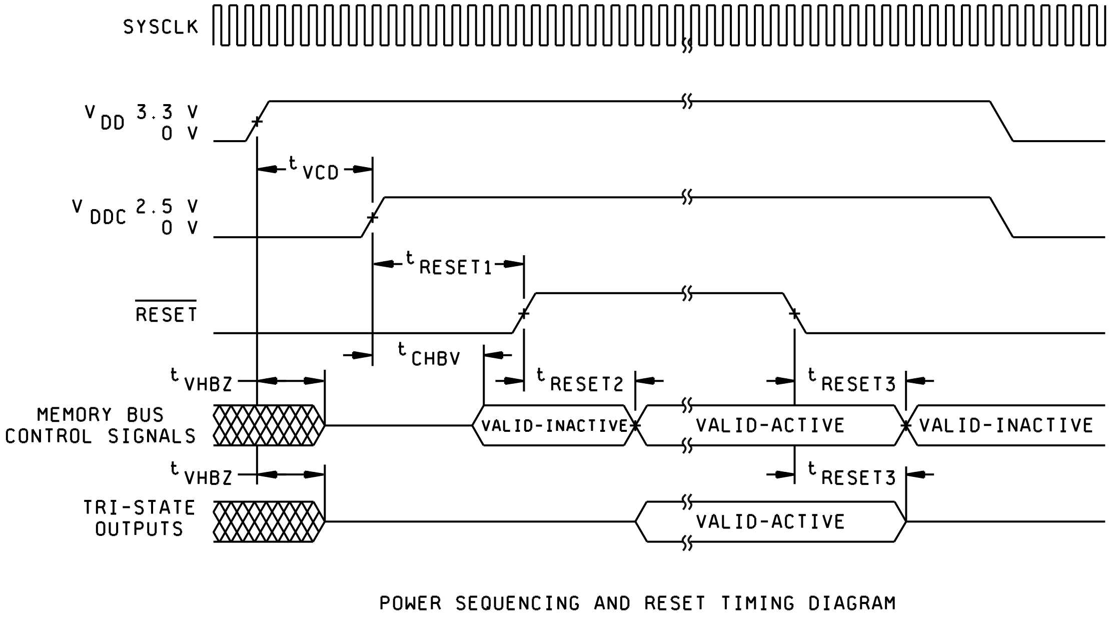


FIGURE 6. Timing waveforms and test circuits.

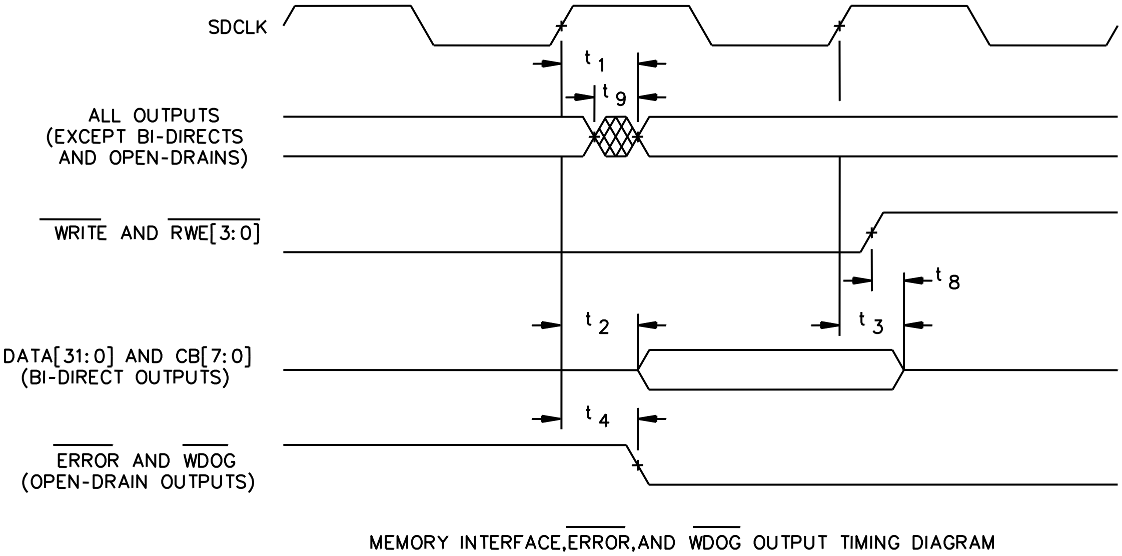


FIGURE 7. Timing waveforms and test circuits.

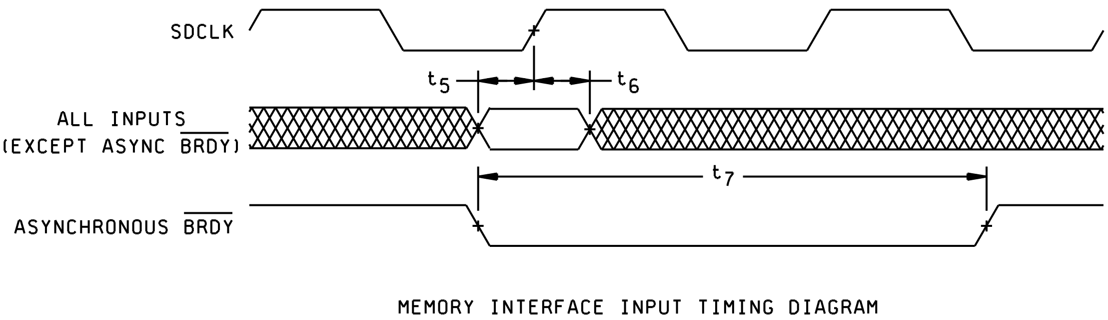


FIGURE 8. Timing waveforms and test circuits.

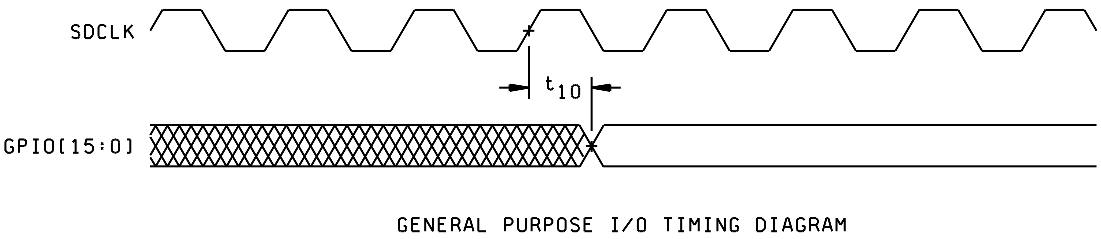


FIGURE 9. Timing waveforms and test circuits.

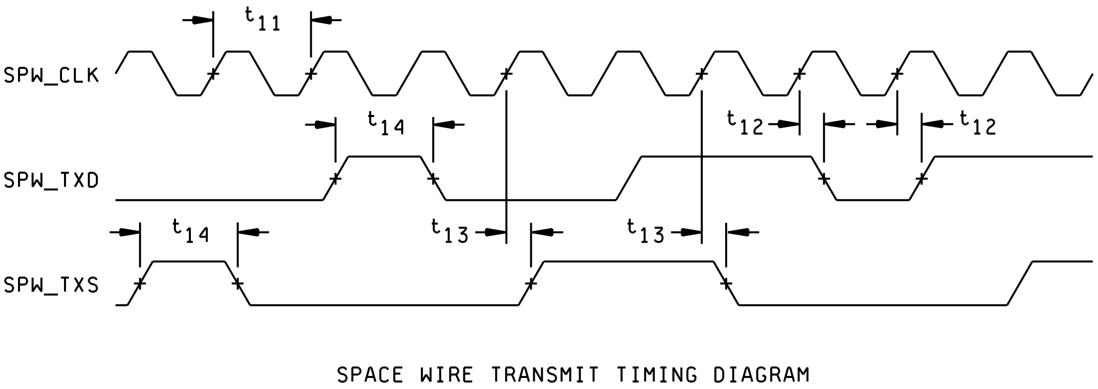


FIGURE 10. Timing waveforms and test circuits.

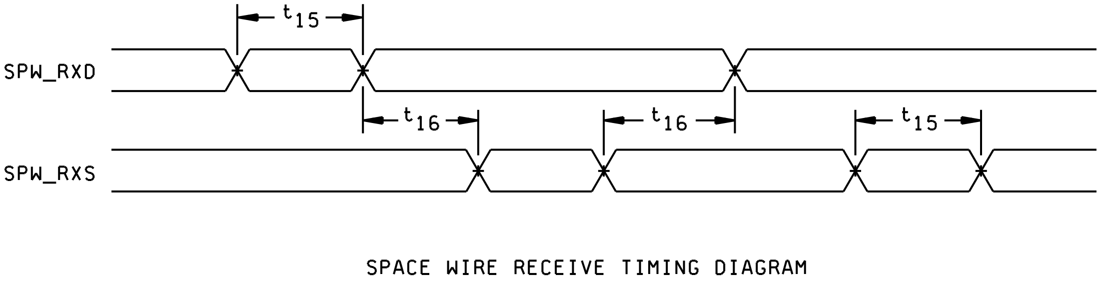


FIGURE 11. Timing waveforms and test circuits.

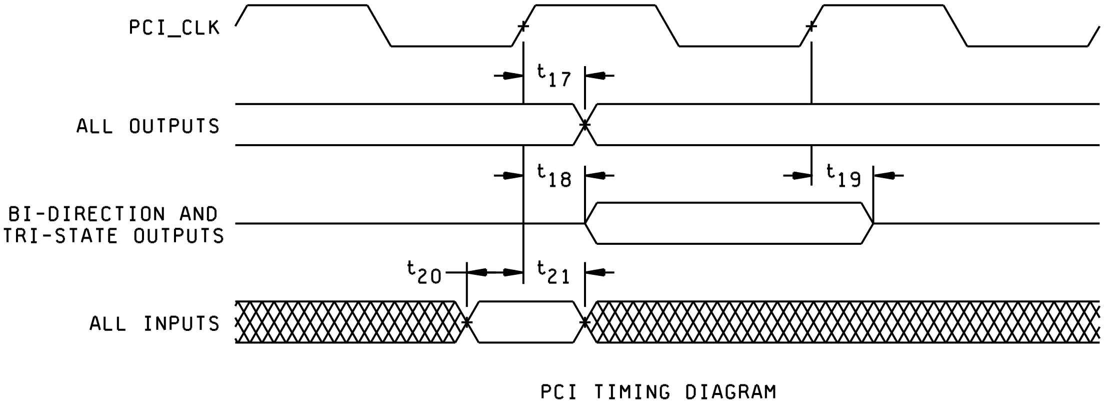
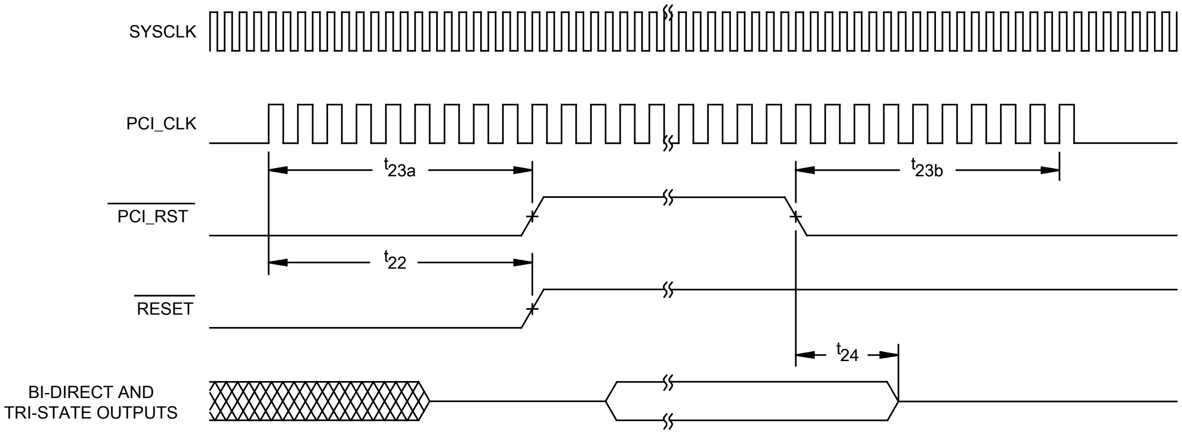
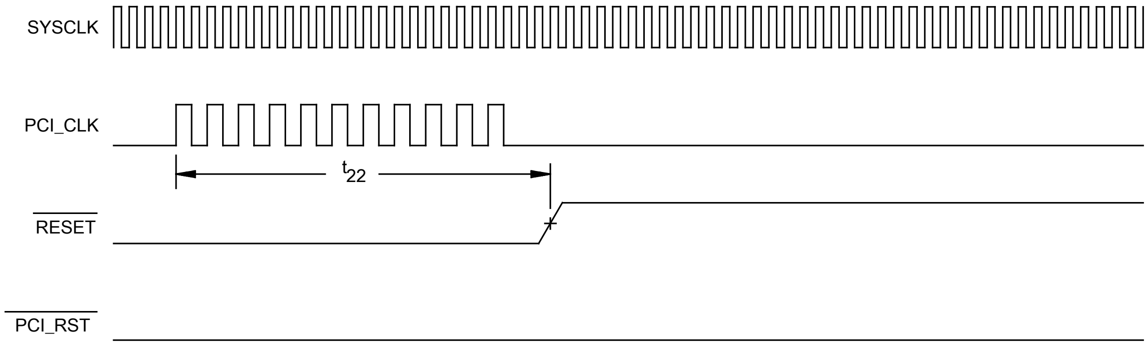


FIGURE 12. Timing waveforms and test circuits.



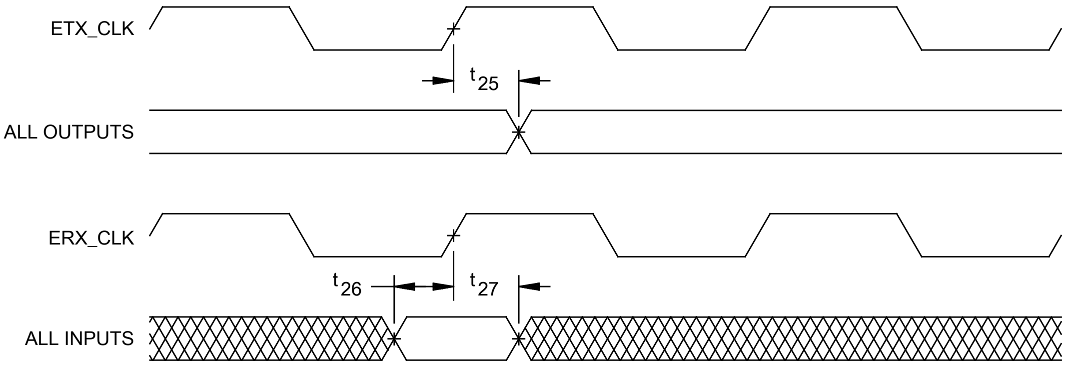
SYSTEM AND PCI RESET TIMING DIAGRAM

FIGURE 13. Timing waveforms and test circuits.



SYSTEM RESET TIMING WHEN PCI IS NOT USED

FIGURE 14. Timing waveforms and test circuits.



ETHERNET TRANSMIT AND RECEIVE TIMING

FIGURE 15. Timing waveforms and test circuits.

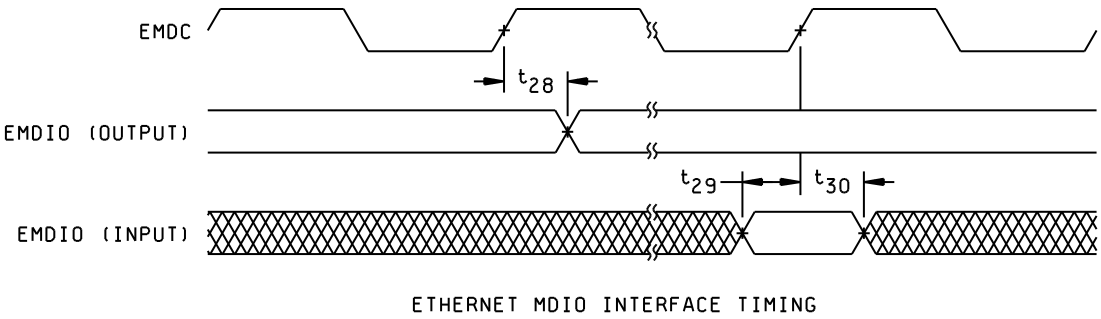


FIGURE 16. Timing waveforms and test circuits.

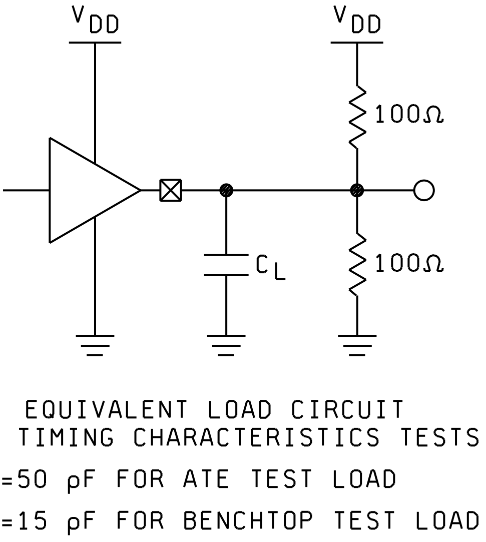


FIGURE 17. Timing waveforms and test circuits.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device type 02.

(1) 100% internal visual, method 2010 condition A of MIL-STD-883.

(2) 100% PIND (Single pass).

(3) Serialization.

(4) 100% X-ray (Top view only).

(5) Group A.

(6) Accelerated dynamic burn-in, deltas, PDA (3%) for Functional Test only, and PDA (5%) for DC and Functional Test combined.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A 8B, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7 and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter 1/	Limit	Unit
I_{DDCS}	± 10% of specified value in table IA	μA
I_{DDS}	± 10% of specified value in table IA	μA

Note: The parameters shall be recorded before and after the required burn-in to determine the delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any process or design changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ±5°C after an exposure of 2×10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° < angle < 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latch-up test temperature shall be maximum rated operating temperature of +125°C.

f. Bias conditions shall be V_{DD} = 3.0 V dc and V_{DDC} = 2.3 V dc for the upset measurements, and V_{DD} = 3.6 V dc and V_{DDC} = 2.7 V dc for the latch-up measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

TABLE III. Pin descriptions.

Pin Function	Description
I	CMOS input
IS	CMOS input Schmitt
O	CMOS output
I/O	CMOS bi-directional
OD	CMOS open drain
PCI-I	PCI input
PCI-O	PCI output
PCI-I/O	PCI bi-directional
PCI-3	PCI three-state

System Signals

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
SYSCLK	I	88	Y20	--	Main system clock.
$\overline{\text{RESET}}$	IS	136	L19	--	System reset.
$\overline{\text{ERROR}}$ 1/	OD	142	K19	--	Processor error mode indicator. This is an active low output.
$\overline{\text{WDOG}}$ 1/	OD	145	J19	--	Watchdog indicator. This is an active low output.

1/ This pin is actively driven low and must be tied to V_{DD} through a pull-up resistor.

TABLE III. Pin descriptions - Continued.

Address Bus

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
ADDR[0]	O	1	W5	Low	Bit 0 of the address bus.
ADDR[1]	O	2	Y5	Low	Bit 1 of the address bus.
ADDR[2]	O	4	W6	Low	Bit 2 of the address bus.
ADDR[3]	O	5	AA5	Low	Bit 3 of the address bus.
ADDR[4]	O	6	Y6	Low	Bit 4 of the address bus.
ADDR[5]	O	7	AB5	Low	Bit 5 of the address bus.
ADDR[6]	O	9	W7	Low	Bit 6 of the address bus.
ADDR[7]	O	10	AA6	Low	Bit 7 of the address bus.
ADDR[8]	O	11	Y7	Low	Bit 8 of the address bus.
ADDR[9]	O	12	AA7	Low	Bit 9 of the address bus.
ADDR[10]	O	16	AB6	Low	Bit 10 of the address bus.
ADDR[11]	O	17	W8	Low	Bit 11 of the address bus.
ADDR[12]	O	18	AB7	Low	Bit 12 of the address bus.
ADDR[13]	O	19	Y8	Low	Bit 13 of the address bus.
ADDR[14]	O	21	AA8	Low	Bit 14 of the address bus.
ADDR[15]	O	22	W9	Low	Bit 15 of the address bus.
ADDR[16]	O	23	AB8	Low	Bit 16 of the address bus.
ADDR[17]	O	24	Y9	Low	Bit 17 of the address bus.
ADDR[18]	O	26	W10	Low	Bit 18 of the address bus.
ADDR[19]	O	27	AB9	Low	Bit 19 of the address bus.
ADDR[20]	O	28	Y10	Low	Bit 20 of the address bus.
ADDR[21]	O	29	AA9	Low	Bit 21 of the address bus.
ADDR[22]	O	31	W11	Low	Bit 22 of the address bus.
ADDR[23]	O	32	AA10	Low	Bit 23 of the address bus.
ADDR[24]	O	33	Y11	Low	Bit 24 of the address bus.
ADDR[25]	O	34	AB10	Low	Bit 25 of the address bus.
ADDR[26]	O	38	AB11	Low	Bit 26 of the address bus.
ADDR[27]	O	39	AA11	Low	Bit 27 of the address bus.

TABLE III. Pin descriptions - Continued.

Data Bus

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
DATA[0]	I/O	43	W12	High-Z	Bit 0 of the data bus.
DATA[1]	I/O	45	W13	High-Z	Bit 1 of the data bus.
DATA[2]	I/O	46	Y12	High-Z	Bit 2 of the data bus.
DATA[3]	I/O	47	AA13	High-Z	Bit 3 of the data bus.
DATA[4]	I/O	48	AA12	High-Z	Bit 4 of the data bus.
DATA[5]	I/O	50	AB13	High-Z	Bit 5 of the data bus.
DATA[6]	I/O	51	W14	High-Z	Bit 6 of the data bus.
DATA[7]	I/O	52	AA14	High-Z	Bit 7 of the data bus.
DATA[8]	I/O	53	Y13	High-Z	Bit 8 of the data bus.
DATA[9]	I/O	57	W15	High-Z	Bit 9 of the data bus.
DATA[10]	I/O	58	AB15	High-Z	Bit 10 of the data bus.
DATA[11]	I/O	59	Y14	High-Z	Bit 11 of the data bus.
DATA[12]	I/O	60	AB14	High-Z	Bit 12 of the data bus.
DATA[13]	I/O	62	W16	High-Z	Bit 13 of the data bus.
DATA[14]	I/O	63	AA18	High-Z	Bit 14 of the data bus.
DATA[15]	I/O	64	Y15	High-Z	Bit 15 of the data bus.
DATA[16]	I/O	66	AB16	High-Z	Bit 16 of the data bus.
DATA[17]	I/O	67	AA15	High-Z	Bit 17 of the data bus.
DATA[18]	I/O	68	AB17	High-Z	Bit 18 of the data bus.
DATA[19]	I/O	69	AA16	High-Z	Bit 19 of the data bus.
DATA[20]	I/O	71	AA19	High-Z	Bit 20 of the data bus.
DATA[21]	I/O	72	W17	High-Z	Bit 21 of the data bus.
DATA[22]	I/O	73	AB18	High-Z	Bit 22 of the data bus.
DATA[23]	I/O	74	Y16	High-Z	Bit 23 of the data bus.
DATA[24]	I/O	78	Y17	High-Z	Bit 24 of the data bus.
DATA[25]	I/O	79	AA17	High-Z	Bit 25 of the data bus.
DATA[26]	I/O	80	W18	High-Z	Bit 26 of the data bus.
DATA[27]	I/O	81	AB19	High-Z	Bit 27 of the data bus.
DATA[28]	I/O	83	Y19	High-Z	Bit 28 of the data bus.
DATA[29]	I/O	84	AB20	High-Z	Bit 29 of the data bus.
DATA[30]	I/O	85	Y18	High-Z	Bit 30 of the data bus.
DATA[31]	I/O	86	AA20	High-Z	Bit 31 of the data bus.

TABLE III. Pin descriptions - Continued.

Check Bits

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
CB[0]	I/O	89	V19	High-Z	Bit 0 of EDAC checkbits.
CB[1]	I/O	90	AA21	High-Z	Bit 1 of EDAC checkbits.
CB[2]	I/O	91	Y21	High-Z	Bit 2 of EDAC checkbits.
CB[3]	I/O	92	W19	High-Z	Bit 3 of EDAC checkbits.
CB[4]	I/O	93	Y22	High-Z	Bit 4 of EDAC checkbits.
CB[5]	I/O	94	W20	High-Z	Bit 5 of EDAC checkbits.
CB[6]	I/O	96	W22	High-Z	Bit 6 of EDAC checkbits.
CB[7]	I/O	97	W21	High-Z	Bit 7 of EDAC checkbits.

Memory Control Signals

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
$\overline{\text{WRITE}}$	O	98	V21	High	PROM and I/O write enable strobe.
$\overline{\text{OE}}$	O	99	U19	High	PROM and I/O output enable.
$\overline{\text{IOS}}$	O	102	T20	High	I/O area chip select.
$\overline{\text{ROMS[0]}}$	O	103	V22	High	PROM chip select.
$\overline{\text{ROMS[1]}}$	O	104	U20	High	PROM chip select.
$\overline{\text{RWE[0]}}$	O	105	U22	High	SRAM write enable strobe.
$\overline{\text{RWE[1]}}$	O	108	T19	High	SRAM write enable strobe.
$\overline{\text{RWE[2]}}$	O	109	T22	High	SRAM write enable strobe.
$\overline{\text{RWE[3]}}$	O	110	T21	High	SRAM write enable strobe.
$\overline{\text{RAMOE[0]}}$	O	111	V20	High	SRAM output enable.
$\overline{\text{RAMOE[1]}}$	O	112	R21	High	SRAM output enable.
$\overline{\text{RAMOE[2]}}$	O	113	R20	High	SRAM output enable.
$\overline{\text{RAMOE[3]}}$	O	114	R22	High	SRAM output enable.
$\overline{\text{RAMOE[4]}}$	O	115	R19	High	SRAM output enable.
$\overline{\text{RAMS[0]}}$	O	117	P22	High	SRAM chip select.
$\overline{\text{RAMS[1]}}$	O	118	P20	High	SRAM chip select.
$\overline{\text{RAMS[2]}}$	O	119	P21	High	SRAM chip select.
$\overline{\text{RAMS[3]}}$	O	120	P19	High	SRAM chip select.
$\overline{\text{RAMS[4]}}$	O	123	N19	High	SRAM chip select.
READ	O	139	K20	High	SRAM, PROM, and I/O read indicator.
$\overline{\text{BEXC}}$	I	140	K22	--	Bus exception.
$\overline{\text{BRDY}}$	I	141	K21	--	Bus ready.

TABLE III. Pin descriptions - Continued.

SDRAM

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
SDCLK	O	41	AB12	High	SDRAM clock.
$\overline{\text{SDRAS}}$	O	124	N22	High	SDRAM row address strobe.
$\overline{\text{SDCAS}}$	O	125	N20	High	SDRAM column address strobe.
$\overline{\text{SDWEN}}$	O	126	N21	High	SDRAM write enable.
$\overline{\text{SDCS[0]}}$	O	128	M21	High	SDRAM chip select.
$\overline{\text{SDCS[1]}}$	O	129	M22	High	SDRAM chip select.
SDDQM[0]	O	131	L21	High	SDRAM data mask.
SDDQM[1]	O	132	M20	High	SDRAM data mask.
SDDQM[2]	O	133	L20	High	SDRAM data mask.
SDDQM[3]	O	134	L22	High	SDRAM data mask.

CAN 2.0 Interface

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
CAN_RXD[0]	I	146	J20	--	CAN receive data.
CAN_TXD[0]	O	147	J22	High	CAN transmit data.
CAN_RXD[1]	I	148	J21	--	CAN receive data.
CAN_TXD[1]	O	150	H22	High	CAN transmit data.

Debug Support Unit (DSU)

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
DSUACT	O	151	H19	Low	DSU mode indicator.
DSUBRE	I	152	H20	--	DSU break.
DSUEN	I	153	G19	--	DSU enable.
DSURX	I	154	G20	--	DSU UART receive data.
DSUTX	O	155	G21	High	DSU UART transmit data.

TABLE III. Pin descriptions - Continued.

JTAG Interface

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
$\overline{\text{TRST}}$	I	156	F20	--	JTAG reset.
$\overline{\text{TMS}}$	I	157	F21	--	JTAG test mode select.
TCK	I	160	G22	--	JTAG clock.
TDI	I	161	F22	--	JTAG test data input.
TDO	O	162	F19	Undefined	JTAG test data output.

Ethernet Interface

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
EMDC	O	163	E22	Low	Ethernet media interface clock.
ERX_CLK	I	166	D22	--	Ethernet RX clock.
EMDIO	I/O	167	D20	High-Z	Ethernet media interface data.
ERX_COL	I	168	E21	--	Ethernet collision error.
ERX_CRS	I	169	E20	--	Ethernet carrier sense detect.
ERX_DV	I	171	D21	--	Ethernet receiver data valid.
ERX_ER	I	172	C21	--	Ethernet reception error.
ERXD[0]	I	173	C22	--	Ethernet receive data.
ERXD[1]	I	174	B21	--	Ethernet receive data.
ERXD[2]	I	175	C20	--	Ethernet receive data.
ERXD[3]	I	176	B20	--	Ethernet receive data.
ETXD[0]	O	177	C19	Low	Ethernet transmit data.
ETXD[1]	O	178	C18	High	Ethernet transmit data.
ETXD[2]	O	179	B18	Low	Ethernet transmit data.
ETXD[3]	O	180	B19	High	Ethernet transmit data.
ETX_CLK	I	182	A19	--	Ethernet TX clock.
ETX_EN	O	184	A18	Low	Ethernet transmit enable.
ETX_ER	O	185	A20	Low	Ethernet transmit error.

TABLE III. Pin descriptions - Continued.

General Purpose I/O

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
GPIO[0]	I/O	191	B17	High-Z	Bit 0 of general purpose I/O.
GPIO[1]	I/O	192	C17	High-Z	Bit 1 of general purpose I/O.
GPIO[2]	I/O	193	A17	High-Z	Bit 2 of general purpose I/O.
GPIO[3]	I/O	194	D17	High-Z	Bit 3 of general purpose I/O.
GPIO[4]	I/O	196	C16	High-Z	Bit 4 of general purpose I/O.
GPIO[5]	I/O	197	D16	High-Z	Bit 5 of general purpose I/O.
GPIO[6]	I/O	198	C15	High-Z	Bit 6 of general purpose I/O.
GPIO[7]	I/O	199	D15	High-Z	Bit 7 of general purpose I/O.
GPIO[8]	I/O	254	C7	High-Z	Bit 8 of general purpose I/O.
GPIO[9]	I/O	255	B5	High-Z	Bit 9 of general purpose I/O.
GPIO[10]	I/O	256	D7	High-Z	Bit 10 of general purpose I/O.
GPIO[11]	I/O	257	A5	High-Z	Bit 11 of general purpose I/O.
GPIO[12]	I/O	259	D6	High-Z	Bit 12 of general purpose I/O.
GPIO[13]	I/O	260	C5	High-Z	Bit 13 of general purpose I/O.
GPIO[14]	I/O	261	C6	High-Z	Bit 14 of general purpose I/O.
GPIO[15]	I/O	262	D5	High-Z	Bit 15 of general purpose I/O.

Space Wire Interface

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
SPW_CLK	I	221	A11	--	Space Wire clock.
SPW_RXS[0]	I	205	A16	--	Space Wire receive strobe.
SPW_RXD[0]	I	206	A15	--	Space Wire receive data.
SPW_TXS[0]	O	207	B16	Low	Space Wire transmit strobe.
SPW_TXD[0]	O	208	B15	Low	Space Wire transmit data.
SPW_RXS[1]	I	212	A14	--	Space Wire receive strobe.
SPW_RXD[1]	I	213	A13	--	Space Wire receive data.
SPW_TXS[1]	O	214	B14	Low	Space Wire transmit strobe.
SPW_TXD[1]	O	215	B13	Low	Space Wire transmit data.
SPW_RXS[2]	I	234	A9	--	Space Wire receive strobe.
SPW_RXD[2]	I	235	A8	--	Space Wire receive data.
SPW_TXS[2]	O	236	B9	Low	Space Wire transmit strobe.
SPW_TXD[2]	O	237	B8	Low	Space Wire transmit data.
SPW_RXS[3]	I	242	A7	--	Space Wire receive strobe.
SPW_RXD[3]	I	243	A6	--	Space Wire receive data.
SPW_TXS[3]	O	244	B7	Low	Space Wire transmit strobe.
SPW_TXD[3]	O	245	B6	Low	Space Wire transmit data.

TABLE III. Pin descriptions - Continued.

UART Interface

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
RXD	I	223	C12	--	UART receive data.
TXD	O	224	C11	High	UART transmit data.

PCI Address and Data Bus

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
PCI_AD[0]	PCI-I/O	266	AA2	High-Z	Bit 0 of PCI address and data bus.
PCI_AD[1]	PCI-I/O	267	AA3	High-Z	Bit 1 of PCI address and data bus.
PCI_AD[2]	PCI-I/O	268	Y1	High-Z	Bit 2 of PCI address and data bus.
PCI_AD[3]	PCI-I/O	269	Y2	High-Z	Bit 3 of PCI address and data bus.
PCI_AD[4]	PCI-I/O	270	Y3	High-Z	Bit 4 of PCI address and data bus.
PCI_AD[5]	PCI-I/O	272	W1	High-Z	Bit 5 of PCI address and data bus.
PCI_AD[6]	PCI-I/O	273	W2	High-Z	Bit 6 of PCI address and data bus.
PCI_AD[7]	PCI-I/O	274	W3	High-Z	Bit 7 of PCI address and data bus.
PCI_AD[8]	PCI-I/O	279	V2	High-Z	Bit 8 of PCI address and data bus.
PCI_AD[9]	PCI-I/O	280	V3	High-Z	Bit 9 of PCI address and data bus.
PCI_AD[10]	PCI-I/O	281	U1	High-Z	Bit 10 of PCI address and data bus.
PCI_AD[11]	PCI-I/O	284	U2	High-Z	Bit 11 of PCI address and data bus.
PCI_AD[12]	PCI-I/O	285	U3	High-Z	Bit 12 of PCI address and data bus.
PCI_AD[13]	PCI-I/O	286	T1	High-Z	Bit 13 of PCI address and data bus.
PCI_AD[14]	PCI-I/O	287	R2	High-Z	Bit 14 of PCI address and data bus.
PCI_AD[15]	PCI-I/O	288	R1	High-Z	Bit 15 of PCI address and data bus.
PCI_AD[16]	PCI-I/O	305	J1	High-Z	Bit 16 of PCI address and data bus.
PCI_AD[17]	PCI-I/O	306	K2	High-Z	Bit 17 of PCI address and data bus.
PCI_AD[18]	PCI-I/O	307	K1	High-Z	Bit 18 of PCI address and data bus.
PCI_AD[19]	PCI-I/O	308	G1	High-Z	Bit 19 of PCI address and data bus.
PCI_AD[20]	PCI-I/O	309	H3	High-Z	Bit 20 of PCI address and data bus.
PCI_AD[21]	PCI-I/O	310	H2	High-Z	Bit 21 of PCI address and data bus.
PCI_AD[22]	PCI-I/O	312	F1	High-Z	Bit 22 of PCI address and data bus.
PCI_AD[23]	PCI-I/O	313	F2	High-Z	Bit 23 of PCI address and data bus.
PCI_AD[24]	PCI-I/O	317	E1	High-Z	Bit 24 of PCI address and data bus.
PCI_AD[25]	PCI-I/O	318	E2	High-Z	Bit 25 of PCI address and data bus.
PCI_AD[26]	PCI-I/O	321	F3	High-Z	Bit 26 of PCI address and data bus.
PCI_AD[27]	PCI-I/O	322	D1	High-Z	Bit 27 of PCI address and data bus.
PCI_AD[28]	PCI-I/O	323	D2	High-Z	Bit 28 of PCI address and data bus.
PCI_AD[29]	PCI-I/O	324	E3	High-Z	Bit 29 of PCI address and data bus.
PCI_AD[30]	PCI-I/O	326	D3	High-Z	Bit 30 of PCI address and data bus.
PCI_AD[31]	PCI-I/O	327	C1	High-Z	Bit 31 of PCI address and data bus.

TABLE III. Pin descriptions - Continued.

PCI Control Signals

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
$\overline{\text{PCI\_RST}}$	PCI-I	265	C3	High-Z	PCI reset input
PCI_CLK	PCI-I	293	C2	High-Z	PCI clock input
PCI_C/$\overline{\text{BE}}$[0]	PCI-I/O	275	V1	High-Z	PCI bus command and byte enable.
PCI_C/$\overline{\text{BE}}$[1]	PCI-I/O	289	P2	High-Z	PCI bus command and byte enable.
PCI_C/$\overline{\text{BE}}$[2]	PCI-I/O	302	H1	High-Z	PCI bus command and byte enable.
PCI_C/$\overline{\text{BE}}$[3]	PCI-I/O	316	G2	High-Z	PCI bus command and byte enable.
PCI_PAR	PCI-I/O	290	P1	High-Z	PCI parity checkbit.
$\overline{\text{PCI\_FRAME}}$ 1/	PCI-3	301	L1	High-Z	PCI cycle frame indicator.
$\overline{\text{PCI\_IRDY}}$ 1/	PCI-3	300	L2	High-Z	PCI initiator ready indicator.
$\overline{\text{PCI\_TDRY}}$ 1/	PCI-3	299	M1	High-Z	PCI target ready indicator.
$\overline{\text{PCI\_STOP}}$ 1/	PCI-3	295	N1	High-Z	PCI target stop indicator.
$\overline{\text{PCI\_DEVSEL}}$ 1/	PCI-3	296	M2	High-Z	PCI device select.
PCI_IDSEL	PCI-I	315	G3	--	PCI initializion device select.
$\overline{\text{PCI\_REQ}}$	PCI-O	329	A4	High-Z	PCI request to arbiter in point to point configuration.
$\overline{\text{PCI\_GNT}}$	PCI-I	328	B2	--	PCI bus access indicator in point to point configuration.
$\overline{\text{PCI\_HOST}}$	PCI-I	330	AB3	--	PCI host enable input (Connect to SYSEN# in PCI bus.).

1/ This pin must be tied to V_{DD} through a pull-up resistor.

TABLE III. Pin descriptions - Continued.

PCI Arbiter

Pin Name	Function	Pin Number		Reset Value	Description
		Case outline X	Case outline Y		
$\overline{\text{PCI\_ARB\_REQ[0]}}$	PCI-I	331	B4	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[1]}}$	PCI-I	332	AB4	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[2]}}$	PCI-I	337	Y4	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[3]}}$	PCI-I	339	T3	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[4]}}$	PCI-I	343	P3	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[5]}}$	PCI-I	344	M3	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[6]}}$	PCI-I	348	K3	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_REQ[7]}}$	PCI-I	350	C4	--	PCI arbiter bus request.
$\overline{\text{PCI\_ARB\_GNT[0]}}$	PCI-O	333	B3	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[1]}}$	PCI-O	336	AA4	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[2]}}$	PCI-O	338	W4	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[3]}}$	PCI-O	342	R3	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[4]}}$	PCI-O	345	N3	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[5]}}$	PCI-O	347	L3	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[6]}}$	PCI-O	349	J3	High-Z	PCI arbiter bus grant.
$\overline{\text{PCI\_ARB\_GNT[7]}}$	PCI-O	351	A3	High-Z	PCI arbiter bus grant.

Power and Ground Pins, Case outline X

Pin Name	Pin Number	Description
V_{DD}	3, 15, 25, 35, 40, 44, 54, 65, 75, 87, 95, 106, 116, 127, 135, 137, 149, 158, 170, 181, 190, 200, 203, 211, 217, 222, 226, 229, 233, 241, 247, 251, 263, 271, 283, 292, 294, 304, 314, 325, 335, 346	I/O supply voltage.
V_{SS}	8, 20, 30, 42, 49, 61, 70, 82, 107, 130, 138, 159, 183, 187, 195, 204, 216, 219, 225, 230, 238, 246, 250, 258, 264, 278, 282, 303, 311, 334, 352	I/O supply ground (pins 187 and 264 must be tied to V_{SS}).
V_{DDC}	14, 37, 56, 77, 101, 122, 144, 165, 186, 188, 201, 209, 220, 227, 232, 239, 249, 252, 276, 297, 319, 340	Core supply voltage.
V_{SSC}	13, 36, 55, 76, 100, 121, 143, 164, 189, 202, 210, 218, 228, 231, 240, 253, 277, 298, 320, 341	Core supply ground.
N/C	248	This pin must be left floating.
Unused	291	This pin must be tied to V_{DD} through a 10 kΩ resistor.

TABLE III. Pin descriptions - Continued.

Power and Ground Pins, Package Outline Y

Pin Name	Pin Number	Description
V_{DD}	B1,B10,B12,B22,E7,E9,E14,E16,F6,F10,F13,F17, G5,G9,G14,H6,H8,H10,H13,H15,J7,J16,J18,K5, K8,K15,K17,L6,M6,N5,N8,N15,N17,P7,P16,P18, R6,R8,R10,R13,R15,T5,T9,T14,U6,U9,U11,U12,U14 U17,V10,V13,AA1,AA22	I/O supply voltage.
V_{SS}	A1,A12,A22,B11,C8,C10,C13,D4,D9,D14,D18, D19,E4,E6,E10,E13,E17,E19,F4,G4,G8,G11, G12,G15,G17,H4,H7,H16,H18,J2,J4,J9,J14,K4, K10,K13,L7,L11,L12,L17,M7,M11,M12,M17,N4, N10,N13,P4,P9,P14,R4,R7,R16,R18,T2,T4,T8, T15,T17,U4,U10,U13,V4,V5,V8,V11,V12,V15, V18,AB1,AB22	I/O supply ground (pins 187 and 264 must be tied to V_{SS}).
V_{DDC}	A2,A21,D10,D13,E5,E11,E12,E18,F8,F15,G7, G10,G13,G16,G18,H5,H9,H11,H12,H14,H17, J6,J8,J15,K7,K16,L4,L8,L15,L18,M4,M8,M15, M18,N7,N16,P6,P8,P15,R5,R9,R11,R12,R14, R17,T7,T10,T13,T16,T18,U8,U15,V6,V17,AB2, AB21	Core supply voltage.
V_{SSC}	A10,C9,C14,D11,D12,E8,E15,F5,F7,F9,F11, F12,F14,F16,F18,G6,H21,J5,J10,J11,J12,J13, J17,K6,K9,K11,K12,K14,K18,L5,L9,L10,L13, L14,L16,M5,M9,M10,M13,M14,M16,M19,N6,N9, N11,N12,N14,N18,P5,P10,P11,P12,P13,P17,T6, T11,T12,U5,U7,U16,U18,U21,V7,V9,V14,V17	Core supply ground.
N/C	D8	This pin must be left floating.
Unused	N2	This pin must be tied to V_{DD} through a 10 kΩ resistor.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-02-19

Approved sources of supply for SMD 5962-08228 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F0822801QXC	65342	UT699-XQC
5962R0822801QXC	65342	UT699-XQC
5962F0822802QXC	65342	UT699-XQC
5962R0822802QXC	65342	UT699-XQC
5962F0822801VXC	65342	UT699-XVC
5962R0822801VXC	65342	UT699-XVC
5962F0822801QYC	65342	UT699-ZQC
5962R0822801QYC	65342	UT699-ZQC
5962F0822802QYC	65342	UT699-ZQC
5962R0822802QYC	65342	UT699-ZQC
5962F0822801VYC	65342	UT699-ZVC
5962R0822801VYC	65342	UT699-ZVC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486

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