National Semiconductor

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

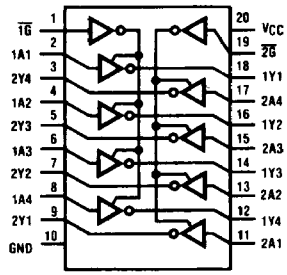
General Description

The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250 pF and 500 pF load capacitances.

Features

- t_{pd} specified with 250 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

Connection Diagram



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Top View

Order Number DP84240J or DP84240N
See NS Package Numbers J20A or N20A

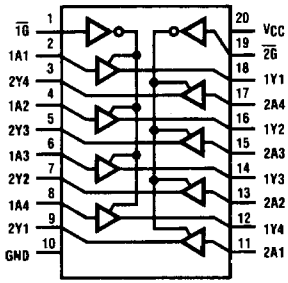
Truth Table

DP84240

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244



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Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	L
L	H	H

Top View

Order Number DP84244J or DP84244N
See NS Package Numbers J20A or N20A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Cavity Package	1150 mW
Molded Package	1300 mW
Lead Temperature (soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C. (Notes 2 and 3.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 2.7V		0.1	20	μA
		V_{IN} = 7.0V			100	μA
$I_{IN(0)}$	Logical "0" Input Current	0 ≤ V_{IN} ≤ 0.4V		−50	−200	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −18 mA		−1	−1.2	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100 μA I_{OH} = −1 mA	V_{CC}−1.15 V_{CC} −1.5	4.3 3.9		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 10 μA I_{OL} = 12 mA		0.2 0.3	0.4 0.5	V
I_{1D}	Logical "1" Drive Current	V_{OUT} = 1.5V	−75	−250		mA
I_{0D}	Logical "0" Drive Current	V_{OUT} = 1.5V	+100	+150		mA
Hi-Z	TRI-STATE Output Current	0.4V ≤ V_{OUT} ≤ 2.7V	−100		+100	μA
I_{CC}	Supply Current DP84240	All Outputs Open All Outputs High All Outputs Low All Outputs Hi-Z		 16 74 80	 50 125 125	mA
	DP84244	All Outputs High All Outputs Low All Outputs Hi-Z		40 100 115	75 130 150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

Switching Characteristics V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C, all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (Note 3.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay from LOW-to-HIGH Output	*Figures 1 & 3*	CL = 250 pF C_L = 500 pF	9 10	16 20	27 33	ns
t_{PHL}	Propagation Delay from HIGH-to-LOW Output		C_L = 250 pF C_L = 500 pF	9 12	16 20	25 31	ns
t_{PLZ}	Output Disable Time from LOW	*Figures 2 & 4*, S = 1, C_L = 50 pF			11	24	ns
t_{PHZ}	Output Disable Time from HIGH	*Figures 2 & 4*, S = 2, C_L = 50 pF			12	24	ns
t_{PZL}	Output Enable Time to LOW	*Figures 2 & 4*, S = 1, C_L = 500 pF			30	45	ns
t_{PZH}	Output Enable Time to HIGH	*Figures 2 & 4*, S = 2, C_L = 500 pF			23	35	ns
t_{SKEW}	Output-to-Output Skew (Note 4)	*Figures 1 & 3*, C_L = 500 pF			3		ns

Capacitance T_A = 25°C, f = 1 MHz, V_{CC} = 5V ±10%. (Note 3.)

Parameter	Conditions	Typ	Units
C_{IN}	All Other Inputs Tied Low	6	pF
C_{OUT}	Output in TRI-STATE Mode	20	pF

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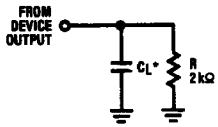
Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

Switching Test Circuits



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*C_L INCLUDES PROBE AND JIG CAPACITANCES

FIGURE 1. Capacitive Load Switching

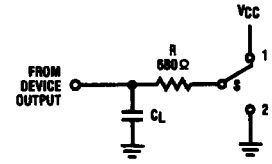

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FIGURE 2. TRI-STATE Enable/Disable

Typical Switching Characteristics

Voltage Waveforms

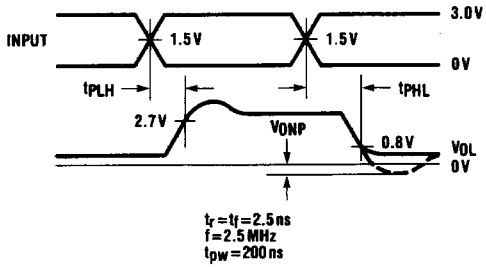

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FIGURE 3. Output Drive Levels

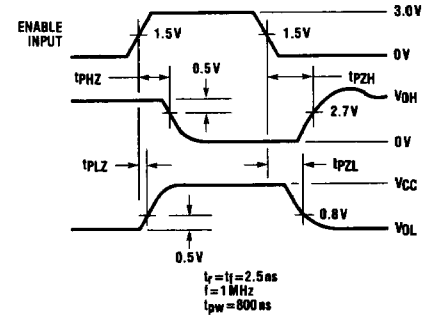

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FIGURE 4. TRI-STATE Control Levels

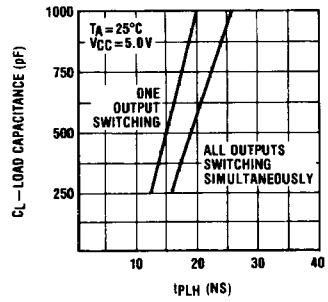

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FIGURE 5. t_{PLH} Measured to 2.7V on Output vs. C_L

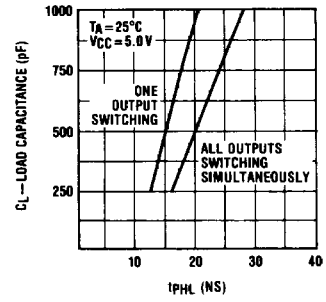

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FIGURE 6. t_{PHL} Measured to 0.8V on Output vs. C_L

Typical Switching Characteristics (Continued)

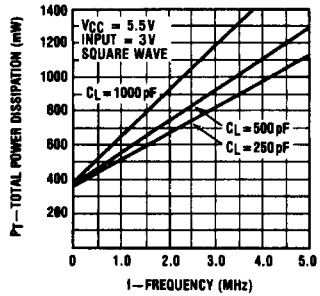

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FIGURE 7. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

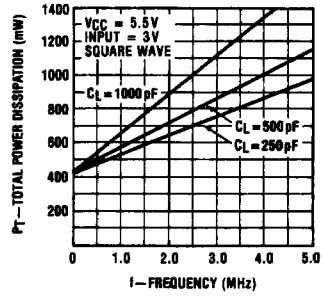

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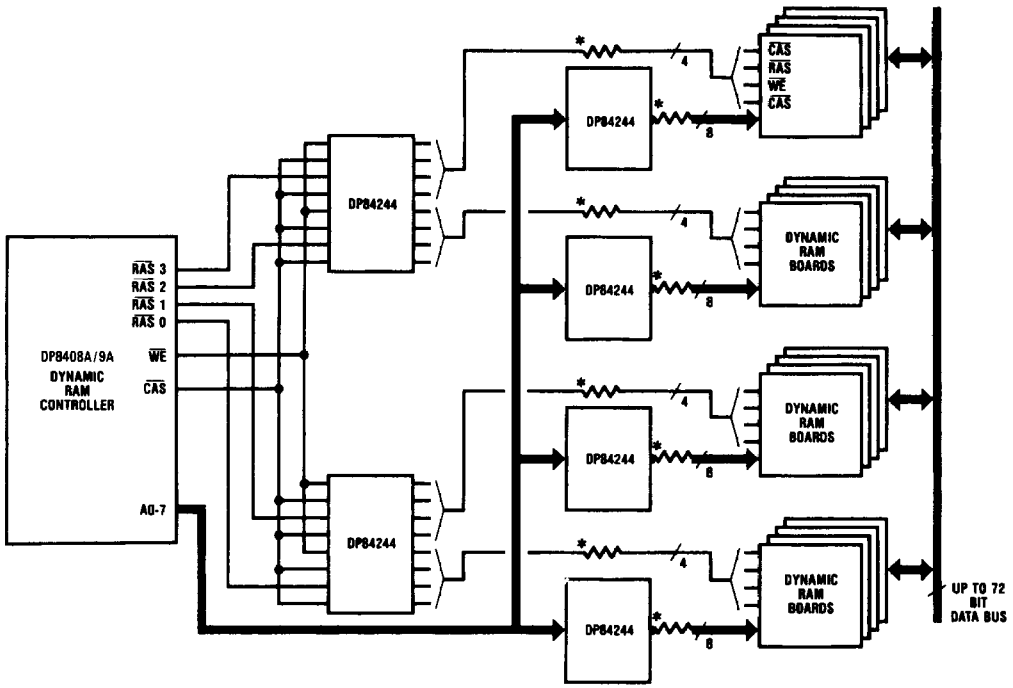
FIGURE 8. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

Typical Application

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)



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