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AK2391

BASE BAND FILTER FOR π/4 SHIFT QPSK MODULATION

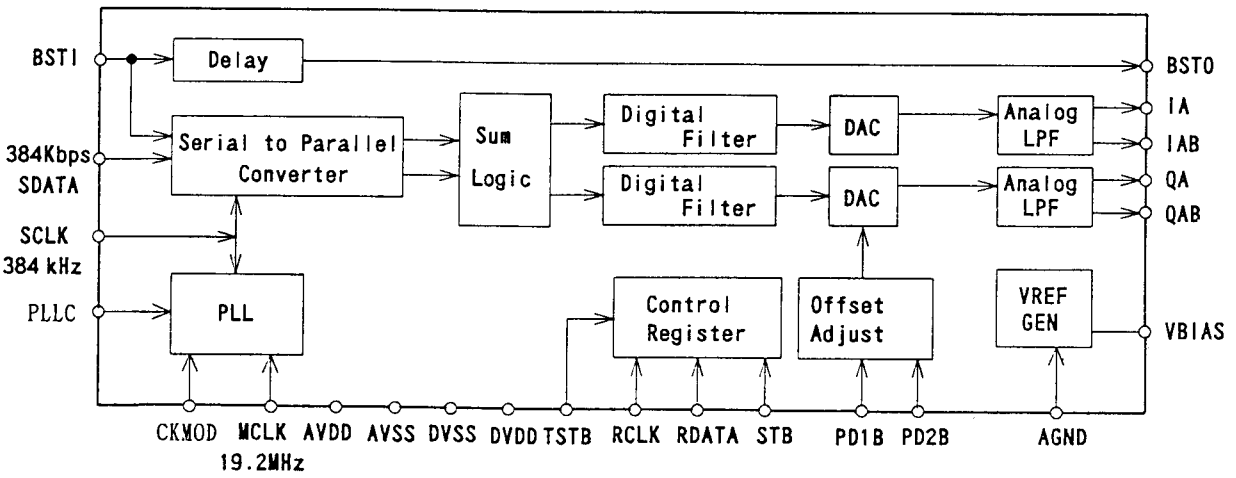
General Description

The AK2391 is a band limiting filter for π/4 shift QPSK modulation of Personal Handy phone System (PHS) in Japan. The AK2391 is compliant with Personal Handy phone System standard of RCR in Japan. The AK2391 consists of a Sum logic, Root Nyquist-Roll-offfilters and DA converters etc.

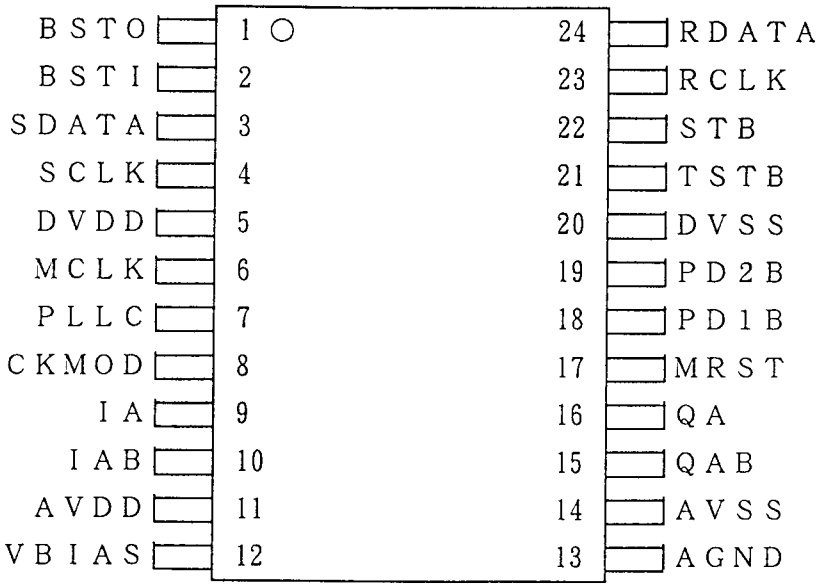
Features

- ☐ Compliant with Personal Handy phone System (PHS) in Japan
- ☐ Transmission Rate 384kbps
- ☐ Roll-off Filter (Digital Filter + Analog Filter)
  - * Root Nyquist Frequency Response
  - * Roll-off Rate $\alpha = 0.5$
  - * Pass Band (3dB) 96kHz
  - * Stop Band Attenuation Min 60dB(at 600kHz)
    Min 65dB(at 900kHz)
- ☐ Modulation Error 1.7%rms Typ.
- ☐ Ramp response circuit
- ☐ D/A converter
- ☐ Adjustable Output Level and DC Offset Voltage
- ☐ Differential logical circuit conforming to the π/4 shift QPSK modulation system
- ☐ Supply Current Normal Mode 7.0mA Typ.
  Power Saving Mode 20μA Typ.
- ☐ Supply Voltage 2.7V～5.5V
- ☐ Package 24 Pin VSOP

■ Block Diagram



■ Package／Pin Assignments



Pin/Function Descriptions

Pin	Name	I/O	Function
3	SDATA	I	Serial data input pin. Serial data is sampled on the rising edge of SCLK. Partitioning of the parallel data is decided on the rising edge of BSTI .
4	SCLK	I	Serial clock input pin. Clock frequency is 384kHz.
6	MCLK	I	Master clock input pin. Clock frequency is 19.2MHz. In the master clock mode, MCLK is distributed to all circuits.
8	CKMOD	I	Clock mode select pin. Setting CKMOD to "L" puts the AK2391 in the master clock mode. Setting CKMOD to "H" puts the AK2391 in the PLL clock mode.
7	PLLC	O	PLL buffer pin. Must be connected to the ground through a 4700pF±20% capacitor.
2	BSTI	I	Burst signal input pin. BSTI is synchronously sampled on the rising edge of SCLK.
1	BSTO	O	Burst signal output pin.
9	IA	O	Positive output pin for in phase. Ro≧10kΩ Note 1), Co≦20pF Note 2)
10	IAB	O	Negative output pin for in phase. Ro≧10kΩ Note 1), Co≦20pF Note 2)
16	QA	O	Positive output pin for quadrature phase. Ro≧10kΩ Note 1), Co≦20pF Note 2)
15	QAB	O	Negative output pin for quadrature phase. Ro≧10kΩ Note 1), Co≦20pF Note 2)
12	VBIAS	O	Op-amp bias voltage output pin. Must be connected to the analog ground through resister. Ro=47KΩ±5%
18 19	PD1B PD2B	I	Power down control pins. A power down mode can be selected by using both PD1B and PD2B.
23	RCLK	I	Clock pin for control register data. RDATA is sampled on the rising edge of RCLK.
24	RDATA	B	Control data input pin on the on-chip registers.
22	STB	I	Strobe pin for control register data. RDATA is stored to the register on the rising edge of STB.
21	TSTB	I	Test mode control pin. Setting TSTB to "H" puts the AK2391 in the normal mode. Setting TSTB to "L" puts the AK2391 in the test mode. (see "Setting of control register")
17	MRST	I	Master reset pin. H level input causes all registers reset to L.
11	AVDD	–	Analog power supply pin.
14	AVSS	–	Analog ground pin.
5	DVDD	–	Digital power supply pin.
20	DVSS	–	Digital ground pin.
13	AGND	–	AGND input pin.

Note 1)Register must be connected between XA and XAB.
Note 2)At power down mode. these pins are high impedance. (The voltage is $V_{DD}/2$.)

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min	Max	Units
DC Supply (Referenced to GND)				
	DVDD	-0.3	7.0	V
	AVDD	-0.3	7.0	V
Input Current	I_{IN}	-10	+10	mA
Input Voltage	V_{TD}	-0.3	AVDD+0.3	V
Storage Temperature	T_{stg}	-55	130	℃

Note 1) AVDD≧DVDD

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes .

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Referenced to GND)					
	DVDD	2.7		5.5	V
	AVDD	2.7		5.5	V
Operating Temperature	T_a	-30		85	℃

Note: AVSS, DVSS=0V

ELECTRICAL CHARACTERISTICS

■ DC Characteristics

Parameter		Symbol	Min	Typ	Max	Units
Supply Current	Mode 1 All circuits are turned off.	I_{DD}		20	30	μA
	Mode 2 VREF and PLL circuits are turned on.			2.0	3.0	mA
	Mode 3 VREF circuit is only turned on.			500	700	μA
	Mode 4 (Master Clock) Normal Operating mode			7.0	9.0	mA
	Mode 4 (PLL) Normal Operating mode			8.5	13.0	mA
Input Leakage Current		I_I			±10	μA
Digital High-Level Output Voltage I_{OH}=-2mA (Note1)		V_{OH}	V_D-1.0			V
Digital Low-Level Output Voltage I_{OL}=2mA (Note1)		V_{OL}			0.5	V
Digital High-Level Input Voltage		V_{IH}	0.7V_D			V
Digital Low-Level Input Voltage		V_{IL}			0.3V_D	V

Note 1) BSTO Pin only

■ Analog Characteristics
(AVDD=2.7～5.5V, DVDD=2.7～5.5V)

Parameter		Symbol	min	typ	max	単位
MCLK Frequency		f_S		19.2		MHz
SCLK Frequency		f_I		384		KHz
Analog Ground Reference Voltage $\frac{IA+IAB}{2}$, $\frac{QA+QAB}{2}$		V_{REF}	0.5AVDD±0.2			V
Analog Output Level (Note 1)		V_{UNIT}	0.460	0.500	0.575	V_{PP}
Adjustable Range of Analog Output Level			+15.0 -17.5	+17.5 -20.0	+20.0 -22.5	%
Stop Band Attenuation (Note 2)	at 600kHz±96kHz				-60	dB
	at 900kHz±96kHz				-65	dB
Spurious Level (Note 2)					-60	dB
Modulation Error				1.7	3	%rms
Temperature Drift of Analog Output Level					±200	PPM/℃
DC Offset Voltage |IA-IAB| , |QA-QAB|					30	mV
Adjustable Range of DC Offset Voltage			35	40	50	mV

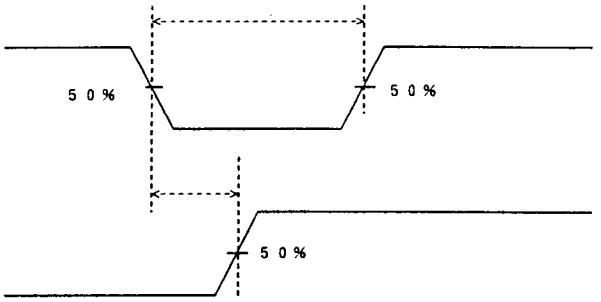
Note 1: Output load impedance is more than 10KΩ, and data streams from DATA pin are all zero.

Note 2: Referenced to twice of the power between 0Hz to 96kHz.

■ Switching Characteristics

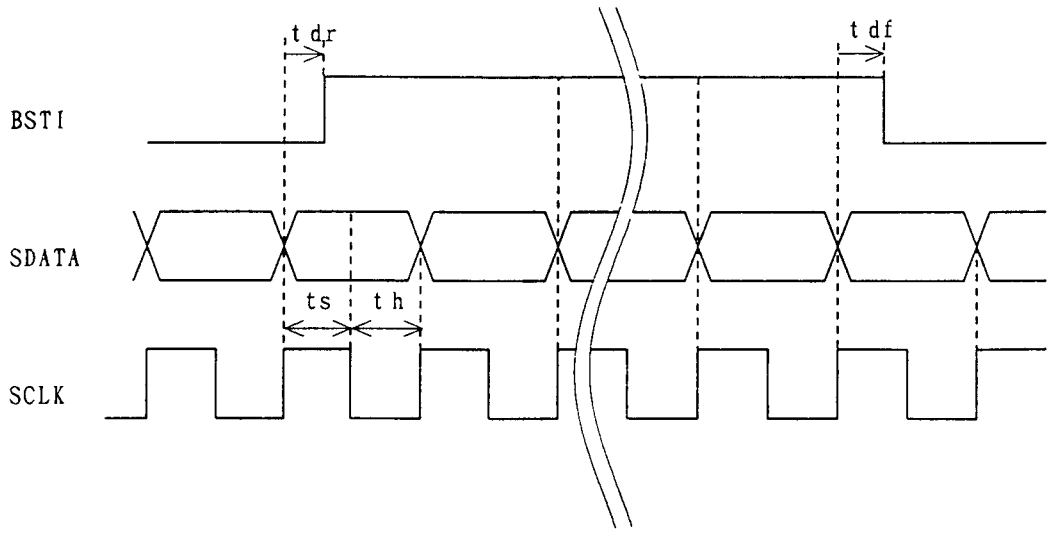
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	f_{clk}		19.2		MHz
BSTI Input Timing					
BSTI DELAY TIME FROM SCLK RISING EDGE	t_{dr}, t_{df}	-0.65		0.65	μs
SDATA Input Timing					
SDATA SET UP TIME	t_s	0.65			μs
SDATA HOLD TIME	t_h	0.65			μs
RDATA Input Timing					
REGISTER CLK FREQUENCY	f_{rclk}			5	MHz
REGISTER DATA SET UP TIME	t_{rs}	50			ns
REGISTER DATA HOLD TIME	t_{rh}	50			ns
STROBE SET UP TIME	t_{su}	50			ns
STROBE PULSE WIDTH	t_{pw}	50			ns
STROBE HOLD TIME	t_{ht}	50			ns

Digital Signal Timing Characteristics

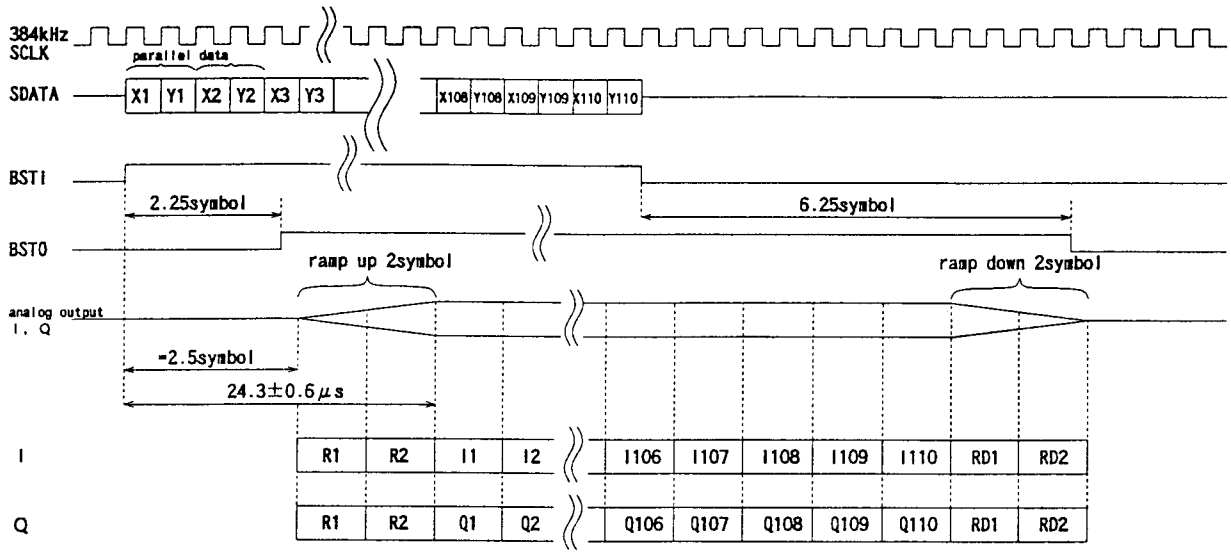


For all digital Timing.

SDATA Input Timing Diagram

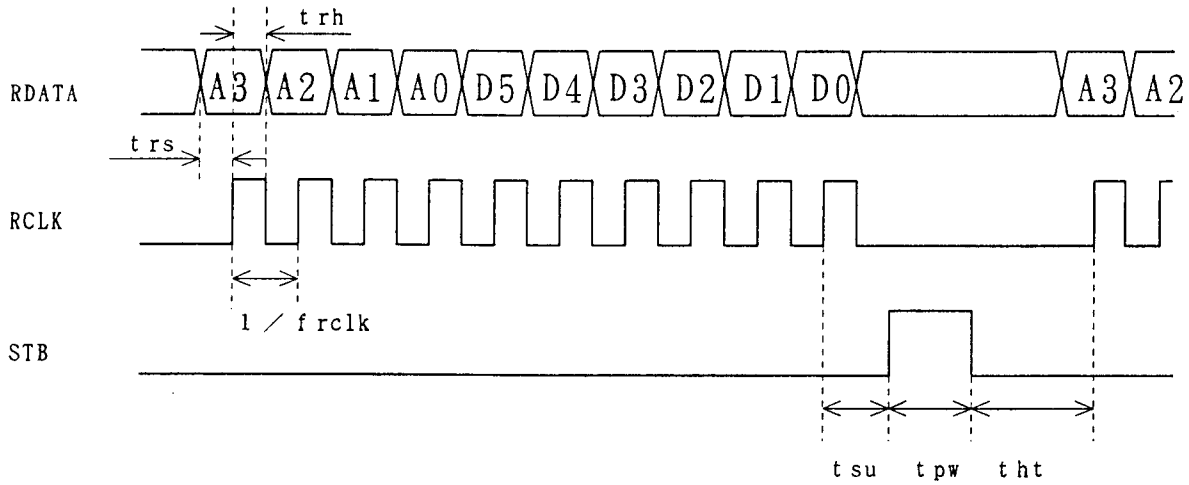


BSTI Input Timing Diagram



○Ramp up 2symbol
○Ramp down 2symbol
○Delay time(From BSTI to BSTO) :2.25symbol
○Parallel data(Xk,Yk) is modulated to (Ik,Qk).
○Delay time of modulation :24.3±0.6μs
○Data for ramp_up and ramp_down are generated automatically.
ramp_up data 0000(4 bits)
ramp_down data 0000(4 bits)

RDATA Input Timing Diagram



Specifications in regard to the BSTI input

① The "first BSTI " is defined as first burst signal input after recover of power down mode (full power down condition[mode 1] or partial energization condition [mode 2]). (Ref. Fig.3) All timing inside the AK2391 use the rising edge of "first BSTI" as the start point. So,384kHz internal clock, output signal, and another timing are decided by this rising edge.

② Both "H" length and "L" length of the BSTI should be even symbol lengths. AK2391 expect these lengths for modulation. (Ref. Fig.4)

③ According to ① and ②, in some cases you would not be sure whether BSTI lengths are even or not. We recommend you to use the power down mode (mode 1 or mode 2) during BSTI "L". It is a good method to prevent timing errors.

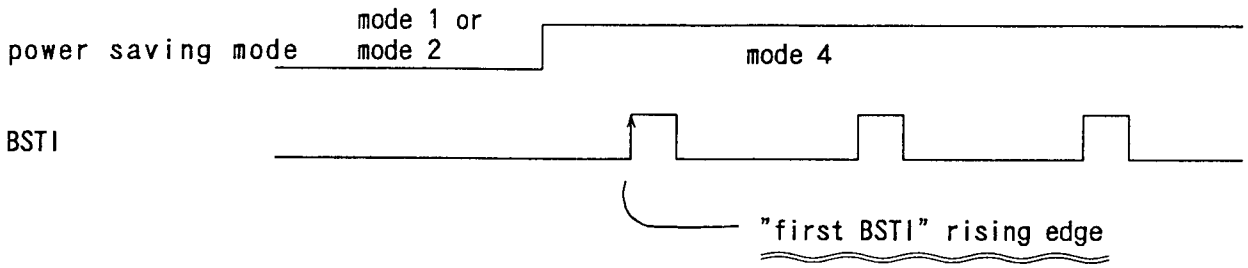
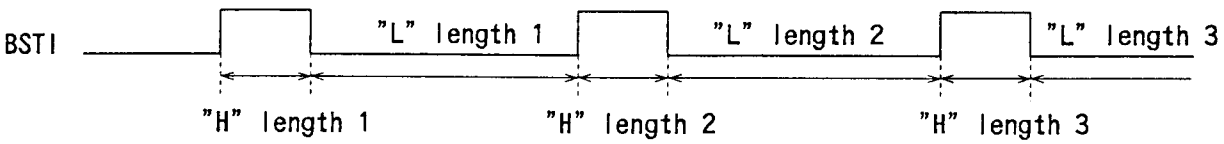


Fig.3

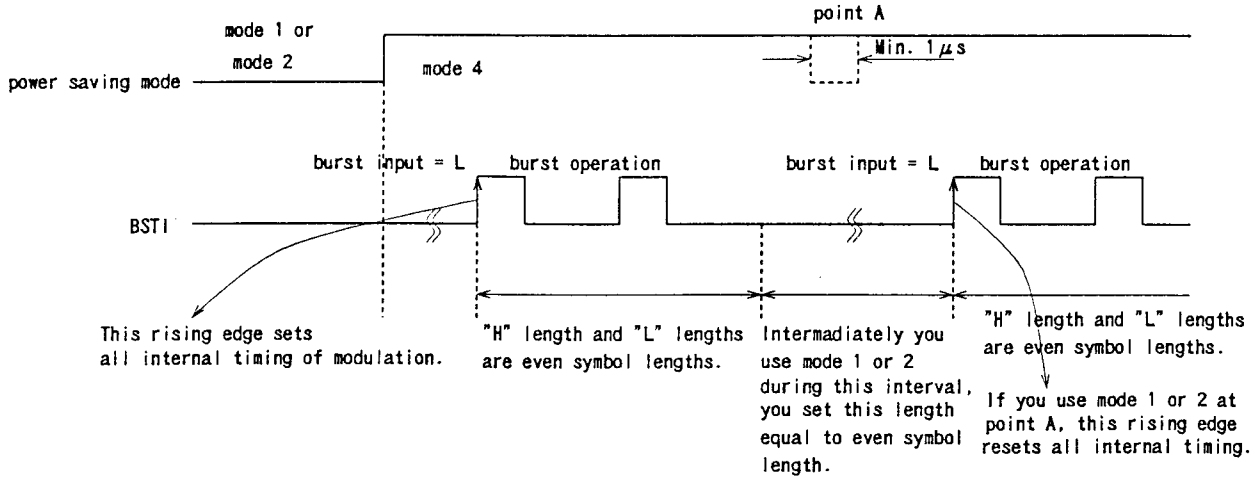


"H" length 1,2,3··· and "L" length 1,2,3··· must be equal to even symbol lengths.

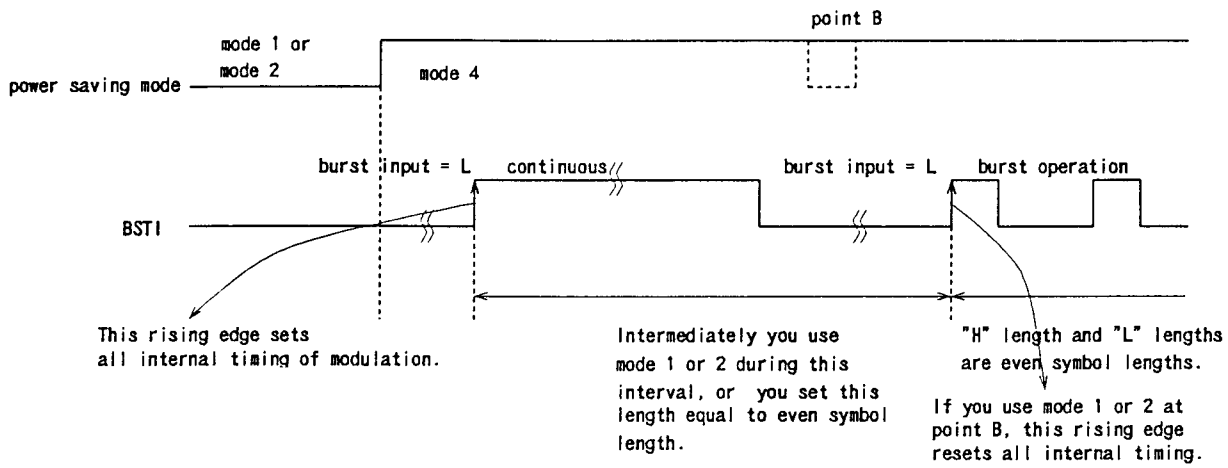
Fig.4

Useful examples are shown below.

(Example 1) In case of burst operation after power-down cancellation



(Example 2) In case of continuous operation after power-down cancellation



■ Power saving mode

1)Current consumption

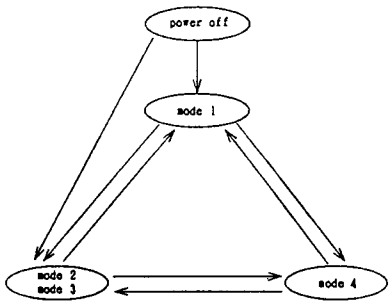
Power saving mode	Switch status			Current consumption(max)	
	PD1B	PD2B	CKMOD	external clock mode	PLL mode
Mode 1 (STAND BY)	0	×	×	30μA	30μA
Mode 2 (NON TRANSMITTING)	1	0	1	-	3mA
Mode 3 (NON TRANSMITTING)	1	0	0	700μA	-
Mode 4 (TRANSMITTING)	1	1	×	9mA	13mA

This LSI selects the above four modes according to the status of the power down control pins (PD1B, PD2B) and the clock mode select pin. PLL mode is selected at the time of CKMOD =1, and external clock mode is selected at the time of CKMOD=0. The "transmitting" of mode 4 indicates the normal operation condition.

2) Rising-up time

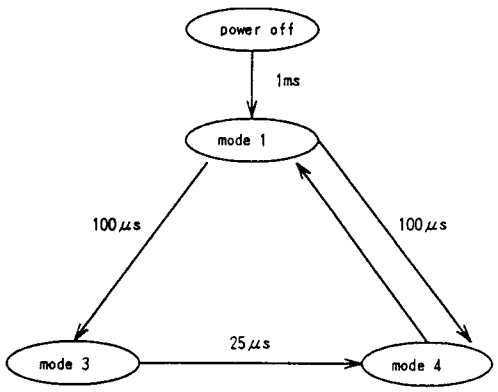
The time required for stabilization of the blocks becoming active at the time of shifting from one mode to another (shifting time) is shown in the following table.

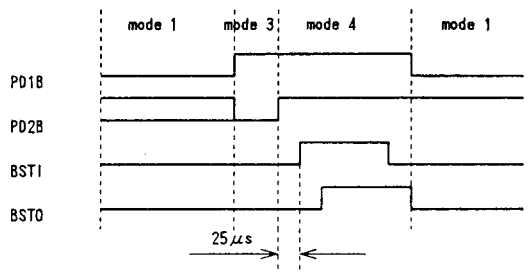
Clock mode	Status shifting	Shifting time
External clock mode	Power off → mode 1	1ms
	Power off → mode 3	1ms
	mode 1 → mode 3	100μs
	mode 1 → mode 4	100μs
	mode 3 → mode 4	25μs
	Other shifting	0s
PLL mode	Power off → mode 1	10ms
	Power off → mode 2	10ms
	mode 1 → mode 2	10ms
	mode 1 → mode 4	10ms
	mode 2 → mode 4	25μs
	Other shifting	0s



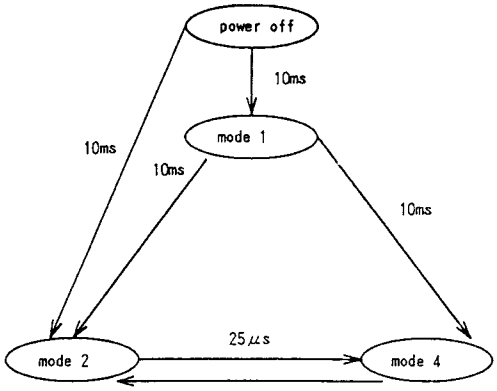
The shifting times between modes (max. value) and use examples are shown in the following figure.

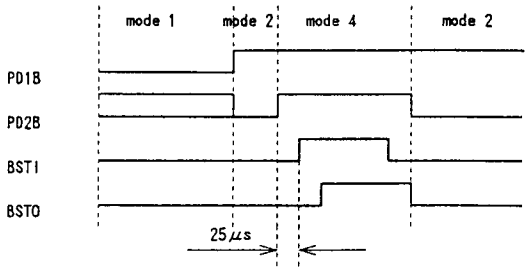
(At the time of external clock mode: CKMOD=0)



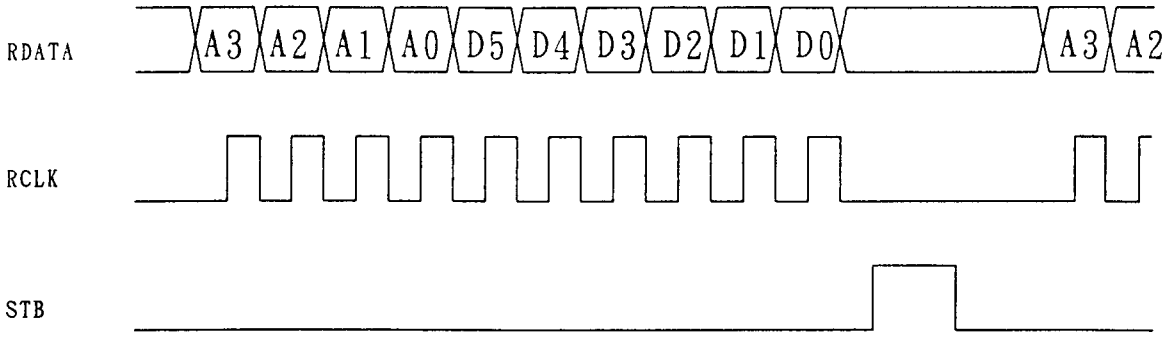


(At the time of PLL mode;CKMOD=1)





■ Setting of control register



A3	A2	A1	A0	D5	D4	D3	D2	D1	D0	
0	1	0	0	□	□	□	□	□	□	Ich Offset
0	1	0	1	□	□	□	□	□	□	Qch Offset
0	1	1	0	×	×	□	□	□	□	Ich Gain
0	1	1	1	×	×	□	□	□	□	Qch Gain
0	0	0	1	×	×	×	×	I	Q	FTEST
0	0	1	0	×	×	×	×	X_1	Y_1	CONSTANT INPUT DATA TEST

Output gain can be controlled by setting of control register. (-20.0% to +17.5% :step 2.5%). Output off-set voltage(IA-IAB, QA-QAB)can be controlled. (-41.9mV to +40.6mV :step 1.3mV). Note that one step of off-set voltage is changed if output gain level is pre-set.

(Reset of control registers)

After power is supplied, contents of control registers are unknown. So, please set control registers after power is supplied. If you want to initilize all control registers to zero, please use MRST pin.

(Table of gain control)

Register data						Output gain (Percentage of standard output level)
D 5	D 4	D 3	D 2	D 1	D 0	
×	×	0	1	1	1	117.5
×	×	0	1	1	0	115.0
×	×	0	1	0	1	112.5
×	×	0	1	0	0	110.0
×	×	0	0	1	1	107.5
×	×	0	0	1	0	105.0
×	×	0	0	0	1	102.5
×	×	0	0	0	0	100.0
×	×	1	1	1	1	97.5
×	×	1	1	1	0	95.0
×	×	1	1	0	1	92.5
×	×	1	1	0	0	90.0
×	×	1	0	1	1	87.5

Register data						output gain (Percentage of standard output level)
D 5	D 4	D 3	D 2	D 1	D 0	
×	×	1	0	1	0	85.0
×	×	1	0	0	1	82.5
×	×	1	0	0	0	80.0

(Table of off-set voltage)

Register data						Off-set voltage (mV) TYP
D 5	D 4	D 3	D 2	D 1	D 0	IA−IAB (QA−QAB)
0	1	1	1	1	1	40.3
~						
0	0	0	0	1	1	3.9
0	0	0	0	1	0	2.6
0	0	0	0	0	1	1.3
0	0	0	0	0	0	0
1	1	1	1	1	1	-1.3
1	1	1	1	1	0	-2.6
1	1	1	1	0	1	-3.9
~						
1	1	1	1	0	0	-5.2
1	0	0	0	0	0	-41.6

(Test mode)
With test mode, the following outputs can be selected in regard to the data written into the registers with the addresses 0001 and 0010. For test mode, writing to the register is executed with the TSTB terminal in "H" condition, and test mode then is reached when the TSTB terminal is switched to "L".
Test mode sequence example
1. Write data to address 0001 or 0010.
2. Set TSTB to "L". (Shifting to test mode)
3. Set BSTI to "H". (Output start)
4. Write data to address 0110 or 0111. (Gain adjustment)
5. Write data to address 0100 or 0101. (Offset adjustment)
6. Set BSTI to "L". (Output completion)
7. Set TSTB to "H". (Shift to normal mode)

① FTEST (in regard to the data written to the register of the address 0001)

Register data						Test mode
D 5	D 4	D 3	D 2	D 1	D 0	Output
×	×	×	×	0	0	I = 0, Q = 0
×	×	×	×	0	1	I = 0, Q = V_{UNIT}
×	×	×	×	1	0	I = V_{UNIT}, Q = 0
×	×	×	×	1	1	I = V_{UNIT}, Q = V_{UNIT}

Note: Vunit is the voltage corresponding to the output when the input data all are zero, corresponding to the value when gain and offset have been adjusted.

② Constant input DATA TEST(in regard to the data written to the register of the address 0010)

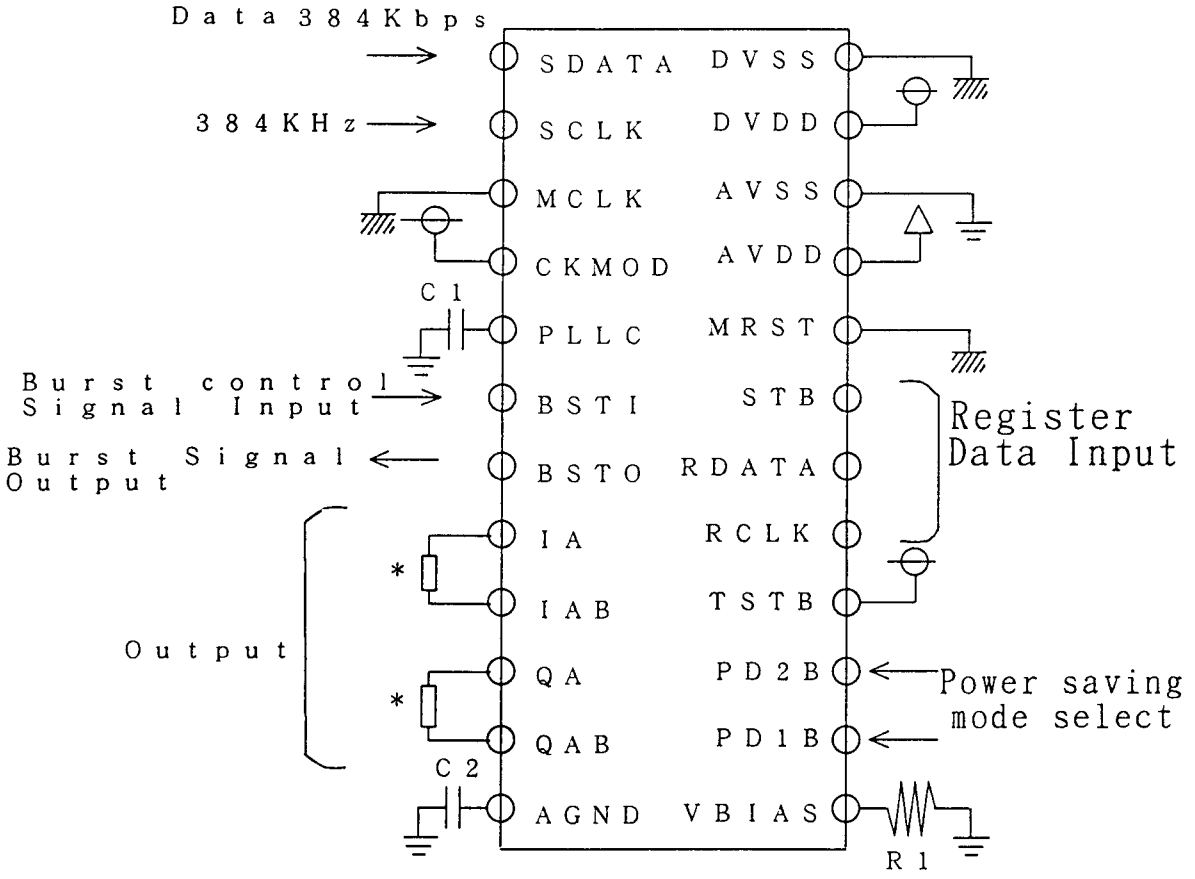
Register data						Test mode	
D 5	D 4	D 3	D 2	D 1	D 0	Output	
×	×	×	×	0	0	Output for (Xn, Yn)=(0, 0)	n=1, 2, 3···
×	×	×	×	0	1	Output for (Xn, Yn)=(0, 1)	n=1, 2, 3···
×	×	×	×	1	0	Output for (Xn, Yn)=(1, 0)	n=1, 2, 3···
×	×	×	×	1	1	Output for (Xn, Yn)=(1, 1)	n=1, 2, 3···

Note 1) FTEST and Constant input DATA TEST are active if TSTB is set to 'L' and BSTI is se t to 'H'.
Note 2) Ramping response is not executed in the TEST mode.

Application Circuit

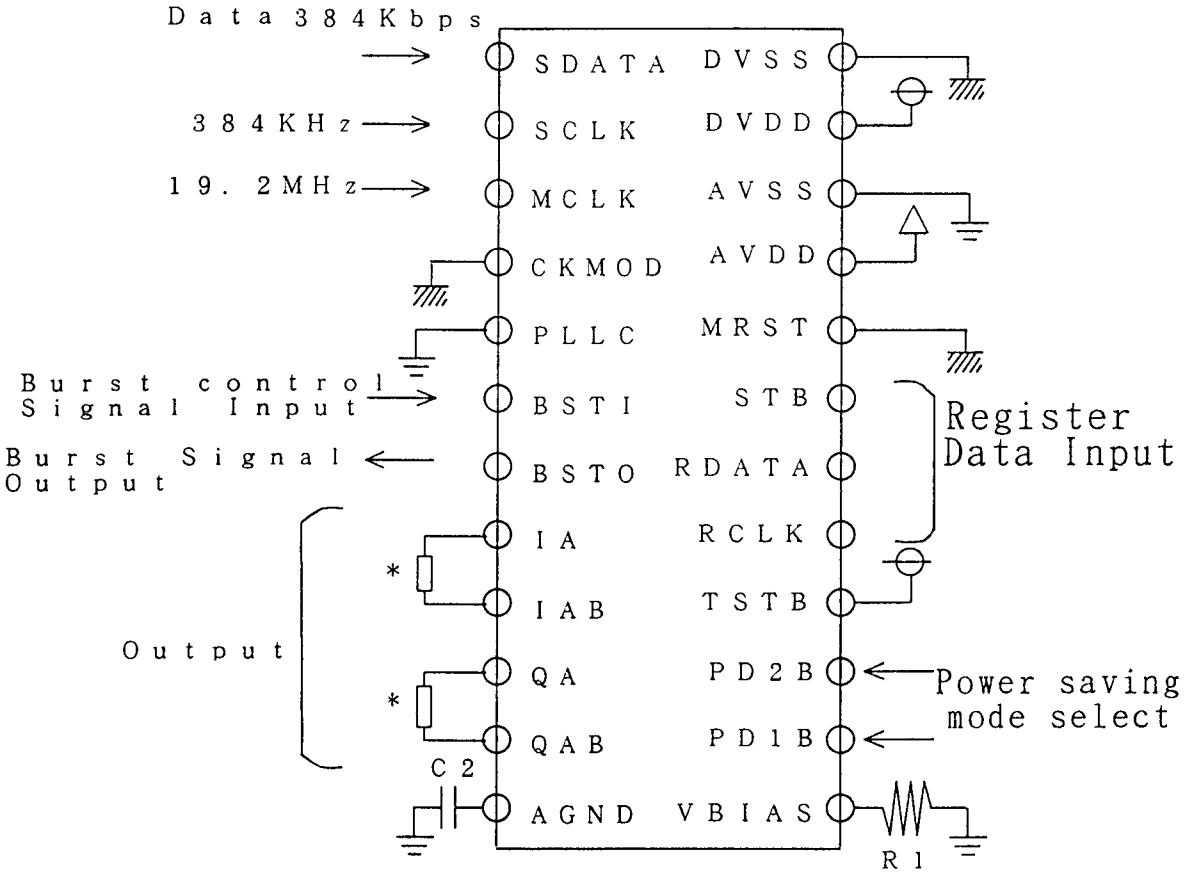
◎Connection for PLL mode

Operation is made using the 384 kHz clock entered from the serial data input clock terminal (SCLK). At this time, fix the CKMOD terminal to "H" and the MCLK terminal to DVDD or DVSS.



C1＝4700pF±20%
C2＝1000pF
R1＝47KΩ ±5%
＊ Load…≧10KΩ、≦20pF

◎Connection for external clock mode
Operation is made using the 19.2 kHz clock entered from the MCLK terminal. At this time, set the CKMOD terminal to "L", synchronize the SCLK terminal to the rise of the 19.2 MHz, and provide 384 kHz as input.

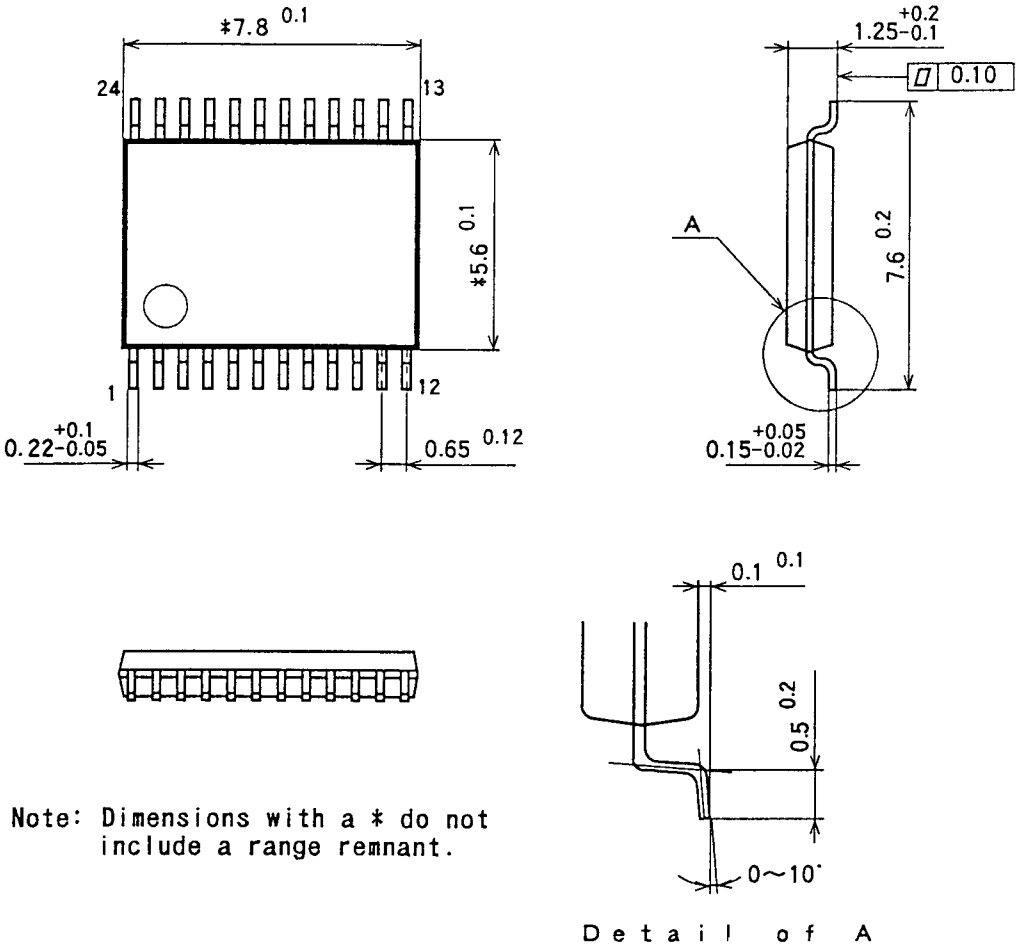


C2 = 1000pF
R1 = 47KΩ ±5%
＊ Load… ≧10KΩ、≦20pF

■ Package size

24 Pin VSOP

Unit : mm



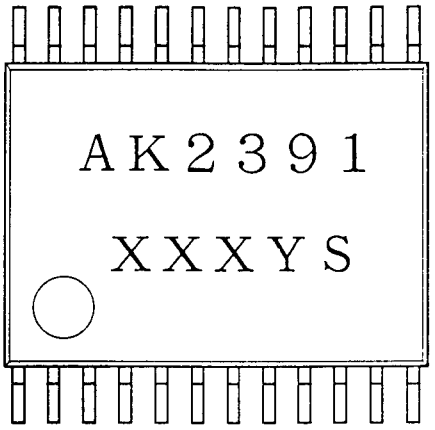
Note: Dimensions with a * do not include a range remnant.

Detail of A

[Material] Resin :Low Stress Type Epoxy Resin
Lead Frame:42 Alloy

Package

■Marking



[XXXYS Content]

XXX : Manufacturing Data
Last digit of AD year, 2 digits of week number.

Y : Manufacturing Lot Number
(Using A~Z Alphabet, without I,O,U,Z)

S : Assembly Plant Code

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