AK7832A

2.0W Stereo Audio Class-D Amp. with ALC

GENERAL DESCRIPTION

The AK7832A is a Stereo, Filter-free Class-D amplifier for driving 4Ω/8Ω dynamic speakers.
Built-in "Automatic Level Control (ALC)" function can normalize incoming variable music data to comfortable level.
The AK7832A is capable of "Low EMI" performance that allow to be applied for RF application easily rather than traditional Class-D amplifier.
The AK7832A is available in a small 24-pin WL-CSP package.

FEATURES

☐Class-D Amplifier

- 2.0W x 2ch @RL=4Ω, THD+N=10%, VDDX=5V
- 1.2W x 2ch @RL=8Ω, THD+N=10%, VDDX=5V
- Very "Low EMI"
- Selectable either Mono or Stereo mode
- Available both Single-ended and Full differential input
- Digital BTL output
- Gain adjustable : 6dB/9.5dB/12dB/15dB
- Pop-free design
- Filter-free solution

☐ALC

- ALC-Limiter and ALC-Recovery with Fast recovery function
- ALC control registers
- ALC function can be bypassed

☐Control function

- Available I2C interface
  - Mono / Stereo
  - Gain adjust
  - ALC parameters, etc.
- Also capable of Pin control

☐Operating Voltage VDD1/2 : 2.7V ~ 5.0V, DVDDI : 1.65V ~ 5.0V
☐Operating Temperature -30 ~ +85℃
☐Package WL-CSP 24-pin (2.5mm x 2.5mm)

BLOCK DIAGRAM

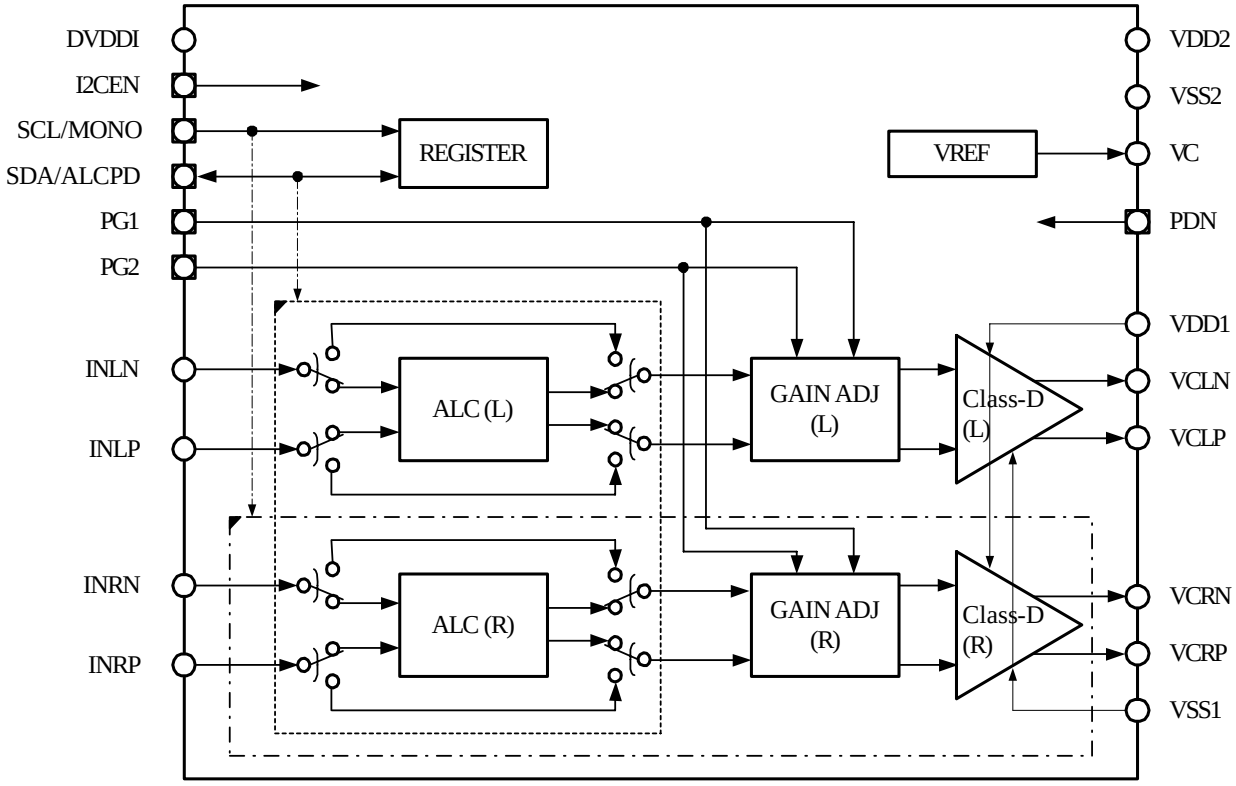


Figure 1: Block Diagram

■ Ordering Guide

AK7832AB	–30 ~ +85°C, 24pin WL-CSP（BGA, 0.5mm pitch : （Figure 38）
AK7832ABB	AK7832AB with black resin sheet on surface (Figure 39)
AKD7832A	AK7832A Evaluation Board

■ Pin Assignment

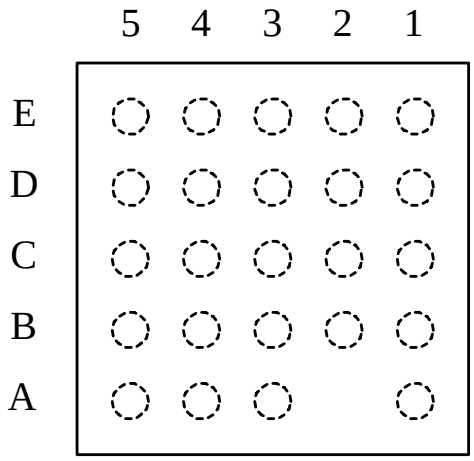


Figure 2: Pin Location (Top View)

	5	4	3	2	1
E	NC	VCRP	VDD1	VCLP	NC
D	PG2	VCRN	VSS1	VCLN	PG1
C	DVDDI	SDA/ALCPDN	PDN	I2CEN	VDD2
B	SCL/MONO	INRP	INLP	VSS2	VC
A	NC	INRN	INLN	<index>	NC

Table 1: Pin Assignment (AK7832AB)

PIN / FUNCTION

No.	Pin Name	I/O	Function
A1	NC	—	(Note 2)
A2	—	—	<Index>
A3	INLN	—	L-channel negative input
A4	INRN	—	R-channel negative input
A5	NC	—	(Note 2)
B1	VC	—	Internal analog reference voltage output pin. Connect to VSS via 0.01µF capacitor.
B2	VSS2	—	Analog Ground
B3	INLP	—	L-channel positive input
B4	INRP	—	R-channel positive input
B5	SCL	I	when I2CEN= "H" I2C Control clock (SCL) input pin
	MONO	I	when I2CEN= "L" Mono / Stereo select pin "H" : Mono (R-ch Power-down) "L" : Stereo
C1	VDD2	—	Analog Power supply
C2	I2CEN	I	I2C interface enable pin "H": I2C interface enable "L": I2C interface disable (Can not access internal registers)
C3	PDN	I	Power Down pin: H=power on, L=power down and reset registers
C4	SDA	I/O	when I2CEN= "H" Register Control Data pin
	ALCPDN	I	when I2CEN pin ="L" ALC block Power ON/OFF pin "H": ALC Power On "L": ALC Power OFF
C5	DVDDI	—	Power supply for digital interface
D1	PG1	—	when I2CEN="L": Pre-Gain control pin 1 when I2CEN="H": connect it to VSS
D2	VCLN	—	Left channel Class D amp negative output (-)
D3	VSS1	—	Ground pin for amplifier
D4	VCRN	—	Right channel Class D amp negative output (-)
D5	PG2	—	when I2CEN="L": Pre-Gain control pin 2 when I2CEN="H": connect it to VSS
E1	NC	—	(Note 2)
E2	VCLP	—	Left channel Class D amp positive output (+)
E3	VDD1	—	Power supply for class D amplifier
E4	VCRP	—	Right channel Class D amp positive output (+)
E5	NC	—	(Note 2)

Note 1: All input pins except analog input pins (INLN, INLP, INRN INRP) shall not be floating.
Note 2: NC pin must be connected to VSS.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Category	Pin Name	Setting
Analog	INLP, INRP, INRN, VCRN, VCRP	Open
Digital	SCL, SDA, PG1, PG2	Connect to VSS

ABSOLUTE MAXIMUM RATINGS

(VSS1/2=0V; Note 3)

Parameter		Symbol	Min	Max	Units
Power Supplies (Note 4)	Speaker Amp (VDD1) Analog (VDD2)	VDDX	–0.3	6.5	V
	Digital I/F	DVDDI	–0.3	6.5	V
Input Current, Any Pin Except Supplies		IIN	-10	+10	mA
Analog Input Voltage (Note 5)(Note 7)		VINA	–0.3	VDDX+0.3	V
Digital Input Voltage (Note 6)(Note 7)		VIND	–0.3	DVDDI +0.3	V
Continuous total power dissipation (Note 8)		Pd		1400	mW
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 3: All voltages are with respect to ground. Connect VSS1 and VSS2 to the same analog ground plane.
Note 4: Power Supplies must be DVDDI ≦ VDDX
Note 5: INRN, INRP, INLN and INLP
Note 6: SDA, SCL, PDN, I2CEN, PG1, and PG2 pin
Note 7: A maximum value must not exceed 6.5V even if VDDX or DVDDI is more than 6.2V
Note 8: *Testing environment:* Ta=25℃, no wind.
Board environment: Mount WLCSP package under conditions below implementing WLCSP Package. 80mm x 120mm x 15mm(FR4), more than 10 of the surface of the board (counting front-back both side) is covered by Cu interconnects.

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed under these extreme conditions.

RECOMMENDED OPERATING CONDITIONS

(VSS1/2 =0V;Note 3)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies (Note 9)	VDD1, VDD2	VDDX	2.7	3.6	5.0	V
	Digital I/F	DVDDI	1.65	2.8	VDDX	V

Note 9: Power supply order must be VDDX → DVDDI. (Figure 5)

WARNING: AKEMD assumes no responsibility for the outcomes in usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS 1

Ta=25℃, VDDX=5.0V, DVDDI=2.8V, VSS1/2=0V, input=sinewave 1kHz single-ended, Output Load Impedance Z_L = 8 Ω +10uH (series), measurement band frequency=20～20kHz, unless otherwise specified.

Parameter	Conditions		Min	Typ	Max	Units
Output Power @VCLP/N, VCRP/N (Note 10)	THD=10%			1.2		W
	THD=1%			1.0		
	THD=10%,VDDX=3.6V			0.7		
	RL=4Ω+10μH, THD=10% (Note 13)			2.0		
PSRR (Note 14)	VDDX=3.6V (DC) + 0.2Vpp (AC),sinewave, f=1kHz			60		dB
CMRR (Note 14)	INLP/N=1.2V(DC)+1.0Vpp(AC), sinewave, f=1kHz INRP/N=1.2V(DC)+1.0Vpp(AC), sinewave, f=1kHz			50		dB
Idd (Note 11)	VDDX=3.6V, ALC:on			3.3	4.3	mA
	VDDX=3.6V, ALC:off			2.2	3.1	
Shut-Down Current	PDN="L"			0.1	10	μA
Switching Frequency.			225	250	275	kHz
THD+N @VCLP/N, VCRP/N	Output Power=0.6W/ch (Input level= 2Vpp)		50			dB
SNR	Output Power=0.6W/ch, A-weighted		70	80		dB
Cross Talk @VCLP/N, VCRP/N	INLN=No Input, INRN=2Vpp INRN=No Input, INLN=2Vpp			70		dB
Maximum Input level	Single-ended input, Differential input				2	Vpp
Input Impedance			25	50	75	kΩ
Startup Time (Figure 6)	VDDX=3.0V PDN ="H" → Output signal stabilization		20	25	30	ms
Output Level (Note 12)	@Single-ended INLN=–5.0dBV ALC:off	PG2=0, PG1=0	0.0	1.0	2.0	dBV
		PG2=0, PG1=1	3.5	4.5	5.5	
		PG2=1, PG1=0	6.0	7.0	8.0	
		PG2=1, PG1=1	9.0	10.0	11.0	

Note 10: Output power per one channel

Note 11: While no input.

Note 12: While I2CEN="H", PG1 and PG2 stand for the register 03h{PRGAIN:PG1, PG2}.
While I2CEN="L", they stand for PG1 pin and PG2 pin.

Note 13: When a Load is 4Ω and output power is 2W/ch and ambient temperature is more than 85℃, the power consumption may exceed continuous total power dissipation (Pd). Under such case, take actions such as to lower the ambient temperature to around 50℃, to adopt six layer board or to raise interconnect density to more than 80 percent.

Note 14: These specifications are guaranteed by design and characterization and are not tested in production.

DC CHARACTERISTICS

(Ta=25°C, VDDX =2.7~5.0V, DVDDI=1.65V~VDDX)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage 1 (Note 15)		VIH1	70%DVDDI		–	V
Low-Level Input Voltage 1 (Note 15)		VIL1	–		30%DVDDI	V
High-Level Input Voltage 2 (Note 16)	DVDDI<2.25V	VIH2	80%DVDDI		–	V
	DVDDI≧2.25V		70%DVDDI		–	
Low-Level Input Voltage 2 (Note 16)	DVDDI<2.25V	VIL2	–		20%DVDDI	V
	DVDDI≧2.25V		–		30%DVDDI	
Hysterisys Voltage 1 (Note 17) (Note 20)		VHS1	5%DVDDI			V
Hysterisys Voltage 2 (Note 18) (Note 20)	DVDDI = 3.6V	VHS2		0.57		V
	DVDDI = 1.7V			0.30		
Low-Level Output Voltage (Note 19)		VOL			0.4	V
Input Leakage CurrentI		IL	–10		+10	μA

Note 15: Applied to SDA and SCL pin (inputs with Schmitt triggers).
Note 16: Applied to PDN, PG1, PG2, and I2CEN pin (inputs with Schmitt triggers).
Note 17: Applied to SDA and SCL pin (inputs with Schmitt triggers) while using I^2CBus as high-speed mode.
Note 18: Applied to PDN, PG1 and PG2 pin (inputs with Schmitt triggers)
Note 19: Applied to SDA pin (open drain output). When Iout (@SDA)=3mA.
Note 20: These specifications are guaranteed by design and characterization and are not tested in production.

SWITCHING CHARACTERISTICS

■ I2CBus Interface Specification.

(1) Standard Mode

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL clock frequency		100	kHz
t_{HIGH}	SCL clock “High” time	4.0		μs
t_{LOW}	SCL clock “Low” time	4.7		μs
t_R	SDA and SCL rise time		1.0	μs
t_F	SDA and SCL fall time		0.3	μs
$t_{HD:STA}$	Start Condition hold time	4.0		μs
$t_{SU:STA}$	Start Condition setup time	4.7		μs
$t_{HD:DAT}$	SDA hold time (vs. SCL falling edge)	0		μs
$t_{SU:DAT}$	SDA setup time (vs. SCL rising edge)	250		ns
$t_{SU:STO}$	Stop Condition setup time	4.0		μs
t_{BUF}	Bus free time	4.7		μs

(２)High Speed Mode

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL clock frequency		400	kHz
t_{HIGH}	SCL clock “High” time	0.6		μs
t_{LOW}	SCL clock “Low” time	1.3		μs
t_R	SDA and SCL rise time	20+0.1xCb (Note 21)	300	ns
t_{F1} (Note 22)	SDA and SCL fall time	20+0.1xCb (Note 21)	300	ns
t_{F2} (Note 23)	SDA fall time	15	300	ns
t_{F3} (Note 24)	SDA fall time	20+0.1xCb (Note 21)	300	ns
$t_{HD:STA}$	Start Condition hold time	0.6		μs
$t_{SU:STA}$	Start Condition setup time	0.6		μs
$t_{HD:DAT}$	SDA hold time (vs. SCL falling edge)	0		μs
$t_{SU:DAT}$	SDA setup time (vs. SCL rising edge)	100		ns
$t_{SU:STO}$	Stop Condition setup time	0.6		μs
t_{BUF}	Bus free time	1.3		μs
t_{SP}	Noise suppression pulse width		30	ns

Note 21: Cb: Total Capacitance at 1 line(unit : pF)
Note 22: t_{F1}: Falling time when SDA/SCL signal is input signal for AK7832A.
Note 23: t_{F2}: Falling time AK7832A makes SDA signal H to L under following conditions.
(Conditions: DVDDI > 2.0V、C_b = 10～100(pF), sink current <= 3mA)
Note 24: t_{F3}: Falling time AK7832A makes SDA signal H to L under following conditions
(Conditions: DVDDI < 2.0V, C_b = 10~100(pF), sink current <= 3mA)

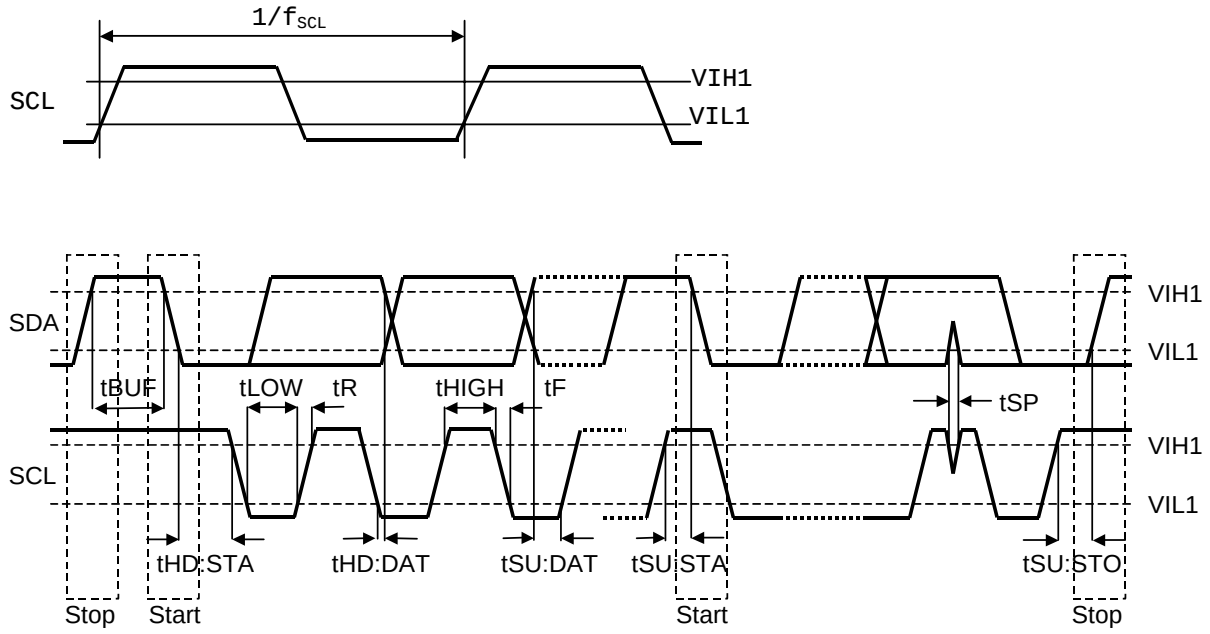


Figure 3: I2C Interface Timing

OPERATION OVERVIEW

■ Class-D amplifier.

The AK7832A, a stereo Class-D audio amplifier, has higher efficiency compared to Class-AB amplifier. It can drive both 8Ω and 4Ω dynamic speakers, would eliminate output LC filters by using a unique circuit composition, corresponds to both single and differential input by just changing external circuit outside of input pins. (Figure 33 ~ Figure 36)

■ Gain Adjustment

Users can change gain by setting PG1/2 pins (Figure 4) or control registers. When using PG1/PG2 pins set I2CEN pin = "L". When using control registers set I2CEN pin = "L" and refer to the section of Detailed Register Settings.

PG2 pin	PG1 pin	Gain [dB]
L	L	6
L	H	9.5
H	L	12
H	H	15

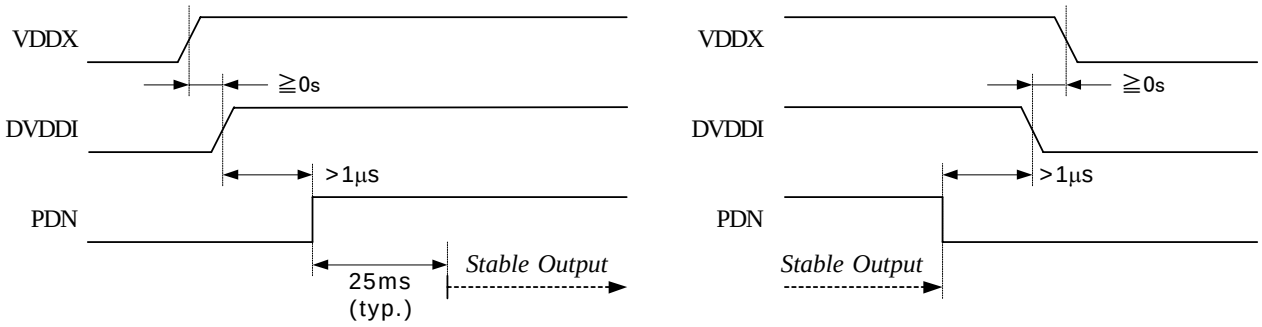
Figure 4: Gain setting by using PG1 and PG2 pins.

■ Control Registers.

8 bit registers can change many settings, ALC parameters, Pre Gain values, and so on through I2C control during both Standard and High-speed mode. When I2CEN pin is set "H", I2C interface will be active. Once I2CEN pin is set "L", SCL pin will become changing Mono/Stereo and SDA pin will become ALC power control, then control registers cannot be accessed.

■ Power Control pin

Once PDN pin is set "L", all circuits will power down and all registers will be initial condition.
DVDDI can be turned off while VDDX is turning on, VDDX CANNOT be turned off while is on. Output signal is stable after 25ms (typ) from PDN pin switched "L" to "H", as shown in Figure 5.



Power Up Sequence Power Down Sequence

Figure 5: Power Up/Down Sequence

Power up/down flowchart is shown in Figure 6 below.

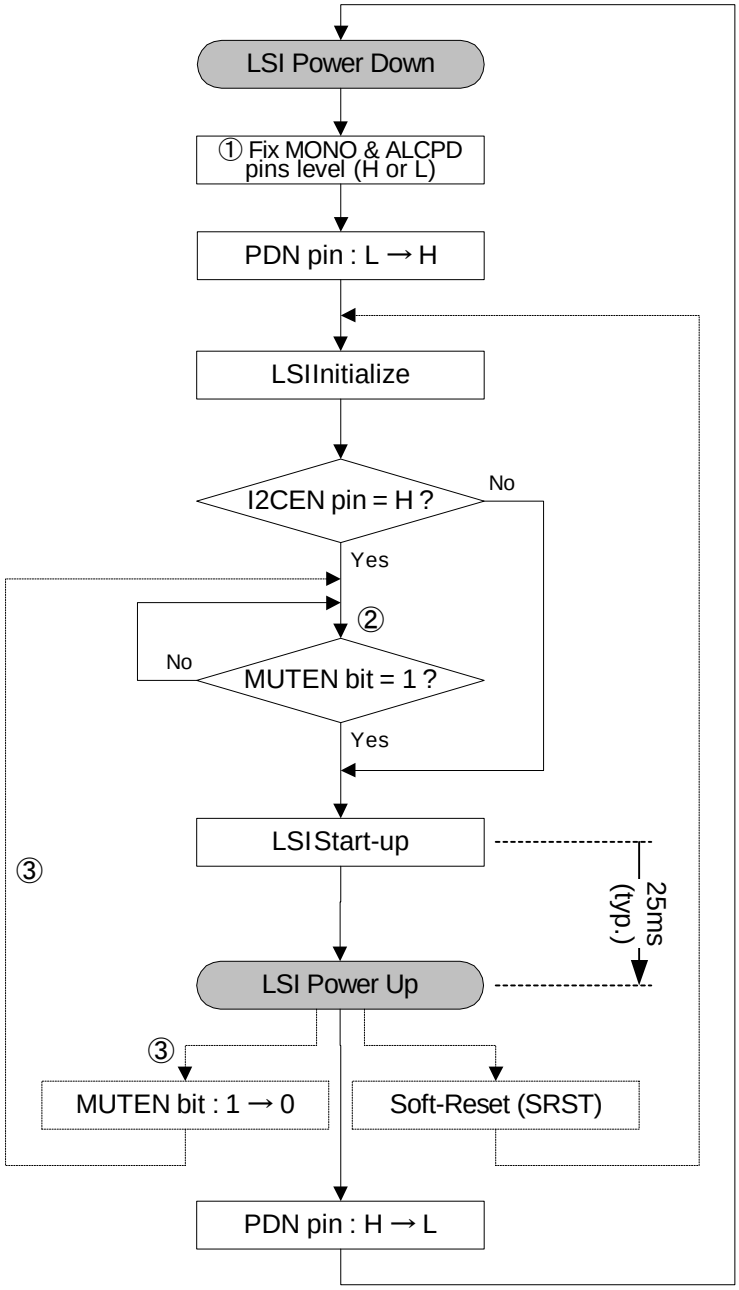


Figure 6: Power Up/Down Flow Chart

① When not using I2C interface (I2CEN = ”L”), Mono and ALCPDN pins must be set before PDN pin is set from “L” →”H”.

② When using I2C interface (I2CEN = ”H”), set register adress02h {PDNMODE:MUTEN} bit 0→1 to activate AK7832A. Then, registers with respect to Mono/Stereo and ALC must be set before MUTEN bit 0→1. (Note 25)

③ If ALC parameters are going to be changed during AK7832A is active, address 06h{ALCCTRL3:ALC} bit must be 0 (Note 25), and then furthermore, set MUTEN bit to 0 to avoid pop noise.

■ Protection circuit

(1) Short Protection

Class-D amp in AK7832A has a short protection circuit, which suppress rise in temperature when between following pins are shorted, VCLP/VCRP pin⇔VCLN/VCRN pin, VCLP/VCRP/VCLN/VCRN pins⇔Gound.

(2) Thermal Protection

AK7832A has the thermal shut down function to protect the device from being damaged from the rise in temperature.

Parameter		Min	Typ	Max	Units
Output Short Protection	@VCLP⇔VCLN or @VCRP⇔VCRN	–	60	120	mA
Thermal Shut-Down	Detection Temperature	–	150	–	℃
	Recovery Temperature	–	120	–	

■ Path Setting

Function block path settings are shown in Figure 7. It is changeable by I2CEN, SCL/MONO and SDA/ALCPDN pin during not using I2C interface, by ALC and MONO registers during using I2C interface.

Pin			Register		Path
I2CEN	SDA/ALCPDN	SCL/MONO	{ALC}	**{MONO}**	Path Case 1) & 2)
L	L	L	–	–	1) Input Signal → Gain Adj → Class-D Amp.
L	L	H	–	–	1) Input Signal → Gain Adj → Class-D Amp. (MONO)
L	H	L	–	–	2) Input Signal → ALC → Gain Adj → Class-D Amp.
L	H	H	–	–	2) Input Signal → ALC → Gain Adj → Class-D Amp. (MONO)
H	–	–	0	0	1) Input Signal → Gain Adj → Class-D Amp.
H	–	–	0	1	1) Input Signal → Gain Adj → Class-D Amp. (MONO)
H	–	–	1	0	2) Input Signal → ALC → Gain Adj → Class-D Amp.
H	–	–	1	1	2) Input Signal → ALC → Gain Adj → Class-D Amp. (MONO)

Figure 7: Path Cases

■ Level Diagram

Level diagram is shown in following figures, according to above Path cases.

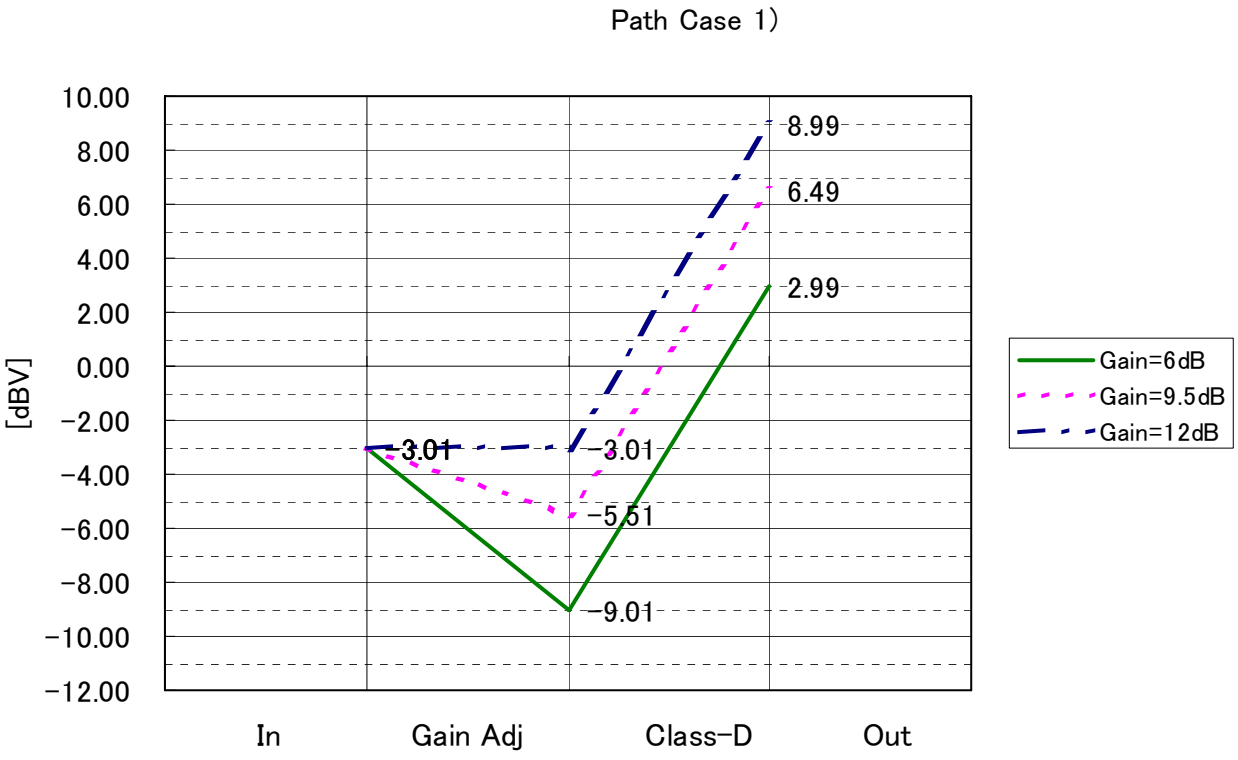


Figure 8: Level Diagram, Path Case 1)

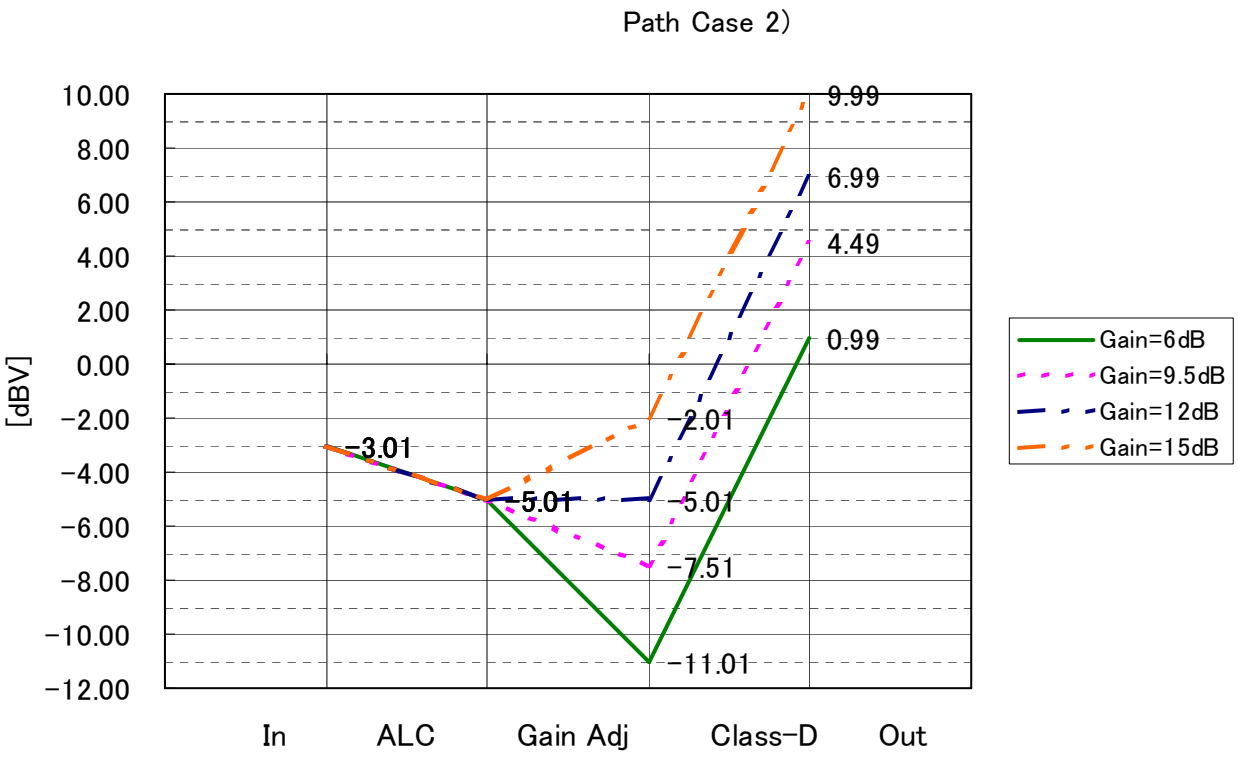


Figure 9: Level Diagram, Path Case 2)

■ Serial Control Interface (I2C-bus Interface)

AK7832A supports both standard mode (max. 100kHz) and high-speed mode (max. 400kHz).
Turn I2CENpin “H” when using I2C control registers.

Data transfer

All commands are preceded by the START condition. After the START condition, a slave address (1 byte) will be sent. After AK7832A recognizes the START condition, the device interfaced to bus waits for the slave address that is transmitted through SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to “Low” (ACKNOWLEDGE).
The data transfer is always terminated by STOP condition generated by the master device.

The data on SDA line must be stable during the “High” period of clock (SCL). The “High” or “Low” state of data line can only change, while the clock signal on SCL line is “Low” except for the START and STOP condition.

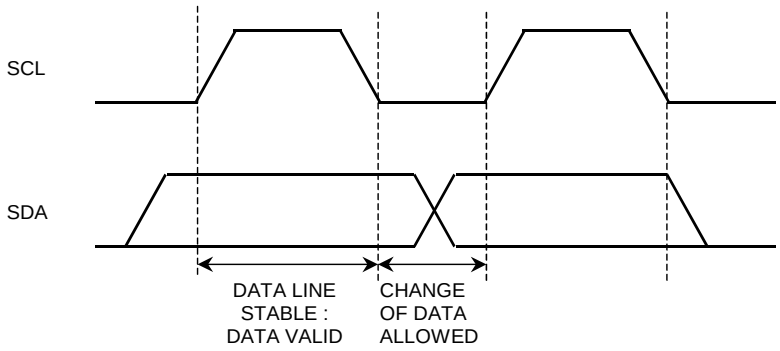


Figure 10: Data Change

START and STOP conditions

A “High” to “Low” transition on SDA line while SCL is “High” indicates START condition.
All sequences start from the START condition.
A “Low” to “High” transition on SDA line while SCL is “High” indicates STOP condition.
All sequences end by the STOP condition.

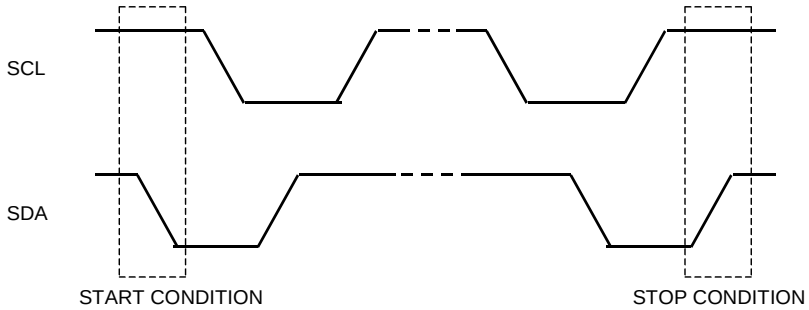


Figure 11: START and STOP conditions

Acknowledge

Acknowledge is a convention used to indicate successful data transfers.
The transmitting device will release SDA line (“High”) after transmitting eight bits. The receiver must pull down the SDA line to “L” while the clock pulse for Acknowledge is “High” in order to generate Acknowledge. The receiver will generate Acknowledge after each byte has been received.
During read mode, AK7832A will transmit eight bits of data, release the SDA line and monitor the line for Acknowledge. If it is detected, the slave (AK7832A) will continue to transmit data. If it not detected, the slave will terminate further data transmissions and wait for the STOP condition.

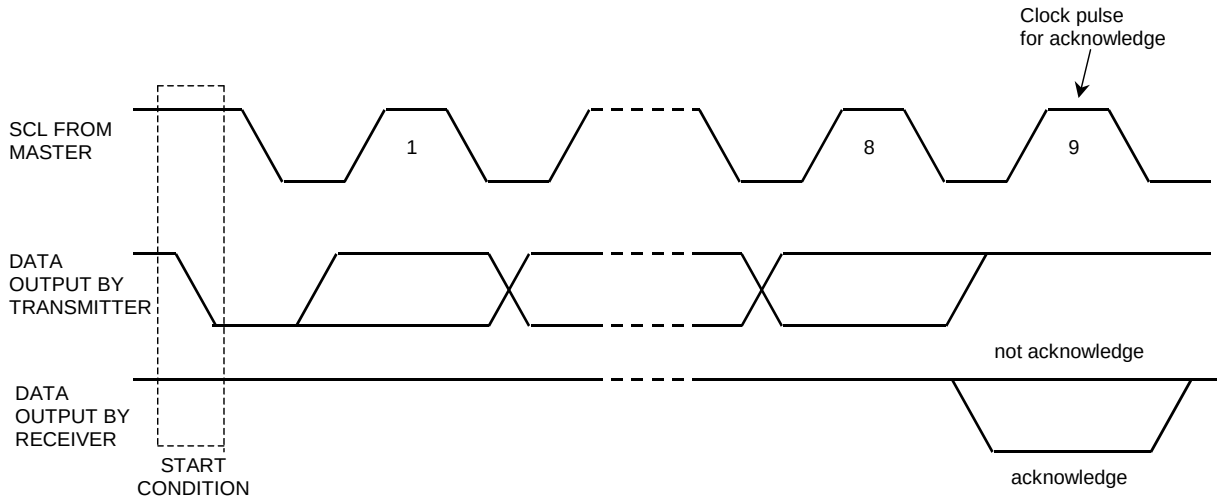


Figure 12: Generation of Acknowledge

Slave Address

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address of one of the devices alongside the BUS, the receiver that has been addressed pulls down the SDA line.
The most significant seven bits of the slave address are fixed as “0010000”.
The eighth bit (LSB) of first byte (R/W bit) defines whether the master requests a write or read condition. “1” = Read, “0” = Write.

MSB							LSB
0	0	1	0	0	0	0	R/W

Figure 13: Slave Address

(1) Write Operations

Set R/W bit to “0” for the WRITE operation of AK7832A.
After receiving the start condition and the first byte (slave address), AK7832A generates Acknowledge, and waits for the second byte (register address). The second byte consists of the address for control registers of AK7832A. The format is in MSB first, and the most significant three bits are “Don’t care”.

MSB							LSB
*	*	*	A4	A3	A2	A1	A0

(*: Don’t care)

Figure 14: Register Address

After receiving the second byte (register address), AK7832A generates an Acknowledge, and waits for the third byte. Those data after the second byte will be control data. The format is in MSB first, 8bit.

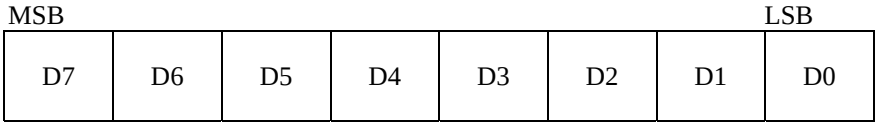


Figure 15: Control Data

AK7832A is capable of more than one byte write operation with in one sequence.
After receiving the third byte (control data), AK7832A generates an Acknowledgement, and waits for the next data. The master can transmit more than one word at a time without terminating the write cycle after the first data word is transferred. After receiving each data, the internal 6bit address counter is incremented by one, and the next data is taken into next address automatically.
If the address exceeds “09h” prior to generating the stop condition, the internal address counter will roll over to “00h” address and the previous data will be overwritten.

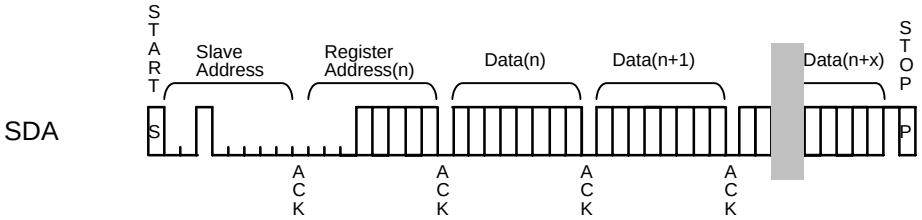


Figure 16: WRITE Operation

(2) READ Operations

Set R/W bit to “1” for the READ operation of AK7832A.
After transmission of a data, the master can read the next address by generating the Acknowledge instead of terminating the write cycle after receiving the first data word. After the receiving of each data, the internal 6bit address counter is incremented by one, and the next data is taken into next address automatically.
If the address exceeds “09h” prior to generating the stop condition, the internal address counter will roll over to “00h” address and the previous data will be read.

AK7832A supports two basic read operations (**CURRENT ADDRESS READ** and **RANDOM READ**).

CURRENT ADDRESS READ

AK7832A contains an internal address counter that maintains the address of last word accessed, incremented by one. For example, if the last access (either a read or write) had addressed n, the next CURRENT READ operation would access data from the address n+1.
After receiving the slave address with R/W bit set to “1”, AK7832A generates Acknowledge and transmits 1byte of data which address is set by the internal address counter and increments the internal address counter by 1.
If the master does not generate an Acknowledge to the data but generates the stop condition, AK7832A discontinues transmission.

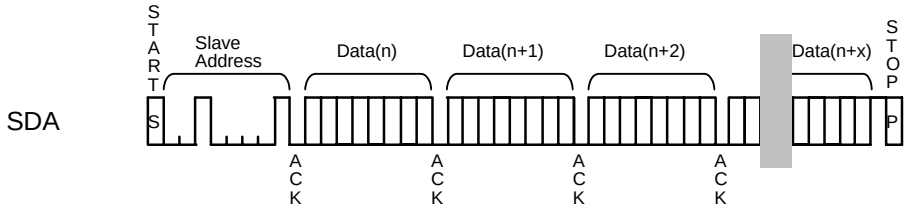


Figure 17: Current Address READ

RANDOM READ

Random read operation allows the master to access any memory location randomly.

Prior to issuing the slave address with R/W bit set to “1”, the master must perform a “dummy” write operation. The master issues the start condition, slave address (R/W=“0”), and then the register address to read. After the register address’s Acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to “1”. Then AK7832A corresponds to the slave address by generating Acknowledge, and output the designated address data, then increments the internal address counter by 1.If the master does not generates Acknowledge to the data but generates the stop condition, AK7832A discontinues transmission.

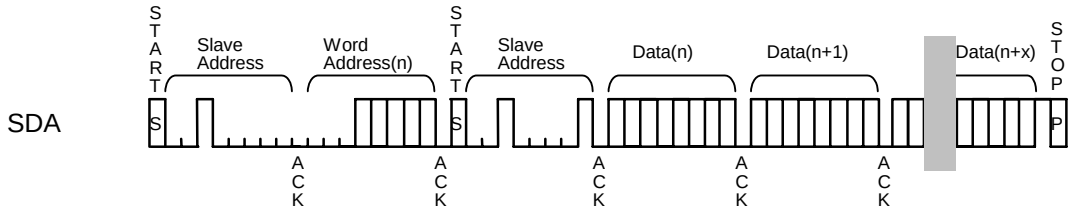


Figure 18: Random READ

■ ALC Block

ALC block is active while ALC bit = “1”(while I2CENpin =”H”) or SDA/ALCPDN pin =”H” (while I2CEN pin =”L”). Otherwise ALC block will not be active and bypassed. (Figure 7)

(1) ALC Limiter Operation

➢ **In the case of zero cross detection is not active (ZELMN=”1”)**

When the output level exceeds ALC limiter detection level (LMTHP), it begins to be attenuated every 128μs until it will be in between following 2dB range.

“(Recovery waiting counter reset level) ≦ Output Signal < (Limiter detection level)”

Then, ATT level (attenuation step) is 0.5dB per one step regardless of LMATP[1:0], registers for attenuation step.

While output level is in the 2dB range, limiter function does not operate. After finishing limit operation, if output signal exceed the limiter detection level (LMTHP), output signal begin to be attenuated as the same process above.

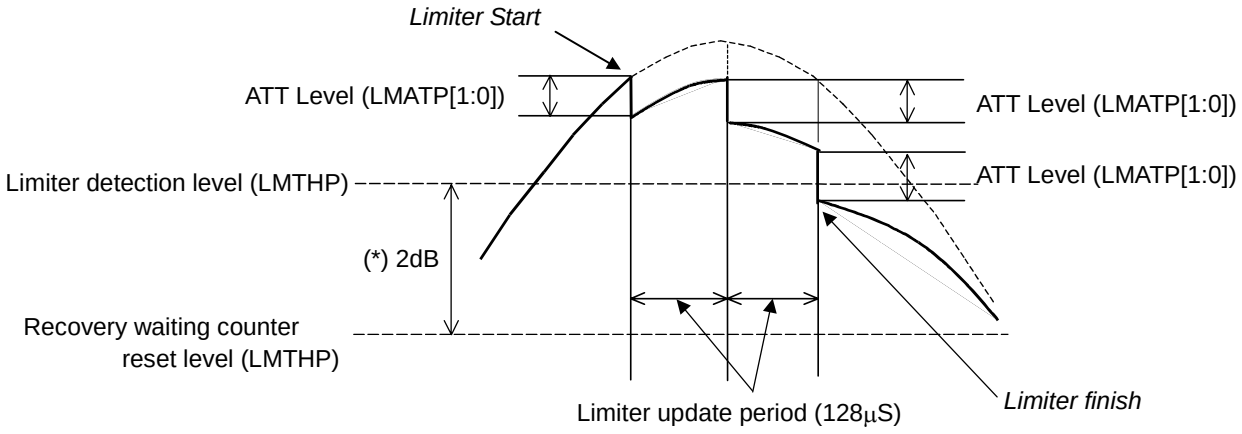


Figure 19: ALC Limiter operation [When zero cross detection is disabled (ZELMN=”1”)]

(*) Range of Both limiter and recovery function is halted.

- **In the case of zero cross detection is active (ZELMN="0")**

  Zero cross time out is changeable by setting ZTM[1:0] bit.
  Output level is attenuated when it cross zero level (L/Rch zero cross detection is independent of each other). Even if zero cross is not detected within ZTM[1:0] period, attenuation will also be carried out simultaneous with the ending of the zero cross time out.

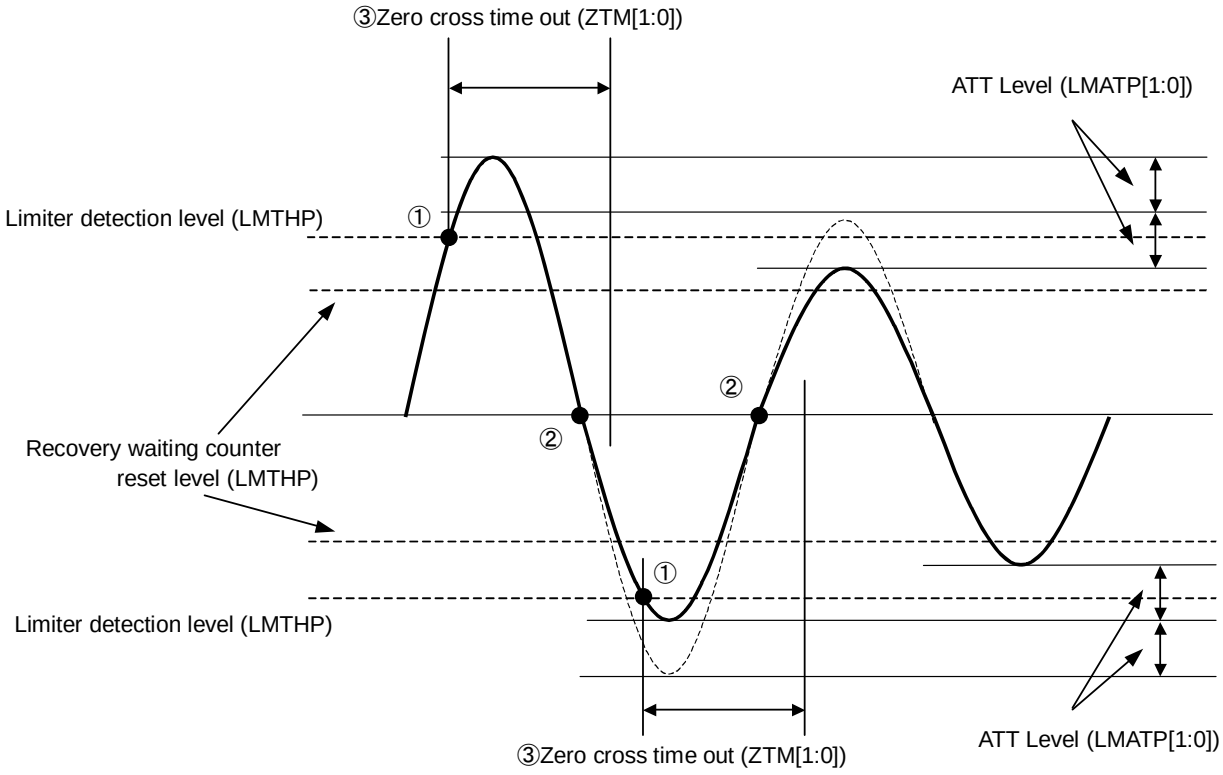


Figure 20: Continuous limiter operation (While ZELMN="0")

① Every time output signal exceed the limiter detection level, a zero cross counter as well as the limiter function begin to operate.

② The zero cross detection. As soon as detecting zero cross, output signal will be attenuated according to the value of ATT level (LMAT[1:0]) and limiter will be halted.

③ Zero cross time out is changeable by setting ZTM[1:0] bit, however, the first zero cross time out in a continuous limiter operation may be shorter than the time set by ZTM[1:0]. (e.g. where limiter is carried out during recovery operation.)

(2) ALC Recovery Operation

Zero cross detection and zero cross transition are always active during ALC recovery operation.
Once output level becomes less than “Recovery waiting counter reset level”, the ALC recovery operation begins. But it waits for a “Recovery waiting time” which is set by WTMP[1:0]. And if the output signal does not exceed the “Recovery waiting counter reset level” during that period, the output level begins to be increased up to the reference level (REFP[5:0]) or to the “Limiter detection level”.

A period of the recovery is “Recovery waiting time (WTMP[1:0])” and a step (dB) is set by RGAINP bit (Refer to latter part).

In the recovery operation, as soon as output level exceeds the “Limiter detection level”, ALC limiter operation will be carried out. Or as soon as the output level move into following condition, recovery waiting time is reset (=recovery operation is halted).

“(Recovery waiting counter reset level) ≦ Output Signal < (Limiter detection level)”

Restart of the recovery is after the output level move to “(Recovery waiting counter reset level)> Output Signal“ next time.

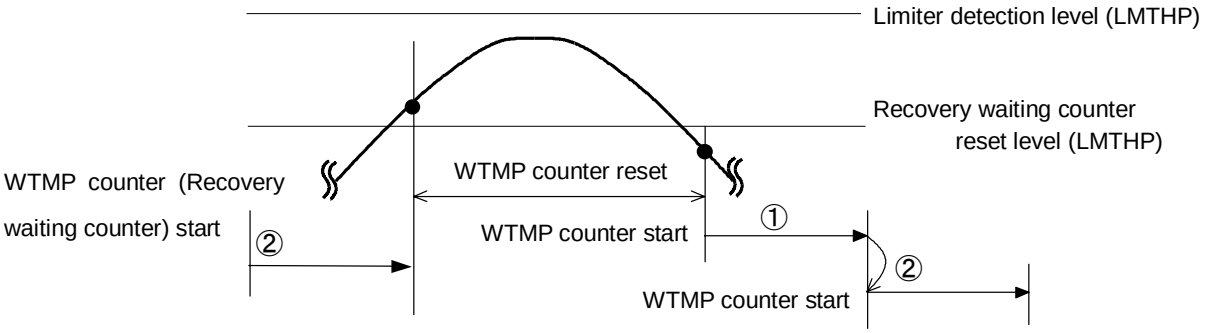


Figure 21: ALC recovery waiting counter

① Once output level becomes less than “Recovery waiting counter reset level”, the ALC waits for a “Recovery waiting time” which is set by WTMP[1:0].
② If the output level does not exceed the “Recovery waiting counter reset level” during WTMP, output level is increased one step according to RGAINP bit. Then WTMP counter starts again.

Zero cross detection and zero cross transition are always active during ALC recovery operation.
Output level is increased when it cross zero level (L/Rch zero cross detection is independent of each other). Even if zero cross is not detected within ZTM[1:0] period, recovery will also be carried out simultaneously with the ending of the zero cross time out.

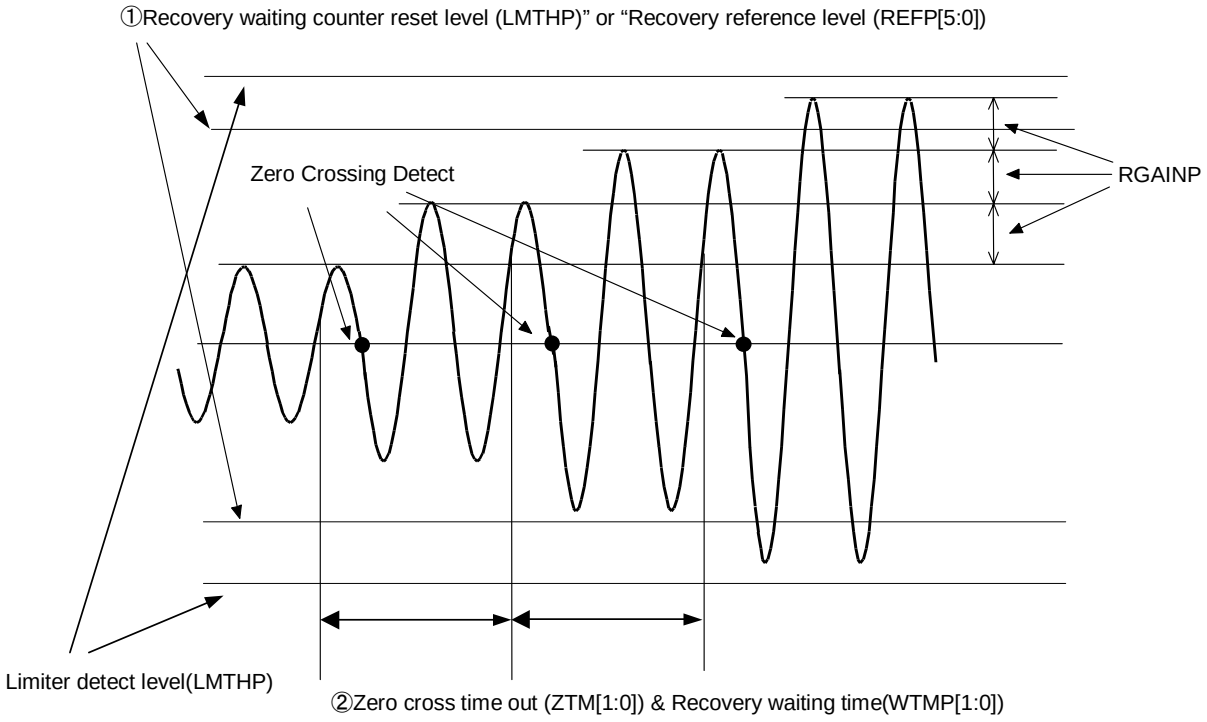


Figure 22: Continuous recovery operation

① Once output level go beyond "Recovery counter reset level", recovery is halted. Restart of the recovery is after the output level move to "(Recovery waiting counter reset level)> Output Signal " next time.

② ZTM[1:0] sets "Zero cross time out" period and WTMP[1:0] sets "Recovery waiting time" (= Recovery period)
Be sure to set "WTMP[1:0] ≧ ZTM[1:0]" as zero cross time out has a priority over the "Recovery waiting time". Recovery period would not be stable when "ZTM[1:0] > WTMP[1:0]" and zero cross is not detected during ZTM[1:0] period.

(3) ALC – Input/Output characteristics

Followings are “ALC Input/Output characteristics” when input signal level is swept both ALC is turned-on and turned-off.
“Full Scale level (“FS”)” descrived in the following figures are calculated;

2.0Vpp （=0.707Vrms）×（Gain setting by {PRGAIN[1:0]}）

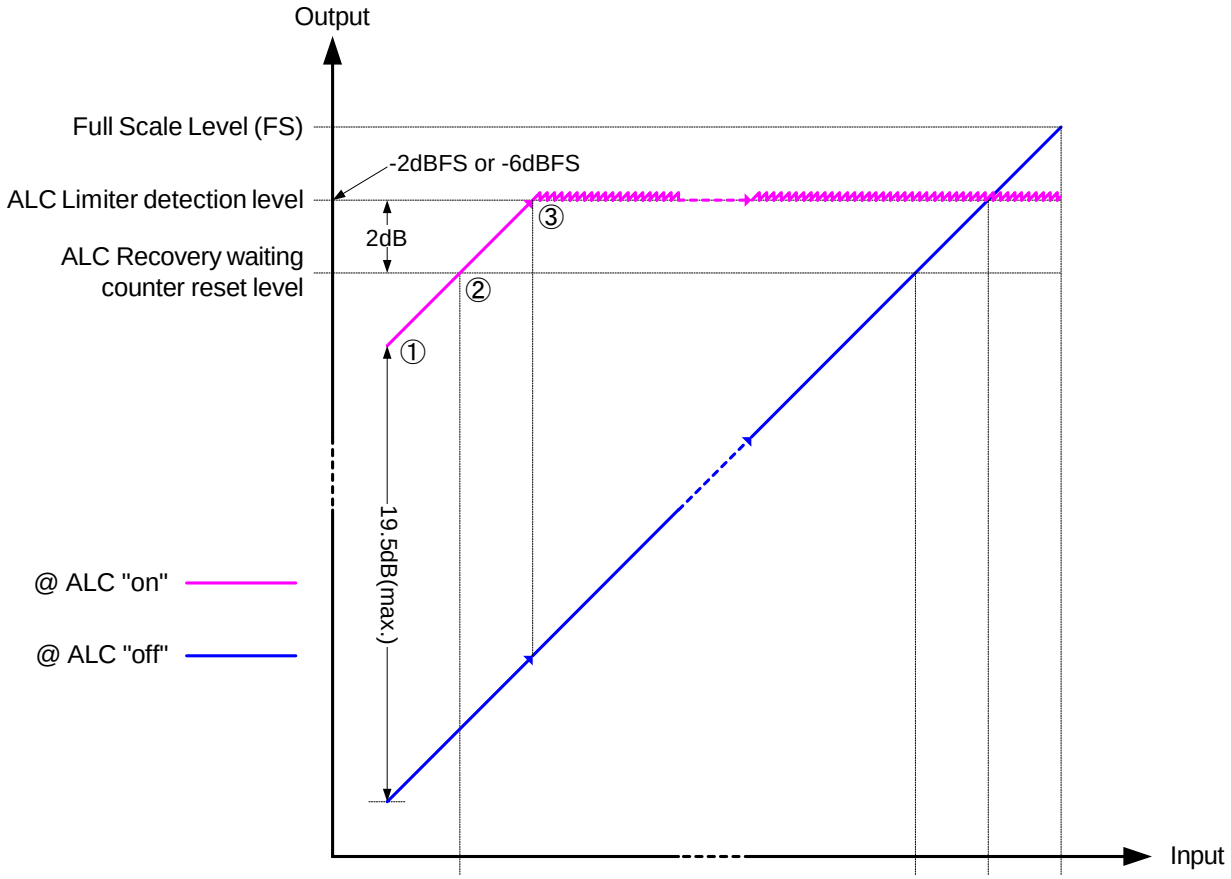


Figure 23: Input/Output characteristic (1)

Figure 23 shows Input/Output characteristic when sweeping Input signal level from minimum to maximum.

① At this point, as an output signal level is below “ALC recovery waiting counter reset level”, then ALC recovery operation is applied. Accordingly, output signal level increases up to the reference level set by REFP[5:0] (max. +19.5dB). This operation continues during ① to ②.

② At a period during ② to ③, as an output signal level is; “(Recovery waiting counter reset level) ≦ Output Signal < (Limiter detection level)”, both limiter and recovery operation are halted. Output signal form follows its input.

③ When output signal level stands at “ALC Limiter detection level”, ALC limiter operation is applied. Accordingly, output signal level keeps going below “ALC Limiter detection level”.

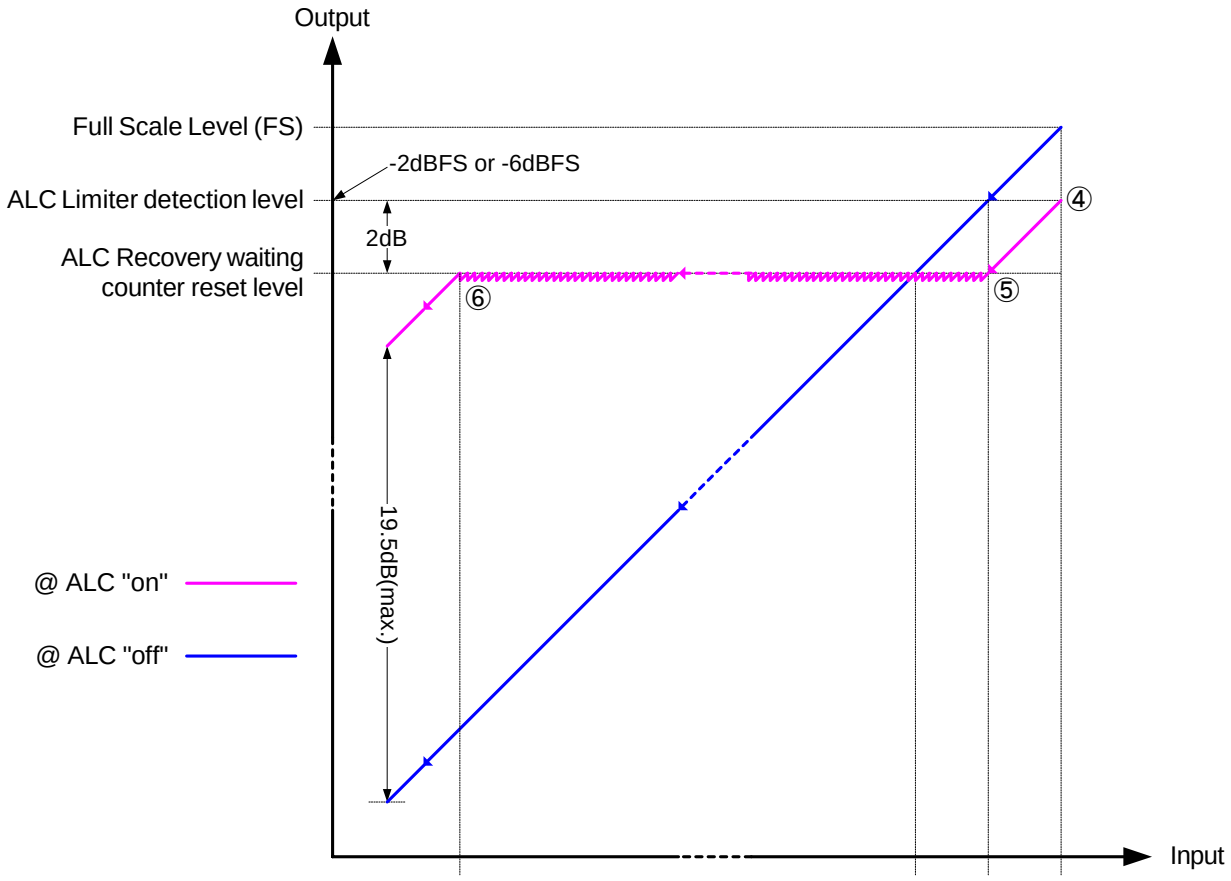


Figure 24: Input/Output characteristic (2)

Figure 24 shows Input/Output characteristic when sweeping Input signal level from maximum to minimum.

④ At this point, as an output signal level is over “ALC limiter detection level”, then ALC limiter operation is applied. Accordingly, output signal level is limited to “ALC limiter detection level”.

⑤ At a period during ④ to ⑤, as an output signal level is; “(Recovery waiting counter reset level) ≦ Output Signal < (Limiter detection level)”, both limiter and recovery operation are halted. Output signal form follows its input.
When output signal level stands at “ALC recovery waiting counter reset level”, ALC recovery operation is applied. Accordingly, output signal level keeps going “ALC recovery waiting counter reset level”. (⑤→⑥)。

⑥ When a difference between input signal level and “ALC recovery waiting counter reset level” exceeds the reference level set by REFP[5:0] (max. +19.5dB), ALC recovery operation is suspended and output signal level decays following input signal level decrease.

(4) Impulse-like Noise Detection and Fast Recovery

ALC function of AK7832A corresponds to impulse-like noise for example applause, fireworks, gunshots and so on. Recovery speed will be four or eight times faster than normal when impulse-like noise is input.

Fast recovery mode can be set ON/OFF by adress07h: {ALCCTRL4[FR]} bit.
Recovery speed of Fast recovery is changeable by 07h: {ALCCTRL4[FRSEL]} bit.

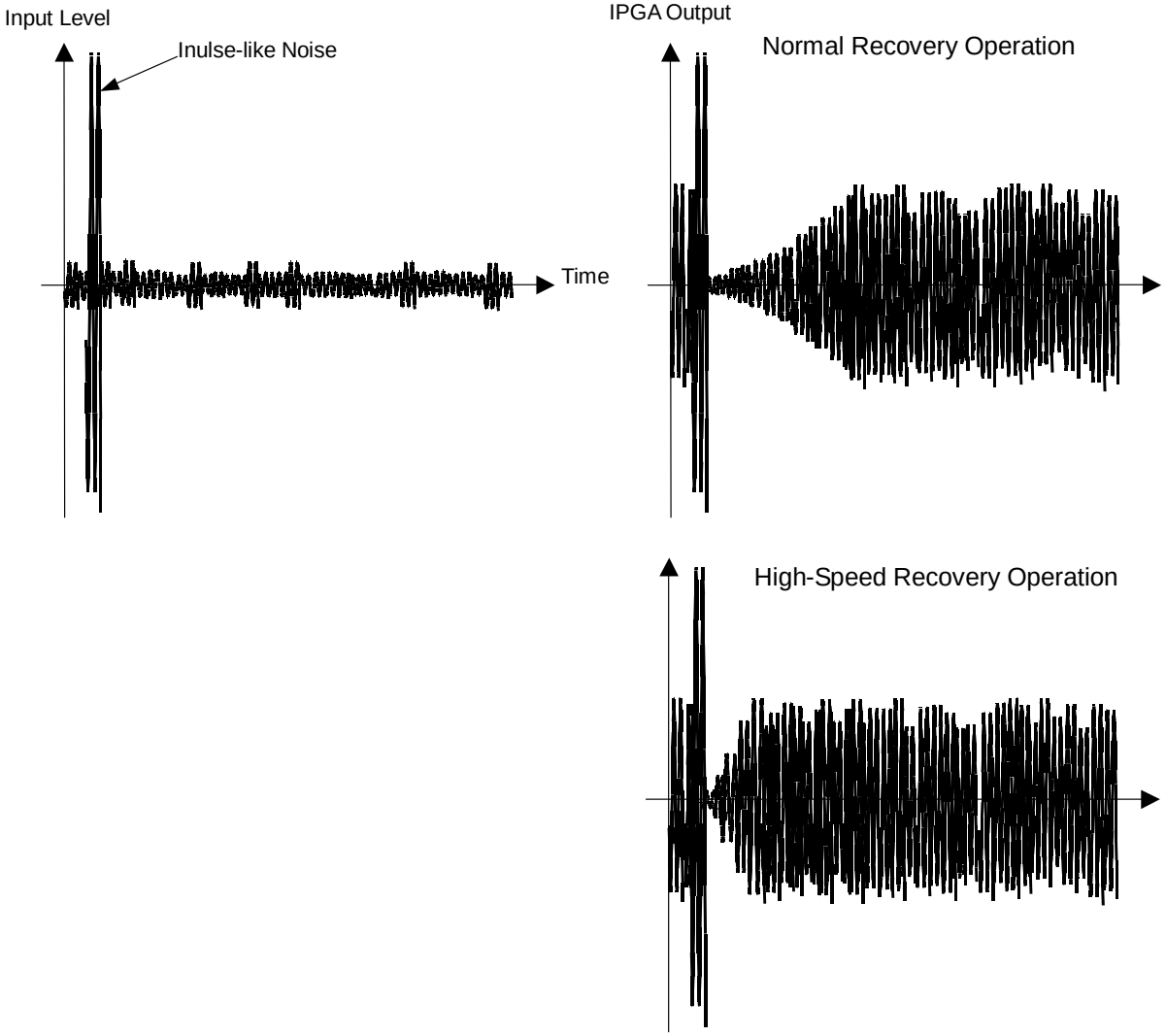


Figure 25: Fast and Normal Recovery

ALC block has a reference value for Impulse noise detection, which changes RAGAIN (ALC recovery gain step) per step, at a period of WTMP[1:0](ALC recovery waiting time).

① When Impulse like noise is detected, limiter operation begin and lower the ALC gain rapidly.

② Reference value follows ALC gain but can change one step at every period. Fast recovery starts when the difference between Reference value and ALC gain is 9 or 17 steps

Impulse-like noise detection level is set by 07h: {ALCCTRL4[GAPSEL]} bit.
Normal recovery restart as soon as ALC gain has become the same as value as Reference value.

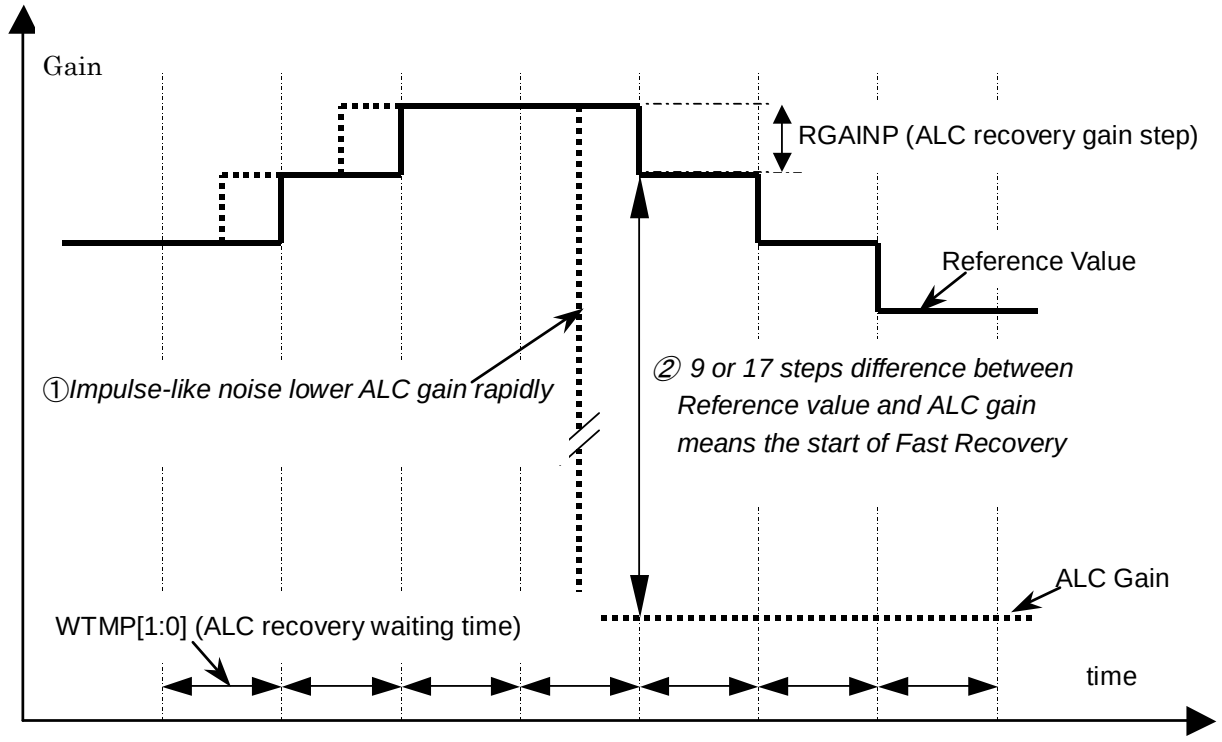


Figure 26: Impulse-like Noise Detection

(5)ALC setting example

Figure 27 shows an example of ALC setting. The default ALC gain is 0dB.

Register Name	Comment	Data	Note
LMTHP	Limiter detection Level	1	-6dBFS
ZELMN	Limiter Zero crossing Enable	0	Enable
WTMP[1:0]	ALC Recovery Time	00	32ms
REFP[5:0]	Maximum gain at recovery operation	30h	+12dB
LMATP[1:0]	Limiter ATT Step	00	0.5dB
ZTM[1:0]	Zero Crossing Time-out	00	32ms
RGAINP	Recovery GAIN Step	0	0.5dB
ALC	ALC Enable bit	1	Enable

Figure 27: ALC Configuration example

Note 25: Do not change registers below while ALC is active.
These bits must be changed after stopping ALC (ALC bit="0").
(Refer to flowchart Figure 6)

LMTHP, LMATP[1:0], WTMP[1:0], RGAINP, REFP[5:0], ZTM[1:0], ZELMN, FR, FRSEL, GAPSEL

Performance characteristics

※ The following various characteristics are typical characteristic data in the typical condition. It is not the one necessarily to secure the characteristic of the description.

Input Signal=1kHz, Sinwave Single - ended, ALC=OFF,
Measurement Band Frequency = 20～20 kHz,unless otherwise specified.

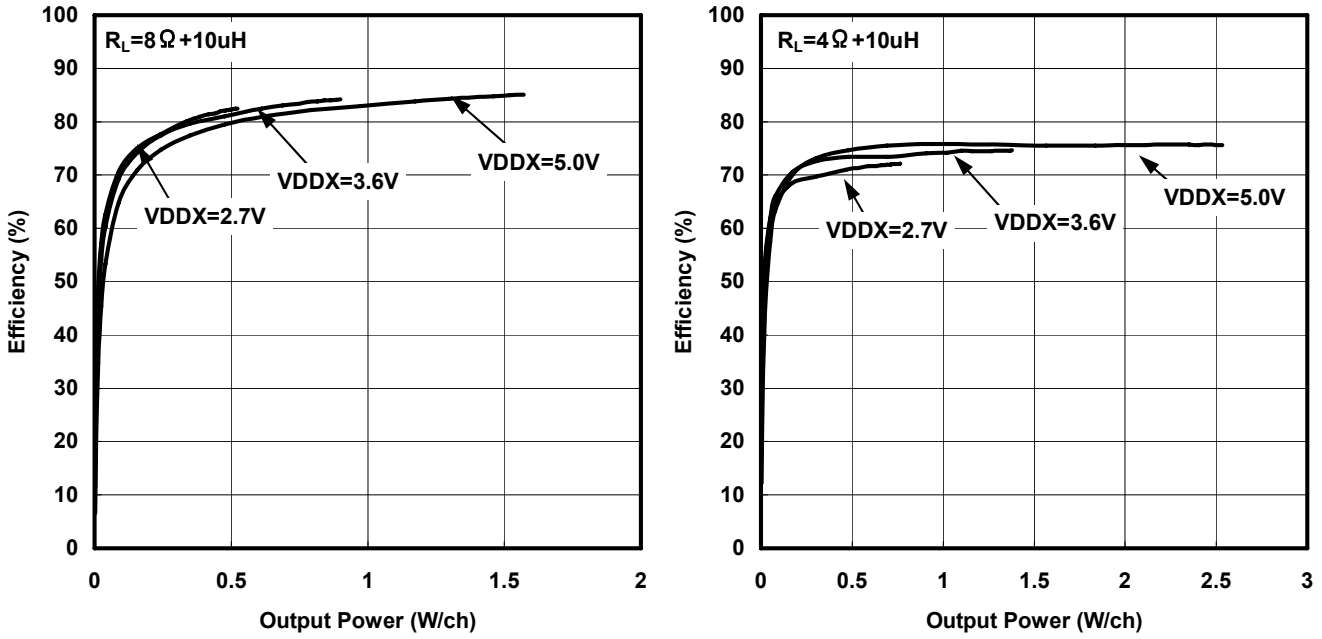


Figure 28: Output Power vs Efficiency

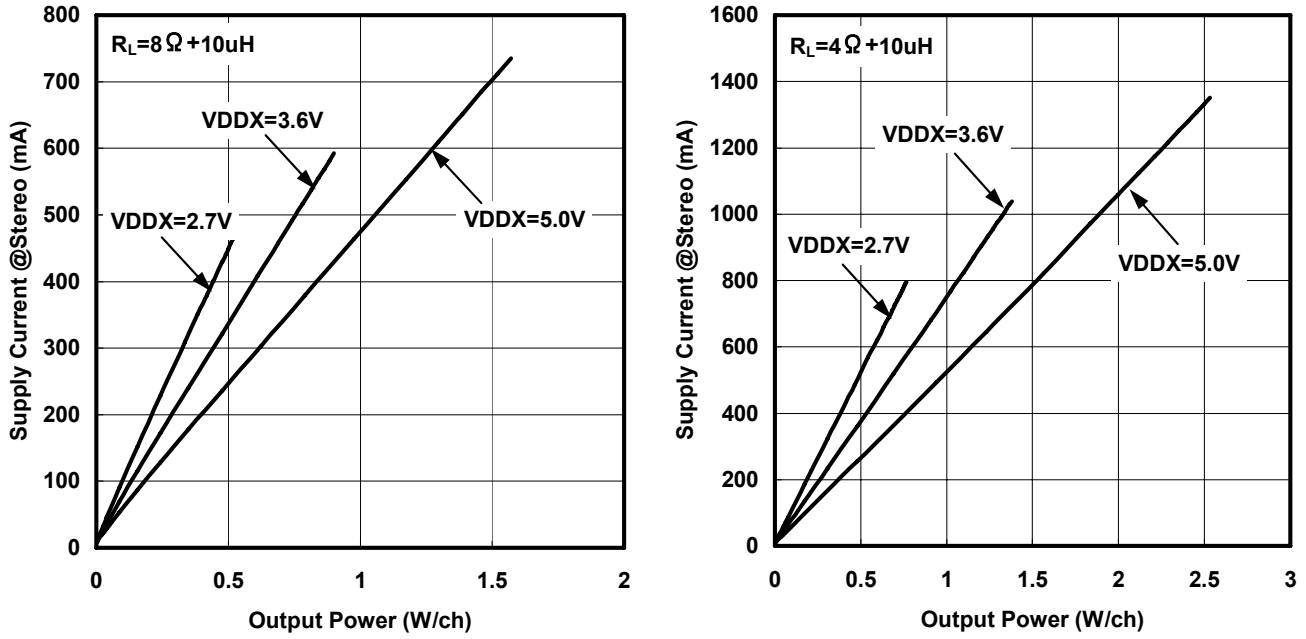


Figure 29: Output Power vs Supply Current

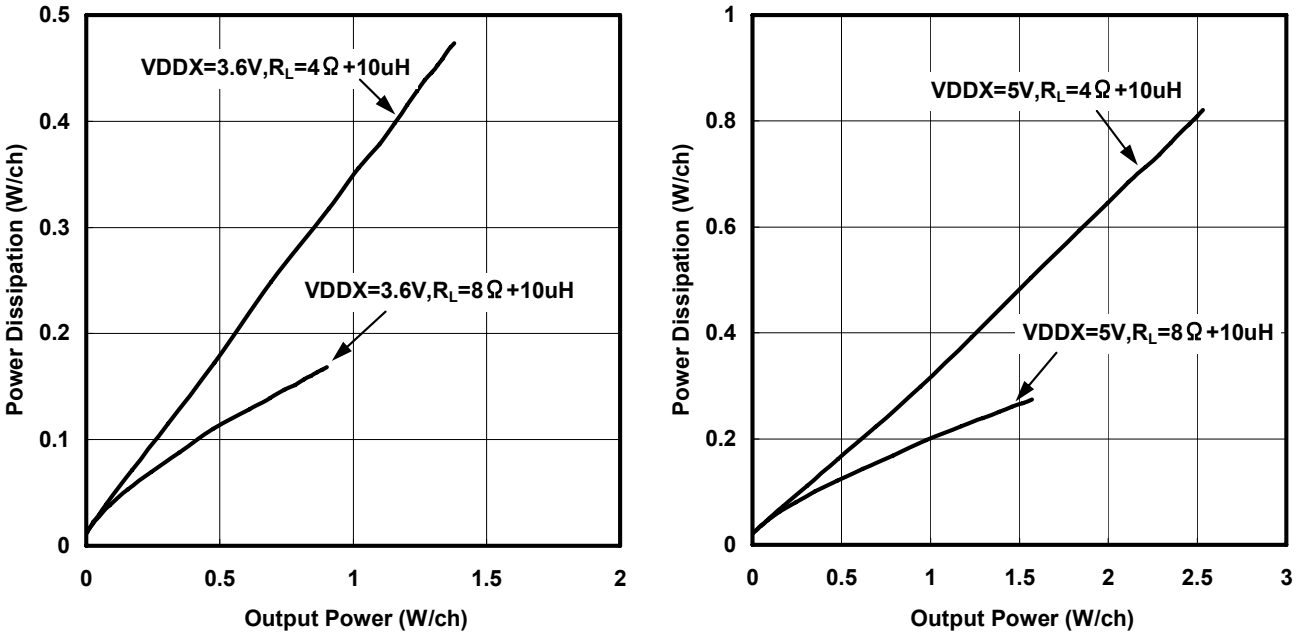


Figure 30: Output Power vs power Dissipation

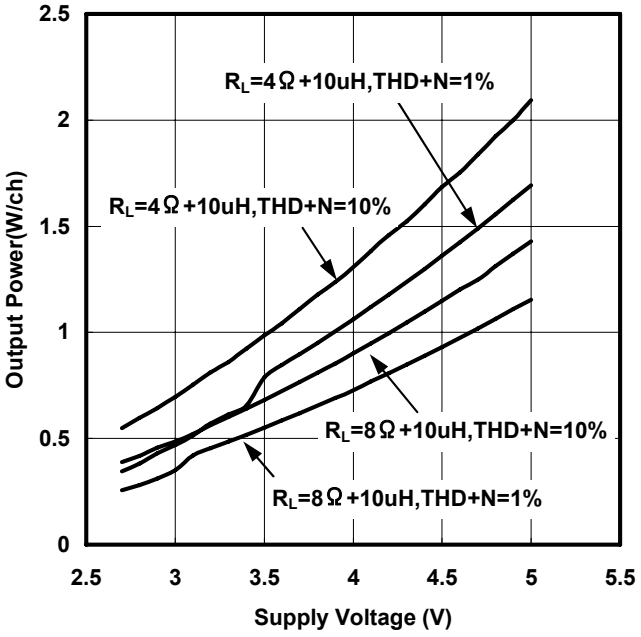


Figure 31: Output Power vs Supply Voltage

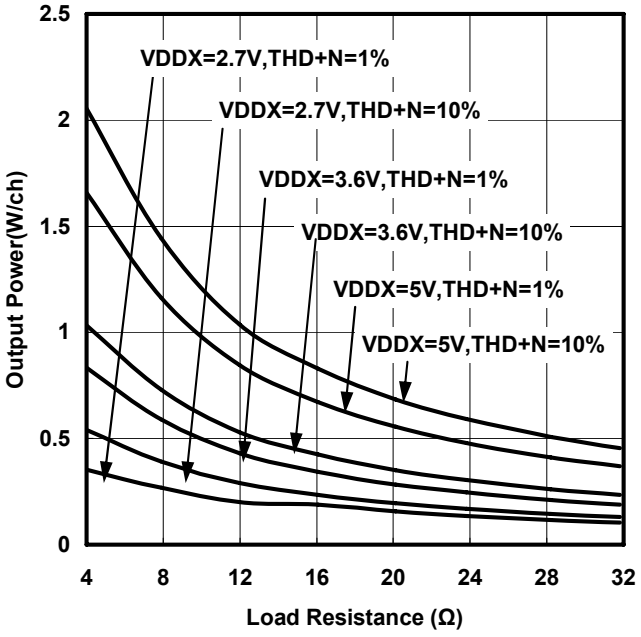


Figure 32: Output Power vs Load Resistance

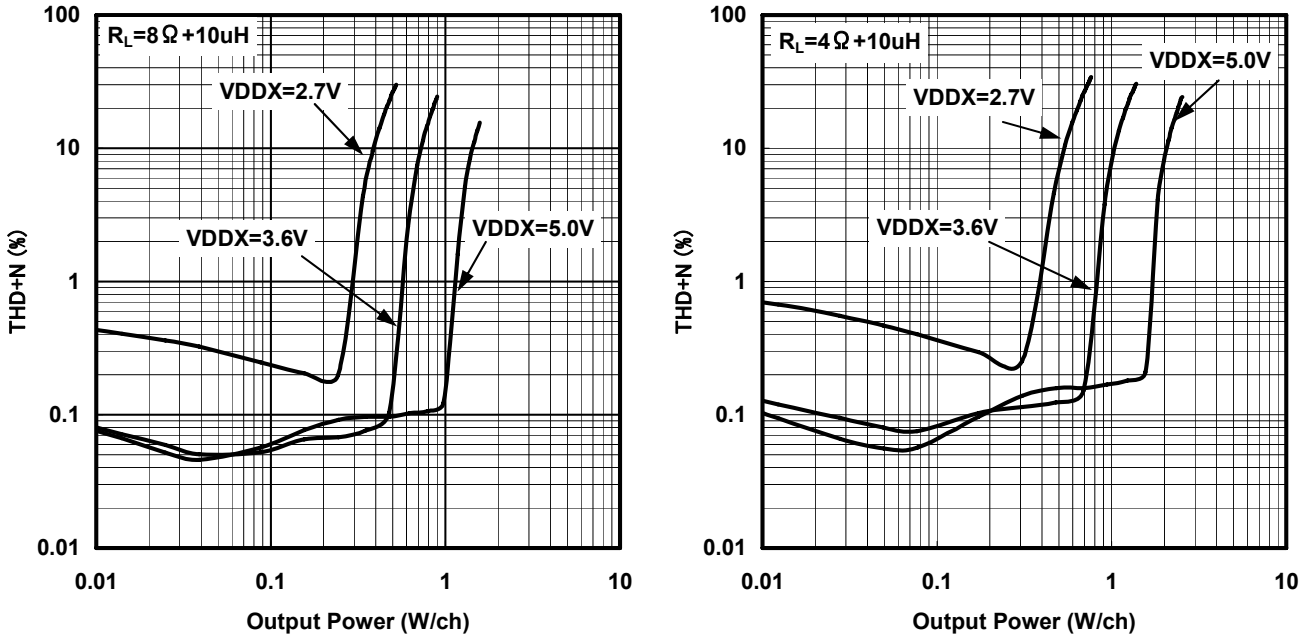


Figure 33: Output Power vs THD+N

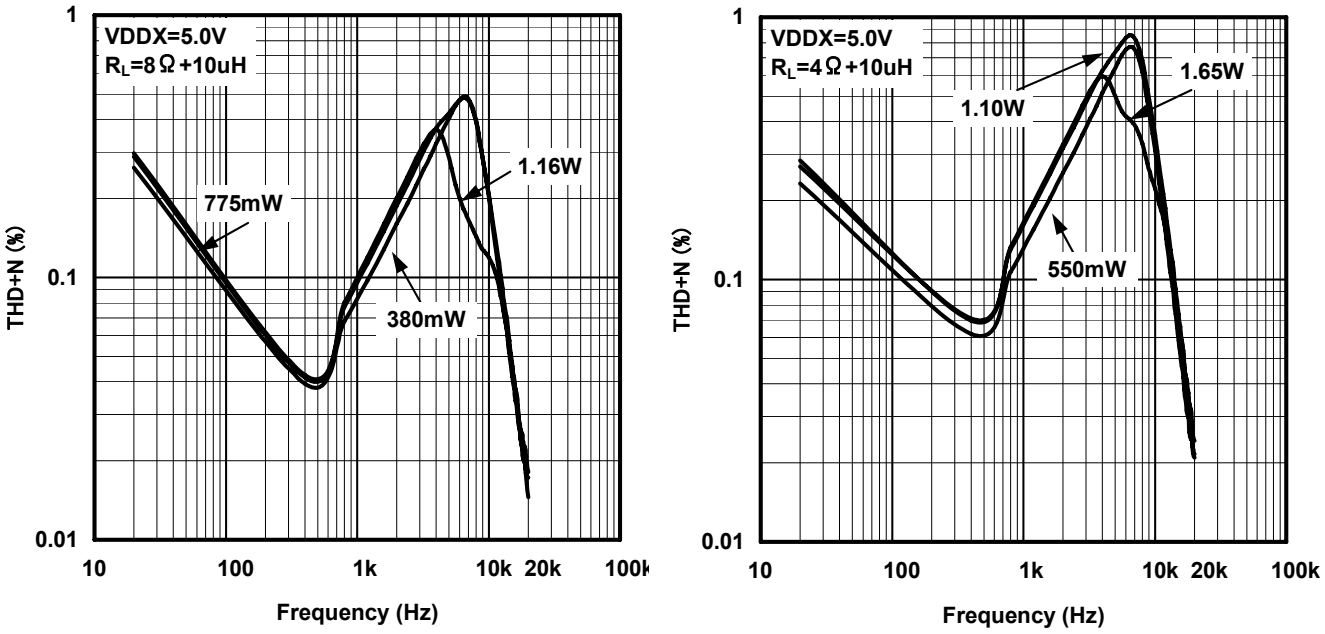


Figure 34: Frequency vs THD+N@VBAT=5V

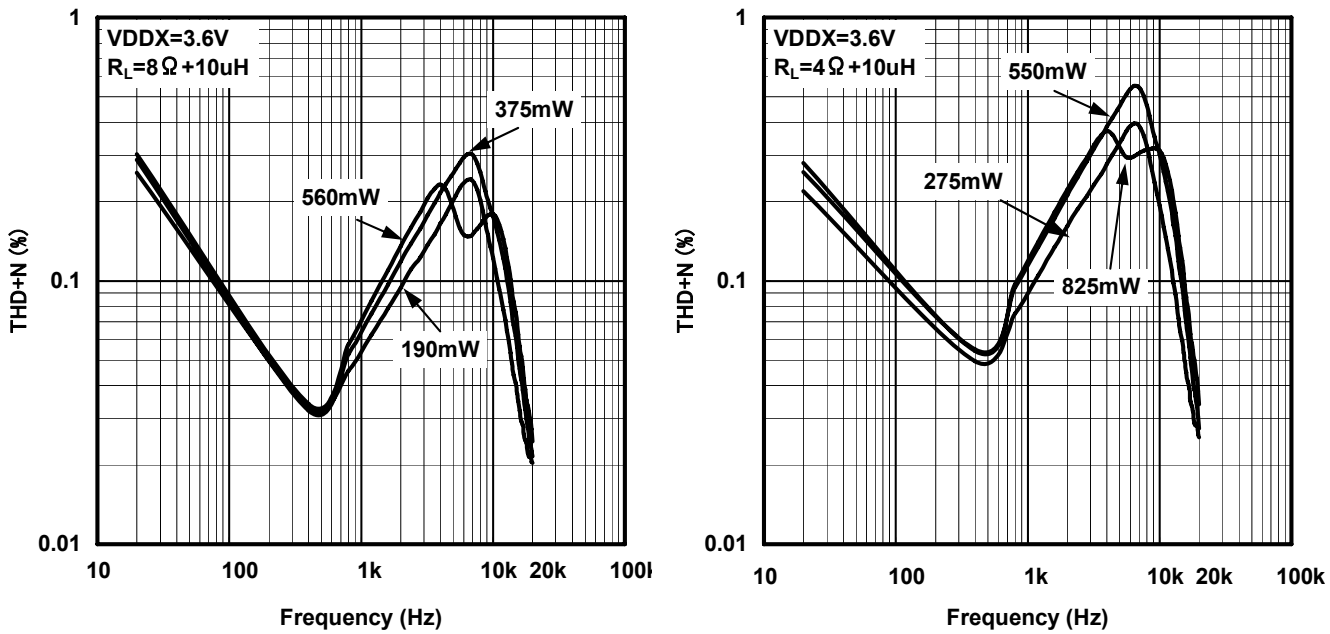


Figure 35: Frequency vs THD+N@VBAT=3.6V

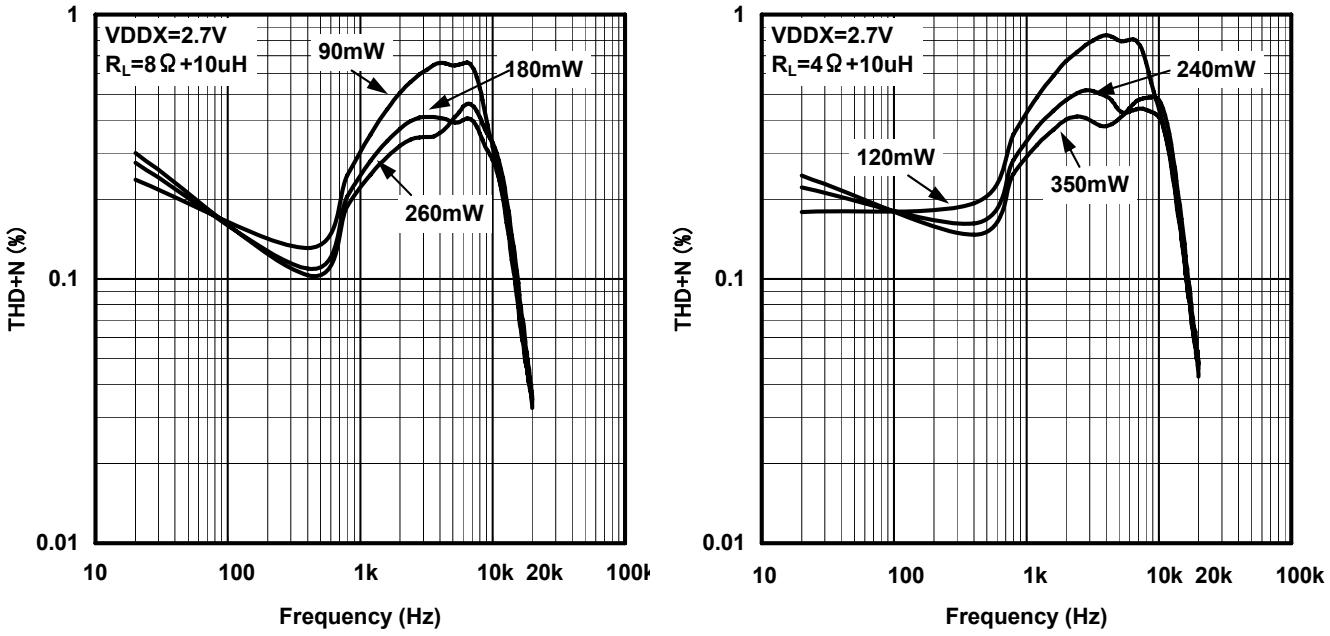


Figure 36: Frequency vs THD+N@VBAT=2.7V

Registers

■ Register Map

(Note 26), (Note 27), (Note 28)

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	(Reserved)	–	–	–	–	–	–	–	–
01h	SYSRST	SRST							
02h	PDNMODE	0	0	0	0	0	0	MONO	MUTEN
03h	PRGAIN	0	0	0	0	0	0	PG2	PG1
04h	ALCCTRL1	0	0	REFP5	REFP4	REFP3	REFP2	REFP1	REFP0
05h	ALCCTRL2	0	0	ZELMN	ZTM1	ZTM0	LMATP1	LMATP0	LMTHP
06h	ALCCTRL3	ALC	0	GAPSEL	FRSEL	FR	WTMP1	WTMP0	RGAINP
07h	(Reserved)	0	0	0	0	0	0	0	0
08h	(Reserved)	0	0	0	0	0	0	0	0
09h	(Reserved)	0	0	0	0	0	0	0	0
10h	(TEST)	–	–	–	–	–	–	–	–
～	～	～							
1Dh	(TEST)	–	–	–	–	–	–	–	–

Note 26: PDN pin = “L” resets the registers to their default values.

Note 27: While multi-byte Write or Read operations; If the address exceeds “09h” prior to generating a stop condition, the internal address counter will roll over to “00h” address and the previous data will be overwritten or read.

Note 28: Addresses from “10h” to “1Dh” are registers for AKEMD device test. Do not access these registers at any time.

■ Detailed Register Settings

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	(Reserved)	–	–	–	–	–	–	–	–
Default		–	–	–	–	–	–	–	–

This address is reserved. To access this registers do not affect AK7832A operation.

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
01h	SYSRST	SRST							
Default		–							

SRST : Software reset

Writing arbitrary data into this register causes the software-reset and also all of the control registers of AK7832A will be reset to their initial value. The following diagram illustrates the software-reset timing. (Refer to Figure 6 as well)

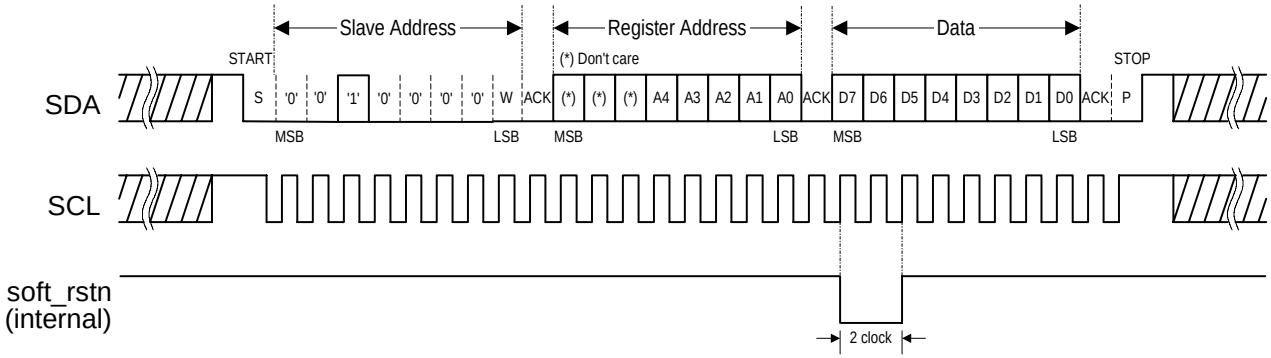


Figure 37: Software Reset Sequence

The register address is identified on the falling edge of the 8th SCL bit (A0). If it is “01h”, then an internal “soft_rstn” is generated on the rising edge of the first SCL bit (D7), during a 2-clock period (Normal mode: min. 20μs; High Speed mode: min. 5μs) for software reset. Internal counter is used for counting SCL number. This counter will be reset as soon as hardware reset is done by PDN pin.

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
02h	PDNMODE	0	0	0	0	0	0	MONO	MUTEN
Default		0	0	0	0	0	0	0	0

MUTEN: Output On/OFF
0: OFF (Default)
1: ON

Class-D amp is powered down while MUTEN=0
(Refer to Figure 6 about operation)

MONO: Mono/Stereo switching
0: Stereo (Default)
1: Mono

In the case of Mono mode, use only Lch. Rch is automatically powered down

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
03h	PRGAIN	0	0	0	0	0	0	PG2	PG1
Default		0	0	0	0	0	0	1	0

PG1, PG2: Gain adjustment
Pre Gain can be set as follows by combination of PG1 and PG2.

PG2	PG1	Gain [dB]
0	0	6
0	1	9.5
1	0	12
1	1	15

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
04h	ALCCTRL1	0	0	REFP5	REFP4	REFP3	REFP2	REFP1	REFP0
Default		0	0	0	1	1	0	0	0

REFP[5:0]: Gain Setting at ALC Recovery mode
ALC recovery gain is set by REFP[5:0]

REFP[5:0]	GAIN [dB]	
3Fh	+19.5	
3Eh	+19.0	
3Dh	+18.5	
3Ch	+18.0	
～	～	
19h	+0.5	
18h	0.0	(default)
17h	-0.5	
～	～	
02h	-11.0	
01h	-11.5	
00h	-12.0	

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
05h	ALCCTRL2	0	0	ZELMN	ZTM1	ZTM0	LMATP1	LMATP0	LMTHP
Default		0	0	0	0	0	0	0	0

LMTHP: ALC limiter detection level and recovery waiting counter reset level setting

LMTHP	ALC limiter detection level	ALC recovery waiting counter reset level
0	ALC Output ≥ -2dBFS	-2dBFS > ALC Output ≥ -4dBFS
1	ALC Output ≥ -6dBFS	-6dBFS > ALC Output ≥ -8dBFS

* "FS" = 2.0Vpp (0.707Vrms) × Gain setting {PRGAIN[1:0]}

LMATP[1:0]: ALC limiter attenuation step setting

ZELMN	LMATP1	LMATP0	ATT STEP	
1	X	X	1 step	0.5dB
0	0	0	1 step	0.5dB
0	0	1	2 step	1.0dB
0	1	0	4 step	2.0dB
0	1	1	8 step	4.0dB

ZTM[1:0]: ALC zero cross time out setting

ZTM1	ZTM0	ZERO CROSS TIMEOUT
0	0	32ms
0	1	65ms
1	0	524ms
1	1	1048ms

ZELMN: Zero cross detection ON/OFF while ALC limiter
0: ON (Default)
1: OFF

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
06h	ALCCTRL3	ALC	0	GAPSEL	FRSEL	FR	WTMP1	WTMP0	RGAINP
Default		0	0	0	0	0	0	0	0

RGAINP: ALC recovery gain step setting
0: 1step = 0.5dB(Default)
1: 1step = 1.0dB

WTMP[1:0]: ALC recovery waiting time setting

WTMP1	WTMP0	ALC RECOVERY TIME
0	0	32ms
0	1	65ms
1	0	524ms
1	1	1048ms

FR: Fast Recovery setting
0: Corresponding to Impulse-like noise(Default)
1: Normal recovery

FRSEL: Fast recovery speed against normal WTMP[1:0] and ZTM[1:0]
0: 4 times faster than normal (Default)
1: 8 times faster than normal

GAPSEL: Steps that the detection of Impulse-like noise need between the ALC gain and the Reference value
0: At or more than 9 steps (Default)
1: At or more than 17 steps

ALC: ALC ON/OFF setting
0: ALC OFF (Default)
1: ALC ON

(Refer to Figure 6 and Note 25 about operation.)

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
07h ～ 09h	(Reserved)	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0

These addresses are reserved. Users can Read/Write on here. Written values are read unalterably. Default values are all 0.

Address 07h~09h may be used for control AK7832A for the future.

Ad	Name	D7	D6	D5	D4	D3	D2	D1	D0
10h ～ 1Dh	(TEST)	–	–	–	–	–	–	–	–
Default		–	–	–	–	–	–	–	–

Addresses "10h" to "1Dh" are registers for AKEMD device test. Do not access these registers at any time.
AKEMD is not responsible for the outcome when users access these registers. (Note 28)

Typical Connection Diagram

■ Single-ended input

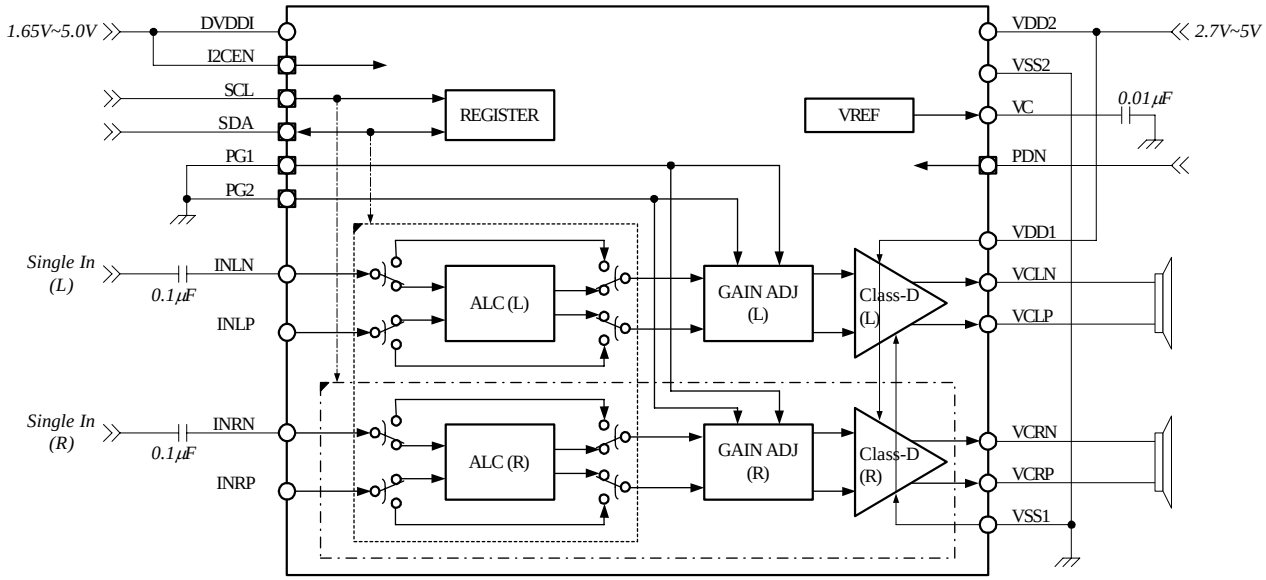


Figure 42: Single-ended Input (I2C Interface)

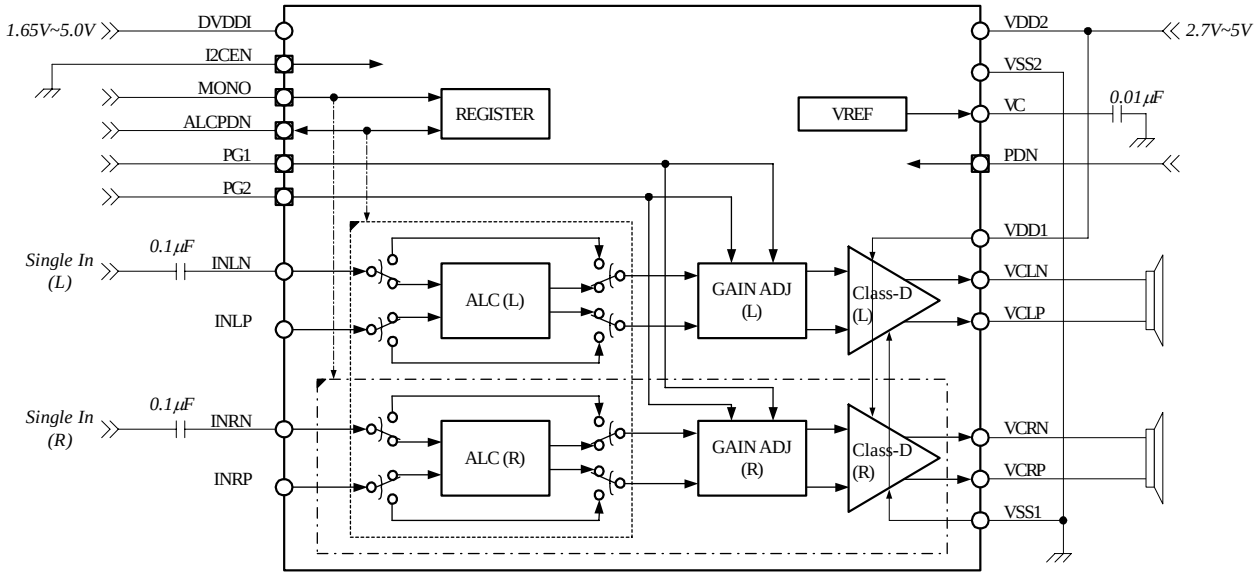


Figure 43: Single-ended Input (Pin control)

■ Differential input

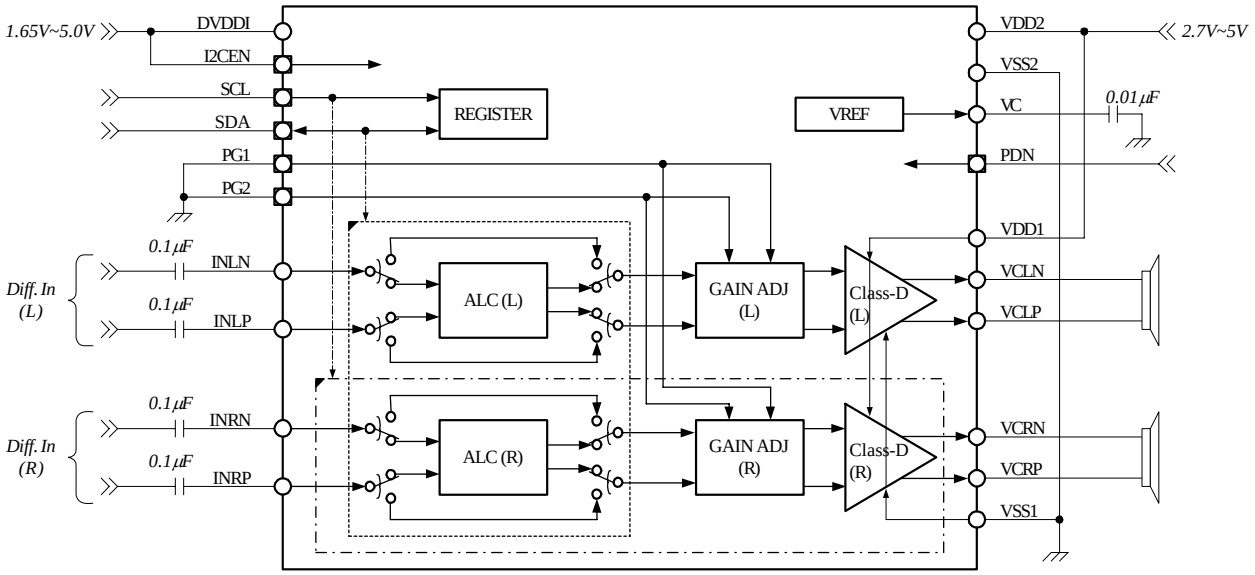


Figure 44: Differential Input (I2C Interface)

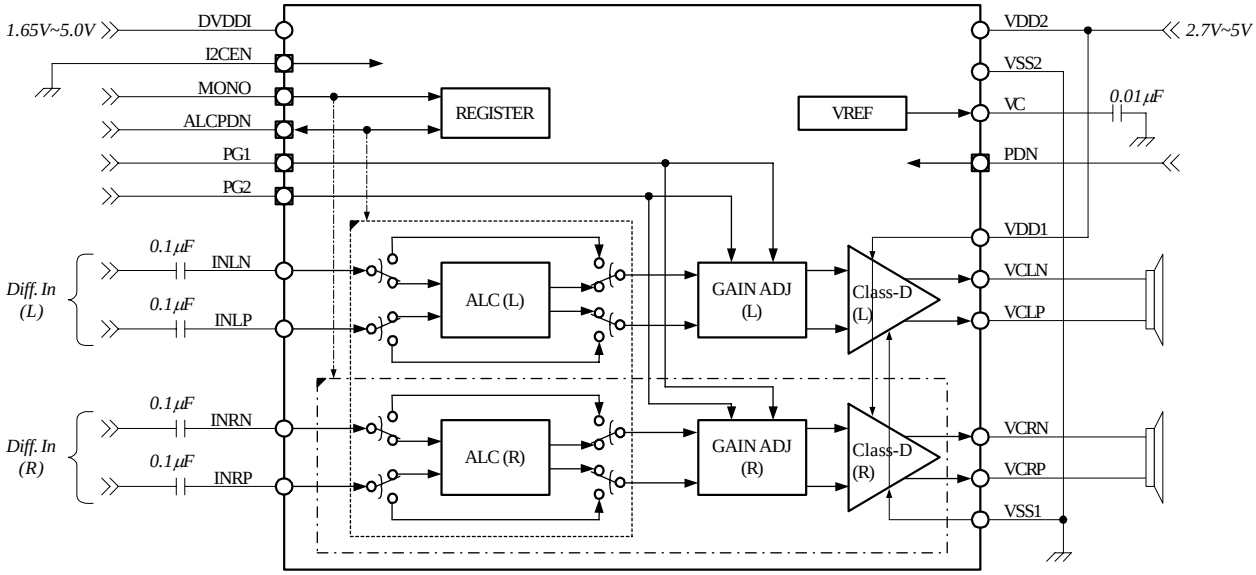


Figure 45: Differential Input (Pin control)

1. Grounding and Power Supply Decoupling

The AK7832A requires careful attention to power supply and grounding arrangements. Supply VDD1 and VDD2 with analog power supply. Connect VSS1 and VSS2 to the analog ground plane. System analog and digital ground should be isolated from each other and be connected nearby the power supply pin on the printed circuit board. Decoupling capacitors should be as close to VDD1 and VDD2 pin as possible.

2. Voltage Reference

VC is analog ground of this chip. Attach a 0.01μF ceramic capacitor between VC pin and VSS2 pin to eliminate high frequency noise. This capacitor should be as close to VC pin as possible. Do not take out load current from the VC pin. All digital signals, especially clocks, should be kept away from the VC pin in order to avoid unwanted coupling with VC pin.

3. Analog Inputs

During single-ended input, use INLN and INRN pins. (Figure42, Figure43)
Usually, DC component of input signal is supposed to be cut by a capacitor. (0.1μF is recommended.)
Note that, both INLP and INRP are sensitive to noise. Keep them away from signal/power line or connect capacitors that has the same value (0.1μF is recommended) as those of INLN and INRN side respectively, in between IN[L/R]P and the ground.
During differential input, use INLN/P, INRN/P pins. (Figure44, Figure45)
Also in this case, DC component of input signal is supposed to be cut by a capacitor. (0.1μF is recommended.)

4. Class-D Outputs

The Class-D outputs are in BTL signal format. Locate the outputs close to the speaker to minimize interconnect resistance and capacitance to suppress sound degradation. Match the length and pattern of the positive and negative output interconnect.

PACKAGE

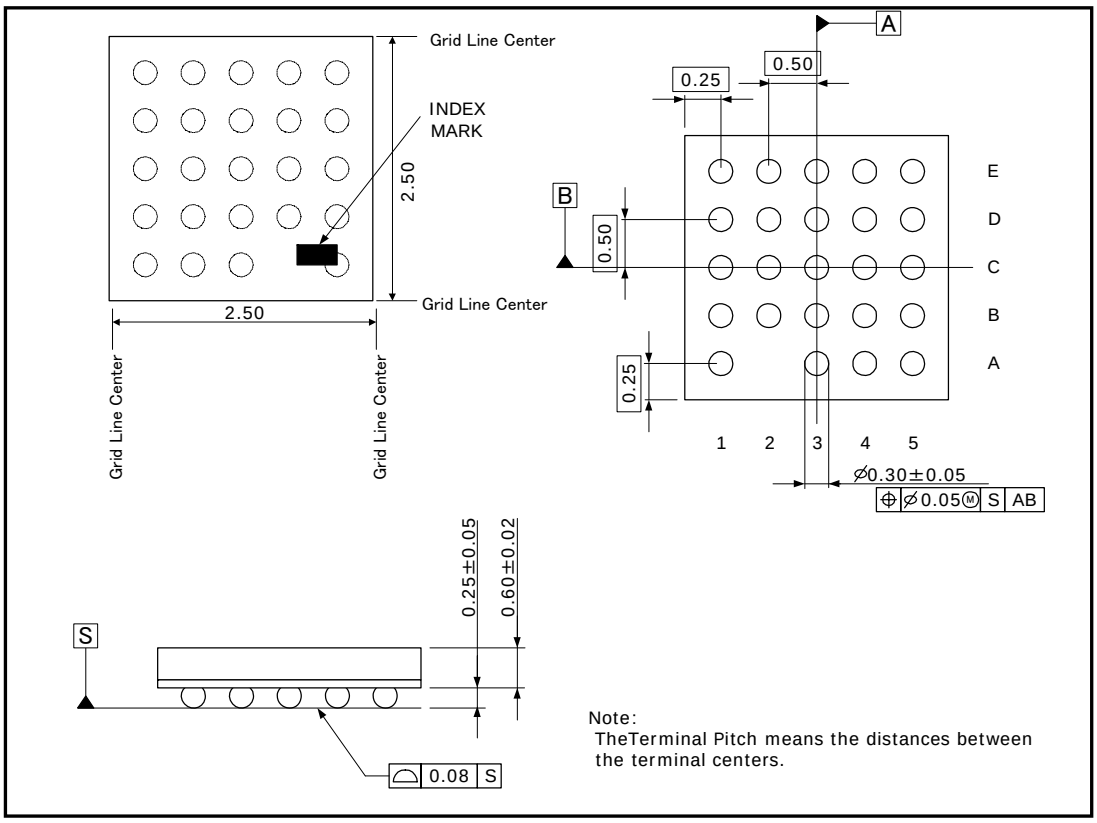


Figure 38: Package Dimensions (AK7832AB)

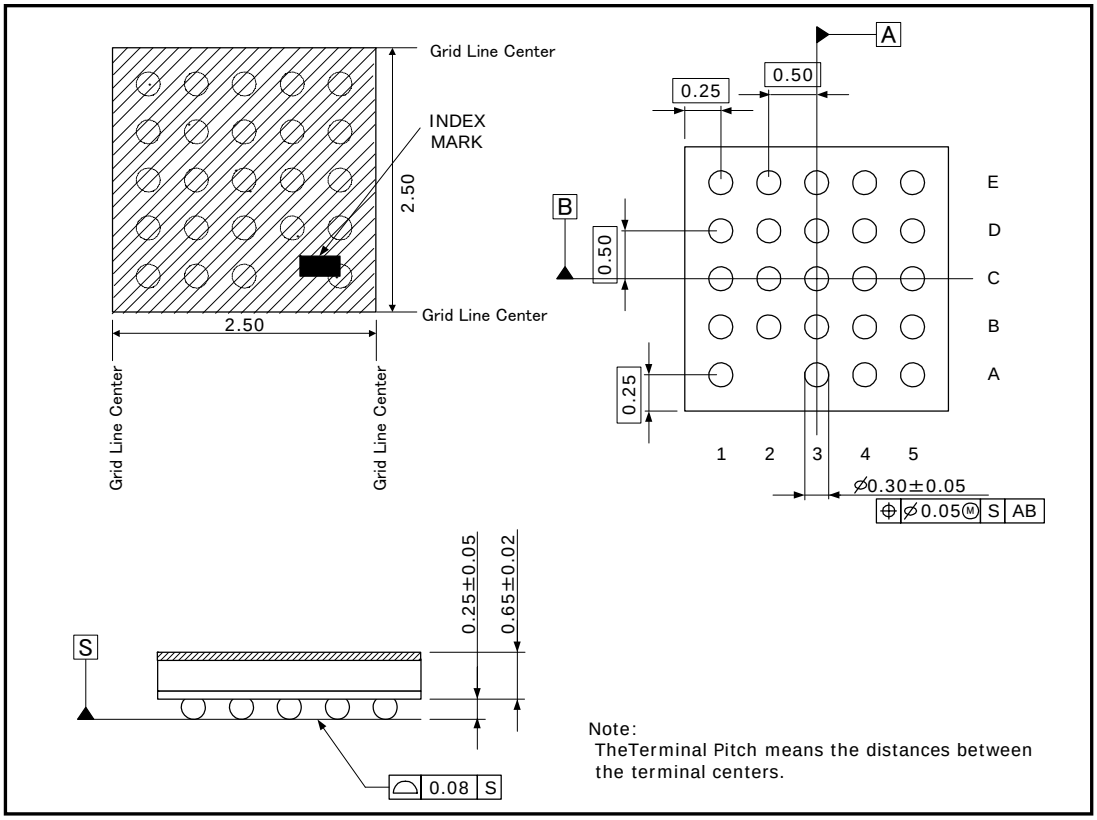


Figure 39: Package Dimensions (AK7832ABB)

MARKING

(a) Market number : "7832A"

(b) Date code(four digits)

Y : Last one digits of Christian year (ex. "2007" → "7")
WW : Manufactured week
L : Wafer lot number, which manufactured in same week ("A", "B", "C", ・・・)

(c) Index indication : "A2" pin location

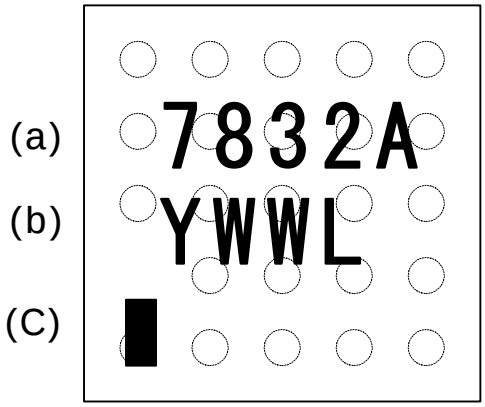


Figure 48: Package Marking (AK7832AB/AK7832ABB)

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.
- AKM assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components$_{Note1)}$ in any safety, life support, or other hazard related device or system$_{Note2)}$, and AKM assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKM. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.