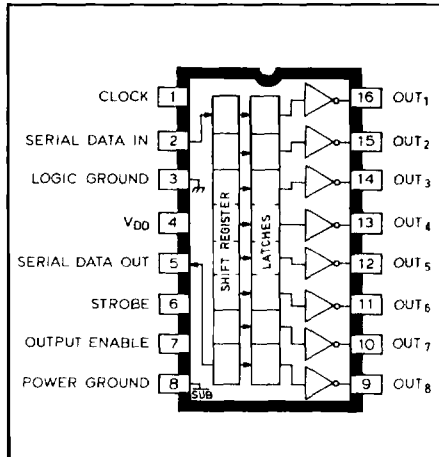


5822

MIL-STD-883 COMPLIANT

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER



Dwg. PP-026

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT}	80 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	-55°C to +125°C
Storage Temperature Range, T_S	-65°C to +150°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Intended for military, aerospace, and related applications. The UCS5822H 8-bit, serial-input, latched driver combines bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output allows cascading these devices for interface applications requiring additional drive lines.

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 85°C at a 51% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

The UCS5822H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

FEATURES

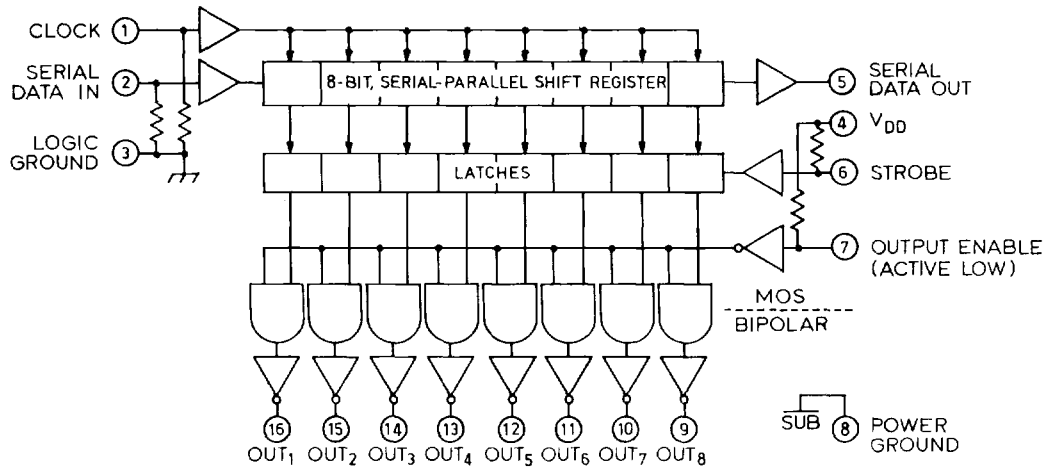
- 3.3 MHz Minimum Data Input Rate
- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Always order by complete part number: **UCS5822H883**.

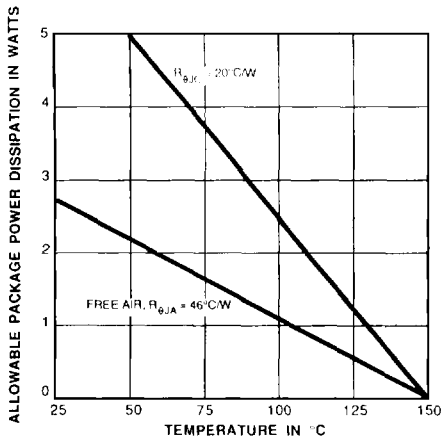
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BIMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER

FUNCTIONAL BLOCK DIAGRAM



Dwg FP-013



Dwg GM-002

Number of Outputs ON ($I_{OUT} = 200\text{ mA}$)	Maximum Allowable Duty Cycle at $V_{DD} = 5\text{ V}$ and T_A of 85°C
8	51%
7	58%
6	70%
5	84%
4	100%
3	100%
2	100%
1	100%

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BIMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER

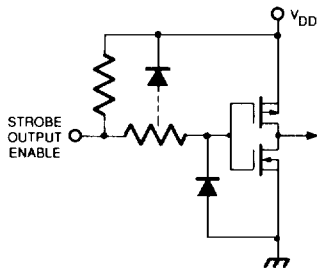
ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\text{ V}$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{ mA}$	—	1.1	V
		$I_{OUT} = 200\text{ mA}$	—	1.3	V
		$I_{OUT} = 350\text{ mA}$, $V_{DD} = 7.0\text{ V}$	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{ V}$	10.5	—	V
		$V_{DD} = 5.0\text{ V}$ (see note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\text{ V}$	50	—	$\text{k}\Omega$
		$V_{DD} = 10\text{ V}$	50	—	$\text{k}\Omega$
		$V_{DD} = 5.0\text{ V}$	50	—	$\text{k}\Omega$
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{STROBE} = V_{DD} = 12\text{ V}$	—	4.5	mA
		One Driver ON, $V_{STROBE} = V_{DD} = 10\text{ V}$	—	3.9	mA
		One Driver ON, $V_{STROBE} = V_{DD} = 5.0\text{ V}$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\text{ V}$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\text{ V}$	—	2.9	mA

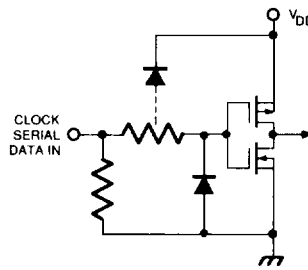
* Pulsed test.

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

TYPICAL INPUT CIRCUITS

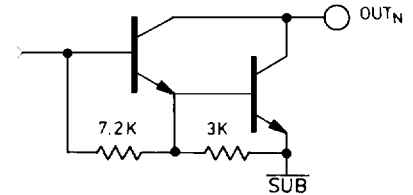


Dwg. EP-010-3



Dwg. EP-010-4

TYPICAL OUTPUT DRIVER



Dwg. No. A-14.314

ELECTRICAL CHARACTERISTICS at $T_A = -55^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\text{ V}$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{ mA}$	—	1.3	V
		$I_{OUT} = 200\text{ mA}$	—	1.5	V
		$I_{OUT} = 350\text{ mA}$, $V_{DD} = 7.0\text{ V}$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{ V}$	10.5	—	V
$V_{DD} = 5.0\text{ V}$ (see note)		3.5	—	V	
Input Resistance	R_{IN}	$V_{DD} = 12\text{ V}$	35	—	$\text{k}\Omega$
		$V_{DD} = 10\text{ V}$	35	—	$\text{k}\Omega$
		$V_{DD} = 5.0\text{ V}$	35	—	$\text{k}\Omega$
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{STROBE} = V_{DD} = 12\text{ V}$	—	5.5	mA
		One Driver ON, $V_{STROBE} = V_{DD} = 10\text{ V}$	—	4.5	mA
		One Driver ON, $V_{STROBE} = V_{DD} = 5.0\text{ V}$	—	3.0	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\text{ V}$	—	2.0	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\text{ V}$	—	3.5	mA

* Pulsed test

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input logic high.

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BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER

ELECTRICAL CHARACTERISTICS at $T_A = +125^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\text{ V}$	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{ mA}^*$	—	1.3	V
		$I_{OUT} = 200\text{ mA}^*$	—	1.5	V
		$I_{OUT} = 350\text{ mA}^*$, $V_{DD} = 7.0\text{ V}$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{ V}$	10.5	—	V
$V_{DD} = 5.0\text{ V}$ (see note)		3.5	—	V	
Input Resistance	R_{IN}	$V_{DD} = 12\text{ V}$	50	—	$\text{k}\Omega$
		$V_{DD} = 10\text{ V}$	50	—	$\text{k}\Omega$
		$V_{DD} = 5.0\text{ V}$	50	—	$\text{k}\Omega$
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{STROBE} = V_{DD} = 12\text{ V}$	—	4.5	mA
		One Driver ON, $V_{STROBE} = V_{DD} = 10\text{ V}$	—	3.9	mA
		One Driver ON, $V_{STROBE} = V_{DD} = 5.0\text{ V}$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\text{ V}$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\text{ V}$	—	2.9	mA

* Pulsed test.

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

