Integrated Device Technology, Inc.

# 8K x 8
# 16K x 8 CMOS
# CMOS DUAL-PORT STATIC
# RAM MODULE (MASTER)

**IDT7M134S**
**IDT7M135S**

## FEATURES:

- High-density 64K/128K CMOS Dual-Port RAM modules
- 16K x 8 (IDT7M135) or 8K x 8 (IDT7M134)option
- Fully asynchronous read/write operation from either port
- Fast access time
  - commercial: 30ns (max.)
  - military: 40ns (max.)
- Low power consumption
- On-chip port arbitration logic
- $\overline{BUSY}$ flags
- Single 5V (±10%) power supply
- Dual Vcc and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{BUSY}$ flag option
- Inputs and outputs directly TTL-compatible

## DESCRIPTION:

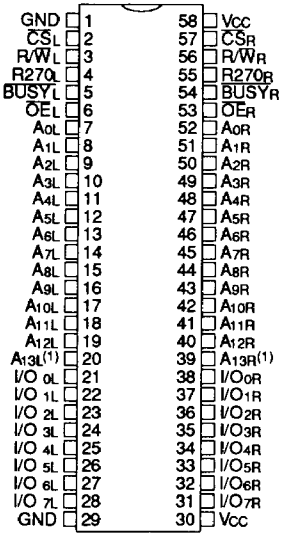
The IDT7M134/IDT7M135 are 64K/128K high-speed CMOS Dual-Port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port static RAMs (IDT7M134) or eight IDT7132 dual-port static RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses $A_{L11-13}$ and $A_{R11-13}$ to select one of the eight 2K x 8 dual-port static RAMs. (On IDT7M134 8K x 8 option, $A_{L13}$ and $A_{R13}$ need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port static RAMs). Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port static RAM, fabricated in IDT's high-performance CEMOS™ technology.

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{BUSY}$ flag of the delayed port. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive).

The IDT7M134/IDT7M135 are available with access times as fast as 30ns commercial and 40ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

## PIN CONFIGURATION (2)




DIP
TOP VIEW

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## PIN NAMES

| Left Port | Right Port | Names |
|---|---|---|
| $A_{0L}$-$A_{13L}$ | $A_{0R}$-$A_{13R}$ | Address |
| $I/O_{0L}$-$IO_{7L}$ | $I/O_{0R}$-$I/O_{7R}$ | Data Input/Output |
| $\overline{CS}_L$ | $\overline{CS}_R$ | Chip Select |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | Read/Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | $\overline{BUSY}$ Flag (Open Drain) |
| $R270_L$ | $R270_R$ | PULL-UP Resistors for Open-drain $\overline{BUSY}$ Flag option |
| $V_{CC}$ | $V_{CC}$ | Power |
| GND | GND | Ground |

**NOTES:**
1. On 8K x 8 IDT7M134 option $A_{13L}$ and $A_{13R}$ need to be externally connected to ground for proper operation.
2. For module dimensions, please refer to module drawing M12 in the packaging section.

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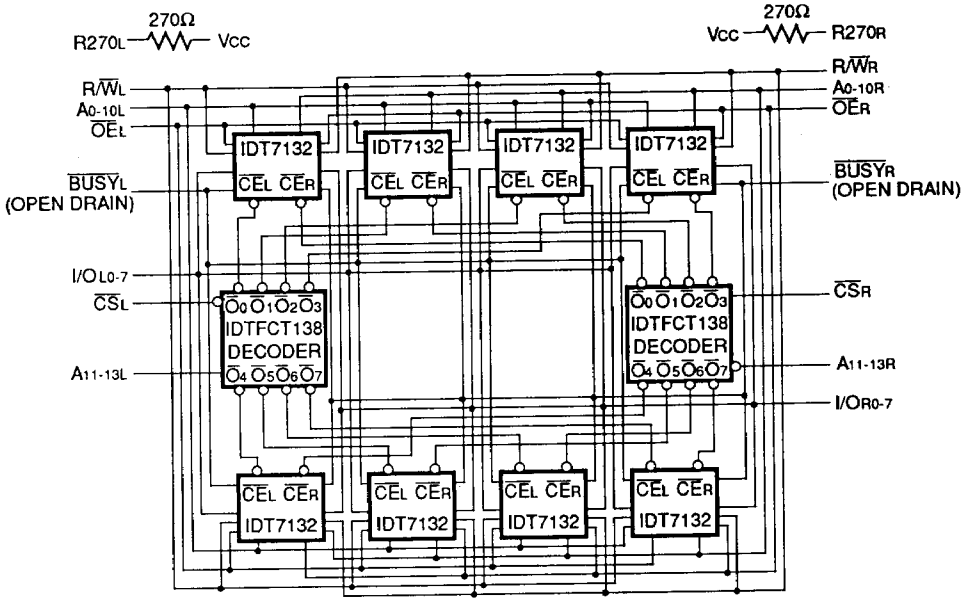
## FUNCTIONAL BLOCK DIAGRAMS

### IDT7M135 (16K x 8)

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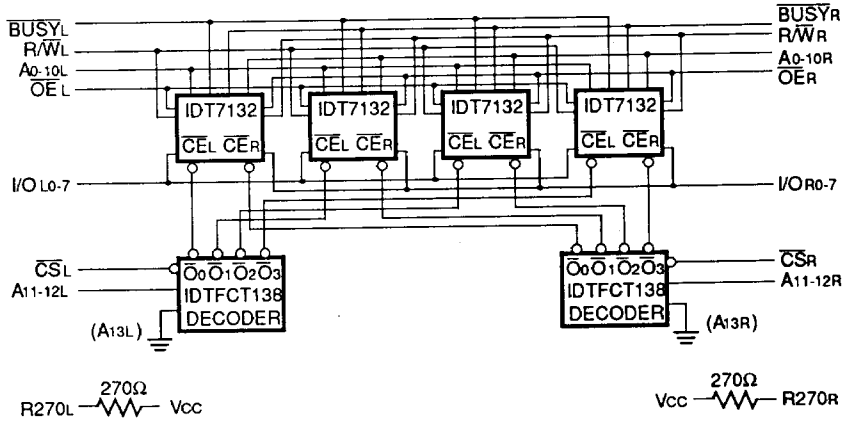
### IDT7M134 (8K x 8)

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## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | -0.5(1) | — | 0.8 | V |

**NOTE:**
1. $V_{IL}$ = -3.0V for pulse width less than 20ns.

## DC ELECTRICAL CHARACTERISTICS(4)

(Vcc = 5.0V ± 10%, $T_A$ = -55°C to +125°C and 0°C to +70°C)

| Symbol | Parameter | Test Conditions | IDT7M134S Min. | IDT7M134S Typ.(1) | IDT7M134S Max. | IDT7M135S Min. | IDT7M135S Typ.(1) | IDT7M135S Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | Vcc = 5.5V, $V_{IN}$ = 0V to Vcc | — | — | 15 | — | — | 20 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = 0V to Vcc | — | — | 15 | — | — | 20 | µA |
| $V_{IH}$ | Input High Voltage | — | 2.2 | — | 6.0 | 2.2 | — | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | — | -1.0(2) | — | 0.8 | -1.0(2) | — | 0.8 | V |
| $I_{CC}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CS}$ = $V_{IL}$, Outputs Open, f = $f_{MAX}$ | — | 190 | 380 | — | 320 | 640 | mA |
| $I_{SB}$ | Standby Current (Both Ports Standby) | $\overline{CS_L}$ and $\overline{CS_R}$ ≥ $V_{IH}$, Vcc = Max., Both Ports Output Open | — | 130 | 260 | — | 260 | 520 | mA |
| $I_{SB1}$ | Standby Current (One Port Standby) | $\overline{CS_L}$ or $\overline{CS_R}$ ≥$V_{IH}$, Vcc = Max. Active Port Outputs Open | — | 160 | 320 | — | 290 | 580 | mA |
| $I_{SB2}$ | Full Standby Current (Both Ports Full Standby) | Both Ports $\overline{CS_L}$ and $\overline{CE_R}$ ≥ Vcc -0.2V $V_{IN}$ ≥ Vcc -0.2V or $V_{IN}$ ≤ 0.2V | — | 4 | 120(3) | — | 10 | 240(3) | mA |
| $V_{OL}$ | Output Low Voltage ($I/O_0$-$I/O_7$) | $I_{OL}$ = 4mA, Vcc = 4.5V<br>$I_{OL}$ = 8mA, Vcc = 4.5V | —<br>— | —<br>— | 0.4<br>0.5 | —<br>— | —<br>— | 0.4<br>0.5 | V<br>V |
| $V_{OL}$ | Open Drain Output Low Voltage ($\overline{BUSY}$) | $I_{OL}$ = 16mA, Vcc = 4.5V | — | — | 0.5 | — | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA, Vcc = 4.5V | 2.4 | — | — | 2.4 | — | — | V |

**NOTES:**
1. Vcc = 5V, $T_A$ = +25°C.
2. $V_{IL}$ min. = -3.0V for pulse width less than 20ns.
3. $I_{SB2}$ max. of IDT7M134/IDT7M135 at commercial temperature = 80mA/150mA.
4. For tAA = 30, 35, 40ns versions all D.C. parameters are preliminary only.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 10ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1, 2 and 3 |

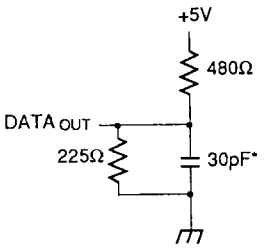


Figure 1. Output Load

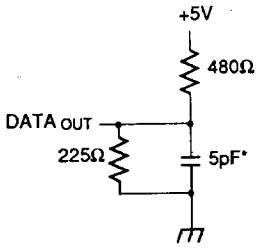


Figure 2. Output Load
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

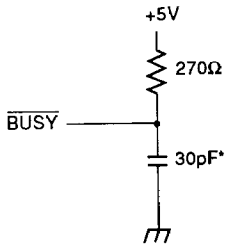


Figure 3. $\overline{\text{BUSY}}$ Output Load

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* Including scope and jig. 30pF for fast speed versions. Consult factory for further details.

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## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5.0V ± 10%, $T_A$ = -55°C to +125°C and 0°C to +70°C)

| Symbol | Parameter | 7M134S30 7M135S30 (Com'l. Only) Min. | Max. | 7M134S35 7M135S35 (Com'l. Only) Min. | Max. | 7M134S40 7M135S40 Min. | Max. | 7M134S45 7M135S45 Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ CYCLE** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 30 | — | 35 | — | 40 | — | 45 | — | ns |
| $t_{AA}$ | Address Access Time | — | 30 | — | 35 | — | 40 | — | 45 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 30 | — | 35 | — | 40 | — | 45 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 15 | — | 20 | — | 25 | — | 30 | ns |
| $t_{OH}$ | Output Hold From Address Change | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{CLZ}$[1] | Chip Select to Output in Low Z | 5 | — | 5 | — | 5 | — | 10 | — | ns |
| $t_{CHZ}$[1] | Chip Select to Output in High Z | — | 10 | — | 15 | — | 15 | — | 20 | ns |
| $t_{OHZ}$[1] | Output Enable to Output in High Z | — | 10 | — | 15 | — | 15 | — | 30 | ns |
| $t_{OLZ}$[1] | Output Enable to Output in Low Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{PU}$[1] | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$[1] | Chip Deselect to Power Down Time | — | 50 | — | 50 | — | 50 | — | 50 | ns |
| **WRITE CYCLE** | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 30 | — | 35 | — | 40 | — | 45 | — | ns |
| $t_{CW}$ | Chip Select to End of Write | 25 | — | 30 | — | 35 | — | 40 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 25 | — | 30 | — | 35 | — | 40 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 20 | — | 25 | — | 30 | — | 35 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | 5 | — | ns |
| $t_{DW}$ | Data Valid to End of Write | 20 | — | 20 | — | 22 | — | 25 | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | 5 | — | ns |
| $t_{OHZ}$[1] | Output Enable to Output in High Z | — | 10 | — | 15 | — | 15 | — | 20 | ns |
| $t_{WHZ}$[1] | Write Enabled to Output in High Z | — | 10 | — | 15 | — | 15 | — | 20 | ns |
| $t_{OW}$[1] | Output Active From End of Write | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| **$\overline{BUSY}$ TIMING** | | | | | | | | | | |
| $t_{BAA}$ | $\overline{BUSY}$ Access Time to Address | — | 35 | — | 35 | — | 40 | — | 40 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable Time to Address | — | 30 | — | 35 | — | 35 | — | 35 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access Time to Chip Select | — | 30 | — | 35 | — | 35 | — | 40 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable Time to Chip Select | — | 30 | — | 30 | — | 30 | — | 35 | ns |
| $t_{BDD}$ | $\overline{BUSY}$ Disable to Valid Data | — | 20 | — | 25 | — | 30 | — | 30 | ns |
| $t_{WDD}$ | Write Pulse to Data Delay | — | 50 | — | 55 | — | 60 | — | 65 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data | — | 25 | — | 30 | — | 35 | — | 40 | ns |
| $t_{APS}$ | Arbitration Priority Set-up Time | 10 | — | 10 | — | 10 | — | 10 | — | ns |

**NOTE:**
1. This parameter is guaranteed by design, but not tested.

## AC ELECTRICAL CHARACTERISTICS (Continued)

($V_{CC}$ = 5.0V ± 10%, $T_A$ = -55°C to +125°C and 0°C to +70°C)

| Symbol | Parameter | IDTM134S50 IDTM135S50 Min. | Max. | IDTM134S60 IDTM135S60 Min. | Max. | IDTM134S70 IDTM135S70 (Mil. Only) Min. | Max. | IDTM134S90 IDTM135S90 (Mil. Only) Min. | Max. | IDTM134S100 IDTM135S100 (Mil. Only) Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ CYCLE** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 50 | — | 60 | — | 70 | — | 90 | — | 100 | — | ns |
| $t_{AA}$ | Address Access Time | — | 50 | — | 60 | — | 70 | — | 90 | — | 100 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 50 | — | 60 | — | 70 | — | 90 | — | 100 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 35 | — | 40 | — | 40 | — | 45 | — | 50 | ns |
| $t_{OH}$ | Output Hold From Address Change | 0 | — | 0 | — | 5 | — | 10 | — | 10 | — | ns |
| $t_{CLZ}$[1] | Chip Select to Output in Low Z | 10 | — | 10 | — | 10 | — | 15 | — | 15 | — | ns |
| $t_{CHZ}$[1] | Chip Select to Output in High Z | — | 25 | — | 35 | — | 35 | — | 45 | — | 50 | ns |
| $t_{OHZ}$[1] | Output Enable to Output in High Z | — | 40 | — | 40 | — | 30 | — | 40 | — | 40 | ns |
| $t_{OLZ}$[1] | Output Enable to Output in Low Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{PU}$[1] | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$[1] | Chip Deselect to Power Down Time | — | 50 | — | 50 | — | 50 | — | 50 | — | 50 | ns |
| **WRITE CYCLE** | | | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 50 | — | 60 | — | 70 | — | 90 | — | 100 | — | ns |
| $t_{CW}$ | Chip Select to End of Write | 45 | — | 50 | — | 60 | — | 80 | — | 95 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 45 | — | 50 | — | 60 | — | 80 | — | 95 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 40 | — | 45 | — | 45 | — | 50 | — | 55 | — | ns |
| $t_{WR}$ | Write Recovery Time | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{DW}$ | Data Valid to End of Write | 25 | — | 25 | — | 30 | — | 40 | — | 40 | — | ns |
| $t_{DH}$ | Data Hold Time | 5 | — | 5 | — | 10 | — | 10 | — | 10 | — | ns |
| $t_{OHZ}$[1] | Output Enable to Output in High Z | — | 25 | — | 35 | — | 35 | — | 40 | — | 40 | ns |
| $t_{WHZ}$[1] | Write Enabled to Output in High Z | — | 25 | — | 35 | — | 35 | — | 40 | — | 40 | ns |
| $t_{OW}$[1] | Output Active From End of Write | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| **$\overline{BUSY}$ TIMING** | | | | | | | | | | | | |
| $t_{BAA}$ | $\overline{BUSY}$ Access Time to Address | — | 40 | — | 45 | — | 45 | — | 45 | — | 50 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable Time to Address | — | 40 | — | 45 | — | 45 | — | 45 | — | 50 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access Time to Chip Select | — | 40 | — | 40 | — | 40 | — | 40 | — | 50 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable Time to Chip Select | — | 35 | — | 35 | — | 35 | — | 35 | — | 50 | ns |
| $t_{BDD}$ | $\overline{BUSY}$ Disable to Valid Data | — | 35 | — | 40 | — | 50 | — | 50 | — | 60 | ns |
| $t_{WDD}$ | Write Pulse to Data Delay | — | 75 | — | 85 | — | 90 | — | 100 | — | 120 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data | — | 50 | — | 60 | — | 70 | — | 80 | — | 100 | ns |
| $t_{APS}$ | Arbitration Priority Set-up Time | 10 | — | 10 | — | 10 | — | 10 | — | 10 | — | ns |

**NOTE:**
1. This parameter is guaranteed by design, but not tested.

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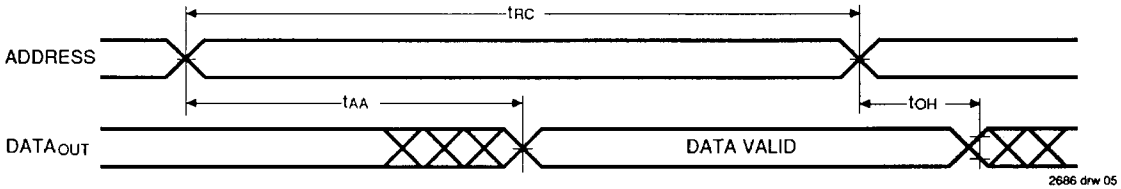
## CAPACITANCE[1,2] ($T_A$ = +25°C, f = 1.0MHz)

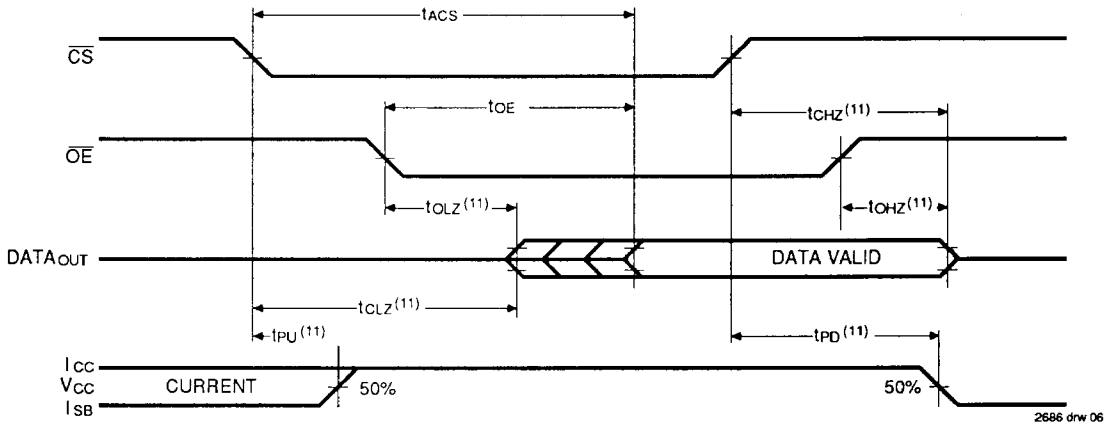
| Symbol | Parameter | Conditions | IDT7M134S | IDT7M135S | Unit |
|---|---|---|---|---|---|
| $C_{IN(D)}$ | Input Capacitance (Data) | $V_{IN}$ = 0V | 50 | 95 | pF |
| $C_{IN(A)}$ | Input Capacitance (Address) | $V_{IN}$ = 0V | 50 | 100 | pF |
| $C_{IN(C)}$ | Input Capacitance ($\overline{CS}$) | $V_{IN}$ = 0V | 14 | 14 | pF |
| $C_{IN(C)}$ | Input Capacitance ($\overline{BUSY}$, $\overline{OE}$) | $V_{IN}$ = 0V | 50 | 95 | pF |
| $C_{IN(C)}$ | Input Capacitance (R/$\overline{W}$) | $V_{IN}$ = 0V | 50 | 95 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 50 | 95 | pF |

**NOTES:**
1. This parameter is guaranteed by design but not tested.
2. Typical values.

## TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,6]

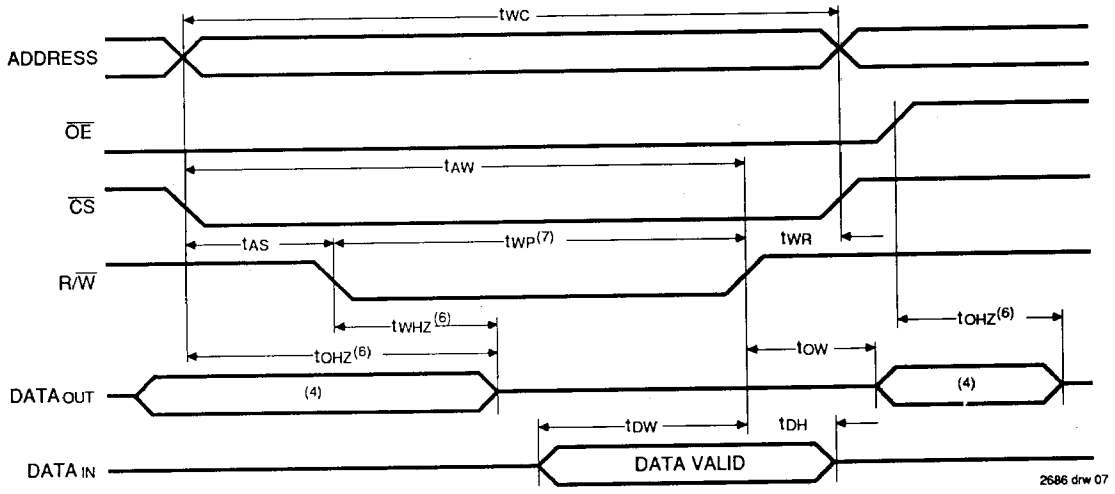



## TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE[1,3]

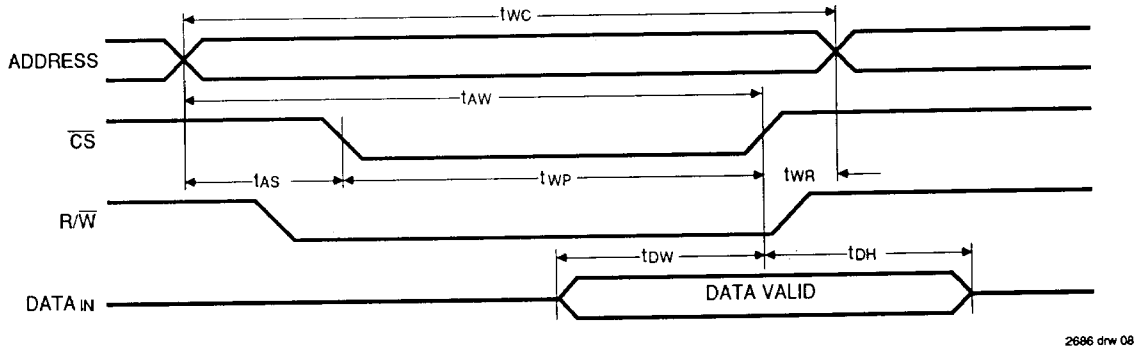



**NOTES:**
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = $V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. If $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CS}_L$ = $\overline{CS}_R$ ≤ $V_{IL}$
6. $\overline{OE}$ = $V_{IL}$
7. R/$\overline{W}$ = $V_{IH}$ during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)




## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)




**NOTES:**
1. R/$\overline{W}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a R/$\overline{W}$ controlled write cycle, write pulse (tWP > tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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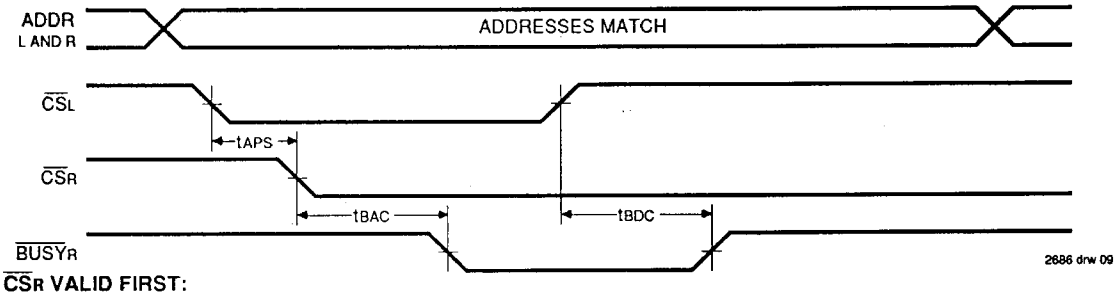
## TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CS}$ ARBITRATION

**$\overline{CS}_L$ VALID FIRST:**

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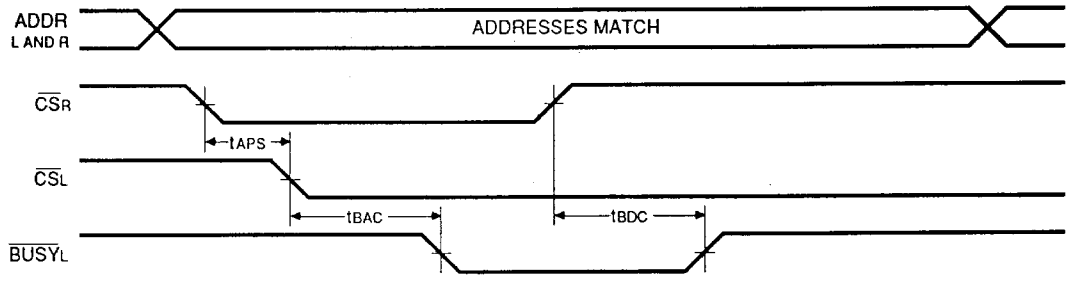
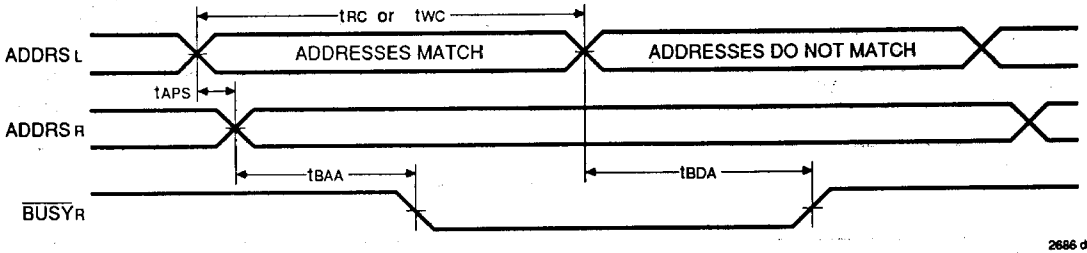
**$\overline{CS}_R$ VALID FIRST:**




2686 drw 10

## TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(5)

### LEFT ADDRESS VALID FIRST:

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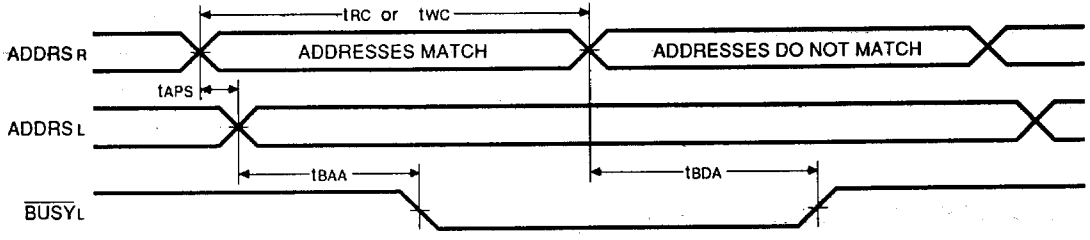
### RIGHT ADDRESS VALID FIRST:

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**NOTES:**
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = $V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. If $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CS}_L = \overline{CS}_R \leq V_{IL}$
6. $\overline{OE}$ = $V_{IL}$
7. R/$\overline{W}$ = $V_{IH}$ during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

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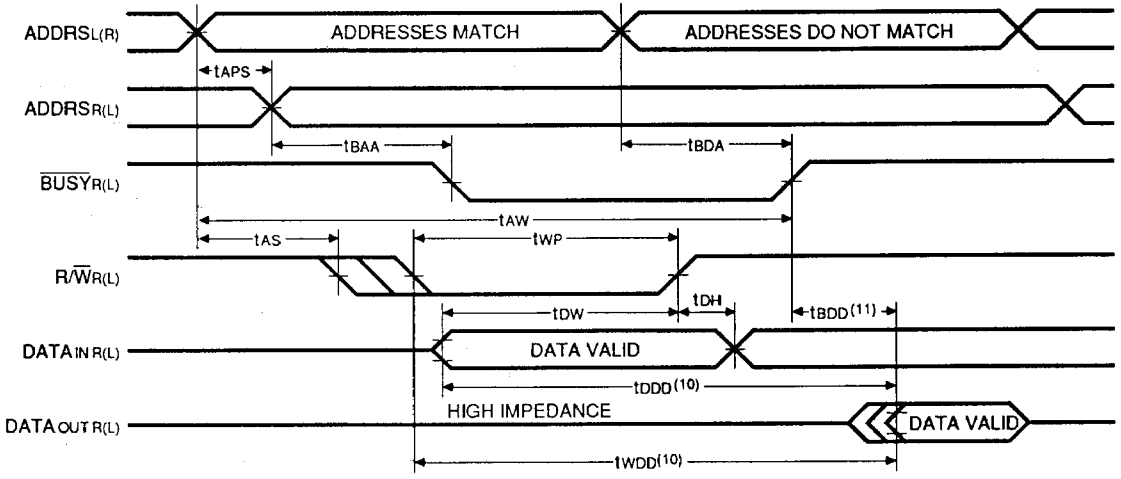
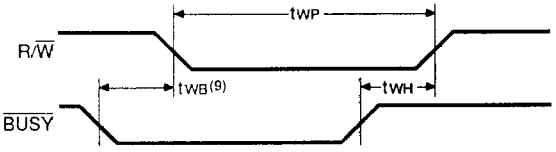
## TIMING WAVEFORM OF READ WITH BUSY(5)




2686 drw 13

## TIMING WAVEFORM OF WRITE WITH BUSY(5)




2686 drw 14

**NOTES:**
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CS}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. If $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CS}_L$ = $\overline{CS}_R$ ≤ VIL
6. $\overline{OE}$ = VIL
7. R/$\overline{W}$ = VIH during address transition.
8. Transition is measured at +500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
9. For SLAVE port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

## FUNCTIONAL DESCRIPTION

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M134/IDT7M135 have an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

## ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip select match down to 10ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and set the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CS}$, on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access; or (2) if the $\overline{CS}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access complete its operation.

## DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port static RAM system implies that several modules will be active at the same time. If each module includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "busy lock-out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port static RAMs in width, the writing of the SLAVE modules must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE module may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems when more than one module is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

## TRUTH TABLES

### TABLE I — NON-CONTENTION READ/WRITE CONTROL, LEFT OR RIGHT PORT[1]

| $R/\overline{W}$ | $\overline{CS}$ | $\overline{OE}$ | $I/O_{0-7}$ | FUNCTION |
|---|---|---|---|---|
| X | H | X | Z | Port Disabled and in Power Down Mode, $I_{SB}$ |
| X | H | X | Z | $\overline{CS}_R = \overline{CS}_L$ = H, Power Down Mode, $I_{SB}$ or $I_{SB2}$ |
| L | L | X | $DATA_{IN}$ | Data on Port Written into Memory[2] |
| H | L | L | $DATA_{OUT}$ | Data in Memory Output on Port[3] |
| H | L | H | Z | High Impedance Outputs |

NOTES:
1. $A_{0L}$-$A_{13L} \neq A_{0R}$-$A_{13R}$
2. If BUSY = L, data is not written.
3. If BUSY = L, data may not be valid, see $t_{WDD}$ and $t_{DDD}$ timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

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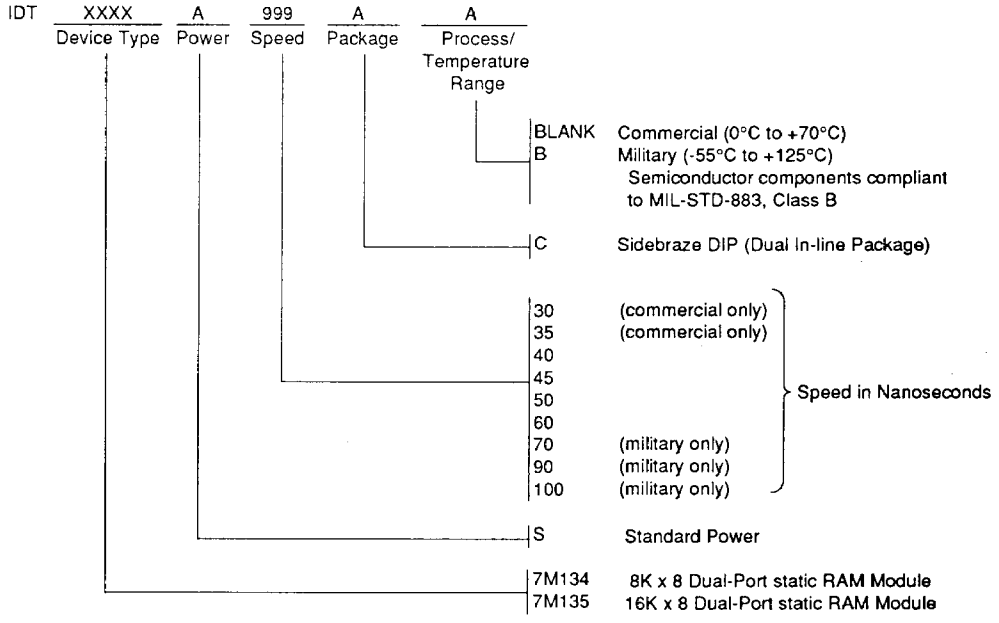
## TABLE III — ARBITRATION

| LEFT PORT | | RIGHT PORT | | FLAGS[1] | | |
|---|---|---|---|---|---|---|
| $\overline{CS}_L$ | $A_{0L}$-$A_{13L}$ | $\overline{CS}_R$ | $A_{0L}$-$A_{13R}$ | $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | FUNCTION |
| H | X | H | X | H | H | No Contention |
| L | Any | H | X | H | H | No Contention |
| H | X | L | Any | H | H | No Contention |
| L | ≠$A_{0R}$-$A_{13R}$ | L | ≠$A_{0L}$-$A_{13L}$ | H | H | No Contention |
| ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH | | | | | | |
| L | LV10R | L | LV10R | H | L | Left-Port Wins |
| L | RV10L | L | LV10L | L | H | Right-Port Wins |
| L | Same | L | Same | H | L | Arbitration Resolved |
| L | Same | L | Same | L | H | Arbitration Resolved |
| $\overline{CS}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$ | | | | | | |
| LL10R | = $A_{0R}$-$A_{13R}$ | LL10R | = $A_{0L}$-$A_{13L}$ | H | L | Left-Port Wins |
| RL10L | = $A_{0R}$-$A_{13R}$ | RL10R | = $A_{0L}$-$A_{13L}$ | L | H | Right-Port Wins |
| LW10R | = $A_{0R}$-$A_{13R}$ | LW10R | = $A_{0L}$-$A_{13L}$ | H | L | Arbitration Resolved |
| LW10R | = $A_{0R}$-$A_{13R}$ | LW10R | = $A_{0L}$-$A_{13L}$ | L | H | Arbitration Resolved |

**NOTE:**
1. X = DON'T CARE, L = LOW, H = HIGH, Same = Left and Right Addresses match within 10ns of each other.
   LV10R = Left Address Valid ≥ 10ns before Right Address.
   RV10L = Right Address Valid ≥ 10ns before Left Address.
   LL10R = Left $\overline{CS}$ = LOW ≥ 10ns before Right $\overline{CS}$.
   RL10L = Right $\overline{CS}$ = LOW ≥ 10ns before left $\overline{CS}$.
   LW10R = Left and Right $\overline{CS}$ = LOW within 10ns of each other.

## ORDERING INFORMATION

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