Signetics

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Status	Product Specification
FAST Products	

FAST 74F563, 74F564 Latch/Flip-Flop

74F563 Octal Transparent Latch (3-State)
74F564 Octal D Flip-Flop (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563	5.0ns	40mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F564	180MHz	50mA

FEATURES

- **74F563 is broadside pinout version of 74F533**
- **74F564 is broadside pinout version of 74F534**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus Interfacing**
- **Common Output Enable**
- **74F573 and 74F574 are non-inverting versions of 74F563 and 74F564 respectively**
- **These are High-Speed replacements for N8TS807 and N8TS808**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F563N, N74F564N
20-Pin Plastic SOL	N74F563D, N74F564D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F563)	Latch Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F564)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_7$	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F563 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.
The 74F563 is functionally identical to the 74F533 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F564 is functionally identical to the 74F534 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F563	Waveform 2	4.0 2.5	5.5 4.0	8.5 6.5	3.5 2.0	9.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 1	5.0 3.0	6.5 5.0	9.5 7.0	4.5 3.0	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.5 8.0	2.5 3.5	8.5 8,5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.5 1.5	3.0 3.0	6.0 5.5	1.0 1.0	7.0 6.0	ns
f_{MAX}	Maximum Clock frequency	74F564	Waveform 1	160	180		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 4.0	4.5 5.5	7.5 8.0	2.0 3.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F563	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 3	3.0 2.5			3.0 2.5		ns
$t_w(H)$	E Pulse width, High		Waveform 1	3.5			3.5		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F564	Waveform 3	2.0 2.0			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 3	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.5 3.5			3.5 3.5		ns