Data Sheet

T7100A X.25 Protocol Controller

Features

- 5-MHz clock (max)
- 250-kb/s serial data rate (max)
- 8-bit data bus
- 16-bit address bus
- Six bidirectional address leads for accessing internal registers
- Link initialization and supervision
- Error detection and automatic recovery via packet retransmission
- Automatic appending and testing of 16-bit frame check sequence (FCS) field
- Zero-bit insertion and deletion (for data transparency)
- Programmable address field
- Modulo-8 frame sequence numbering
- 3-bit programmable window size (k)
- Four independently programmable timers (T1—T4)
- Wait-state generator (on DMA side) for slow memory
- Triple-channel DMA with standard interface
- Programmable retransmission counter (N2)
- Password exchange mechanism for dial-up operation
- Daisy-chain DMA structure for easy expansion to multiple XPC-8 applications
- Transmit and receive data buffers accessed indirectly through a look-up table
- Memory error service via external parity checking circuitry
- Programmable bus interface to enable the XPC-8 to be configured for a Motorola or Intel bus
- Two independent test configurations (far-end loopback and near-end loopback) to verify XPC-8 operation and physical level services
- 3-state output buffers to assist in system diagnostics
- Programmable flag-fill option that specifies the minimum number of flags between frames

Description

The T7100A X.25 Protocol Controller (XPC-8) integrated circuit is a level 2 protocol controller with an 8-bit data bus. It is a single-chip VLSI device fabricated using NMOS silicon gate technology, requires a single 5 V supply, and is available in a 48-pin ceramic DIP. The XPC-8 implements the data link control functions defined in the X.25 packet switching communication standard. It satisfies the X.25 link level (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. The XPC-8 also is in compliance with CCITT X.25 1980 and ISO 7776 (which is at the draft international standard (DIS) level). The protocol controller is byte-oriented, with a maximum transmit and receive data rate of 250 kb/s. All inputs and outputs are TTL-compatible.

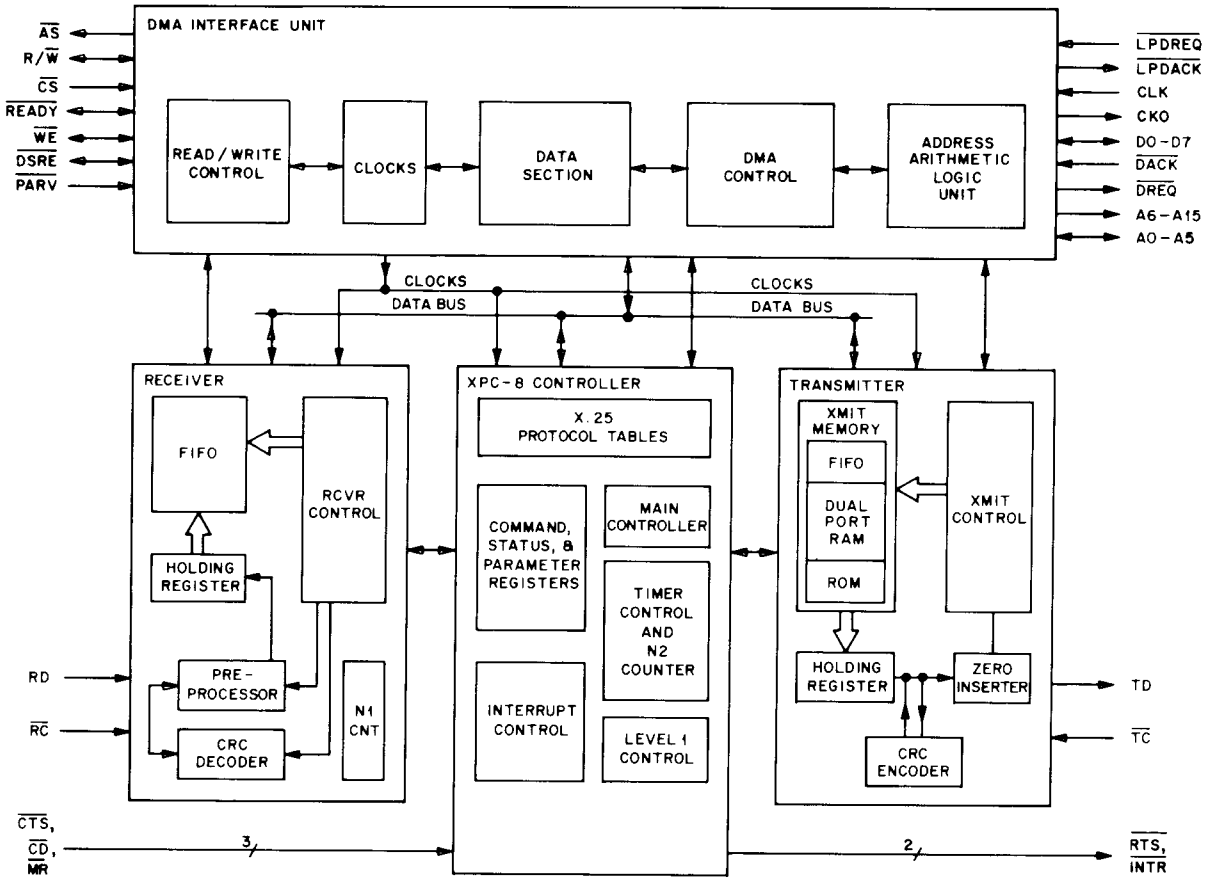
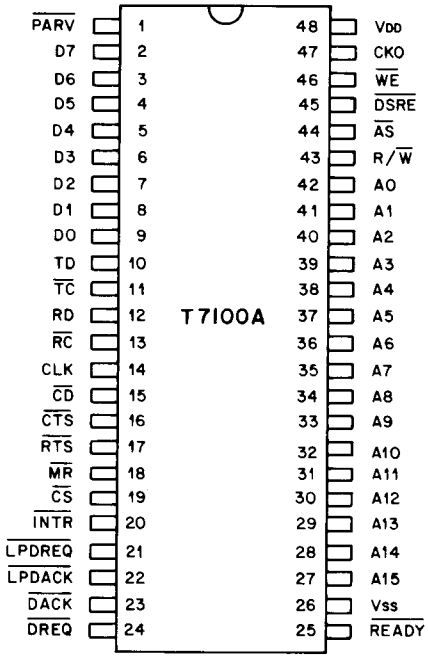


Figure 1. Block Diagram

User Information

Pin Descriptions



Sym	Pin	Sym	Pin	Sym	Pin
A0	42	AS	44	DSRE	45
A1	41	CD	15	INTR	20
A2	40	CKO	47	LPDACK	22
A3	39	CLK	14	LPDREQ	21
A9	38	CS	19	MR	18
A5	37	CTS	16	PARV	1
A6	36	D0	9	RC	13
A7	35	D1	8	RD	12
A8	34	D2	7	READY	25
A9	33	D3	6	RTS	17
A10	32	D4	5	R/W	43
A11	31	D5	4	TC	11
A12	30	D6	3	TD	10
A13	29	D7	2	VDD	48
A14	28	DACK	23	VSS	26
A15	27	DREQ	24	WE	46

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	PARV	I	**Parity Valid (Active Low).** Notifies the XPC-8 that external parity checking circuitry has detected an error on an attempted DMA read or write operation. If this occurs on two consecutive attempts to run a bus cycle, a hard parity error (HPE) interrupt is generated (see Tables 7 and 8).
2—9	D7—D0	I/O*	**8-Bit Data Bus.** Used by the host CPU to access XPC-8 on-chip registers. Used by the XPC-8 during DMA operations to access system memory.
10	TD	O	**Transmit Data.** XPC-8 serial data output lead.
11	TC	I	**Transmit Clock (Active Low).** Data is transmitted at this frequency.
12	RD	I	**Receive Data.** XPC-8 serial data input lead.
13	RC	I	**Receive Clock (Active Low).** Data is received at this frequency.
14	CLK	I	**Master Clock Input.** Controls internal chip sequencing. The clock input must have a minimum frequency of 250 kHz ($f_{CLK} \geq 17\ f_{RC}$ and $f_{CLK} \geq 17\ f_{TC}$) and a maximum frequency of 5 MHz.

* Indicates 3-state output capability during normal operations.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
15	$\overline{CD}$	I	**Carrier Detect (Active Low).** Indicates that the level 1 interface (e.g., a modem) is receiving and modulating a usable signal. Transitions on this signal cause interrupts (see Table 8). The state of the $\overline{CD}$ lead does not otherwise affect XPC-8 operation.
16	$\overline{CTS}$	I	**Clear-To-Send (Active Low).** Indicates to the XPC-8 that the level 1 interface is ready. The data link does not come up until $\overline{CTS}$ is low. $\overline{CTS}$ must remain low while the link is up or an interrupt occurs (see Table 8) and the XPC-8 enters an inactive state until $\overline{CTS}$ is re-asserted (low).
17	$\overline{RTS}$	O	**Request-To-Send (Active Low).** Indicates that the XPC-8 is requesting the physical link. $\overline{RTS}$ remains low while the link is up.
18	$\overline{MR}$	I	**Master Reset (Active Low).** Resets the XPC-8 and selects either the Motorola or the Intel bus configuration. When low, all XPC-8 outputs are in the 3-state condition.
19	$\overline{CS}$	I	**Chip Select (Active Low).** Must be low to allow access to internal XPC-8 registers. When low, R/$\overline{W}$, $\overline{WE}$, $\overline{DSRE}$, and A0—A5 become inputs; $\overline{READY}$ becomes an output.
20	$\overline{INTR}$	O	**Interrupt Request (Active Low).** Indicates that the XPC-8 is requesting interrupt service. This lead goes high when the CPU reads the interrupt register.
21	$\overline{LPDREQ}$	I	**Low Priority DMA Request (Active Low).** Used to daisy-chain DMA requests in systems that use more than one XPC-8 without a bus arbiter. If daisy-chain DMA is not being used, $\overline{LPDREQ}$ must be tied high (5 V).
22	$\overline{LPDACK}$	O	**Low Priority DMA Acknowledge (Active Low).** When the host CPU drives this pin low, it grants the XPC-8 use of the system bus. $\overline{AS}$, $\overline{DSRE}$, R/$\overline{W}$, $\overline{WE}$, and the address pins become outputs.
24	$\overline{DREQ}$	O	**DMA Request (Active Low).** The XPC-8 pulls this pin low to request use of the system bus.
25	$\overline{READY}$	I/O*	**Ready (Active Low).** This pin is pulled low by the XPC-8 when a CPU read or write to an on-chip register is completed. During DMA cycles, the XPC-8 executes wait states until this lead is pulled low, indicating that the current read or write access has been completed.
26	V_{SS}	—	**Ground.**
27—36	A15—A6	O*	**16-Bit Address Bus.** When $\overline{CS}$ is low, A0—A5 are used in the input mode to address the internal registers of the XPC-8. All 16 address lines are used to access system memory during DMA cycles.
37—42	A5—A0	I/O*	

* Indicates 3-state output capability during normal operations.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
43	R/$\overline{W}$	I/O*	**Read or Write (Active Low).** Indicates whether the next data transfer performed is a read (high) or a write (low). This signal can also be used to control the direction of external bidirectional buffers placed on the data leads.
44	$\overline{AS}$	O*	**Address Strobe (Active Low).** This signal is used for both Motorola and Intel read and write operations. When low, it indicates that a valid memory address is currently on the address leads.
45	$\overline{DSRE}$	I/O*	**Data Strobe or Read Enable (Active Low).** The mode of this signal is determined during master reset. In a Motorola bus configuration, $\overline{DSRE}$ is a data strobe; in an Intel bus configuration, $\overline{DSRE}$ is a read enable.
46	$\overline{WE}$	I/O*	**Write Enable (Active Low).** This signal goes low when the XPC-8 performs a DMA write operation in either Intel or Motorola bus modes. For Intel bus mode, $\overline{WE}$ is used as an input when the CPU accesses the internal XPC-8 registers ($\overline{CS}$ = 0). For Motorola bus mode, $\overline{WE}$ should be connected to V_{DD} through an external resistor (10 kΩ typical value). It should not be connected directly to V_{DD} since damage may occur when $\overline{WE}$ switches to an output during DMA operations.
47	CKO	O	**Clock Output.** Buffered internal clock that runs at half the frequency of the input clock.
48	V_{DD}	—	**5 V Supply.**

* Indicates 3-state output capability during normal operation.

Overview

The XPC-8 performs complete link level control according to the X.25 data communications protocol. It generates supervisory and unnumbered frames automatically without intervention by the host (CPU). The CPU must initialize the XPC-8 and supply buffers for the data fields of received and transmitted information frames. It is notified of important events via interrupts. The XPC-8 contains a transmitter, a receiver, an XPC-8 controller, and an interface unit (see Figure 1).

Architecture

Transmitter

The transmitter constructs frames on command from the XPC-8 controller. It handles the transmission of continuous flags, aborts, and idle channel indications automatically. It contains a transmitter controller, 4-byte first-in-first-out (FIFO) buffer, RAM, ROM, holding register, cyclic redundancy check (CRC) encoder, and zero inserter. The FIFO is used for temporary storage of data delivered from host memory to the transmitter by the interface unit via direct memory access (DMA). The transmitter memory (RAM/ROM) is used to store the various bytes needed to construct a frame. Frames are formed by sequentially loading the holding register with bytes read from the transmitter memory and FIFO, serially shifting these bytes through the zero inserter and, finally, sending the bit stream on the transmit data (TD) lead. Data is shifted on the falling edge of the transmit clock ($\overline{TC}$). The CRC encoder calculates the frame check sequence (FCS) and appends it to the control field, or to the data field for frames with data. The zero inserter performs bit stuffing to ensure data transparency.

Receiver

The receiver processes incoming data and notifies the XPC-8 controller of received frames and other link conditions. It contains a preprocessor, receiver controller, 6-byte FIFO, and CRC decoder. The preprocessor detects flags, aborts, and idle conditions on the data link and removes the 0s inserted for data transparency. Frames are identified and checked for proper format by the receiver controller. Data received as part of the information field of a frame is loaded into the FIFO. The interface unit, informed of the presence of received data, is responsible for reading FIFO data and writing it to system memory.

Frames are checked for errors by means of the FCS in the CRC decoder. The XPC-8 acts only on frames that are received error-free; frames received with errors are discarded. Frames with addresses other than the programmed command or response address are also discarded.

Interface Unit

The interface unit provides the interface between the host CPU and the XPC-8 transmitter and receiver via triple-channel DMA. It consists of four sections: an address arithmetic logic unit (AALU), a data section, a read/write controller, and a DMA controller.

The AALU contains four registers (not user-accessible) that are used to calculate and store the buffer pointers and byte counters for the transmit and receive channels. A fifth register is used to implement a third DMA channel for the processing of received acknowledgments. The additional channel enables the host to use its memory more efficiently by freeing the transmit data buffers as acknowledgments are received for them; therefore, data throughput is increased as a result of this extra DMA channel.

The read/write controller generates the control signals needed to access data from the host memory, while the data section routes the data from the host memory to various XPC-8 internal locations. The DMA controller coordinates the actions of the other three sections and connects them to the XPC-8 controller. Under command of the XPC-8 controller, the DMA controller is instructed to open data buffers for the transmitter and receiver in system memory. The locations of these data buffers are specified by the TLOOK and RLOOK table elements that the host CPU supplies.

When data is available for the transmitter, the read-write controller fetches bytes of data from system memory and routes them through the data section to the transmitter FIFO. The DMA continues to load bytes of data into the transmitter FIFO until the FIFO is full. The transmitter signals the interface unit for more data when two bytes or less remain in the FIFO. The loading process ends when the number of bytes specified in the TLOOK element has been loaded into the transmitter FIFO. The TLOOK element corresponding to the frame being sent is then placed in the unacknowledged state.

The reverse process is used for the receiver. The DMA controller instructs the read-write controller to write bytes of received data to system memory via the data section when the receiver FIFO contains two or more bytes of data. The interface unit continues to write data until it is notified by the receiver of an error-free end-of-frame condition. It then finishes writing the remaining bytes of data, updates the RLOOK element with the number of bytes received, and places the element into the frame complete state. If the receiver reports an error condition at the end of the frame, the RLOOK element is untouched and remains in the ready state.

XPC-8 Controller

The XPC-8 controller handles the interface between the transmitter, the receiver, and the interface unit, and contains all the logic needed to implement the X.25 protocol. Specific tasks of the XPC-8 controller include configuring the link as specified by the parameter and command registers, maintaining the status registers, directing the interface unit to acquire receive or transmit data buffers, directing the transmitter to send specific frames, managing timing functions, and using a set of interrupts to notify the host CPU of certain data link conditions.

Principles of Operation

CPU Interface

The CPU has access to 27 internal XPC-8 registers, which it uses to configure and monitor the XPC-8. The CPU configures the XPC-8 by writing the command and parameter registers. Status information, used to monitor XPC-8 operations, is accessed by reading one of the eight status registers. Special events are encoded in the interrupt register, which can then be accessed by the CPU.

Each register is assigned a unique address and can be accessed by providing the proper Motorola or Intel read/write cycle while the XPC-8 is selected ($\overline{CS}$ is low). Table 2 lists the XPC-8 register addresses.

Table 2. XPC-8 Register Addresses

Register Name	Symbol	Address (Hex)
Command register	CR	00
Status register 0	SR0	01
Status register 1	SR1	02
Status register 2	SR2	03
Status register 3	SR3	04
Status register 4	SR4	05
Status register 5	SR5	06
Status register 6	SR6	07
Status register 7	SR7	08
Interrupt register	IR	09
Parameter register 0	PR0	0A
Parameter register 1	PR1	0B
Parameter register 2	PR2	0C
Parameter register 3	PR3	0D
Parameter register 4	PR4	0E
Parameter register 5	PR5	0F
Parameter register 6	PR6	10
Parameter register 7	PR7	11
Parameter register 8	PR8	12
Parameter register 9	PR9	13
Parameter register 10	PR10	14
Parameter register 11	PR11	15
Parameter register 12	PR12	16
Parameter register 13	PR13	17
Parameter register 14	PR14	18
Parameter register 15	PR15	19
Parameter register 16	PR16	1A

XPC-8 Registers

The XPC-8 registers are divided into four types: command, status, interrupt, and parameter.

Command Register. This read/write register controls 7 XPC-8 functions: send permission, receive permission, mandatory disconnect, active/passive link initialization, password exchange mode, password verification, and link disconnect mode (see Table 3).

Status Registers. These 8 read-only registers contain such information as the present state of the XPC-8, V(S), V(R), NA, and LNA (see Figure 3 and Tables 4, 5, and 6).

Interrupt Register. This read-only register contains a 5-bit interrupt code and a lost interrupt (LSTIN) bit. It is backed by a 4-byte FIFO buffer whose output is automatically loaded into the interrupt register as soon as the contents of the register have been read by the CPU. If the 4-byte buffer overflows, the LSTIN bit of this register is set. The LSTIN bit is cleared as soon as the interrupt register is read. A zero-interrupt code indicates that all of the outstanding interrupts have been read by the host (see Tables 7 and 8).

Parameter Registers. These 17 write-only registers specify system constants and modes of operation. Examples include timer values, window size, TLOOK starting address, command and response address, and test modes. Parameter registers 1—16 can be written only when the logical link is disconnected and MDISC = 1 (see Figure 4 and Table 9).

Table 3. Command Register Definitions

Bit	7	6	5	4	3	2	1	0
Field	DISCMOD	PWOK2	PWOK1	PWXCH	ACT/PAS	RECR	MDISC	SEND

Bit	Symbol	Name/Description
0	SEND	**Send.** Controls the transmission of packets. If 0, it inhibits the XPC-8 from sending new packets; if 1, it enables the XPC-8 to send new packets. Retransmissions occur automatically, regardless of the SEND bit state. SEND is cleared during a valid reset or if a hard parity error occurs during a transmit channel DMA operation (see Table 8).
1	MDISC	**Mandatory Disconnect.** If 0, logical link establishment is permitted; if 1, the logical link goes to a logically disconnected state, and the XPC-8 responds to all inquiries with a disconnected mode (DM) frame and idles (transmit all 1s) between frames. MDISC is set during a valid reset.
2	RECR	**Receiver Ready.** Indicates to the XPC-8 the availability of receive data buffers in system memory. If 0, no receive data buffers are available; if 1, receive data buffers have been allocated and are available. RECR is cleared during a valid reset if a hard parity error (see Table 8) occurs during a receive channel DMA operation or a receiver overrun occurs.
3	ACT/PAS	**Active/Passive.** Specifies the XPC-8 action during link set-up. If 1, the XPC-8 actively pursues link set-up; if 0, the XPC-8 passively awaits link set-up. ACT/PAS is cleared during a valid reset.
4	PWXCH	**Password Exchange.** Specifies whether the XPC-8 should actively pursue a password exchange (PWXCH = 1) or passively await the initiation of a password exchange by a remote DTE (PWXCH = 0). PWXCH is cleared during a valid reset.
5	PWOK1	**Password Verified.** These bits are used by the host CPU to notify the XPC-8 of the results of its received password examination. These bits are cleared during a valid reset and are interpreted in conjunction with PWXCH (bit 4) as: **Code** (**b6 b5 b4**) — **Condition** 0 1 0 — Valid password command received 0 1 1 — Valid password response received 1 0 0 — Valid password command not received 1 0 1 — Valid password response not received
6	PWOK2	

Table 3. Command Register Definitions (Continued)

Bit	Symbol	Name/Description
7	DISCMOD	**Disconnect Mode.** Specifies which of two states the XPC-8 assumes when logically disconnected. If 0, the XPC-8 responds to all inquiries (command frames with their poll bits set) with a DM frame while logically disconnected. This implies that link set-up can be successfully pursued only from the local side of the link. If 1, the XPC-8 responds to all inquiries as specified by the X.25 protocol. In this case, link set-up can be successfully pursued from either side of the link. DISCMOD is set during a valid reset.

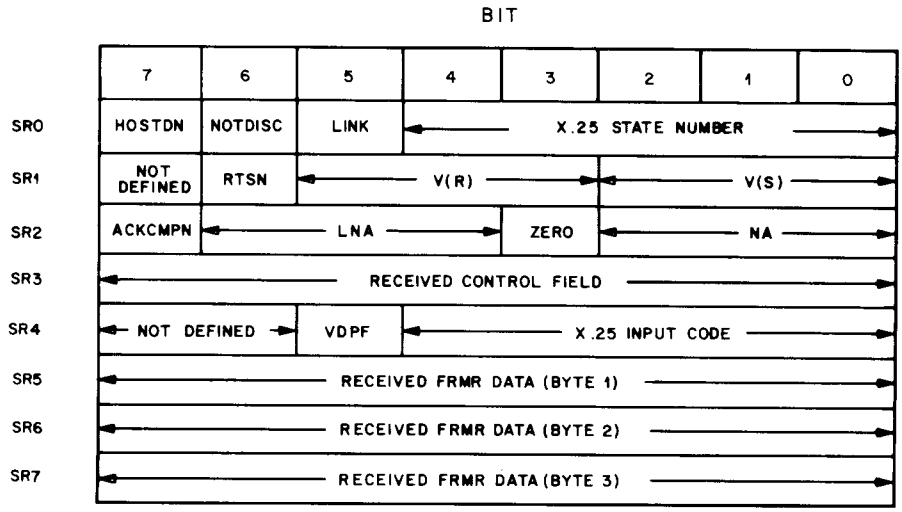


Figure 3. Status Registers

Table 4. Status Registers

Reg	Bit	Symbol	Name/Description
0	0—4	XST	**X.25 State Number.** Indicates the present state of the X.25 protocol (see Table 5).
0	5	LINK	**Link Status.** Indicates whether the XPC-8 has entered the information transfer phase. If 0, the XPC-8 has not entered this phase and information transfer is not permitted; if 1, the XPC-8 is in the information transfer phase (X.25 state $\geq$ S6).
0	6	NOTDISC	**Not Disconnected.** Indicates whether a logical link exists between two level 2 entities. If 0, the logical link is disconnected; if 1, the logical link is connected and the level 2 entities are communicating (X.25 state $\geq$ S4).
0	7	$\overline{\text{HOSTD}}$	**Host Done (Active Low).** Indicates whether the host CPU has reassigned transmit and receive data buffers in preparation for link reinitialization. If 0, the host has completed all transmit data buffer reassignments; if 1, the host must reassign transmit and receive data buffers before link reinitialization is permitted. This bit is cleared when the CPU writes to status register 0. Bits 0—6 of status register 0 cannot be written and $\overline{\text{HOSTD}}$ can only be cleared. It is the act of writing to this register that clears $\overline{\text{HOSTD}}$.

Table 4. Status Registers (Continued)

Reg	Bit	Symbol	Name/Description
1	0—2	V(S)	**Send State Variable.** Denotes the sequence number of the next in-sequence I frame to be transmitted. V(S) is used to index into the TLOOK table to indicate the TLOOK element that describes the next packet to be transmitted.
1	3—5	V(R)	**Receive State Variable.** Denotes the sequence number of the next in-sequence I frame to be received. V(R) is used to index into the RLOOK table to indicate the RLOOK element that describes the receive data buffer for the next received packet.
1	6	$\overline{\text{RST}}$	**Request to Send (Active Low).** If 0, the XPC-8 is requesting to use the physical link.
1	7	—	**Reserved.** This bit is used for testing purposes.
2	0—2	NA	**Next Acknowledge Expected.** Contains the sequence number of the earliest unacknowledged packet. If there are no outstanding packets, NA = V(S).
2	3	—	**Zero.** This bit is not used and must be cleared.
2	4—6	LNA	**Last Next Acknowledge Expected.** When NA is updated, the old value of NA is saved here. NA and LNA can be used to determine how many transmit data buffers have been acknowledged by the remote DXE and subsequently freed by the XPC-8.
2	7	$\overline{\text{ACKCMP}}$	**Acknowledgments Complete (Active Low).** To prepare for logical link reinitialization, the CPU must reallocate transmit buffers. Before reallocation begins, the CPU should check $\overline{\text{ACKCMP}}$ to be sure that the interface unit has finished processing all received acknowledgments. If 0, the interface unit has processed all the acknowledgments received from the remote DXE and the CPU can begin transmit buffer reallocation; if 1, received acknowledgments are still being processed.
3	0—7	RCF	**Received Control Field.** Holds the control field of the most recently received error-free frame.
4	0—4	XCT	**X.25 Input Code.** Contains an encoding of what the X.25 protocol considers its most recent input stimulus (see Table 6).
4	5	VDPF	**Valid Poll/Final.** Indicates whether the poll/final bit of the last error-free frame received was a 1 or a 0.
4	6—7	—	**Reserved.** These bits are used for testing purposes.
5—7	0—7	FRMRDF	**Received Frame Reject (FRMR) Data Field.** Registers 5, 6, and 7 hold the first, second, and third bytes, respectively, of the data field contained in the received FRMR frame.

Table 5. Status Register 0 — Bits 0—4 (XST)

State Number b4	b3	b2	b1	b0	State	Name
0	0	0	0	0	S0	Super logical disconnect
0	0	0	0	1	S1	Logical disconnect
0	0	0	1	0	S2a	Awaiting XID command
0	0	0	1	1	S2b	Awaiting XID response
0	0	1	0	0	S3	Link set-up
0	0	1	1	1	S4	Frame rejected
0	0	1	0	1	S5	Disconnect request
0	0	1	1	0	S6	Information transfer
0	1	0	0	0	S7	REJ frame sent
0	1	0	0	1	S8	Waiting for acknowledgment
1	0	0	0	1	S9	Station busy
0	1	0	1	0	S10	Remote station busy
0	1	1	1	1	S11	States 9 and 10
1	0	0	0	0	S12	States 8 and 9
0	1	0	1	1	S13	States 8 and 10
1	1	0	1	0	S14	States 8, 9, and 10
1	1	0	1	1	S15	States 7 and 9
0	1	1	0	0	S16	States 7 and 10
0	1	1	0	1	S17	States 7, 9, and 10

Table 6. Status Register — 4 Bits 0—4 (XCT)

Input Code	Description	Input Code	Description
0	Local stop	14	RNR command frame received
1	Local start	15	I frame received
2	TI expired	16	UA received
3	T4 expired	17	FRMR received
4	Unrecognized frame	18	DM received
5	Valid XID command received	19	SABM received
6	Station busy	20	Invalid N(R)
7	I frame available (code seen after reset)	21	Valid XID response
		22	T2 expired
8	Busy condition clears	24	Idle link detected for T3
9	Invalid N(S)	25	N2 exceeded
10	Initiate password exchange	26	DISC received
11	Wait for password exchange	28	REJ response received
12	REJ command frame received	29	RR response received
13	RR command frame received	30	RNR response received

Table 7. Interrupt Register

Bit	7	6	5	4 — 0
Field	LSTIN	ZERO	ZERO	INTERRUPT CODE

Bit	Symbol	Name/Description
0—4	—	**Interrupt Code.** This 5-bit number can take on any value from 0 to 27. Each value indicates a different interrupt condition, as described in Table 8.
5—6	—	**Zero.** These bits are not used and must be cleared.
7	LSTIN	**Lost Interrupt.** A 1 in this bit position indicates the loss of one or more interrupt codes due to the overflow of the interrupt FIFO. This bit is cleared upon reading the interrupt register.

Table 8. Interrupt Register Codes

Code	Symbol	Name/Description
0	NULL	**Null.** No interrupt conditions are outstanding.
1	SABM	**Set Asynchronous Balanced Mode Received.** An SABM command frame was received while the XPC-8 was in the information transfer phase.
2	UA	**Unnumbered Acknowledge Received.** An unnumbered acknowledgment frame was received while the XPC-8 was in the information transfer phase.
3	DM	**Disconnect Mode.** A DM frame was received.
4	FRMRR	**Frame Reject Received.** A frame reject (FRMR) frame was received. The data field of the FRMR is stored in status registers 5—7.
5	DISC	**Disconnect.** A disconnect (DISC) frame was received while the XPC-8 was in the information transfer phase.
6	IDLNK	**Idle Link.** An idle link condition has prevailed for a period in excess of T3.
7	N2EXC	**N2/C2 Counter Exceeded.** If this interrupt occurs during a password exchange, it should be interpreted as a C2 counter exceeded condition. Otherwise, it should be interpreted as an N2 counter exceeded condition.
8	RF1P	**Received Final Bit Before Poll.** A response frame with its final bit set was received without having transmitted a command frame with its poll bit set.
9	LK01	**Logical Link Up.** The XPC-8 has entered the information transfer phase (the logical link has come up).
10	LK10	**Logical Link Down.** The XPC-8 has left the information transfer phase (the logical link has gone down).
11	XIDR	**XID Received.** An XID frame was received and its data field placed in system memory.
12	NOXIDR	**No XID Received.** An XID command frame was transmitted and an XID response frame was not received for a period of T4.
13	FRMRXW	**Frame Reject Transmitted (W = 1).** A frame reject was transmitted because a frame was received with an invalid control field.

Table 8. Interrupt Register Codes (Continued)

Code	Symbol	Name/Description
14	FRMRXX	**Frame Reject Transmitted (X = 1, W = 1).** A frame reject was transmitted because a frame was received whose control field is considered invalid because the frame contains an information field that is not permitted, or because the frame is a supervisory or unnumbered frame of incorrect length.
15	FRMRXY	**Frame Reject Transmitted (Y = 1).** A frame reject was transmitted because the information field received exceeded the maximum established capacity set by parameter N1.
16	FRMRXZ	**Frame Reject Transmitted (Z = 1).** A frame reject was transmitted because the control field received contained an invalid N(R).
17	PKR	**Packet Received.** The XPC-8 has received an I frame and stored its information field in system memory.
18	XBA	**Transmitted Block Acknowledged.** The XPC-8 has received and processed acknowledgments for one or more previously transmitted I frames.
19	RCVOVR	**Receiver Overrun.** The receiver FIFO data buffer has overflowed because information field data bytes were being received faster than the interface unit could store them in system memory. The receiver FIFO is 6 bytes deep.
20	XUNDR	**Transmitter Underrun.** The transmitter FIFO data buffer has underflowed because information field data bytes were being transmitted faster than the interface unit could replenish the FIFO with data read from system memory. If the transmitter FIFO is empty when more data is needed for transmission, the transmitter aborts the frame and generates this interrupt. The XPC-8 attempts to retransmit the information frame if the SEND bit remains set. The host CPU may discontinue retransmission attempts by clearing the SEND bit. The transmitter FIFO is 4 bytes deep.
21	RLKNRDY	**RLOOK Not Ready.** The XPC-8 has read the RLOOK table element referenced by V(R) and it was not ready (i.e., RECRDY = 0). The XPC-8 goes to a station busy state.
22	CTSLST	**Clear-to-Send Lost.** The clear-to-send ($\overline{CTS}$) input has gone high while the XPC-8 was in the information transfer phase.
23	CARFND	**Carrier Found.** The carrier detect ($\overline{CD}$) signal from the physical link has been established (went low).
24	CARLST	**Carrier Lost.** The carrier detect ($\overline{CD}$) signal from the physical link has been lost (went high).
25	NOAD	**No Address.** The TLOOK starting address is 0 (not a valid starting address).
26	HPE	**Hard Parity Error.** The XPC-8 was notified of a parity error, via the $\overline{PARV}$ pin, on each of two attempts to complete a DMA read or write cycle. If the error occurred during a transmit channel DMA operation, the SEND bit of the command register is cleared. If the error occurred during a receive channel DMA operation, the RECR bit of the command register is cleared.
27	NULIF	**Null I Frame Received.** An I frame without an information field was received. The XPC-8 treats null I frames as any other I frame except that it generates this interrupt.

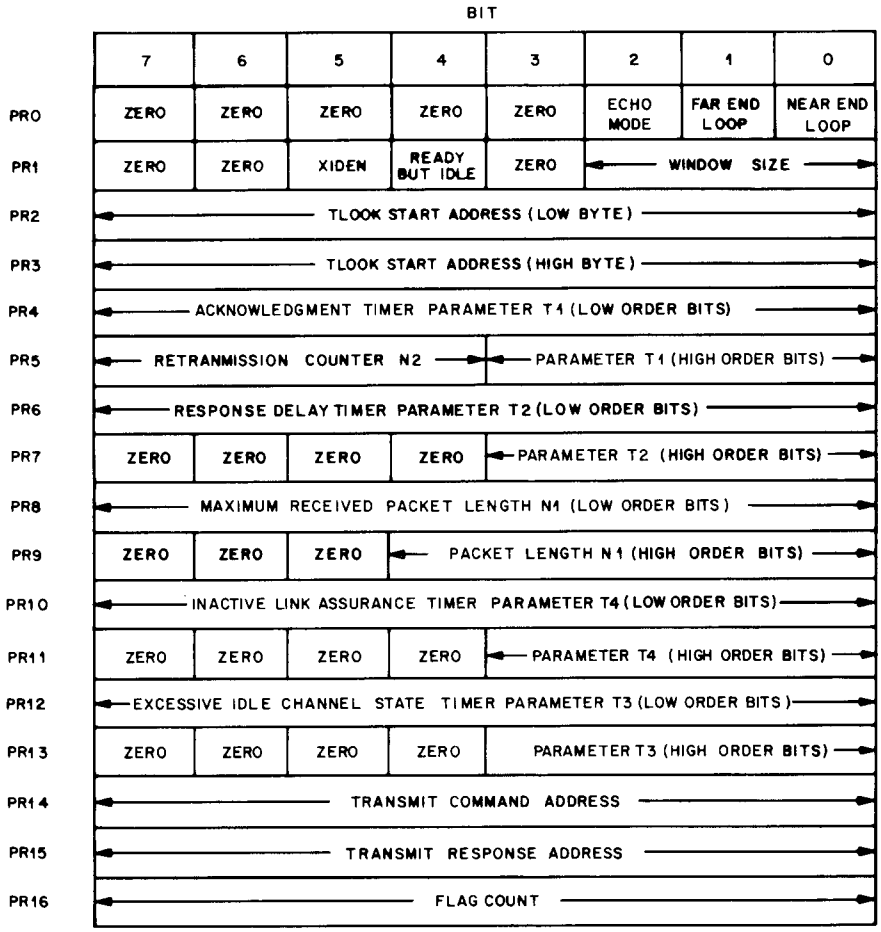


Figure 4. Parameter Registers

Table 9. Parameter Register Definitions

Reg	Bit	Symbol	Name/Description
0	0	NELT	**Near-End Loop Test.** Setting this bit causes the XPC-8 to enter the near-end loopback test mode.
0	1	FELT	**Far-End Loop Test.** Setting this bit causes the XPC-8 to enter the far-end loopback test mode.
0	2	ECHO	**Echo Mode.** Setting this bit causes the XPC-8 to transmit what it receives unaltered (i.e., the RD and TD pins are internally connected).
0	3—7	—	**Zero.** These bits must be cleared.
1	0—2	k	**Window Size.** Maximum allowable number of outstanding I frames. An outstanding I frame is any frame that has not been acknowledged by the remote DXE (either DTE or DCE). The window size must not equal 0.
1	3	—	**Reserved.** This bit must be cleared.
1	4	RDYIDL	**Ready But Idle.** The bit has meaning only when the logical link is disconnected and MDISC = 0. If RDYIDL is 0, the XPC-8 sends flags between frames; if 1, the XPC-8 idles between frames.
1	5	XIDEN	**XID Enable.** Setting this bit enables the password exchange mechanism.
1	6—7	—	**Zero.** These bits must be cleared.

Table 9. Parameter Register Definitions (Continued)

Reg	Bit	Symbol	Name/Description
2—3	0—7	TLOOKSA	**TLOOK Table Starting Address.** Indicates the starting address in system memory of the first element in the transmitter look-up TLOOK table. The address must not equal 0.
4	0—7	T1 (low byte)	**Acknowledgment Timer Parameter.** T1 is the maximum time that the XPC-8 waits for an acknowledgment. The period of the T1 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T1} = 32{,}768 \times \frac{\text{T1 parameter}}{f_{CKO}}$.
5	0—3	T1 (high bits)	
5	4—7	N2	**Transmission and Retransmission Counter.** The maximum allowable number of transmissions and retransmissions of a frame without receiving an acceptable response.
6	0—7	T2 (low byte)	**Response Timer Parameter.** T2 is the maximum time that the XPC-8 waits before responding to an inquiry from the remote DXE. The period of the T2 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T2} = 32{,}768 \times \frac{\text{T2 parameter}}{f_{CKO}}$.
7	0—3	T2 (high bits)	
7	4—7	—	**Zero.** These bits must be cleared.
8	0—7	N1 (low byte)	**Maximum Received Packet Length.** The maximum number of bytes that the receiver accepts in the information field of a frame before rejecting the received frame.
9	0—4	N1 (high bits)	
9	5—7	—	**Zero.** These bits must be cleared.
10	0—7	T4 (low byte)	**Inactive Link Assurance Timer Parameter.** During intervals when the T1 timing function is not performed (i.e., there are no outstanding unacknowledged I frames or P-bit frames), an appropriate S-format command frame with the P-bit set is transmitted every T4 time units to verify the status of the remote DXE. The period of the T4 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T4} = 32{,}768 \times \frac{\text{T4 parameter}}{f_{CKO}}$.
11	0—3	T4 (high bits)	
11	4—7	—	**Zero.** These bits should be cleared.
12	0—7	T3 (low byte)	**Excessive Idle Channel State Timer Parameter.** T3 specifies the amount of time that the XPC-8 accepts the reception of an idle condition before taking alternate actions. The period of the T3 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T3} = 32{,}768 \times \frac{\text{T3 parameter}}{f_{CKO}}$.
13	0—3	T3 (high bits)	
13	4—7	—	**Zero.** These bits must be cleared.
14	0—7	TCA	**Transmit Command Address.** Address field of the command frames transmitted by the XPC-8 (the station address of the far end of the link).

Table 9. Parameter Register Definitions (Continued)

Reg	Bit	Symbol	Name/Description
15	0—7	TRA	**Transmit Response Address.** Address field of the response frames transmitted by the XPC-8 (the station address of this station).
16	0—7	FLGCNT	**Flag Count.** Specifies the minimum number of extra flags between frames. The value of FLGCNT is cleared on reset. A value of 0 causes the minimum number of flags between frames to default to 1. FLGCNT is a special feature of the XPC-8 and is not part of the X.25 protocol.

Bus and I/O Logic

Bits A0—A5 of the address bus are bidirectional and are used to access the 27 internal registers. When the XPC-8 is selected, R/$\overline{W}$, $\overline{WE}$, $\overline{DSRE}$, and address lines A0—A5 become inputs; $\overline{READY}$ becomes an output.

DMA operations are controlled by the interface unit. The XPC-8 uses DMA to access system memory to read and write TLOOK table elements, RLOOK table elements, and data fields of information frames. A daisy-chain DMA priority scheme can be implemented for multiple XPC-8 applications.

The data bus can be configured to be either Motorola or Intel compatible. Master reset is used for bus mode selection.

XPC-8 Master Reset

When the master reset ($\overline{MR}$) is low, all outputs are put into the high-impedance state and the parameter registers except for the TLOOK starting address (parameter registers 2 and 3) = 0 are cleared. The command register is set to 82H (DISCMOD = 1, MDISC = 1, all other bits = 0).

In addition, the master reset is used to choose between the Intel and Motorola bus modes. A reset pulse must be held low for at least six cycles of CKO to be considered a valid reset request. Glitch protection circuitry guarantees that glitches of less than one CLK period are ignored. If a single valid reset request is provided, the XPC-8 bus is configured for the Motorola bus standard. If a second valid reset request is provided within 30 cycles of CKO, the XPC-8 switches to the Intel bus standard. $\overline{MR}$ must be held high for at least six cycles of CKO after a reset pulse before the XPC-8 can recognize a second reset pulse. Any reset pulses occurring after the 30 cycles of CKO are interpreted as a new reset sequence (see Figure 11).

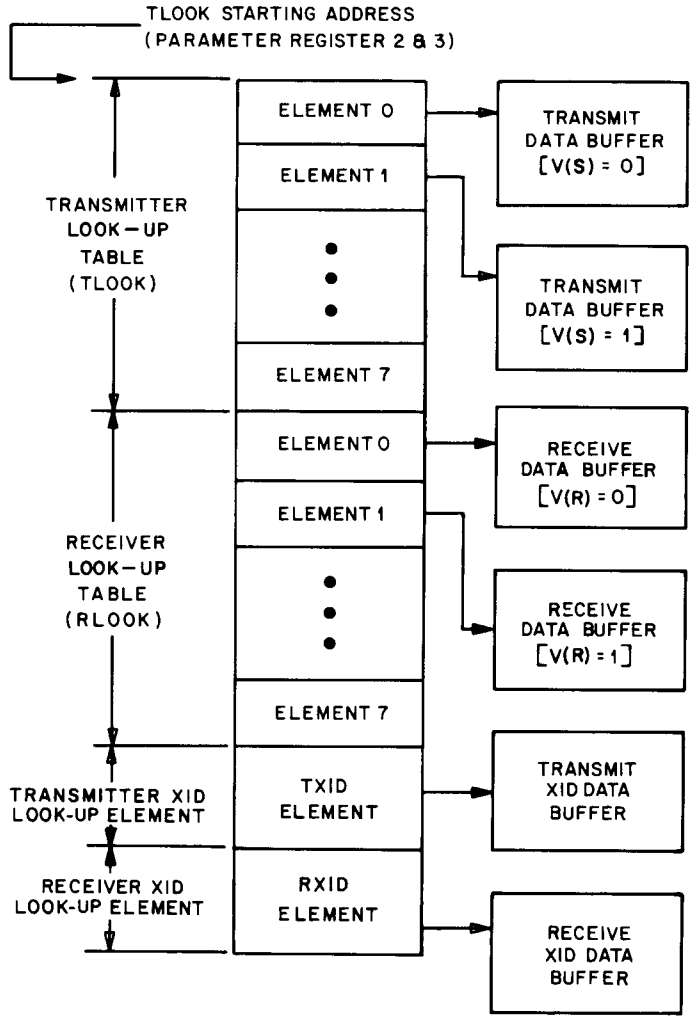
Transmitter and Receiver Look-Up Tables

System memory contains data buffers that store transmit and receive data. The pointers used to access these buffers are stored in look-up tables in system memory. The location of data to be transmitted is described by pointers in the transmitter look-up table (TLOOK) elements and the location of data to be received is described by pointers in the receiver look-up table (RLOOK) elements. Figure 5 is a diagram of the system memory interface.

The TLOOK table is a block of eight 8-byte elements in system memory that starts at the TLOOK starting address (parameter registers 2 and 3). Each element in the TLOOK table describes a buffer corresponding to one packet of data to be transmitted by the XPC-8. The TLOOK list of elements is a modulo-8 circular queue. Figure 6 and Table 10 present the bit assignments and descriptions for the TLOOK elements.

The RLOOK table is a block of eight 8-byte elements in system memory that immediately follows the TLOOK table. Each element in the RLOOK table describes a buffer corresponding to one packet to be received by the XPC-8. The RLOOK list of elements is also a circular queue. Figure 7 and Table 11 present the bit assignments and descriptions for the RLOOK elements.

In addition to the two look-up tables described above, there are two single-element look-up tables (TXID and RXID) that are used only during password exchange. They are located in system memory immediately following the RLOOK elements. The TXID and RXID look-up tables are used to describe the transmit password and receive password data buffers, respectively. Their format is identical to that of the TLOOK and RLOOK elements.



Note: Each element has 8 bytes of data.

Figure 5. XPC-8/CPU System Memory Interface

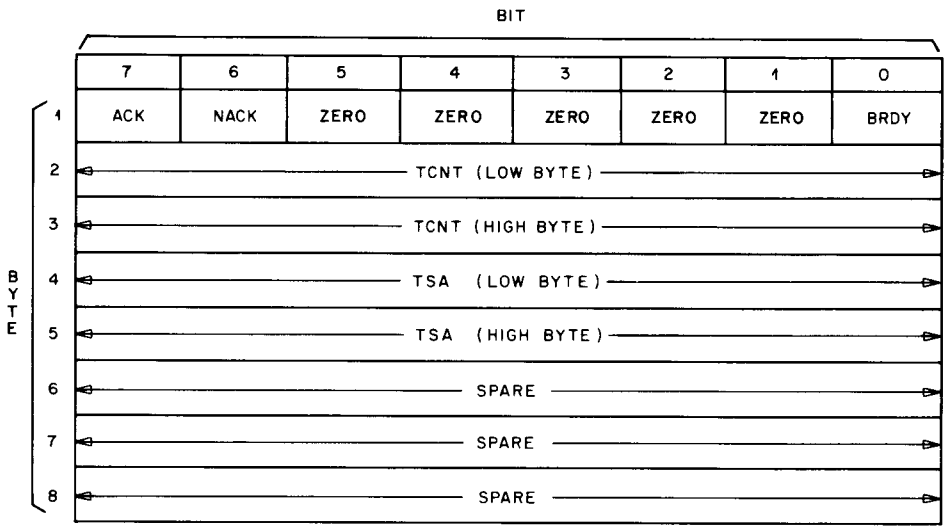


Figure 6. TLOOK Element

Table 10. TLOOK Element Definitions

Reg	Bit	Symbol	Name/Description
1	0	BRDY	**Buffer Ready.** Setting this bit indicates to the XPC-8 that data associated with this element is ready to be transmitted. BRDY should be the last bit of the TLOOK element to be set by the CPU after preparing a buffer. The SEND bit of the command register should then be set to command the XPC-8 to begin transmitting packets. The XPC-8 clears BRDY and sets NACK after all of the data associated with this element has been accessed by DMA and loaded into the transmitter FIFO.
1	1—5	—	**Zero.** These bits should be cleared.
1	6	NACK	**Not Acknowledged.** The XPC-8 sets NACK and clears BRDY after all the data associated with this look-up element has been accessed and loaded into the transmitter FIFO. The XPC-8 clears this bit when the frame associated with this element has been acknowledged.
1	7	ACK	**Acknowledged.** The XPC-8 sets ACK and clears NACK when an acknowledgment is received for the packet associated with this look-up element. An XBA interrupt is generated to notify the CPU of one or more acknowledgments.
2	0—7	TCNT (low byte)	**Transmit Count.** The number of bytes in a transmit data packet is specified by this 16-bit number. The X.25 protocol standard limits the number of bytes in an information field to 4 K + 4 (including the packet header) and, therefore, bits 6 and 7 of byte 3 should always be cleared.
3	0—7	TCNT (high byte)	
4	0—7	TSA (low byte)	**Transmit Start Address.** This 16-bit number is the location in system memory of the first byte of transmit data associated with this TLOOK element.
5	0—7	TSA (high byte)	
6—8	0—7	—	**Reserved.** Not used.

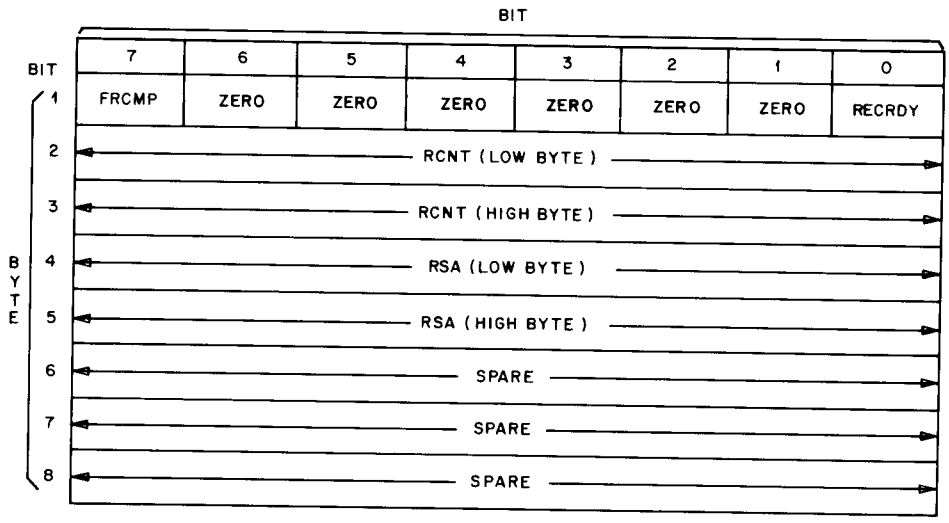


Figure 7. RLOOK Element

Table 11. RLOOK Element Definitions

Reg	Bit	Symbol	Name/Description
1	0	RECRDY	**Receiver Ready.** Setting this bit indicates to the XPC-8 that the data buffer associated with this element is ready to receive data. The receive start address field of the RLOOK element should be specified before the CPU sets the RECRDY bit. After the XPC-8 receives a valid packet and stores the information field in the buffer associated with the look-up element, it clears RECRDY and sets FRCMP.
1	1—6	—	**Zero.** These bits should be cleared.
1	7	FRCMP	**Frame Complete.** When a valid packet is received, the XPC-8 writes the receive count, clears RECRDY, and sets FRCMP. A PKR interrupt is used to notify the CPU of the received packet.
2	0—7	RCNT (low byte)	**Receiver Count.** This 16-bit number specifies how many bytes of system memory have been filled by the receive packet. The XPC-8 writes this location after a valid information frame has been received and written to system memory without error.
3	0—7	RCNT (high byte)	
4	0—7	RSA (low byte)	**Receive Start Address.** This 16-bit number specifies the address in system memory of the first byte of receive data in the packet. This address is written only by the CPU.
5	0—7	RSA (high byte)	
6—8	0—7	—	**Reserved.** Not used.

DMA Operation

DMA on the XPC-8 is used to read and write data fields of I frames, data fields of XID frames, and the TLOOK and RLOOK tables in system memory. To initiate a DMA cycle, the XPC-8 requests the use of the data bus by forcing $\overline{\text{DREQ}}$ low. The host CPU signifies that the bus is available for use by the XPC-8 by forcing $\overline{\text{DACK}}$ low. This allows $\overline{\text{DSRE}}$, $\overline{\text{WE}}$, R/$\overline{\text{W}}$, $\overline{\text{AS}}$, and A0—A15 to become outputs.

Once the XPC-8 has control of the system bus, it expects to have use of the bus until it finishes its DMA operations. The XPC-8 holds the system bus for a maximum of 5 read or write cycles.

Slow memory handshaking is provided through the $\overline{\text{READY}}$ input. A read or a write continues until $\overline{\text{READY}}$ goes low. A DMA write cycle must not extend more than 100 μs.

Parity checks are not performed on-chip. The results of any off-chip parity checking schemes should be supplied through $\overline{\text{PARV}}$. $\overline{\text{PARV}}$ is sampled on the falling edge of the CKO cycle following the detection of valid $\overline{\text{READY}}$. If $\overline{\text{PARV}}$ is sampled low, parity is assumed to be valid. If $\overline{\text{PARV}}$ is high, the XPC-8 makes a second attempt to complete the read or write operation. If the second attempt also fails, a hard parity error interrupt is generated and DMA operations halts. $\overline{\text{PARV}}$ should be tied low if parity is not being checked.

A priority DMA scheme can be implemented with no additional hardware in a daisy-chain fashion for multiple XPC-8 applications. The $\overline{\text{DREQ}}$ of the lowest priority XPC-8 is tied to the $\overline{\text{LPDREQ}}$ input of the next highest priority XPC-8. The $\overline{\text{DREQ}}$ of the highest priority XPC-8 is tied to the $\overline{\text{BUSREQUEST}}$ input of the CPU. The $\overline{\text{BUSGRANT}}$ output of the CPU is tied to the $\overline{\text{DACK}}$ of the highest priority XPC-8. The $\overline{\text{LPDACK}}$ of the highest priority XPC-8 is tied to $\overline{\text{DACK}}$ of the next highest priority XPC-8 and this continues until the lowest priority XPC-8 is reached. The $\overline{\text{LPDREQ}}$ of the lowest priority XPC-8 must be tied high (see Figure 8).

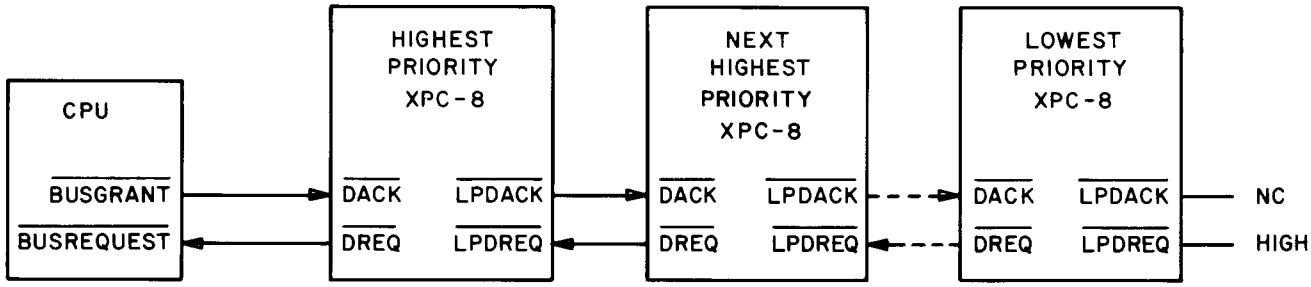


Figure 8. DMA Priority Scheme Interconnection

Test Modes

The XPC-8 has four test modes: near-end loopback, far-end loopback, echo, and output 3-state.

The near-end loopback test permits the XPC-8 to talk to itself. The transmitter output and receiver input are internally connected while in this mode of operation. The receiver automatically interchanges the command and response addresses to allow the protocol to function properly.

The far-end loopback test is used to check the near-end XPC-8 and the data link. The local XPC-8 is placed in far-end loopback test mode, while the remote XPC-8 is placed in echo mode. The receiver in the local XPC-8 interchanges the command and response addresses. Data arriving at the remote XPC-8, which is in the echo mode, is internally routed without CPU or XPC-8 intervention to the transmitter data output.

Output buffers are 3-stated whenever $\overline{\text{MR}}$ is forced low. This feature should be used during board testing/debugging.

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input voltage:					
low	V_{IL}	—	0.8	V	—
high	V_{IH}	2.2*	—	V	—
Output voltage:					
low	V_{OL}	—	0.4	V	I_{OL} = 2.2 mA
high	V_{OH}	2.4	—	V	I_{OH} = −400 μA
Power supply current	I_{DD}	—	460	mA	—
Output off current:					
low	I_{OZL}	—	−10	μA	V_{OL} = 200 mV
high	I_{OZH}	—	10	μA	V_{OH} = 5.25 V
Power dissipation	PD	—	2.2	W	V_{DD} = 5.0 V

* MOS input level.

Maximum Ratings

Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Ambient operating temperature (T_A) range ..... 0 to 70 °C
Storage temperature (Tstg) range ..... 0 to 85 °C
Power dissipation (PD) ..... 2.5 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Table 12. DMA Timing

Symbol	Description	Min	Max	Unit
tCKOHASH	$\overline{AS}$ release offset	—	125	ns
tCKOHASL	$\overline{AS}$ offset	—	102	ns
tCKOLAV	Address settle time	—	92	ns
tCKOLAZ	Address disable offset	—	160	ns
tCKOHCKOH	CKO period	400	8000	ns
tCKOLDRH	$\overline{DREQ}$ release offset	—	95	ns
tCKOLDRL	$\overline{DREQ}$ offset	—	140	ns
tCKOHDV	Data valid offset	—	200	ns
tCKOHREH	$\overline{RE}$ release offset	—	160	ns
tCKOLDSH	$\overline{DS}$ release offset (write)	—	100	ns
tCKOHDSH	$\overline{DS}$ release offset (read)	—	160	ns

Table 12. DMA Timing (Continued)

Symbol	Description	Min	Max	Unit
tCKOLDSL	$\overline{DS}$ low offset (Motorola, read)	—	44	ns
tCKOLDSL	$\overline{DS}$ low offset (Motorola, write)	—	44	ns
tCKOLREL	$\overline{RE}$ low offset (Intel, read)	—	44	ns
tCKOLWEH	$\overline{WE}$ release offset	—	70	ns
tCKOLWEL	$\overline{WE}$ low offset (Intel, write)	—	34	ns
tCLKHCKOH	CLK offset	—	130	ns
tCLKHCLKH	CLK period	200	4000	ns
tDALAV	Address enable offset	—	135	ns
tDALCKOL	$\overline{DACK}$ set-up time	230	—	ns
tDVCKOH	Data set-up time	170	—	ns
tPALCKOL	$\overline{PARV}$ set-up time	180	—	ns
tRDYLCKOH	$\overline{READY}$ set-up time	145	—	ns

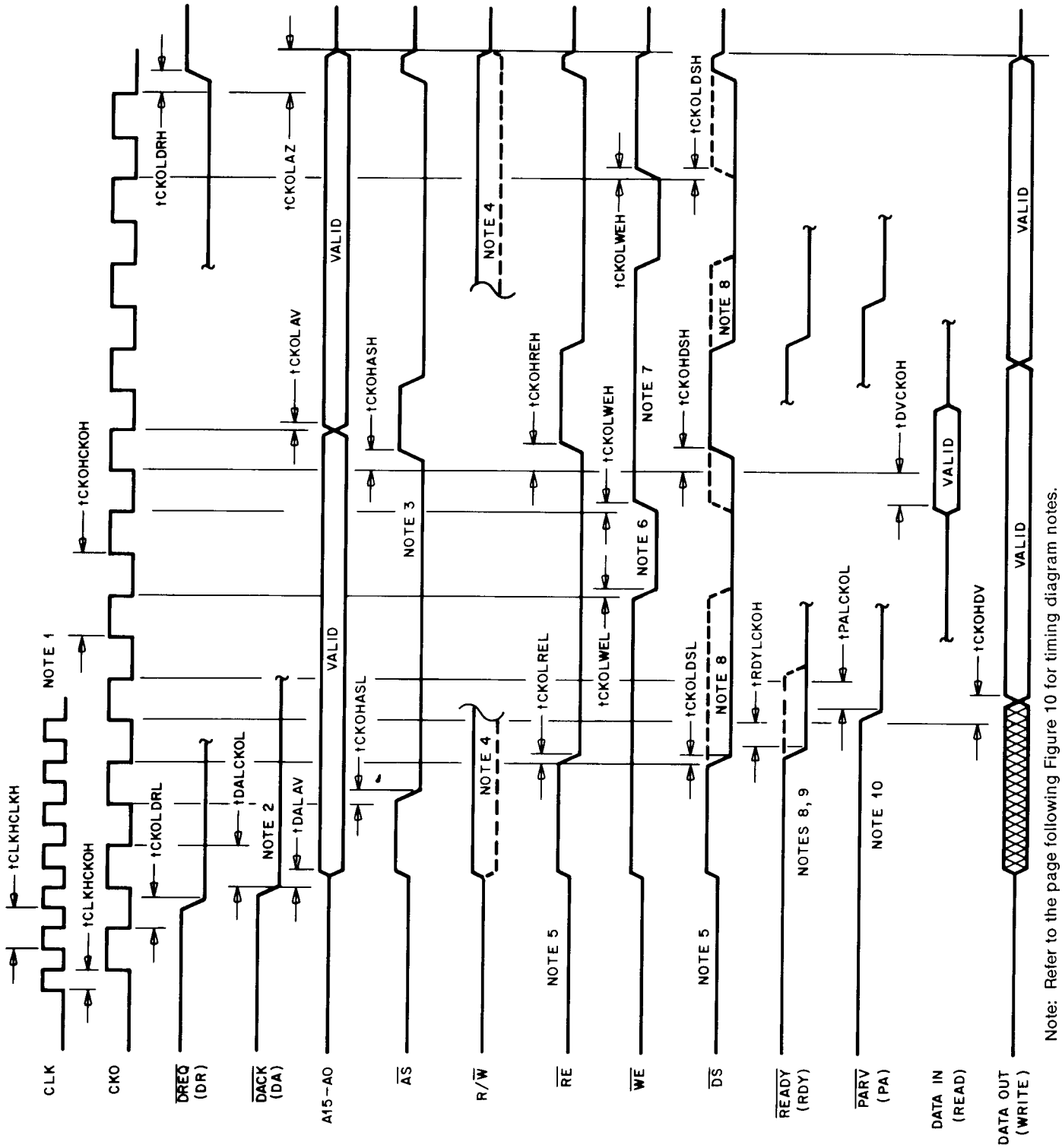
Table 13. CPU Read and Write Timing

Symbol	Description	Min	Max	Unit
tAVCSL	Address valid before $\overline{CS}$ low (address set-up)	0	—	ns
tDSLDV	$\overline{DS}$ low to data valid (access time)	—	150	ns
tRELDV	$\overline{RE}$ low to data valid (access time)	—	150	ns
tDSHDZ	$\overline{DS}$ high to data 3-state	—	190	ns
tREHDZ	$\overline{RE}$ high to data 3-state	—	190	ns
tCKOHRDYH	$\overline{READY}$ release offset (read)	—	250	ns
tCKOHRDYH	$\overline{READY}$ release offset (write)	—	345	ns
tCKOHRDYL	$\overline{READY}$ active offset (read)	—	160	ns
tCKOHRDYL	$\overline{READY}$ active offset (write)	—	160	ns
tCSLCKOL	$\overline{CS}$ set-up time	390	—	ns
tDSHRWV	$\overline{DS}$ release to R/$\overline{W}$ change	50	—	ns
tRWVDSL	R/$\overline{W}$ release to $\overline{DS}$ change	90	—	ns
tDSHCKOL	$\overline{DS}$ release set-up time	390	—	ns
tDSLCKOL	$\overline{DS}$ set-up time	212	—	ns
tDSHAX	$\overline{DS}$ high to address change	0	—	ns
tAVDSL	Address valid Before $\overline{DS}$ low (address set-up)	0	—	ns
tDVCKOH	Data set-up time	0	—	ns
tDXCKOH	Data hold time	155	—	ns
tREHCKOL	$\overline{RE}$ release set-up time	390	—	ns
tRELCKOL	$\overline{RE}$ set-up time	212	—	ns
tREHAX	$\overline{RE}$ high to address change	0	—	ns
tAVREL	Address valid before $\overline{RE}$ low (address set-up)	0	—	ns
tWEHCKOL	$\overline{WE}$ release set-up time	280	—	ns
tWELCKOL	$\overline{WE}$ set-up time	250	—	ns
tWEHAX	$\overline{WE}$ high to address change	0	—	ns
tAVWEL	Address valid before $\overline{WE}$ low (address set-up)	0	—	ns

Table 14. Reset Timing

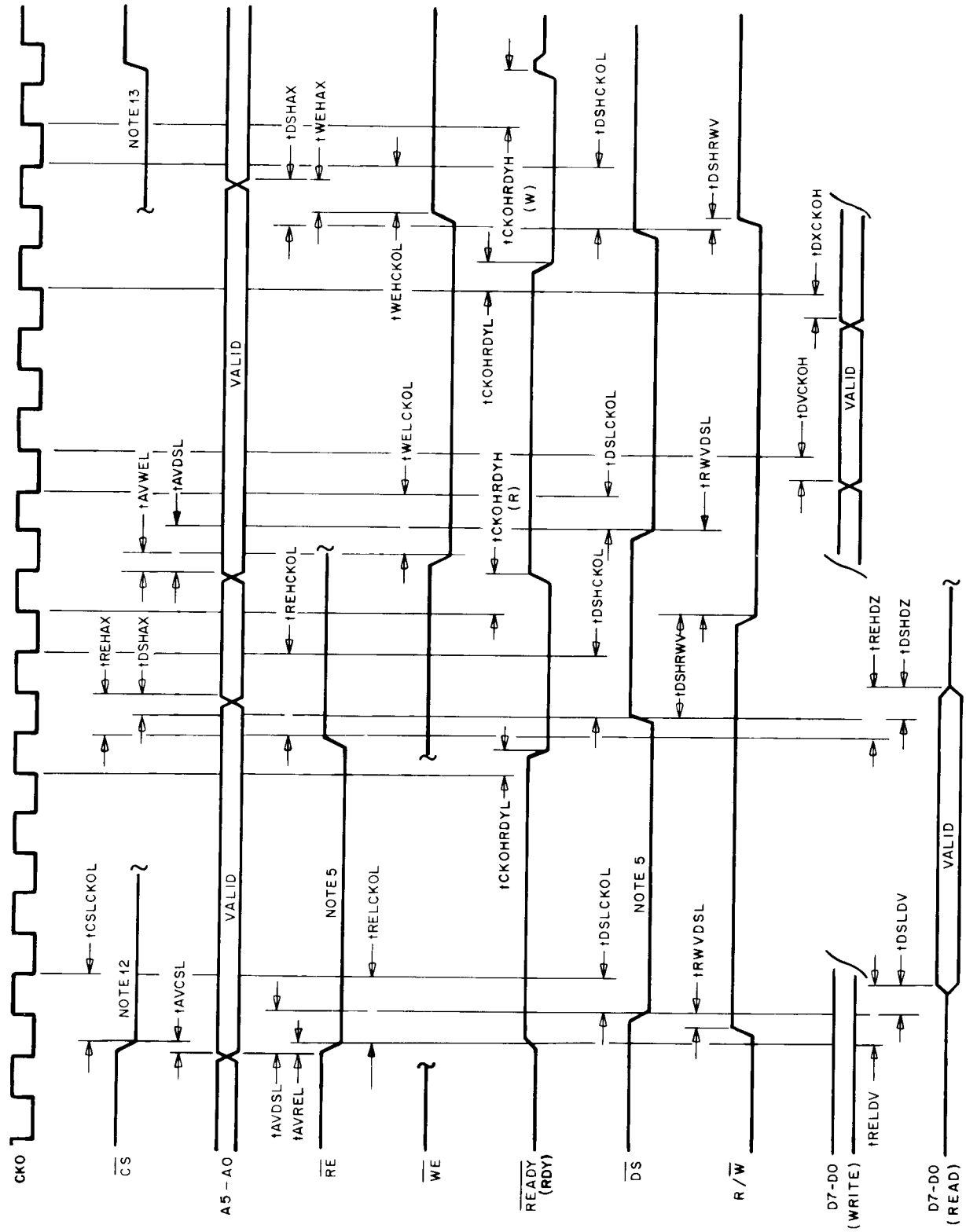
Symbol	Description	Min	Max	Unit
tMRHMRH	Time allowed for switching to Intel bus mode (Intel)	—	30tCKOHCKOH	—
tMRHMRL	Time between reset pulses (Intel)	6tCKOHCKOH	—	—
tMRLMRH	Valid reset time (Motorola and Intel)	6tCKOHCKOH	—	—
tPU	Power-up delay time (Motorola and Intel)	40tCKOHCKOH	—	—

Timing Diagrams



Note: Refer to the page following Figure 10 for timing diagram notes.

Figure 9. DMA Timing Diagram

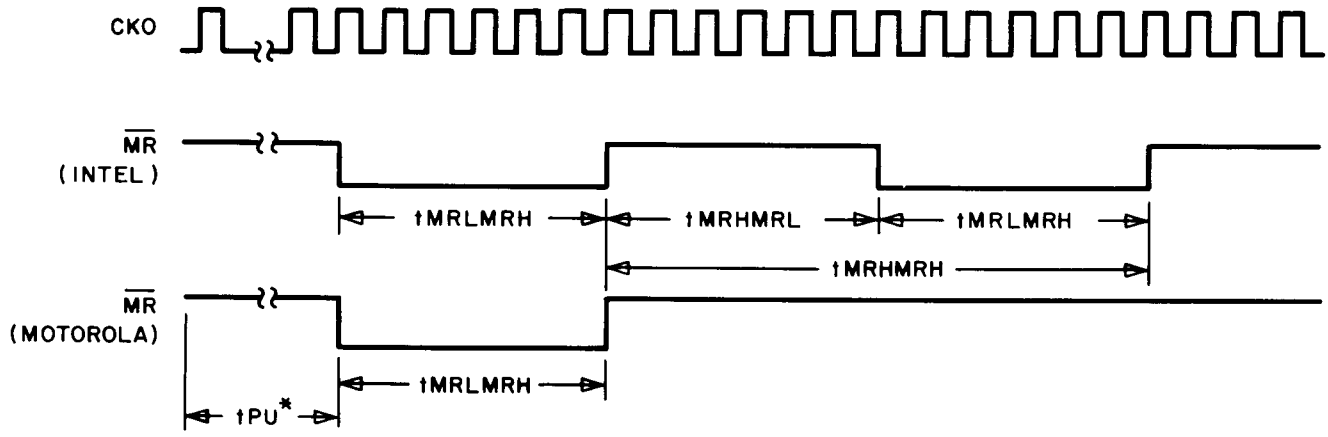


Note: Refer to the page following Figure 10 for timing diagram notes.

Figure 10. CPU Read and Write Cycles

Timing Diagram Notes for Figures 9 and 10

1. CLK must have a duty cycle of between 45% and 55%.
2. $\overline{DACK}$ is sampled on every falling edge of CKO until it tests low.
3. Read or write cycles can extend for one extra CKO cycle to allow for internal synchronization.
4. R/$\overline{W}$ is valid by the first falling edge of $\overline{AS}$. The dotted line is for write cycle only. Entire DMA cycle is for either a read or a write.
5. $\overline{DS}$ and $\overline{RE}$ are multiplexed on the same pin. $\overline{RE}$ is selected for the Intel bus configuration; $\overline{DS}$ is selected for the Motorola bus configuration.
6. The write cycle must not be extended (using $\overline{READY}$) for more than 100 μs.
7. If a $\overline{PARV}$ error occurs, the trailing edge of $\overline{WE}$ is concurrent with the trailing edge of $\overline{AS}$.
8. The dotted line is for write only.
9. $\overline{READY}$ is sampled on every rising edge of CKO until it tests low.
10. $\overline{PARV}$ is sampled on the falling edge of CKO following the detection of a valid $\overline{READY}$.
11. During TLOOK and RLOOK element reads, the read cycles are extended an additional two CKO cycles.
12. Due to internal synchronization, there may be an extra CKO cycle inserted before the falling edge of $\overline{READY}$.
13. Forcing $\overline{CS}$ high while executing a read or write cycle ends that cycle.

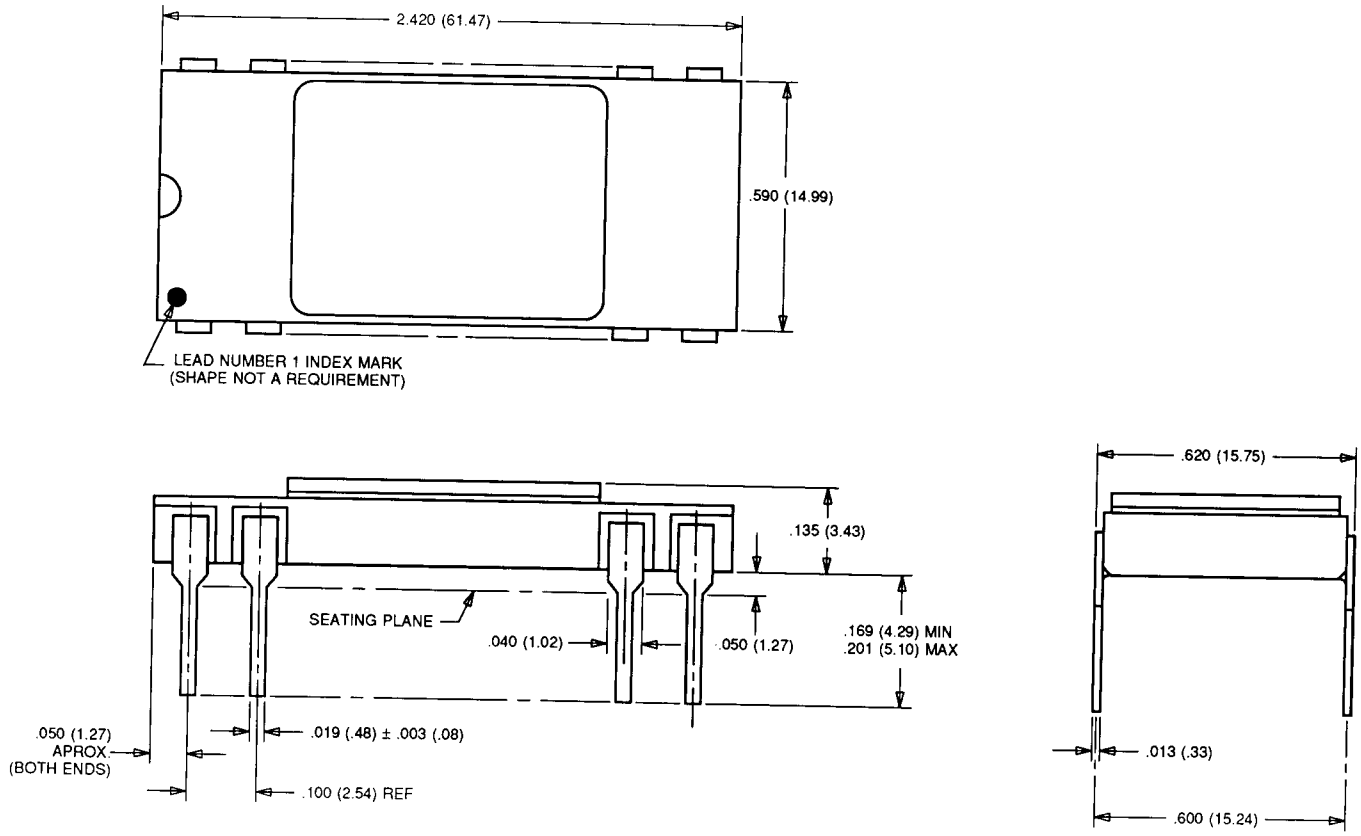


* Time required from power-up to the first reset.

Figure 11. Motorola and Intel Reset Sequences

Outline Diagram

Dimensions in inches and (millimeters).



Ordering Information

Device Code	Package	Temperature
T7100A-BC	48-pin ceramic DIP	0 to 70°C

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- AT&T Microelectronics
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  555 Union Boulevard
  Allentown, PA 18103
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  Tel. 259-6622
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