Signetics

74194, LS194A, S194
Shift Registers

4-Bit Bidirectional Universal Shift Register
Product Specification

Logic Products

- **Buffered clock and control inputs**
- **Shift left and shift right capability**
- **Synchronous parallel and serial data transfers**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

DESCRIPTION

The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74194	36MHz	39mA
74LS194A	36MHz	15mA
74S194	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74194N, N74LS194AN, N74S194N
Plastic SO-16	*N74LS194AD, N745194D*

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
$Q_0 - Q_3$	Outputs	10ul	10Sul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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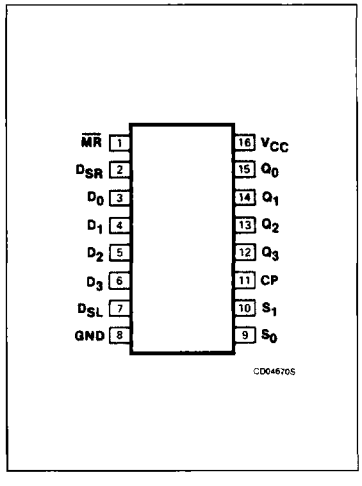
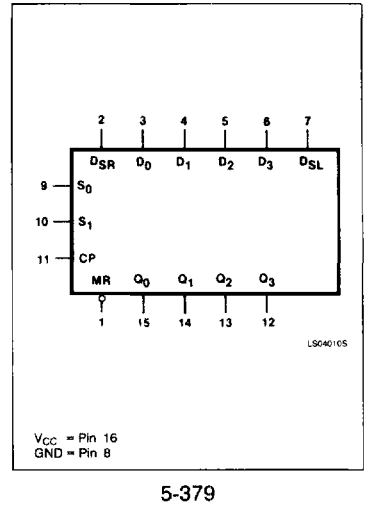
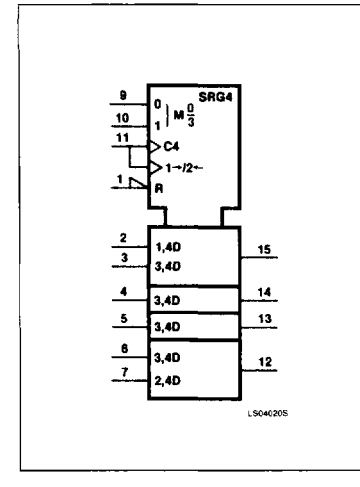
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



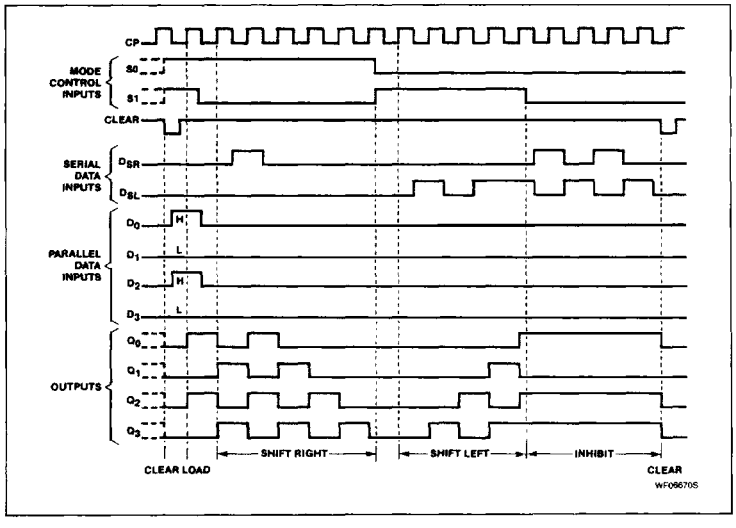
MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l[a]	l[a]	X	X	X	q_0	q_1	q_2	q_3
Shift left	↑	H	h	l[a]	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l[a]	X	h	X	q_1	q_2	q_3	H
Shift right	↑	H	l[a]	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l[a]	h	h	X	X	H	q_0	q_1	q_2
Parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

NOTE:
a. The HIGH-to-LOW transition of the S_0 and S_1 inputs on the 74194 should only take place while CP is HIGH for conventional operation.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES

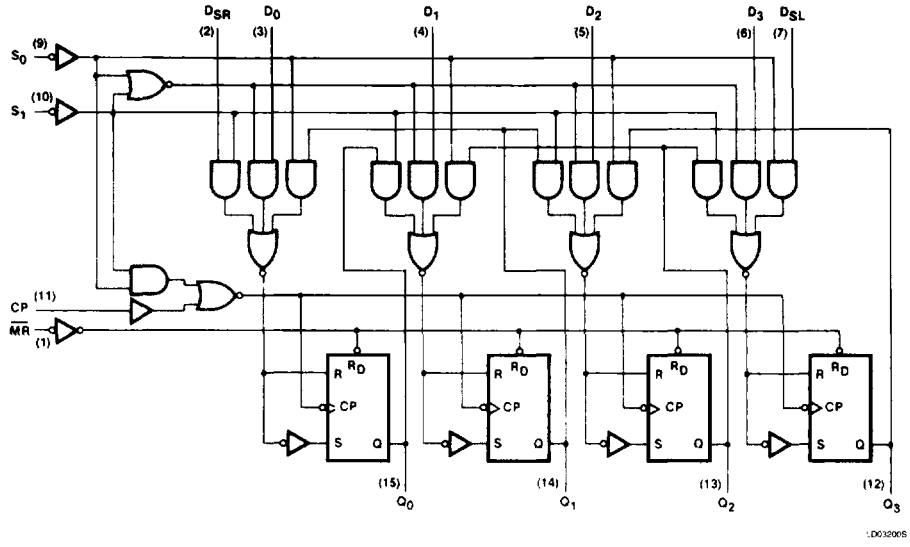


The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or, right to left (shift left, $Q_3 \rightarrow Q_2$, etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 74S194 and 74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one set-up time prior to the positive transition of the clock pulse. The Mode Select inputs of the 74194 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs ($D_0 - D_3$) are D-type inputs. Data appearing on $D_0 - D_3$ inputs when S_0 and S_1 are HIGH is transferred to the $Q_0 - Q_3$ outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

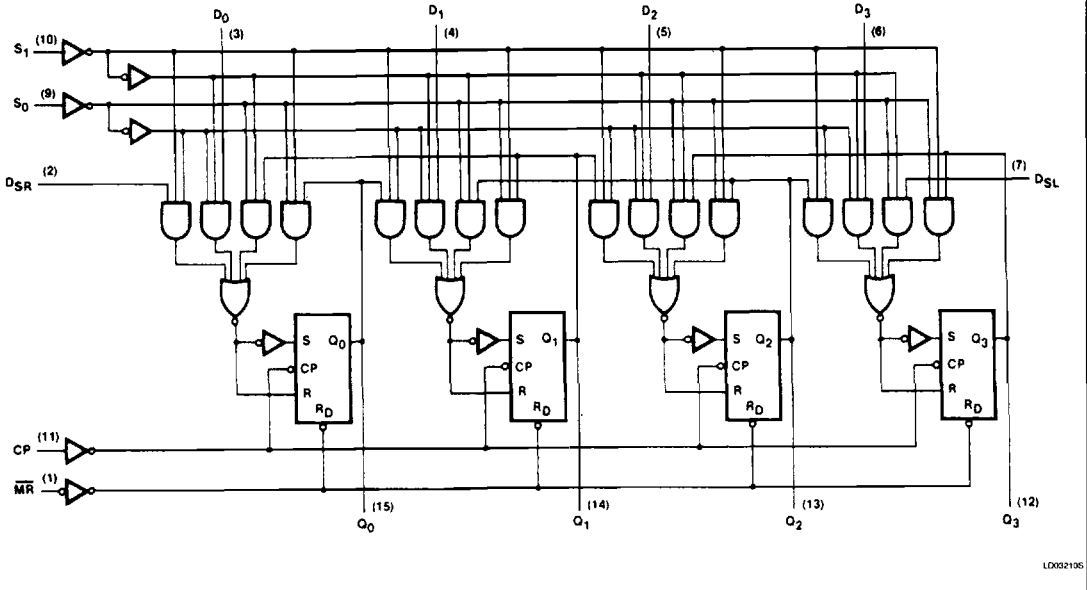
LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

74194

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

74S194, 74LS194A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18			−18	mA
I_{OH}	HIGH-level output current			−800			−400			−1000	μA
I_{OL}	LOW-level output current			16			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74194			74LS194A			74S194			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4	3.4		2.7	3.5		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA (74LS)					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.5			−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V			1.0						1.0	mA
			V_I = 7.0V						0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V			40							μA
			V_I = 2.7V						20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V			−1.6			−0.4				mA
			V_I = 0.5V									−2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−57	−20		−100	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			39	63		15	23		85	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, D_i inputs grounded and 4.5V applied to S_0, S_1, $\overline{MR}$ and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		$C_L = 15pF$, $R_L = 280\Omega$		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		70		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26		22 26	4.0 4.0	12 16.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		37		30		18.5	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			Min	Max	Min	Max	Min	Max	
$t_W(H)$	Clock pulse width HIGH	Waveform 1	20		20		7		ns
$t_W(L)$	$\overline{MR}$ pulse width, LOW	Waveform 2	20		20		12		ns
t_s	Set-up time, data to clock	Waveform 3	20		20		5.0		ns
t_h	Hold time, data to clock	Waveform 3	0		0		3.0		ns
$t_s(L)$	Set-up time LOW, S_n to CP[a]	Waveform 4	30		30		11		ns
$t_s(H)$	Set-up time HIGH, S_N to CP	Waveform 4	30		30		11		ns
t_h	Hold time, S_n to CP	Waveform 4	0		0		3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	25		25		9.0		ns

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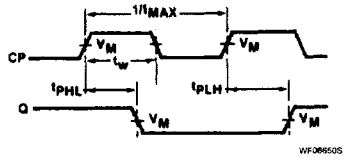
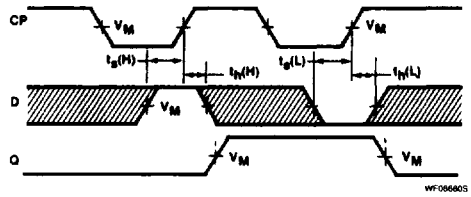
AC WAVEFORMS



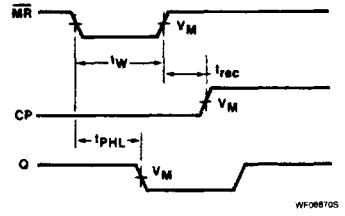
V_M = 1.5V for 74S; V_M = 1.3V for 74LS.

Waveform 1. Clock To Output Delays And Clock Pulse Width



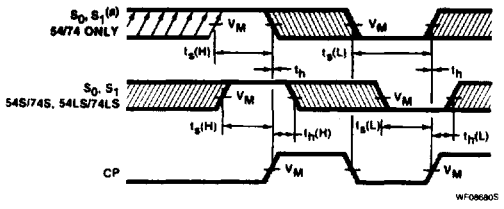
V_M = 1.5V for 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2. Data Set-up And Hold Times



V_M = 1.5V for 74S; V_M = 1.3V for 74LS.

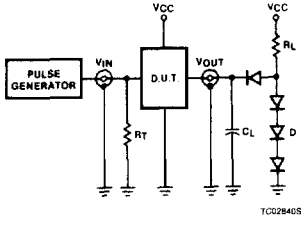
Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



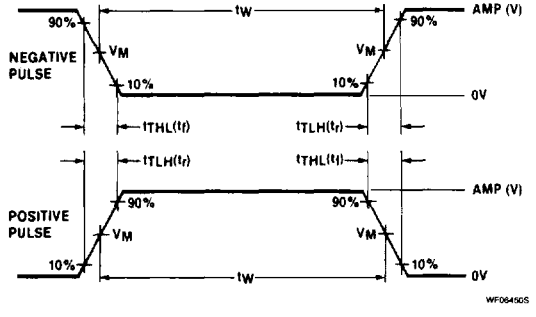
V_M = 1.5V for 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Set-up And Hold Times For S_0 And S_1 Inputs

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns