RF5C16A/RP5C16

CRT CONTROLLER

■ General description

RP5C16/RF5C16A are LSI developed under CMOS process technology for application to CRT controller. They allow to display the various patterns on the CRT by control commands and image data fed from 8 bit CPU including 8085, Z80, etc. With use of this 5C16, CRT controller system can be configurated by merely connecting DRAM.

Note)

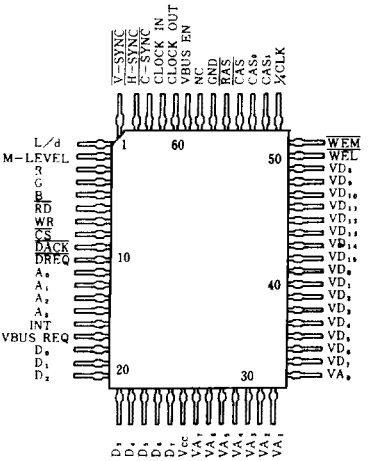
RF5C16A is the 64 pin FLAT packaged product.
RP5C16 is the 64 pin DIL packaged product.

■ Features

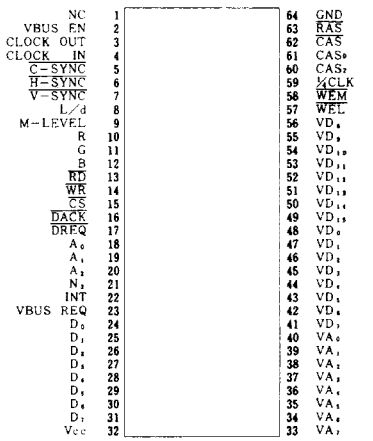
- 4 modes
  - ·Color picture with 80 X 25 characters
  - ·Color picture with 640 X 200 dots
  - ·2 color pictures with 40 X 25 characters and 40 X 25 characters
  - ·2 color pictures with 320 X 200 dots and 40 X 25 characters
- Display of maximum 15 colors with RGB output (2 values or 3 values)
- Virtual screen
- Smooth scroll to horizontal and vertical directions are practicable.
- Abundant attribute function (transverse invert, longitudinal invert, vertical invert and black white invert)
- Cursor built-in (for mouse)
- Master/Slave mode (Superimpose practicable)
- Redefinable character set
- Buffer register and address counter built-in for updating of V-RAM (Video RAM)
- Low power consumption for the sake of CMOS process
- 60 Hz non-interlace display

■ Pin configuration

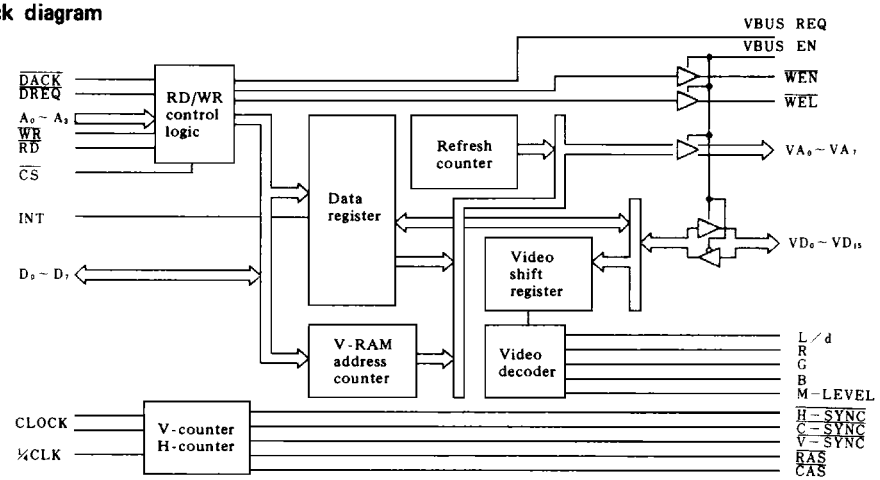
RF5C16A



RP5C16



■ Block diagram



■ Pin description

(1) CPU interface

Symbol	Name	Input/output	Logic	Function
$\overline{CS}$	Chip Select	IN	Active L	Make it possible to Read and Write of control register, address register and buffer register
$\overline{RD}$	Read Strobe	IN	L	
$\overline{WR}$	Write Strobe	IN	L	
$A_0 \sim A_3$	Address 0 ~ Address 3	IN	(positive)	Selective line of control register
$D_0 \sim D_7$	Data 0 ~ Data 7	IN/OUT	(positive)	Data bus Data 0 = LSB Data 7 = MSB
INT	Interrupt	OUT	Active H	
$\overline{DREQ}$	DMA Request	OUT	L	
$\overline{DACK}$	DMA Acknowledge	IN	L	

(2) V-RAM interface

Symbol	Name	Input/output	Logic	Function
$\overline{RAS}$	ROW Address Strobe	OUT	Active L	Set Row Address, Provide Timing
$\overline{CAS}$	Column Address Strobe	OUT	L	Set Column Address, Provide Timing
$\overline{CAS_0}$	Column Address Strobe 0	OUT	L	$\overline{CAS}$ which turns to active only when address is 0 ~ 3 FFFH.
$\overline{CAS_1}$	Column Address Strobe 1	OUT	L	$\overline{CAS}$ which turns to active only when active is 4000H ~ 7 FFFH.
VBUS EN	VIDEO BUS ENABLE	IN	H	When L, it turns $\overline{CAS}$, $\overline{CAS_0}$, $\overline{CAS_1}$, $\overline{RAS}$, $\overline{WEL}$, $\overline{WEM}$, $VA_{0\sim7}$ and $VD_{0\sim15}$ to Hi-Z.
VBUS REQ	VIDEO BUS REQUEST	OUT	H	5C16 accesses VBUS, it turns to active before 4 clock.
$\overline{WEM}$	Write Enable MSB	OUT	L	Write is early write operation
$\overline{WEL}$	Write Enable LSB	OUT	L	Write is early write operation
$VA_0 \sim VA_7$	Video Memory Address 0 ~ 7	OUT	(positive)	
$VD_0 \sim VD_{15}$	Video Memory Data 0 ~ 15	IN/OUT	(positive)	Data 0 = LSB Data 15 = MSB

(3) Clock and Video output

Symbol	Name	Input/output	Logic	Function
CLOCK IN CLOCK OUT	Clock In Clock Out			14.31818 MHz which connects quartz crystal.
M-LEVEL	Middle Level	IN		When RGB3 value output, it provides CRTC with intermediate level
Vcc, GND	Vcc, GND	–	–	
R, G, B L/d	Red, Green, Blue Light and dark	OUT	(positive)	Video output (2 values or 3 values)
$\overline{\text{C-SYNC}}$	Composite Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input H-SYNC when slave mode
$\overline{\text{V-SYNC}}$	Vertical Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input V-SYNC when slave mode
$\overline{\text{H-SYNC}}$	Horizontal Synchronous	OUT/IN	(negative)	Output (open drain output) when master mode and input H-SYNC when slave mode
¼ CLK	¼ CLOCK	OUT		Clock ¼ frequency division output

■ Absolute maximum rating

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply voltage		−0.3 ~ +7.0	V
VI	Input voltage		−0.3 ~ +7.0	V
VO	Output voltage		−0.3 ~ +7.0	V
Pd	Maximum power consumption	Ta = 25°C	300	mW
Ta	Operating ambient temperature		−10 ~ 70	°C
Tstg	Storage temperature		−40 ~ 125	°C

■ Recommended operating condition

Symbol	Parameter	Condition	Value	Unit
Vcc	Supply voltage		4.5 ~ 5.5	V
Vss	Supply voltage		0	V
VIH	"H" input voltage		2.0 ~ Vcc + 0.3	V
VIL	"L" input voltage		−0.3 ~ 0.8	V
Ta	Ambient temperature		−10 ~ 70	°C

■ DC electrical characteristics (Vcc = 5.0V ± 10%, Ta = −10 ~ 70°C)

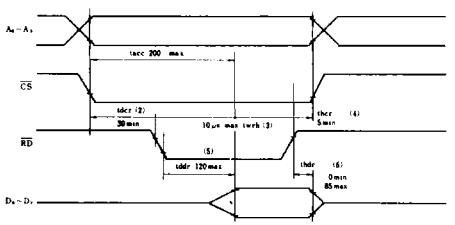
Symbol	Parameter	Condition	Value			Unit
			Min.	Typ.	Max.	
VIH	"H" input voltage		2.0		Vcc + 0.3	V
VIL	"L" input voltage		−0.3		0.8	V
VOH	"H" output voltage	IOH = −400 μA	2.4			V
VOL	"L" output voltage	IOL = 3.2 mA			0.4	V
ILI	Input leakage current	0 ≦ VI ≦ Vcc			10	μA
ILO	3-state floating current	0.4 ≦ VI ≦ 2.4			10	μA
Icc	Supply current				50	mA
VINφ	Clock input "H" input voltage		0.7 x Vcc			V
VILφ	Clock input "L" input voltage				0.3 x Vcc	V

■ AC characteristics (Vcc = 5.0V ± 10%, Ta = −10~70°C) and Timing diagram (Unit : ns)

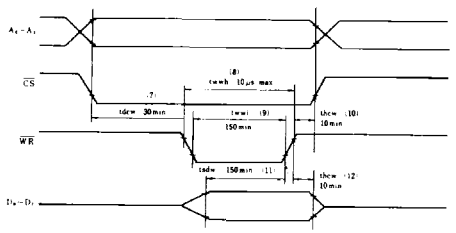
(1) CPU-5C16 READ/WRITE

No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	tacc	Access time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$			200	ns
2	tdcr	$\overline{RD}$ delay time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$	30			ns
3	twrh	$\overline{RD}$ pulse width (H-threshold)			10	ns
4	thcr	$\overline{CS}$, A_0~A_3 and $\overline{DACK}$ hold time during read	5			ns
5	tddr	Data delay time from $\overline{RD}$			120	ns
6	thdr	Data hold time during read	0		85	ns
7	tdcw	$\overline{WR}$ delay time from $\overline{CS}$, A_0~A_3 and $\overline{DACK}$	30			ns
8	twwh	$\overline{WR}$ pulse width (H-threshold)			10	ns
9	twwl	$\overline{WR}$ pulse width (L-threshold)	150			ns
10	thcw	$\overline{CS}$, A_0~A_3 and $\overline{DACK}$ hold time from $\overline{WR}$	10			ns
11	tsdw	Data setup time	150			ns
12	thdw	Data hold time during write	10			ns
13	tddgl	$\overline{DREG}$ ↓ delay time from CLK OUT			90	ns
14	tddgh	$\overline{DREG}$ ↑ delay time from CLK OUT			60	ns
15	tdinl 1	INT ↓ delay time from $\overline{RD}$ or $\overline{WR}$ (End of INT by Buffer Ready)			410	ns
16	tdinl 2	INT ↓ delay time from CLK OUT			120	ns
17	tdinh	INT ↑ delay time from CLK OUT			90	ns

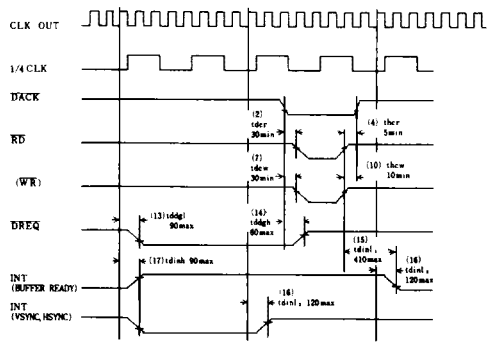
(1−1) CPU READ 5C16



(1−2) CPU WRITE IN 5C16



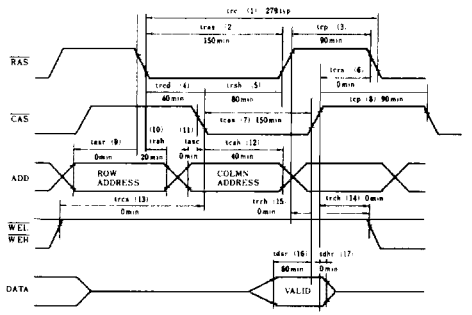
(1−3) INT, $\overline{DREQ}$, $\overline{DACK}$



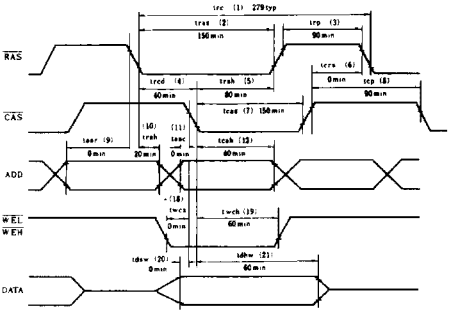
(2) 5C16-V-RAM READ/WRITE

No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	trc	Read cycle time	270	279		ns
2	tras	$\overline{RAS}$ pulse width	150			ns
3	trp	$\overline{RAS}$ pre-charge time	90			ns
4	trcd	$\overline{RAS}$-$\overline{CAS}$ delay time	40			ns
5	trsh	$\overline{RAS}$ hold time	80			ns
6	tcrs	$\overline{CAS}$-$\overline{RAS}$ setup time	0			ns
7	tcas	$\overline{CAS}$ pulse width	150			ns
8	tcp	$\overline{CAS}$ pre-charge time	60			ns
9	tasr	Line address setup time	0			ns
10	trah	Line address hold time	20			ns
11	tasc	Column address setup time	0			ns
12	tcah	Column address hold time ($\overline{CAS}$ reference)	40			ns
13	trcs	Read command setup time	0			ns
14	trch	Read command hold time ($\overline{CAS}$ reference)	0			ns
15	trrh	Read command hold time ($\overline{RAS}$ reference)	0			ns
16	tdsr	Data input setup time ($\overline{CAS}$ reference)	60			ns
17	tdhr	Data input hold time ($\overline{CAS}$ reference)	0			ns
18	twcs	Write command setup time	0			ns
19	twch	Write command hold time ($\overline{CAS}$ reference)	60			ns
20	tdsw	Data input setup time ($\overline{CAS}$ reference)	0			ns
21	tdhw	Data input hold time ($\overline{CAS}$ reference)	60			ns
22	tdvr	VBUS REQ delay time from CLK OUT			90	ns
23	thve	Hold time of VBUS EN against CLK OUT	40			ns
24	tsve	Setup time of VBUS against CLK OUT	0			ns
25	tdral	$\overline{RAS}$ ↓ delay time from CLK OUT			100	ns
26	tdraf	Delay time for $\overline{RAS}$ from CLK OUT to turn to floating	0		60	ns
27	tdwev	Delay time for $\overline{WEL}$ or $\overline{WEM}$ from CLK OUT to turn to valid			70	ns
28	tdwef	Delay time for $\overline{WEL}$ or $\overline{WEM}$ from CLK OUT to turn to floating	0		60	ns
29	tdcav	Delay time for $\overline{CAS}$, $\overline{CAS_0}$ and $\overline{CAS_1}$ from CLK OUT to turn from floating to valid			70	ns
30	tdcaf	Delay time for $\overline{CAS}$, $\overline{CAS_0}$ and $\overline{CAS_1}$ from CLK OUT to turn to floating	30		130	ns
31	tdvav	Delay time for $VA_{0\sim7}$ and $VD_{0\sim15}$ from CLK OUT to turn from floating to valid			70	ns
32	tdvaf	Delay time for $VA_{0\sim7}$ and $VD_{0\sim15}$ from CLK OUT to turn to floating	0		60	ns

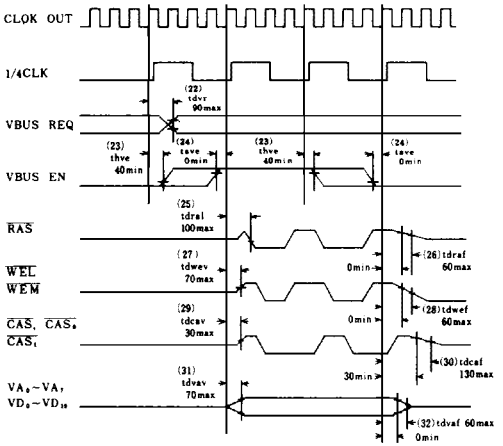
(2-1) 5C16 READ V-RAM



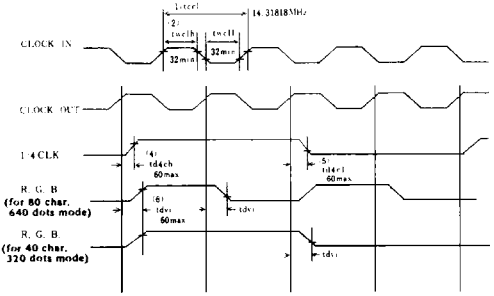
(2-2) 5C16 WRITE V-RAM



(2–3) VBUS REQ, VBUS EN



(3–1) CLK IK, CLK OUT



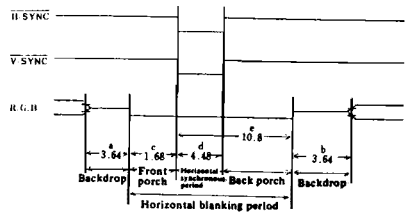
(3) CLK IN, CLK OUT

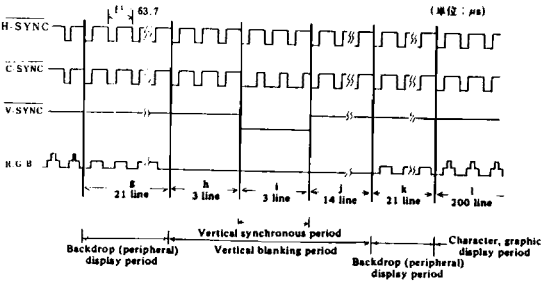
No.	Symbol	Parameter	Value			Unit
			Min.	Typ.	Max.	
1	tccl	Clock frequency	−300	14.318 18	+300	MHz ppm.
2	twch	Clock pulse width (H period)	32			ns
3	twcl	Clock pulse width (L period)	32			ns
4	td4ch	¼ CLK ↑ delay time from CLK OUT			60	ns
5	td4cl	¼ CLK ↓ delay time from CLK OUT			60	ns
6	tdvi	RGB delay time from CLK OUT			60	ns

(4) SYNC wave, R.G.B. output

No.	Symbol	Parameter	Value	Unit
7	a	Backdrop (peripheral) display period front porch side	3.64±0.50	μs
8	b	Backdrop (peripheral) display period back porch side	3.64±0.50	μs
9	c	Front porch	1.68±0.30	μs
10	d	Horizontal synchronous period	4.48±0.30	μs
11	e	Horizontal synchronous period + back porch	10.80±0.30	μs
12	f	Horizontal synchronous signal cycle	63.70±0.50	μs
13	g	Display period of backdrop (peripheral)	21	line
14	h	Blanking period before vertical synchronous period	3	line
15	i	Vertical synchronous period	3	line
16	j	Blanking period after vertical synchronous period	14	line
17	k	Display period of backdrop (peripheral)	21	line
18	l	Display period of character and graphic	200	line

(4–1) SYNC wave, R.G.B. output (Unit : μs)





■ Connectible CPU

8085 6MHz 8085AH-2 8085A-2
Z-80 6MHz Z-80B
6502 3MHz 65C02B
16bitCPU

■ Usable memory

64 X 1bit, 16k X 4bit or 64k X 4bit
・Use Tacc (access time) of below 120 ns.
・Memory at maximum 128K byte is usable.

■ Table of control register

〈WR〉

Register No.	Data b7	b6	b5	b4	b3	b2	b1	b0	CONTENTS
0	←			TR-L				→	Transfer Register – L
1	←			TR-M				→	Transfer Register – M
2	←			Add-L				→	Transfer Address – L
3	←			Add-M				→	Transfer Address – M
4	MV	MH	MB	DMA	1/2	byWR	byRD	ML/L	Transfer mode interrupt mask
5	←MODE→		FG-on	BG-on	R-on	M/S←		AH→	Display mode
6	←			CsHL				→	Cursor coordinate HL
7	←			CsV				→	Cursor coordinate V
8	←	BCG-M				X	←	CsHm→	Chara. Gen. Base Address M cursor coordinate CsHm
9	←	BFG-M				→	×	×	Fore Ground Base Address M
A	←			BBG-L				→	Back Ground Base Address L
B	←			BBG-M				→	Back Ground Base Address M
C	←	CFG3					CFG2	→	FG 3rd color FG 2 color
D	←	CBG3					CBG2	→	BG 3rd color BG 2 color
E	←	CBD-p					CBD-c	→	BD color (peripheral) BD color (center)
F	SL←		SV	→	×	←	SH		Dot Scroll V direction H direction

〈RD〉

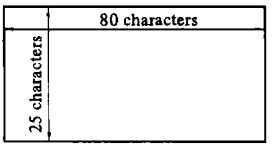
0	←			TR-L				→	Transfer Register – L
1	←			TR-M				→	Transfer Register – M
2	←			Add-L				→	Transfer Address – L
3	←			Add-M				→	Transfer Address – M
4	MV	MH	MB	X	FV	FH	FB	X	Interrupt flag

■ Description of function

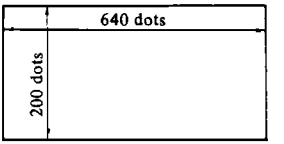
(1) Display mode

- Following 4 display modes are available.

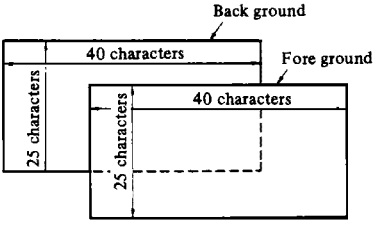
A. 80 character X 25 line character display mode (only back ground)



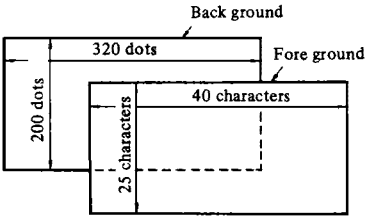
B. 640 X 200 dot graphic dispaly mode (only back ground)



C. 40 characters – 40 character display mode

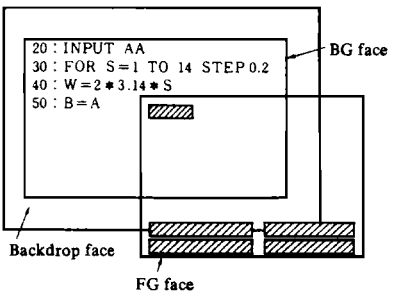


D. 40 character – 320 dot display



(2) Picture simultaneous display (display mode 3 and 4)

- 2 pictures of fore ground face and back ground face are simultaneously displayed.
- When overlapping of FG face pattern with BG face pattern, FG face is displayed.
- In case where there is neither pattern present on FG face nor on BG face, backdrop color (CBD-C) is displayed.
- As far as the distance ranging from the outside of display window to the edge of cathode ray tube, the color of backdrop face (CBD-P) is displayed. (Backdrop color is specified by register E)



(3) 15 color display

15 colors can be displayed.

Color code				Color	Color code				Color
L/d	B	G	R		L/d	B	G	R	
0	0	0	0	Black	1	0	0	0	Black
0	0	0	1	Red	1	0	0	1	Pink
0	0	1	0	Green	1	0	1	0	Light Green
0	0	1	1	Yellow	1	0	1	1	Light Yellow
0	1	0	0	Blue	1	1	0	0	Light Blue
0	1	0	1	Magenta	1	1	0	1	Light Magenta
0	1	1	0	Cyan	1	1	1	0	Light Cyan
0	1	1	1	Gray	1	1	1	1	White

(4) R, G, B output

- Following outputs are held as image signal. R, G, B, L/d, $\overline{\text{C-SYNC}}$, $\overline{\text{V-SYNC}}$ and $\overline{\text{H-SYNC}}$
- RGB terminal takes the following output levels at 3 value output.

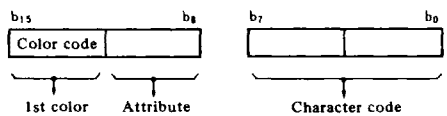
	Min.	Max.
High	4.4	Vcc
Middle	M-LEVEL−0.6	M-LEVEL+0.4
Low	—	0.4

Vcc = 5V, M-LEVEL = 2.5V, Io = ±1mA

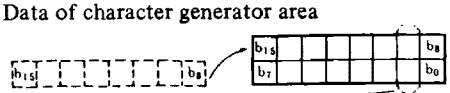
- $\overline{\text{V-SYNC}}$, $\overline{\text{C-SYNC}}$ and $\overline{\text{H-SYNC}}$ terminals turn to output terminal (open drain) under master mode and to input terminal under slave mode.
  (Refer "Terminal function (3) Clock and Video output")

(5) Character display

- The size of character at character display is 8 X 8 dots.
- Fonts are kept in memory area of 2K words from character generator base address (BCG-M). (Max. 256 kinds)
- Data of code area



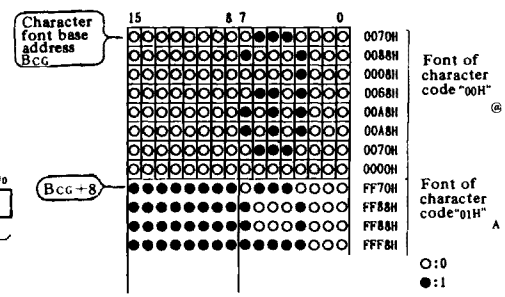
- Data of character generator area



Character generator value	Display color
00	Clear
01	1st color
10	2nd color
11	3rd color

2nd and 3rd colors are specified by control register (C, D).

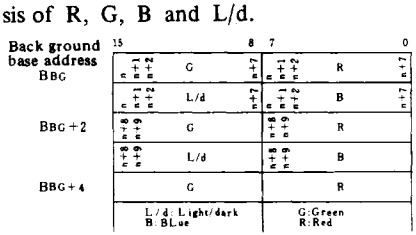
- Configuration of character font

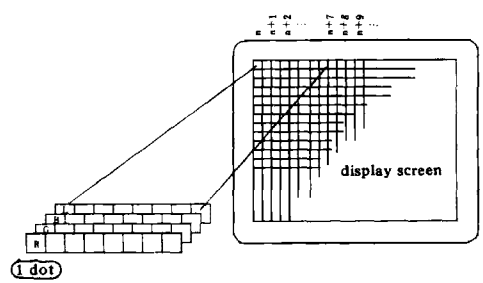


- When displaying MSByte in single color such as alphanumeric character, etc., all "0" or all "1" is used.
- When drawing the picture such as game, etc, 4 colors can be displayed at each dot with 2 bit of combination such as bit 15 with bit 7, bit 14 with bit 6 and so on.

(6) Graphic display

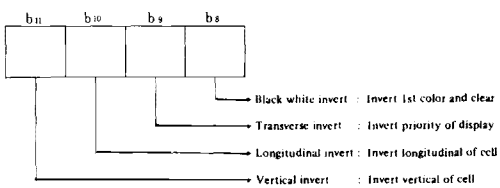
- 1 dot is consisted of 4 bits, and 8 dots are allocated as 1 block.
- Display color is decided by 4 face synthesis of R, G, B and L/d.

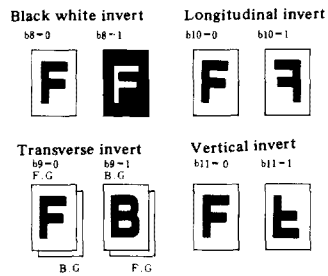




(7) Attribure (character display)

- 4 kinds of attribute can be decided with bit 8 ~ bit 11 of code area data.

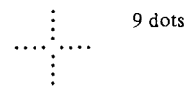




(8) Cursor

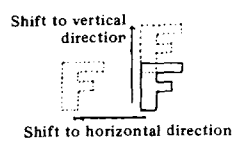
- Cross hair cursor is displayed. The coordinate of cursor in the horizontal direction is specified with 10 bits of cursor register CsHm and CsHL while in the vertical direction with 8 bits of CsV. 2 bits of cursor register CsHm will not become effective unless CsHL is written.

Shape of cursor



(9) Dot scroll (only back ground)

- It allows scroll of 0~7 dots in the horizontal and vertical directions. The number of shift to the horizontal and vertical directions is specified by respective dot scroll register SH and SV.



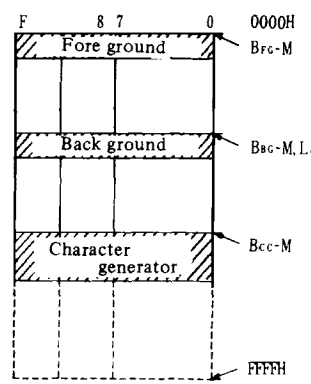
(10) Control of video memory area

- Base address

  BG base address (BBG-M, BBG-L) is consisted of 16 bits and allows to specify by 1 character unit. Therefore, the change of BG base address allows scroll in the column or line direction. BBG-M becomes effective when BBG-L is written. Those subsequent to this address area fall in code data of back ground. In case of graphic, too, data are stored here.

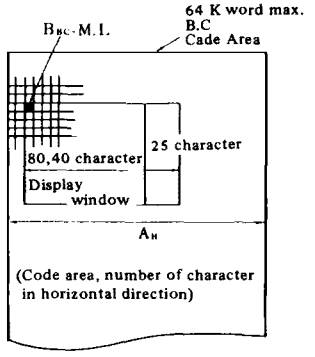
  FG base address (BFG-M) allows paging of each 1,024 characters with 6 bit. Subsequent to this address, code data of fore ground are stored in 1,000 words (40 character X 25 line).

  Character generator base address (BCG-M) is able to specify the start address of character font for each 2,048 words with 5 bit. Character font is consisted of 1 cell 8 words and is able to select 256 patterns. (Refer diagram) It will not be used for only graphic display.



- Width of code area (No. of character AH)

  FG is fixed with 40 characters. BG can be selected from 40 characters (320 dots), 64 characters (512 dots), 80 characters (640 dots) and 128 characters (1,024 dots). With this, the width of virtual screen is set.



(11) Updating function of frame buffer

- Since it has the transfer register and address counter, it allows read/write of frame buffer data, making use of retrace line section in horizontal/vertical direction without relying on externally mounted circuit.
- Write mode/read mode/read modify write mode (see diagram below)
- Word transfer/Byte transfer (see diagram below)

	Write mode		Read mode		Read modify write	
	Word transfer	Byte transfer	Word transfer	Byte transfer	Word transfer	Byte transfer
Read TR-M	–	–	–	Add+1-RT	–	–
Read TR-L	–	–	Add+1-RT	Add+1-RT	–	–
Write TR-M	–	WT-Add+1	–	WT	–	WT-Add+1 -RT
Write TR-L	WT-Add+1	WT-Add+1	WT	WT	WT-Add+1 -RT	WT-Add+1 -RT
Read Add-M	–	–	–	–	–	–
Read Add-L	–	–	–	–	–	–
Write Add-M	–	–	–	–	–	–
Write Add-L	–	–	RT	RT	RT	RT

TR : Transfer register
Add : Address counter
RT : Read transfer (frame buffer read)
WT : (frame buffer write)

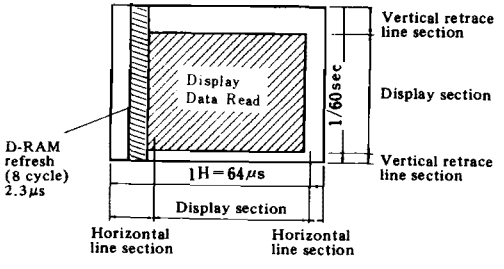
The relationship " – " between read/write operation of transfer register and read/write toward frame buffer represents the sequence of process. For example, when CPU side read TR-L register under (read mode), first of all, number of address counter is set as +1, then, perform read of frame buffer. " – " represents that no steps are being taken for frame buffer.

- The mode of increment +1/+2+2 of address counter is used in graphic display, for example, only the face of BLUE is rewritten in sequence.
- DMA transfer

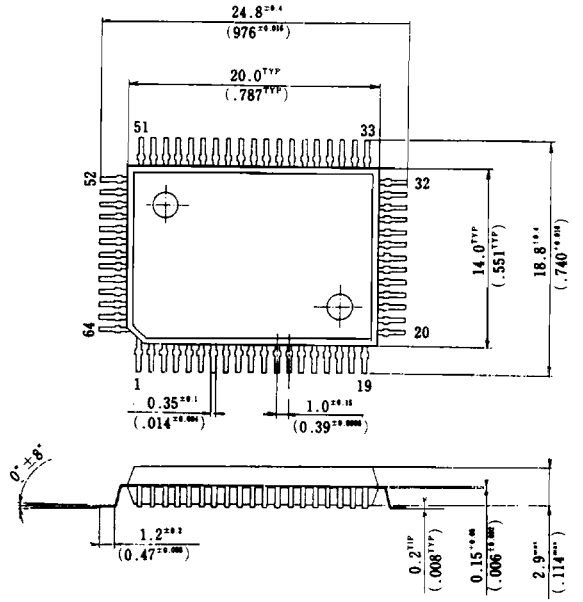
  In case of DMA transfer, it is necessary to set whether to read or write to LSB of transfer register, or to read or write to MSB. In case of word transfer, TR-L and TR-M vary at every 1 byte. In case of byte transfer, it is always written in the register that has been set.

(12) D-RAM refresh

- 8 addresses per 1 H (64 μs) are refreshed within retrace line section.



■ 64 pin flat package dimension (Unit : mm)



■ 64pin DIL package dimension (Unit : mm)